PIC16F88X

PIC16F88X Family
Silicon Errata and Data Sheet Clarification

The PIC16F88X family devices that you have received conform functionally to the current Device Data Sheet (DS41291**G**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2, Table 3 and Table 4.

The errata described in this document will be addressed in future revisions of the PIC16F88X silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2, Table 3 and Table 4 apply to the current silicon revision (**A0** or **A2**, as applicable).

Data Sheet clarifications and corrections start on page 14, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16F88X silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A0	A2
PIC16F882	2000h	00h	
PIC16F883	2020h	00h	
PIC16F884	2040h	00h	
PIC16F886	2060h		02h
PIC16F887	2080h		02h

Note 1: The device and revision data is stored in the Device ID located at 2006h in program memory.

2: Refer to the *"PIC16F88X Memory Programming Specification"* (DS41287) for detailed information.

TABLE 2: SILICON ISSUE SUMMARY (PIC16F882)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A0
LVP	Programming	1.	Programming disruption.	X
MSSP	SPI Master	2.	SPI using Timer2/2.	X
ADC	VP6 Reference	3.	Disruption of the HFINTOSC.	X
MSSP	SPI Master	4.	Write collision on loading.	X
MSSP	I^2C™ Slave	5.	R/W bit on $\overline{ACK}$.	X
MSSP	I^2C™ Master	6.	Clock-stretching handling.	X
MSSP	SPI Slave	7.	Multi-byte transmission.	X
Timer1	Ext. Crystal	8.	Overflow may take additional count.	X
Timer1	Ext. Crystal	9.	Oscillator may stop running at low temps.	X
Timer0	Prescaler	10.	Spurious Reset.	X
MSSP	SPI Master	11.	Disabling the module generates a clock pulse.	X
CCP	Dead-Band Delay	12.	Unpredictable waveforms if dead-band delay is greater than the PWM duty cycle.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 3: SILICON ISSUE SUMMARY (PIC16F883/PIC16F884)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A0
LVP	Programming	1.	Programming disruption.	X
MSSP	SPI Master	2.	SPI using Timer2/2.	X
ADC	VP6 Reference	3.	Disruption of the HFINTOSC.	X
MSSP	SPI Master	4.	Write collision on loading.	X
MSSP	I^2C™ Slave	5.	R/W bit on $\overline{ACK}$.	X
MSSP	I^2C™ Master	6.	Clock-stretching handling.	X
MSSP	SPI Slave	7.	Multi-byte transmission.	X
Timer1	Ext. Crystal	8.	Overflow may take additional count.	X
Timer1	Ext. Crystal	9.	Oscillator may stop running at low temps.	X
Timer0	Prescaler	10.	Spurious Reset.	X
MSSP	SPI Master	11.	Disabling the module generates a clock pulse.	X
CCP	Dead-Band Delay	12.	Unpredictable waveforms if dead-band delay is greater than the PWM duty cycle.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 4: SILICON ISSUE SUMMARY (PIC16F886/PIC16F887)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A2
LVP	Programming	1.	Programming disruption.	X
MSSP	SPI Master	2.	SPI using Timer2/2.	X
ADC	VP6 Reference	3.	Disruption of the HFINTOSC.	X
MSSP	SPI Master	4.	Write collision on loading.	X
MSSP	I^2C™ Slave	5.	R/W bit on $\overline{ACK}$.	X
MSSP	I^2C™ Master	6.	Clock-stretching handling.	X
MSSP	SPI Slave	7.	Multi-byte transmission.	X
Timer1	Ext. Crystal	8.	Overflow may take additional count.	X
Timer1	Ext. Crystal	9.	Oscillator may stop running at low temps.	X
Timer0	Prescaler	10.	Spurious Reset.	X
MSSP	SPI Master	11.	Disabling the module generates a clock pulse.	X
CCP	Dead-Band Delay	12.	Unpredictable waveforms if dead-band delay is greater than the PWM duty cycle.	X
ICSP™	Programming	13.	Memory read and verify operations.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A0** or **A2**, as applicable).

1. Module: Low-Voltage In-Circuit Serial Programming™ (LVP)

If LVP (Low-Voltage Programming) mode is enabled, programming the device using the V_{PP} pin while holding high or toggling the port pin RB3/PGM during Program mode could disrupt the programming sequence.

Work around

Pull down pin RB3/PGM using external circuitry during programming of the device.

Affected Silicon Revisions

PIC16F882

A0							
X							

PIC16F883/PIC16F884

A0							
X							

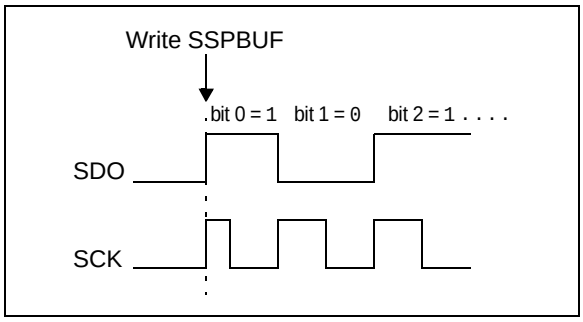
PIC16F886/PIC16F887

A2							
X							

2. Module: MSSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCK pulse may occur on the first bit of the transmitted/received data (Figure 1).

FIGURE 1: SCK PULSE VARIATION USING TIMER2/2



Work around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load SSPBUF with the data to transmit and then turn Timer2 back on. Refer to Example 1 for sample code.

EXAMPLE 1: AVOIDING THE INITIAL SHORT SCK PULSE

```
LOOP BTFSS  SSPSTAT, BF     ;Data received?
                            ;(Xmit complete?)
     GOTO   LOOP            ;No
     MOVF   SSPBUF, W       ;W = SSPBUF
     MOVWF  RXDATA          ;Save in user RAM
     MOVF   TXDATA, W       ;W = TXDATA
     BCF    T2CON, TMR2ON   ;Timer2 off
     CLRF   TMR2            ;Clear Timer2
     MOVWF  SSPBUF          ;Xmit New data
     BSF    T2CON, TMR2ON   ;Timer2 on
```

Affected Silicon Revisions

PIC16F882

A0							
X							

PIC16F883/PIC16F884

A0							
X							

PIC16F886/PIC16F887

A2							
X							

3. Module: Analog-To-Digital Converter (ADC) Module

Selecting the VP6 reference as the analog input source (CHS<3:0> = 1111) for the ADC conversion after sampling another analog channel with input voltages approximately greater than 3.6V can temporarily disturb the HFINTOSC oscillator.

Note:	This only occurs when selecting the VP6 reference ADC channel using the CHS<3:0> bits in the ADCON0 register and NOT during the start of an actual ADC conversion using the GO/$\overline{\text{DONE}}$ bit in the ADCON0 register.

Work around

Select an ADC channel with input voltages lower than 3.6V prior to selecting the VP6 reference voltage input. Any analog channel can be used, even if that channel is configured as a digital I/O (configured as an output) that is driving the output pin low. An alternative is to configure the CV_{REF} module to output a voltage lower than 3.6V and then selecting that analog channel CHS<3:0> = 1110 as the analog input source.

EXAMPLE 2: AVOID DISTURBING THE HFINTOSC OSCILLATOR

```
BANKSEL   ADCON0       ;
MOVLW     B'XX111001'  ;Select ADC
MOVWF     ADCON0       ;Channel CVREF
MOVLW     B'XX111101'  ;Select ADC
MOVWF     ADCON0       ;Channel VP6
```

Affected Silicon Revisions

PIC16F882

A0							
X							

PIC16F883/PIC16F884

A0							
X							

PIC16F886/PIC16F887

A2							
X							

4. Module: MSSP (SPI Master Mode)

With MSSP in SPI Master mode, FOSC/64 or Timer2/2 clock rate and CKE = 0, a write collision may occur if SSPBUF is loaded immediately after the transfer is complete. A delay may be required after the MSSP Interrupt Flag bit, SSPIF, is set or the Buffer Full bit, BF, is set and before writing SSPBUF. If the delay is insufficiently short, a write collision may occur as indicated by the WCOL bit being set.

Work around

Add a software delay of one SCK period after detecting the completed transfer and prior to updating the SSPBUF contents. Verify the WCOL bit is clear after writing SSPBUF. If the WCOL is set, clear the bit in software and rewrite the SSPBUF register.

Date Codes that pertain to this issue:

All engineering and production devices.

Affected Silicon Revisions

PIC16F882

A0							
X							

PIC16F883/PIC16F884

A0							
X							

PIC16F886/PIC16F887

A2							
X							

5. Module: MSSP (I^2C™ Slave Mode)

When the master device wants to terminate receiving any more data from the slave device, it will do so by sending a NACK in response to the last data byte received from the slave. When the slave receives the NACK, the R/W bit of the SSPSTAT register remains set improperly.

Work around

Use the CKP bit of the SSPCON register to determine when the master has responded with a NACK. The CKP bit will be clear when the response is an ACK, and set when the response is a NACK. The CKP bit is automatically cleared to stretch the clock when the master responds to received data with an ACK. This gives the slave time to load the SSPBUF register before setting the CKP bit to release the clock stretching. When the master responds to received data with a NACK, the CKP bit properly remains set and there is no clock stretching.

Affected Silicon Revisions

PIC16F882

A0							
X							

PIC16F883/PIC16F884

A0							
X							

PIC16F886/PIC16F887

A2							
X							

6. Module: MSSP (I^2C™ Master Mode)

When the MSSP is I^2C™ Master mode with a slave device stretching the clock, the clock generation does not function as described in the data sheet.

When a slave device is performing clock stretching by pulling the SCL line low, the master device should continuously sample the SCL line to determine when all slaves have released SCL. When SCL is released, the master device should wait one BRG period to ensure a constant SCL high time.

The current implementation does not ensure accurate SCL high time. During clock stretch, the MSSP device will erroneously continue running the BRG counter. At the end of the clock stretch, the BRG counter continues to count down for the remainder of the BRG period, and then the MSSP device will immediately resume transmitting the data.

Figure 1 illustrates an expected I^2C transmission in which the SCL line is completely controlled by the master device and the slave device does not attempt to stretch the clock period.

Figure 2 illustrates the expected operation of an I^2C transmission in which the slave device has stretched the clock period by holding the SCL line low. The high time of the SCL pulse is constant, regardless of the duration of the clock stretch.

Figure 3 and Figure 4 illustrate an actual I^2C transmission in which the slave has stretched the clock period by holding the SCL line low. Note that the high time of the SCL signal has shortened from the expected time.

FIGURE 1: ACTUAL (CORRECT) OPERATION WITHOUT CLOCK STRETCHING

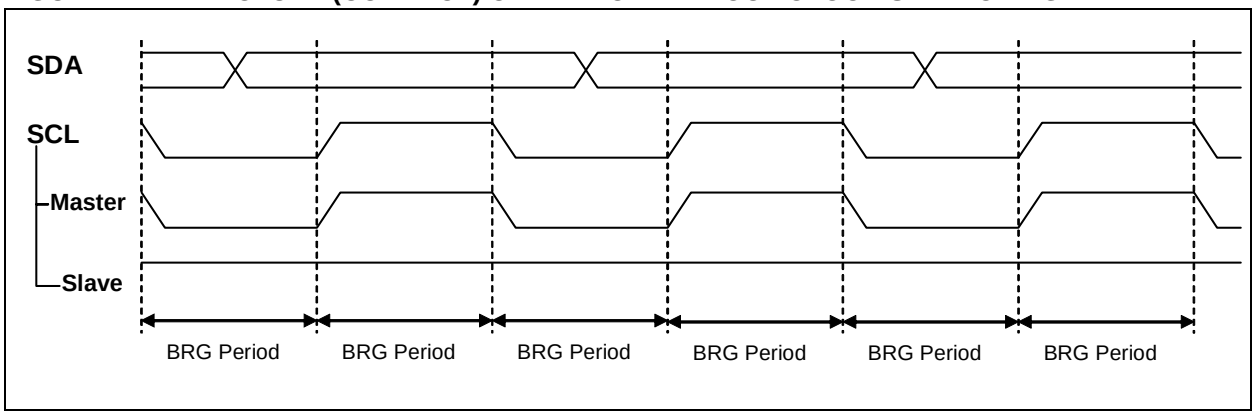


FIGURE 2: EXPECTED OPERATION WITH CLOCK STRETCHING

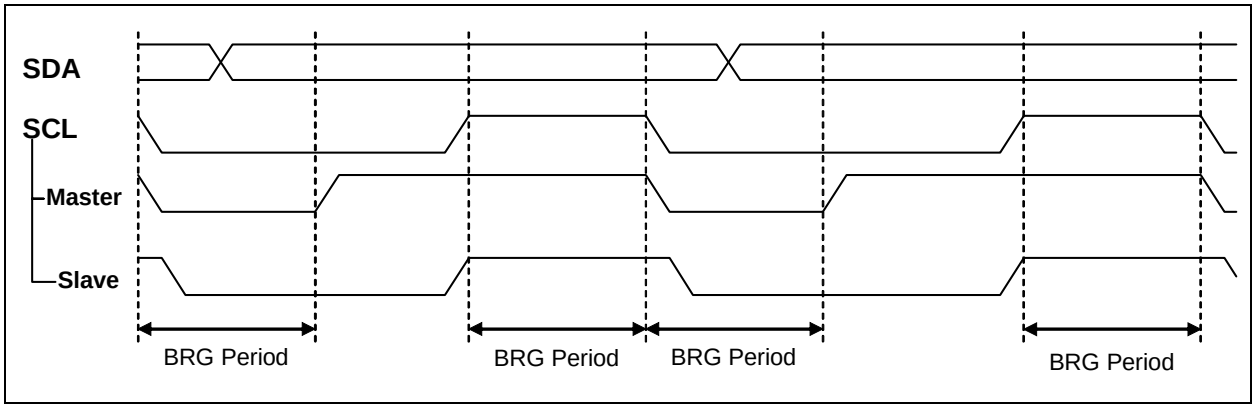


FIGURE 3: ACTUAL (INCORRECT) OPERATION WITH CLOCK STRETCHING – EXAMPLE 1

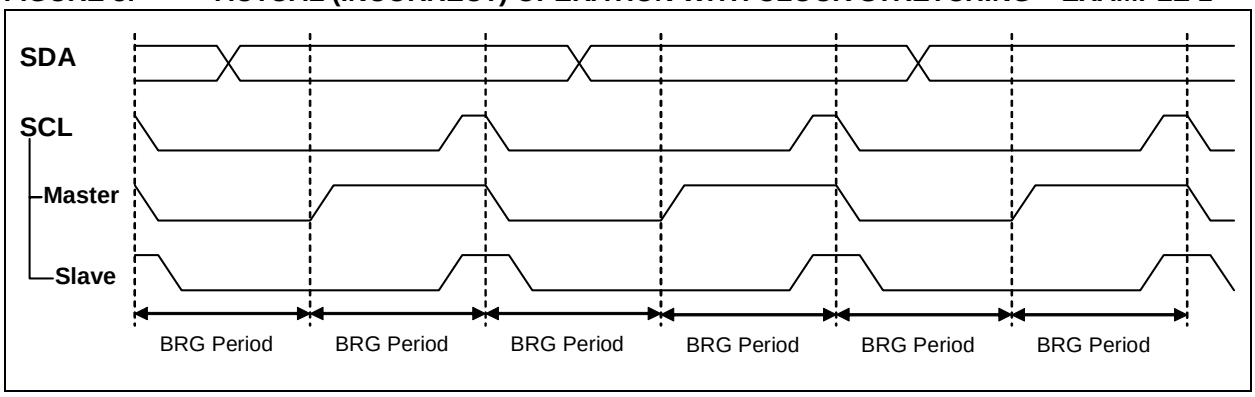
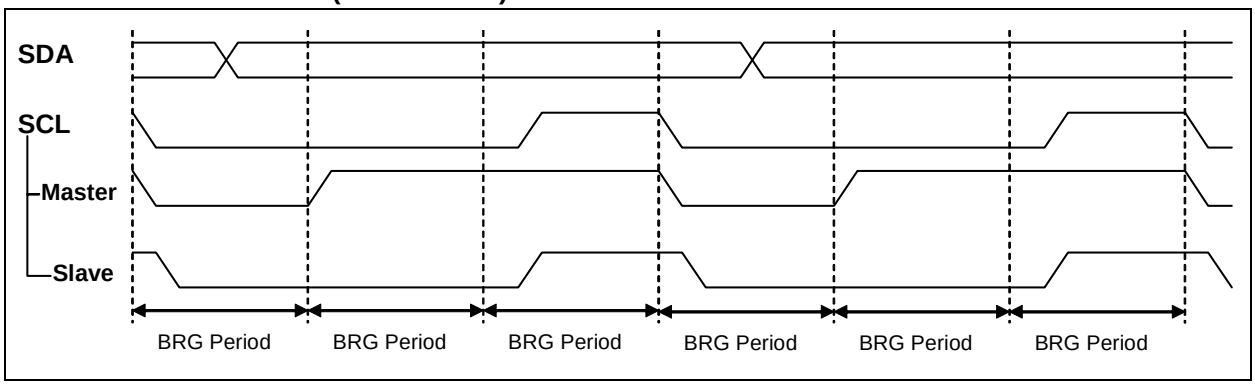


FIGURE 4: ACTUAL (INCORRECT) OPERATION WITH CLOCK STRETCHING – EXAMPLE 2



Work around

Set the communication speed to match the slowest device on the bus. This ensures that no slave device will perform clock stretching.

It is possible to dynamically adjust the communication speed to match the device being addressed by modifying the BRG register. However, the behavior of slower slave devices must be understood and speed adjustments made such that no slave performs clock stretching.

Affected Silicon Revisions

PIC16F882

A0							
X							

PIC16F883/PIC16F884

A0							
X							

PIC16F886/PIC16F887

A2							
X							

7. Module: MSSP

When all of the following conditions are met:

1. The module is configured as a SPI slave
2. CKP = 1
3. CKE = 1
4. Multiple bytes are sent to the Slave with the $\overline{SS}$ line remaining low between bytes

The SSPIF flag will only be set on reception of the first byte and the following bytes will not be correctly received.

Work around

- SPI Master toggles the $\overline{SS}$ line between bytes

or

- On reception of the first byte, modify the SSPM0 bit in the SSPCON register to configure the module as a SPI slave with $\overline{SS}$ pin disabled. Then, restore the SSPM0 bit to the configuration for SPI slave with $\overline{SS}$ pin enabled. The module is then ready for reception of the following byte.

EXAMPLE 3: MODIFICATION OF THE SSPM0 BIT

```
BSF SSPCON, SSPM0
BCF SSPCON, SSPM0
```

Affected Silicon Revisions

PIC16F882

A0							
X							

PIC16F883/PIC16F884

A0							
X							

PIC16F886/PIC16F887

A2							
X							

8. Module: Asynchronous Timer1

This Errata supersedes Errata DS80233 and DS80329.

When TImer1 is started or updated, the timer needs to see a falling edge from the external clock source before a rising edge can increment the counter. If writes to TMR1H and TMR1L are not completed while the external clock pulse is still high, Timer1 will not count the first clock pulse after the update.

When using an external crystal, the pulse width from rising to falling edge is temperature-dependent and may decrease with temperature. As a result, the timer may require an additional oscillation to overflow.

Work around

Switching to the HFINTOSC after reloading, the timer ensures the Timer1 will see a falling edge before switching back to the external clock source.

Due to the time from Timer1 overflow to the reload being application specific, wait for the timer to increment before beginning the reload sequence. This ensures the timer does not miss a rising edge during reload.

EXAMPLE 4: SWITCHING TO HFINTOSC TO ENSURE TIMER1 WILL SEE A FALLING EDGE

```
    BTFSC   TMR1L,0
    GOTO    $-1
    BTFSS   TMR1L,0
    GOTO    $-1             ;Timer has just incremented, 31 µs before next rising edge to
                            ;complete reload

Update:

    BCF     T1CON,TMR1CS    ;Select HFINTOSC for Timer1
    BSF     TMR1H,7         ;Timer1 high byte 0x80
    BCF     T1CON,TMR1ON    ;Timer1 off
    BSF     T1CON,TMR1CS    ;Select external crystal
    BCF     T1CON,TMR1ON    ;Timer1 on


    Critical Timing of code sequence for instructions following last write to TMR1L or TMR1H.
```

Affected Silicon Revisions

PIC16F882

A0							
X							

PIC16F883/PIC16F884

A0							
X							

PIC16F886/PIC16F887

A2							
X							

9. Module: LP/Timer1 Oscillator Operation Below 25°C

1-2% of devices experience reduced drive as temperatures approach -40°C. This will result in a loss of Timer1 counts or stopped Timer1 oscillation.

This can also prevent Timer1 oscillator start-up under cold conditions.

Work around

Use of low-power crystals properly matched to the device will reduce the likelihood of failure. A 1 mΩ resister between OSC2 and V_{DD} will further improve the drive strength of the circuit.

Affected Silicon Revisions

PIC16F882

A0							
X							

PIC16F883/PIC16F884

A0							
X							

PIC16F886/PIC16F887

A2							
X							

10. Module: Timer0 and WDT Prescaler Assignment Spurious Reset

A spurious Reset may occur if the Timer0/ Watchdog Timer (WDT) prescaler is assigned from the WDT to Timer0 and then back to the WDT.

Summary

The issue only arises when all of the below conditions are met:

- Timer0 external clock input (T0CKI) is enabled.
- The Prescaler is assigned to the WDT, then to the Timer0 and back to the WDT.
- During the assignments, the T0CKI pin is high when bit T0SE is set, or low when T0SE is clear.
- The 1:1 Prescaler option is chosen.

Description

On a POR, the Timer0/WDT prescaler is assigned to the WDT.

If the prescaler is reassigned to Timer0 and Timer0 external clock input (T0CKI) is enabled then the prescaler would be clocked by a transition on the T0CKI pin.

On power-up, the T0CKI pin is (by default) enabled for Timer0 in the OPTION register.

If the T0CKI pin is:

- High and Timer0 is configured to transition on a falling edge (T0SE set), or
- Low and Timer0 is configured to transition on a rising edge (T0SE clear)

Then, if the prescaler is reassigned to the WDT, a clock pulse to the prescaler will be generated on the reassignment.

If the prescaler is configured for the 1:1 option, the clock pulse will incorrectly cause a WDT Time-out Reset of the device.

Work around

1. Disable the Timer0 external clock input by clearing the T0CKI bit in the OPTION register.
2. Modify the T0SE bit in the OPTION register to the opposite configuration for the logic level on the T0CKI pin.
3. Select a prescaler rate other than 1:1 and issue a `CLRWDT` instruction before switching to the final prescaler rate.

Affected Silicon Revisions

PIC16F882

A0							
X							

PIC16F883/PIC16F884

A0							
X							

PIC16F886/PIC16F887

A2							
X							

11. Module: MSSP (SPI Master Mode)

When the MSSP module is configured as a SPI master with CKP set, (SPI clock idles high) disabling the module by clearing the SSPEN bit will cause the clock line to be driven low for 2 TOSC before the setting of the RC3 output in the PORTC register takes effect.

Similarly on enabling the module. There is a 1 TOSC period where the clock line will be driven low before the CKP bit takes effect and the line is driven high.

Work around

A pull-up resistor on the SCK line allows the pin to be configured as high-impedance during disabling/ enabling the module and the line to be pulled high by the resistor.

The TRISC3 bit should be set before disabling or enabling the module to tristate the pin, and then cleared before transmission.

Affected Silicon Revisions

PIC16F882

A0							
X							

PIC16F883/PIC16F884

A0							
X							

PIC16F886/PIC16F887

A2							
X							

12. Module: Capture Compare PWM (CCP)

With the ECCP configured for PWM Half-Bridge mode and a dead-band delay greater than or equal to the PWM duty cycle, unpredictable waveforms will result.

Work around

Make sure the dead-band delay is always less than the PWM duty cycle.

Affected Silicon Revisions

PIC16F882

A0							
X							

PIC16F883/PIC16F884

A0							
X							

PIC16F886/PIC16F887

A2							
X							

13. Module: ICSP™

If the supply voltage (VDD) applied to the device is below 2.7V, the device can misread memory locations while performing an In-Circuit Serial Programming™ (ICSP™) read or verify command of the Program Flash Memory (PFM) or the Data EEPROM. This errata applies to both the High-Voltage ICSP and the Low-Voltage ICSP modes of the device, as described in the *"PIC16F88X Memory Programming Specification"* (DS41287). This low-voltage memory misread issue is limited to only the ICSP hardware interface module on the device, which is only used during device programming. In Normal user mode, the device will operate properly down to the specified VDD supply limits, as documented in the device data sheet ("*PIC16F882/883/884/886/887*, *28/40/44-Pin Flash-Based, 8-Bit CMOS Microcontrollers)*"' (DS41291).

Work around

Maintain a minimum VDD voltage setting of 2.7V or above when performing an ICSP read or verify command during programming of the PFM or Data EEPROM Memory.

PIC16F886/PIC16F887

A2							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41291**G**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: ADC (Block Diagram)

Figure 9-1: ADC Block Diagram changes references from AVSS to VSS and AVDD to VDD.

2. Module: ADC

Acquisition Time Example calculation correction.

EQUATION 9-1: ACQUISITION TIME EXAMPLE

Assumptions: $Temperature = 50°C$ *and external impedance of* $10k\Omega$ *5.0V* V_{DD}

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$
$$= 2\mu s + T_C + [(Temperature - 25°C)(0.05\mu s/°C)]$$

The value for T_C *can be approximated with the following equations:*

$$V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) = V_{CHOLD}$$;[1] V_{CHOLD} *charged to within 1/2 lsb*

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD}$$;[2] V_{CHOLD} *charge response to* $V_{APPLIED}$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right)$$;combining [1] and [2]

Solving for T_C*:*

$$T_C = -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ ln(1/2047)$$
$$= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ ln(0.0004885)$$
$$= 1.37\mu s$$

Therefore:

$$T_{ACQ} = 2\mu s + 1.37\mu s + [(50°C - 25°C)(0.05\mu s/°C)]$$
$$= 4.67\mu s$$

3. Module: MSSP (SPI)

The electrical specification parameter number 70 from Table 17-4 has been modified as follows.

TABLE 17-4: SPI MODE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)								
Param No.	**Symbol**	**Characteristic**		**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
SP70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK$\downarrow$ or SCK$\uparrow$ input		**2.25 * Tcy**	—	—	ns	
SP71*	TscH	SCK input high time (Slave mode)		Tcy + 20	—	—	ns	
SP72*	TscL	SCK input low time (Slave mode)		Tcy + 20	—	—	ns	
SP73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	—	ns	
SP74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
SP75*	TdoR	SDO data output rise time	3.0-5.5V	—	10	25	ns	
			2.0-5.5V	—	25	50	ns	
SP76*	TdoF	SDO data output fall time		—	10	25	ns	
SP77*	TssH2doZ	$\overline{SS}\uparrow$ to SDO output high-impedance		10	—	50	ns	
SP78*	TscR	SCK output rise time (Master mode)	3.0-5.5V	—	10	25	ns	
			2.0-5.5V	—	25	50	ns	
SP79*	TscF	SCK output fall time (Master mode)		—	10	25	ns	
SP80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	3.0-5.5V	—	—	50	ns	
			2.0-5.5V	—	—	145	ns	
SP81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge		Tcy	—	—	ns	
SP82*	TssL2doV	SDO data output valid after $\overline{SS}\downarrow$ edge		—	—	50	ns	
SP83*	TscH2ssH, TscL2ssH	$\overline{SS}\uparrow$ after SCK edge		1.5 Tcy + 40	—	—	ns	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev. A Document (2/2007)

First revision of this document.

Added Module 1: Low-Voltage In-Circuit Serial Programming™ (PIC16F884/883 Silicon Rev. A0); Added Module 2: MSSP (SPI Mode).

Clarifications/Corrections to the Data Sheet – Added Module 1: Product Identification System.

Rev. B Document (5/2007)

Clarifications/Corrections to the Data Sheet – Added Module 2: Electrical Specification - Supply Current.

Rev. C Document (7/2007)

Added Module 3: Analog-to-Digital Converter (ADC) Module.

Rev. D Document (8/2007)

Added Module 4: MSSP (SPI Master Mode), Module 5: MSSP (I^2C Slave Mode) and Module 6: MSSP (I^2C Master Mode).

Rev. E Document (4/2009)

Updated Errata to new format.

Data Sheet Clarification: Added Module 1: Timer1 (Block Diagram); Module 2: Comparator (C2 Block Diagram); Module 3: ADC (Block Diagram); Module 4: Comparator Voltage Reference; Module 5: Comparator Voltage Reference.

Added Module 7: MSSP; Added Module 8: Asynchronous Timer1; Added Module 9: LP/Timer1 Oscillator Operation Below 25°C; Module 10: Timer0 and WDT Prescaler Assignment Spurious Reset.

Rev. F Document (8/2009)

Added Module 11: MSSP (SPI Master Mode); Updated Tables 2, 3, 4.

Data Sheet Clarification: Removed Modules 1, 2, 4 and 5 as the Data Sheet has already been updated according to this version of the errata.

Added Module 2: ADC.

Rev. G Document (12/2012)

Added Module 12: Capture Compare PWM (CCP).

Rev. H Document (8/2013)

Added Module 13: ICSP; Other minor corrections.

Rev. J Document (9/2014)

Data Sheet Clarifications: Added Module 3; Other minor corrections.

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