CS1615
CS1616

Single Stage Dimmable Offline AC/DC Controller for LED Lamps

Features

- Best-in-class Dimmer Compatibility
  - Leading-edge (TRIAC) Dimmers
  - Trailing-edge Dimmers
  - Digital Dimmers (Dimmers with an Integrated Power Supply)
- Flicker-free Dimming
- 0% to 100% Smooth Dimming
- Primary-side Regulation (PSR)
- Active Power Factor Correction (PFC)
  - >0.9 Power Factor
- Constant-current Output
  - Flyback
  - Buck-boost
- Tight LED Current Regulation: Better than ±5%
- Low THD: Less Than 20%
- Up to 90% Efficiency
- Fast Startup
- IEC61000-3-2 Compliant
- Meets NEMA SSL 6 Dimming Standard
  - Closely Matches Incandescent S-curve
- Protection Features
  - Output Open Circuit
  - Output Short Circuit
  - External Overtemperature Using NTC

Overview

The CS1615 and CS1616 are high-performance single stage dimmable offline AC/DC controllers. The CS1615/16 is a cost-effective solution that provides unmatched single- and multi-lamp dimmer-compatibility performance for dimmable LED applications. The CS1615 is designed for 120VAC line voltage applications, and the CS1616 is designed for 230VAC line voltage applications.

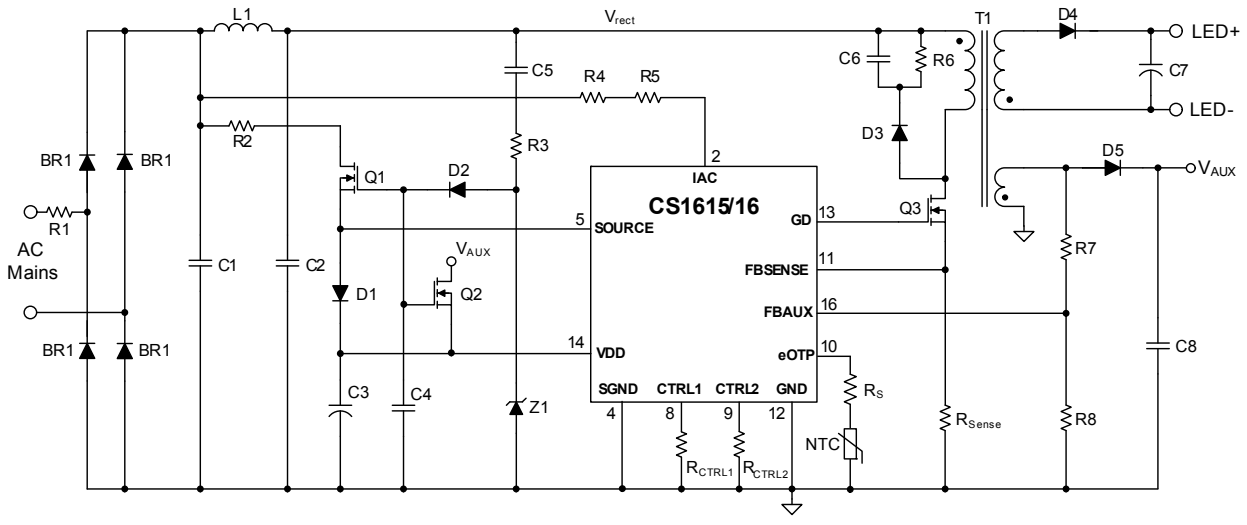
Across a broad range of dimmers, the CS1615/16 provides smooth flicker free dimming, and consistently dims to nearly zero light output, which closely matches the dimming performance of incandescent light bulbs. Cirrus Logic's patent pending approach to dimmer compatibility provides full functionality on a wide range of dimmers, including leading-edge, trailing-edge, and digital dimmers.

Applications

- Retro-fit LED Lamps
- External LED Drivers
- LED Luminaries
- Commercial Lighting

Ordering Information

See **page 14**.



Preliminary Product Information | This document contains information for a product under development. Cirrus Logic reserves the right to modify this product without notice.

1. INTRODUCTION

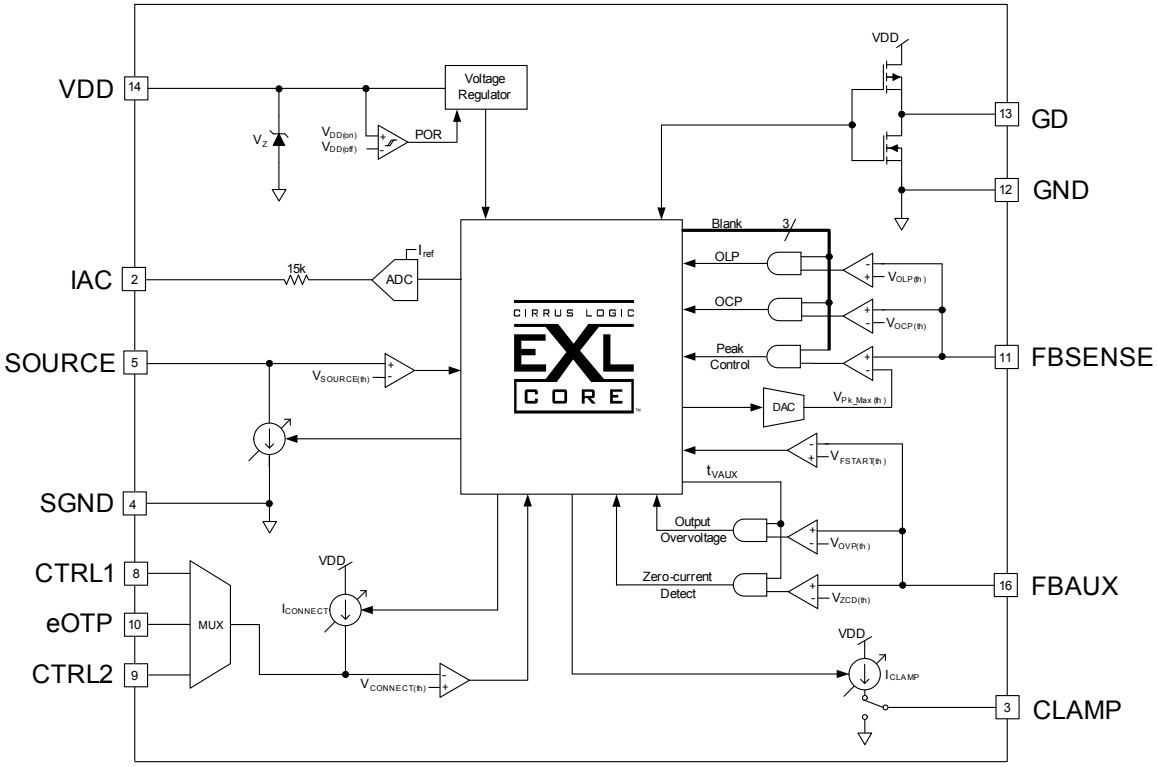


Figure 1. CS1615/16 Block Diagram

A typical schematic using the CS1615/16 IC is shown on the previous page.

Startup current is provided from a patent-pending, external, high-voltage source-follower network. In addition to providing startup current, this unique topology is integral in providing compatibility with digital dimmers by ensuring V_{DD} power is always available to the IC. During normal operation, an auxiliary winding on the flyback transformer or buck-boost inductor back-biases the source-follower circuit and provides steady-state operating current to the IC to improve system efficiency.

Rectified input voltage V_{rect} is sensed as a current into pin IAC and is used to control the adaptive dimmer-compatibility algorithm and to extract the phase of the input voltage for output dimming control. The SOURCE pin is used to provide a control signal for the high-voltage source-follower circuit during Leading-edge Mode and Trailing-edge Mode; it also provides the current during startup.

The digital dual-mode controller is implemented with peak-current mode primary-side regulation, which eliminates the need for additional components to provide feedback from the secondary and reduces system cost and complexity. Voltage across a user-selected resistor is sensed through pin FBSENSE to control the peak current of the primary-side inductor. Leading-edge and trailing-edge blanking on pin FBSENSE prevents false triggering. The required target LED current and average flyback transformer and buck-boost inductor input current are set by attaching resistors R_{CTRL1} and R_{CTRL2} on pins CTRL1 and CTRL2, respectively. The controller ensures half line-cycle averaged constant output current.

Pin FBAUX is used for zero-current detection to ensure quasi-resonant switching of the single stage output. When an external negative temperature coefficient (NTC) thermistor is connected to pin eOTP, the CS1615/16 monitors the system temperature, allowing the controller to reduce the output current of the system. If the temperature reaches a designated high set point, the IC is shut down and stops switching.

2. PIN DESCRIPTION

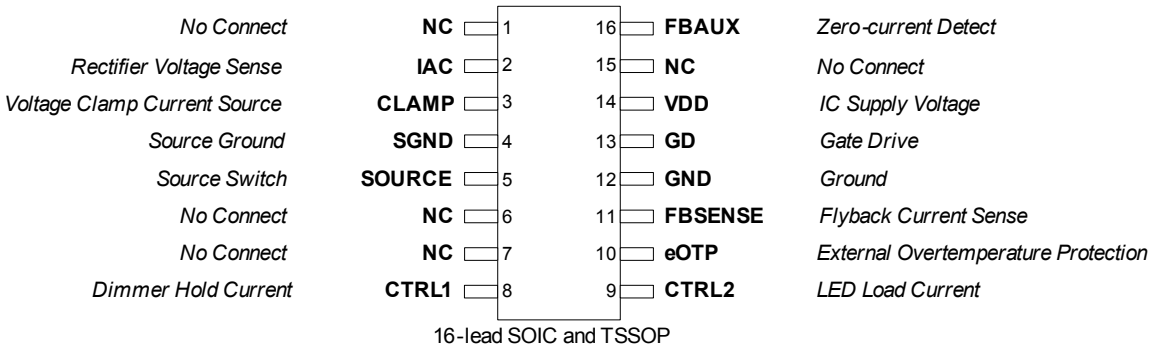


Figure 2. CS1615/16 Pin Assignments

Pin Name	Pin #	I/O	Description
NC	1	IN	**No Connect** — Leave pin unconnected.
IAC	2	IN	**Rectifier Voltage Sense** — A current proportional to the rectified line voltage is fed into this pin. The current is measured with an A/D converter.
CLAMP	3	OUT	**Voltage Clamp Current Source** — Connect to a voltage clamp circuit on the source-switched dimmer-compatibility circuit.
SGND	4	PWR	**Source Ground** — Common reference current return for the SOURCE pin.
SOURCE	5	IN	**Source Switch** — Connected to the source of the source-switched external high-voltage FET.
NC	6	IN	**No Connect** — Connect this pin to VDD using a 47kΩ pull-up resistor.
NC	7	IN	**No Connect** — Connect this pin to VDD using a 47kΩ pull-up resistor.
CTRL1	8	IN	**Dimmer Hold Current** — Connect a resistor to this pin to set the minimum input current being pulled by the flyback/buck-boost stage.
CTRL2	9	IN	**LED Load Current** — Connect a resistor to this pin to set the LED current.
eOTP	10	IN	**External Overtemperature Protection** — Connect an external NTC thermistor to this pin, allowing the internal A/D converter to sample the change to NTC resistance.
FBSENSE	11	IN	**Feedback Current Sense** — The current flowing in the power FET is sensed across a resistor. The resulting voltage is applied to this pin and digitized for use by the computational logic to determine the FET's duty cycle.
GND	12	PWR	**Ground** — Common reference. Current return for both the input signal portion of the IC and the gate driver.
GD	13	OUT	**Gate Drive** — Gate drive for the power FET.
VDD	14	PWR	**IC Supply Voltage** — Connect a storage capacitor to this pin to serve as a reservoir for operating current for the device, including the gate drive current to the power transistor.
NC	15	-	**No Connect** — Leave pin unconnected.
FBAUX	16	IN	**Zero-current Detect** — Connect to the flyback/buck-boost inductor auxiliary winding for demagnetization current zero-crossing detection.

3. CHARACTERISTICS AND SPECIFICATIONS

3.1 Electrical Characteristics

Typical characteristics conditions:
- T_A = 25 °C, V_{DD} = 12 V, GND = 0 V
- All voltages are measured with respect to GND.
- Unless otherwise specified, all currents are positive when flowing into the IC.

Minimum/Maximum characteristics conditions:
- T_J = -40 °C to +125 °C, V_{DD} = 11 V to 17 V, GND = 0 V

Parameter	Condition	Symbol	Min	Typ	Max	Unit
VDD Supply Voltage						
Operating Range	After Turn-on	V_{DD}	11	-	17	V
Turn-on Threshold Voltage	V_{DD} Increasing	$V_{ST(th)}$	-	8.5	-	V
Turn-off Threshold Voltage (UVLO)	V_{DD} Decreasing	$V_{STP(th)}$	-	7.5	-	V
Zener Voltage (Note 1)	I_{DD} = 20 mA	V_Z	18.5	-	19.8	V
VDD Supply Current						
Startup Supply Current	$V_{DD} < V_{ST(th)}$	I_{ST}	-	-	200	µA
Operating Supply Current (Note 2)	C_L = 0.25 nF, $f_{sw} \leq$ 70 kHz		-	4.5	-	mA
Reference						
Reference Current CS1615 CS1616	 V_{rect} = 200 V V_{rect} = 400 V	I_{ref}	 - -	 133 133	 - -	 µA µA
Zero-current Detect						
FBZCD Threshold		$V_{FBZCD(th)}$	-	200	-	mV
FBZCD Blanking		t_{FBZCB}	-	2	-	µs
ZCD Sink Current (Note 3)		I_{ZCD}	-2	-	-	mA
FBAUX Upper Voltage	I_{ZCD} = 1 mA		-	V_{DD}+0.6	-	V
Current Sense						
Max Peak Control Threshold		$V_{Pk\_Max(th)}$	-	1.4	-	V
Leading-edge Blanking		t_{LEB}	-	550	-	ns
Delay to Output			-	-	100	ns
Pulse Width Modulator						
Minimum On Time			-	0.55	-	µs
Maximum On Time			-	12.8	-	µs
Minimum Switching Frequency		$t_{FB(Min)}$	-	6	-	kHz
Maximum Switching Frequency		$t_{FB(Max)}$	-	200	-	kHz
Gate Driver						
Output Source Resistance		Z_{OUT}	-	24	-	Ω
Output Sink Resistance		Z_{OUT}	-	11	-	Ω
Rise Time	C_L = 0.25 nF		-	-	30	ns
Fall Time	C_L = 0.25 nF		-	-	20	ns

Parameter		Condition	Symbol	Min	Typ	Max	Unit
Flyback/Buck-boost Protections							
Overcurrent Protection (OCP)	(Note 4)		$V_{OCP(th)}$	-	1.69	-	V
Overvoltage Protection (OVP)	(Note 5)		$V_{OVP(th)}$	-	1.25	-	V
Open Loop Protection (OLP)	(Note 4)		$V_{OLP(th)}$	-	200	-	mV
External Overtemperature Protection (eOTP)							
Pull-up Current Source – Maximum			$I_{CONNECT}$	-	80	-	µA
Conductance Accuracy	(Note 6)			-	-	±5	%
Conductance Offset	(Note 6)			-	±250	-	nS
Current Source Voltage Threshold			$V_{CONNECT(th)}$	-	1.25	-	V
Internal Overtemperature Protection (iOTP)							
Thermal Shutdown Threshold	(Note 7)		T_{SD}	-	135	-	ºC
Thermal Shutdown Hysteresis	(Note 7)		$T_{SD(Hy)}$	-	14	-	ºC

Notes:
1. The CS1615/16 has an internal shunt regulator that limits the voltage on the VDD pin. Shunt regulation voltage V_Z is defined in the *VDD Supply Voltage* section on *page 4*.
2. For test purposes, load capacitance C_L is connected to pin GD and is equal to 0.25nF.
3. External circuitry should be designed to ensure that the ZCD current drawn from the internal clamp diode when it is forward biased does not exceed specification.
4. Protection is implemented using pin FBSENSE. See the *CS1615/16 Block Diagram* on *page 2*.
5. Protection is implemented using pin FBAUX. See the *CS1615/16 Block Diagram* on *page 2*
6. The conductance is specified in Siemens (S or 1/Ω). Each LSB of the internal ADC corresponds to 250nS or one parallel 4MΩ resistor. Full scale corresponds to 256 parallel 4MΩ resistors or 15.625kΩ.
7. Specifications are guaranteed by design and are characterized and correlated using statistical process methods.

3.2 Thermal Resistance

Symbol	Parameter		SOIC	TSSOP	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance	2 Layer PCB 4 Layer PCB	119 105	138 103	°C/W °C/W
θ_{JC}	Junction-to-Case Thermal Impedance	2 Layer PCB 4 Layer PCB	50 44	44 28	°C/W °C/W

3.3 Absolute Maximum Ratings

Characteristics conditions:

All voltages are measured with respect to GND.

Pin	Symbol	Parameter		Value	Unit
14	V_{DD}	IC Supply Voltage		18.5	V
1,2,8,9, 10,11,16		Analog Input Maximum Voltage		-0.5 to (V_{DD}+0.5)	V
1,2,8,9, 10,11,16		Analog Input Maximum Current		5	mA
13	V_{GD}	Gate Drive Output Voltage		-0.3 to (V_{DD}+0.3)	V
13	I_{GD}	Gate Drive Output Current		-1.0 / +0.5	A
5	I_{SOURCE}	Current into Pin		1.1	A
3	I_{CLAMP}	Clamp Output Current		15	mA
-	P_D	Total Power Dissipation		400	mW
-	T_J	Junction Temperature Operating Range	(Note 8)	-40 to +125	°C
-	T_{Stg}	Storage Temperature Range		-65 to +150	°C
All Pins	ESD	Electrostatic Discharge Capability	Human Body Model Charged Device Model	2000 500	V V

Note: 8. Long-term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation at the rate of 50 mW / °C for variation over temperature.

WARNING:

Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

4. TYPICAL PERFORMANCE PLOTS

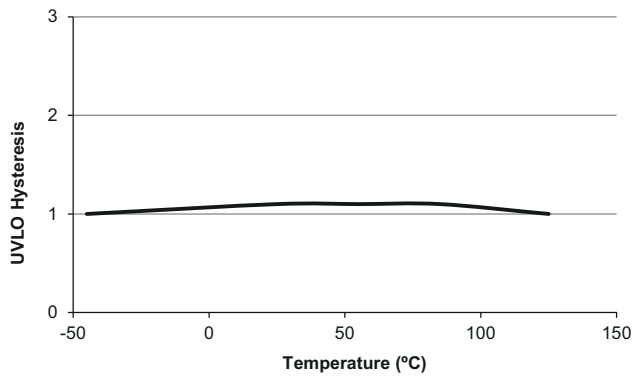


Figure 3. UVLO Characteristics

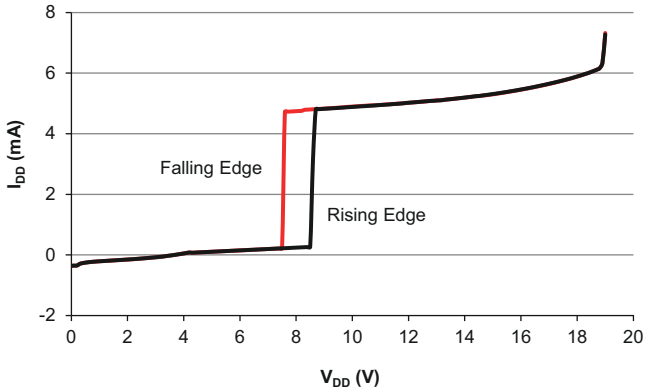


Figure 4. Supply Current vs. Voltage

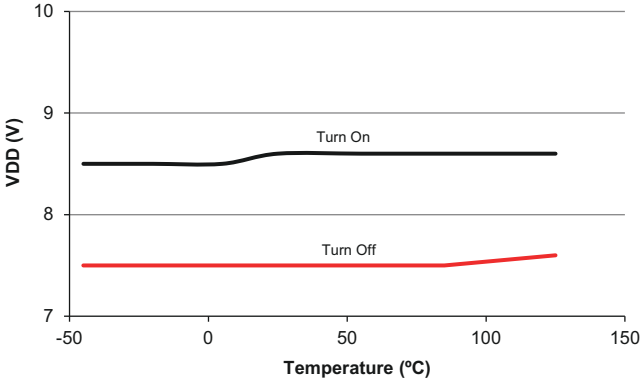


Figure 5. Turn On/Off Threshold Voltage vs. Temperature

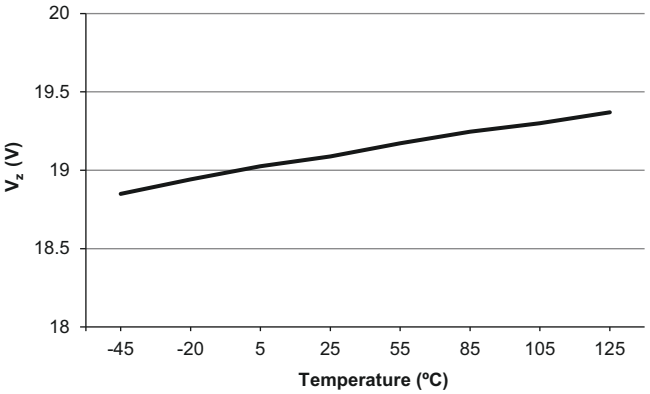


Figure 6. Zener Voltage vs. Temperature

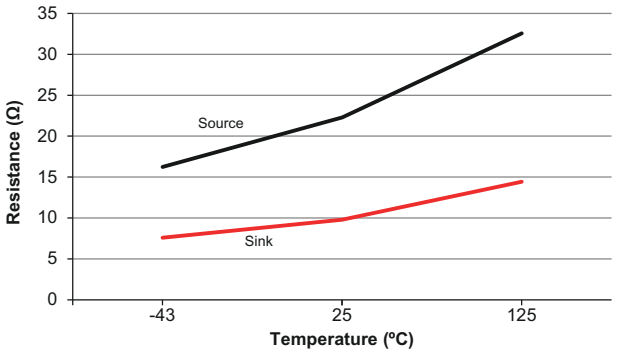


Figure 7. Gate Drive Resistance vs. Temperature

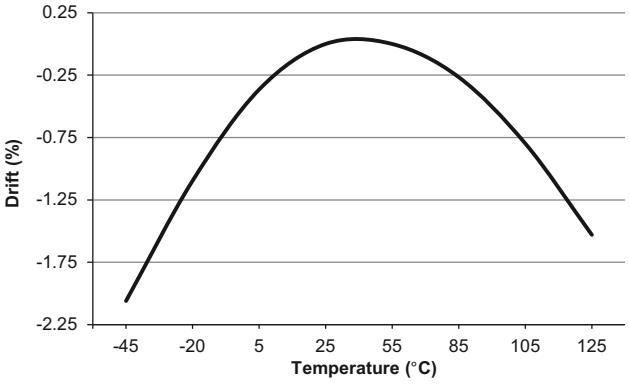


Figure 8. Reference Current (I_{ref}) Drift vs. Temperature

5. GENERAL DESCRIPTION

5.1 Overview

The CS1615 and CS1616 are high-performance single stage dimmable offline AC/DC controllers. The CS1615/16 is a cost-effective solution that provides unmatched single- and multi-lamp dimmer-compatibility performance for dimmable LED applications. The CS1615 is designed for 120VAC line voltage applications, and the CS1616 is designed for 230VAC line voltage applications.

The CS1615/16 features Cirrus Logic's proprietary adaptive dimmer-compatibility algorithm that enables flicker-free operation from 0% to 100% output current with leading-edge dimmers, trailing-edge dimmers, and digital dimmers (dimmers with an integrated power supply). In addition, the CS1615/16 is configurable for isolated and non-isolated topologies.

5.2 IC Startup

A high-voltage source-follower circuit is used to deliver startup current to the IC. During steady-state operation, an auxiliary winding on the transformer/inductor biases this circuit to an off state to improve system efficiency, and all IC supply current is provided from the auxiliary winding. The patent-pending technology of the high-voltage source-follower circuit enables system compatibility with digital dimmers (dimmers containing an internal power supply) by providing a continuous path for the dimmer's power supply to recharge during its off state. During steady-state operation, high-voltage FET Q1 in this circuit is source-controlled by a variable internal current source on the SOURCE pin to create the dimmer-compatibility circuit. A Schottky diode with a forward voltage of less than 0.6V is recommended for D1. Schottky diode D1 will limit inrush current through the internal diode, preventing damage to the IC.

During initial power-up, the IC executes a fast startup algorithm, which drives the converter with peak currents that are above normal to charge the output capacitor. Once the output capacitor reaches a defined voltage, the IC drives the converter with nominal peak currents until normal operation is achieved.

5.3 IC Operation

5.3.1 Dimmer Detection

The CS1615/16 dimmer switch detection algorithm determines if a non-dimming switch, a leading-edge dimmer switch, or a trailing-edge dimmer switch controls the solid-state lighting (SSL) system. For each type of switch, the IC uses a different operating mode: for a non-dimming switch, No-dimmer Mode is used; for a leading-edge dimmer switch, Leading-edge Mode is used; for a trailing-edge dimmer switch, Trailing-edge Mode is used. As a result, the overall performance is optimized in terms of power losses, efficiency, power factor, THD, and dimmer compatibility.

When the IC completes UVLO, it executes in Leading-edge Mode until the dimmer switch detection algorithm determines the appropriate operating mode for the IC. The dimmer switch detection algorithm uses the input line voltage slope and dimmer phase angle to determine the operating mode that matches the type of dimmer switch in the system. From there on, it periodically learns the dimmer type and can change the operating mode if the type of dimmer switch changes.

5.3.1.1 No-dimmer Mode

If the CS1615/16 determines that the line is not phase cut by a dimmer switch, the IC operates the flyback/buck-boost in PFC mode to achieve a power factor greater than 0.9 while regulating the load current to a level set by resistor R_{CTRL2}. In addition, a No-dimmer Mode algorithm is applied to the source-controlled dimmer-compatibility circuit for optimal performance, including less than 20% of THD and highest possible overall efficiency.

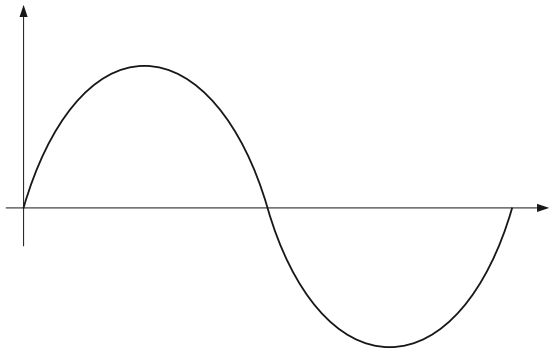


Figure 9. No-dimmer Mode Waveform

5.3.1.2 Leading-edge Mode

If the CS1615/16 determines that the line is phase cut by a leading-edge dimmer switch, the IC operates the flyback/buck-boost in Dimmer Mode and the IC sets the dimmer firing current as well as the attach current using a source-controlled dimmer-compatibility circuit for stable TRIAC dimmer operation.

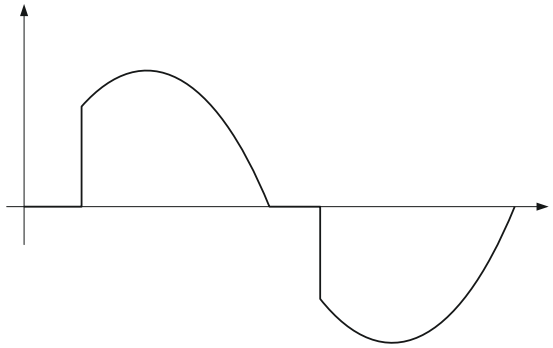


Figure 10. Leading-edge Mode Phase-cut Waveform

5.3.1.3 Trailing-edge Mode

If the CS1615/16 determines that the line is phase cut by a trailing-edge dimmer switch, the IC operates the flyback/buck-boost in Dimmer Mode. The IC charges the capacitor in the

dimmer switch on the falling edge of the input voltage using a source-controlled dimmer-compatibility circuit.

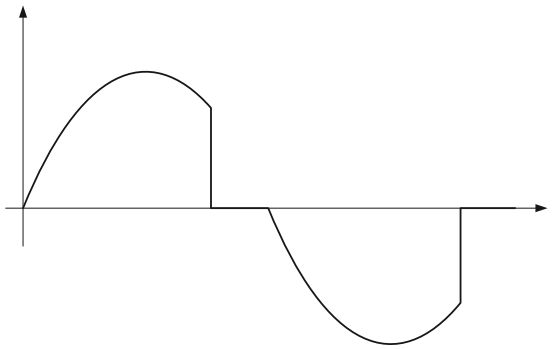


Figure 11. Trailing-edge Mode Phase-cut Waveform

5.3.2 Switch Overpower Protection

To prevent excessive power dissipation on the source-switched FET Q1, the CS1615/16 monitors voltage across Q1 and current flow through Q1 to calculate average power dissipation. If the calculated power exceeds the overpower protection threshold a fault condition occurs. The IC output is disabled and the controller attempts to restart after approximately thirty seconds.

5.4 Voltage Clamp Circuit

To keep trailing-edge dimmer switches conducting and from misfiring, the dimmer switch internal capacitor has to be charged quickly around the trailing edge of the phase-cut waveform. In addition to the dimmer compatible circuit, an optional clamp circuit provides a high-current sinking path for delivering the required amount of charge onto the dimmer switch capacitor in a short amount of time.

The CS1615/16 provides active clamp circuitry on the CLAMP pin, as shown in Figure 12.

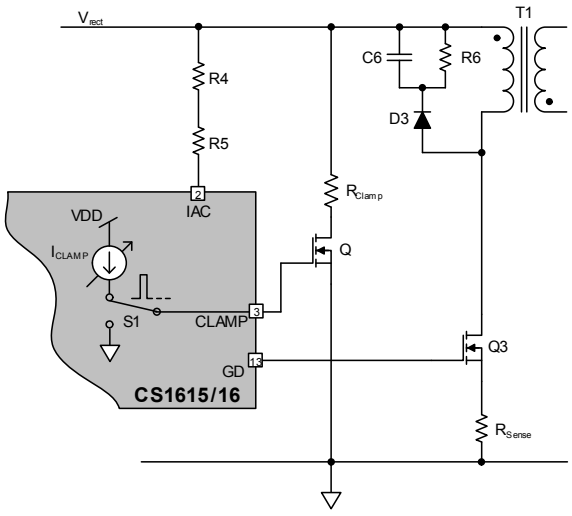


Figure 12. CLAMP Pin Model

5.4.1 Clamp Overpower Protection

The CS1615/16 clamp overpower protection (COP) control logic averages the 'ON' time of the clamp circuit. If the output of the averaging logic exceeds 10%, a COP event is actuated. The clamp circuit is disabled as well as the flyback/buck-boost controller and the dimmer-compatibility circuit. The COP fault state is not cleared until the power to the IC is recycled.

5.5 Dimmer Angle Extraction and the Dim Mapping Algorithm

When operating with a dimmer, the dimming signal is extracted in the time domain and is proportional to the conduction angle of the dimmer. A control variable is passed to the quasi-resonant flyback/buck-boost controller to achieve a wide range of output currents.

5.6 Dual-mode Flyback/Buck-boost

The CS1615/16 is configurable for isolated or non-isolated topologies using a flyback transformer or buck-boost inductor, respectively. The CS1615/16 controls the dual-mode flyback/buck-boost to satisfy the dimmer hold current requirement in Dimmer Mode and provide power factor correction in No-dimmer Mode. The dual-mode ensures a minimum average input current greater than the required dimmer hold current when behind a dimmer and shapes the line current when not behind a dimmer to provide power factor correction. It also ensures half line-cycle averaged constant output current.

Figure 13 illustrates the dual-mode flyback topology. The CS1615/16 regulates output current using primary-side control, which eliminates the need for opto-coupler feedback. The control loop operates in peak current control mode. Demagnetization time of the transformer is sensed by the FBAUX pin using an auxiliary winding and is used as an input to the control loop.

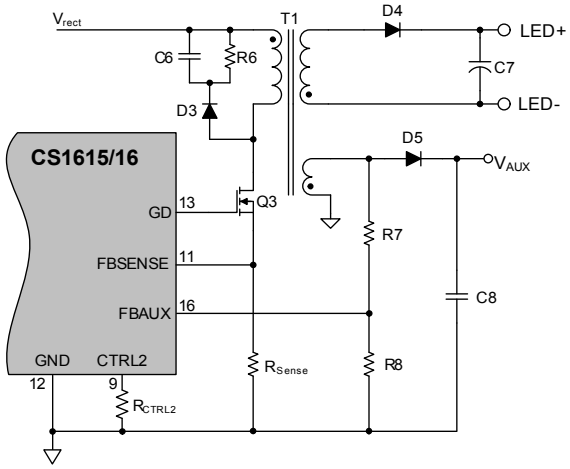


Figure 13. Flyback Model

Figure 14 illustrates the dual-mode buck-boost topology. The CS1615/16 regulates the output current by controlling the peak current to ensure that the target output charge is achieved every half line-cycle. Demagnetization time of the inductor is sensed by the FBAUX pin using an auxiliary winding and is used as an input to the control loop.

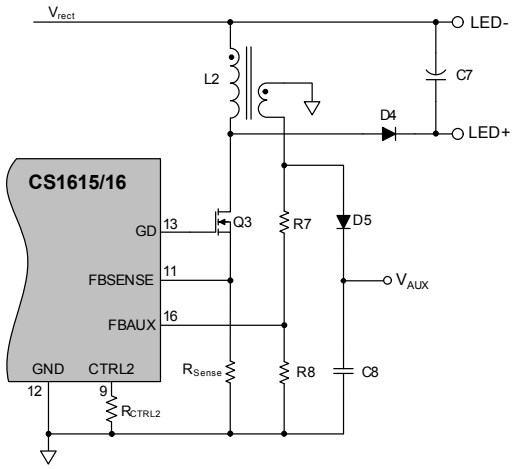


Figure 14. Buck-boost Model

5.6.1 Primary-Side Current Control

All input current shaping and output power transfer is attained using a peak current control algorithm. Demagnetization time of the primary inductor is sensed by the FBAUX pin using an auxiliary winding and is used as an input to the control algorithm. The values obtained from R_{CTRL1} and R_{CTRL2} are the other inputs to the control algorithm that help shape the input current and control the LED current, respectively.

5.6.2 Output Current Regulation

The CS1615/16 regulates output current by controlling the charge transferred over a half line-cycle. The full-scale output current target is set using resistor R_{CTRL2}, which is connected on pin CTRL2. This pin is sampled periodically by an ADC. The value of this resistor can be determined using Equation 1.

$$R_{CTRL2} = \frac{1.4V \times N \times 4M\Omega}{1.25 \times 511 \times R_{Sense} \times I_{OUT}} \quad [Eq.1]$$

where,

N = turns ratio

I_{OUT} = current through LED at maximum output

R_{Sense} = resistor attached to pin FBSENSE

When designing a buck-boost topology the turns ratio N is set to one.

The CS1615/16 uses the value obtained from the resistor along with the phase-cut and line-cycle period information to determine the corresponding target full-scale output charge. The IC controls the inductor switching frequency and peak current to ensure that the target output charge is achieved every half line-cycle, thus regulating the output current.

5.6.3 Input Current Shaping

The CS1615/16 shapes the input current by controlling the peak primary current and the flyback/buck-boost switching frequency. It shapes the currents differently when behind a dimmer compared to when not behind a dimmer.

5.6.3.1 Operation Behind a Dimmer

Operating behind a dimmer, the CS1615/16 controls the switching frequency to ensure that the average input current is greater than the dimmer hold current requirement. The dimmer hold current level is sensed using resistor R_{CTRL1} on pin CTRL1, which is sampled periodically by an ADC. The value of this resistor can be determined using the formula shown in Equation 2.

$$R_{CTRL1} = \frac{1.4V \times 4M\Omega}{511 \times I_{IN(CC)} \times R_{Sense}} \quad [Eq.2]$$

where,

$I_{IN(CC)}$ = constant input current used when designing circuit

R_{Sense} = resistor attached to pin FBSENSE

5.6.3.2 Operation in No-dimmer Mode

Operating in No-dimmer Mode, the CS1615/16 controls the switching frequency to ensure that the average input current follows the line voltage to provide power factor correction. In No-dimmer Mode the controller is designed to operate in quasi-resonant mode to improve efficiency.

5.6.4 Max Primary-side Switching Current

Maximum primary-side switching current $I_{PK(max)}$ is set using resistor R_{Sense} connected to pin FBSENSE of the CS1615/16. The maximum primary-side switching current can be calculated using Equation 3.

$$I_{PK(max)} = \frac{1.4}{R_{Sense}} \quad [Eq.3]$$

5.6.5 Auxiliary Winding Configuration

The auxiliary winding is used for zero-current detection (ZCD), overvoltage protection (OVP), fast startup, and the steady-state power supply. The voltage on the auxiliary winding is sensed through pin FBAUX of the CS1615/16 for zero-current detection, overvoltage protection, and fast startup. The auxiliary winding is also used to provide the steady-state power supply to the CS1615/16.

5.6.6 Output Open Circuit Protection

Output open circuit protection and output overvoltage protection (OVP) are implemented by monitoring the output voltage through the transformer auxiliary winding. If the voltage on the FBAUX pin exceeds a threshold $V_{OVP(th)}$ of 1.25V, a fault condition occurs. The IC output is disabled and the controller attempts to restart after approximately one second.

5.6.7 Overcurrent Protection

Overcurrent protection (OCP) is implemented by monitoring the voltage across the sense resistor. If this voltage exceeds a threshold $V_{OCP(th)}$ of 1.69V, a fault condition occurs. The IC output is disabled and the controller attempts to restart after approximately one second.

5.6.8 Open Loop Protection

Open loop protection (OLP) and sense resistor short protection are implemented by monitoring the voltage across the resistor. If the voltage on pin FBSENSE does not reach the protection threshold $V_{OLP(th)}$ of 200mV, the IC output is disabled, and the controller attempts to restart after approximately one second.

5.7 Overtemperature Protection

The CS1615/16 incorporates internal overtemperature protection (iOTP) and the ability to connect an external overtemperature sense circuit for IC protection. Typically, an NTC thermistor is used.

5.7.1 Internal Overtemperature Protection

Internal overtemperature protection (iOTP) is activated, and switching is disabled when the die temperature of the devices exceeds 135°C. There is a hysteresis of about 14°C before resuming normal operation.

5.7.2 External Overtemperature Protection

The external overtemperature protection (eOTP) pin is used to implement overtemperature protection. A negative temperature coefficient (NTC) thermistor resistive network is connected to pin eOTP, usually in the form of a series combination of a resistor R_S and a thermistor R_{NTC} (see Figure 15). The CS1615/16 cyclically samples the resistance connected to pin eOTP.

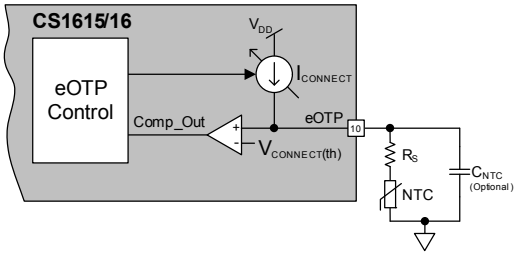


Figure 15. eOTP Functional Diagram

The total resistance on the eOTP pin gives an indication of the temperature and is used in a digital feedback loop to adjust current $I_{CONNECT}$ into the NTC and series resistor R_S to maintain a constant reference voltage $V_{CONNECT(th)}$ of 1.25V. Current $I_{CONNECT}$ is generated from a controlled current source with a full-scale current of 80µA. When the loop is in equilibrium, the voltage on the eOTP pin fluctuates around $V_{CONNECT(th)}$. A resistance ADC is used to generate $I_{CONNECT}$. The ADC output is filtered to suppress noise and compared against a reference that corresponds to 125°C. A second low-pass filter with a time constant of two seconds filters the ADC output and is used to scale down the internal dim level of the system (and hence LED current I_{LED}) if the temperature exceeds 95°C. The large time constant for this filter ensures that the dim scaling does not happen spontaneously and is not noticeable (suppress spurious glitches). The eOTP tracking circuit is designed to function accurately with external capacitance up to 470pF.

The tracking range of this resistance ADC is approximately 15.5kΩ to 4MΩ. The series resistor R_S is used to adjust the resistance of the NTC to fall within the ADC tracking range, allowing the entire dynamic range of the ADC to be well used. The CS1615/16 recognizes a resistance (R_S+R_{NTC}) equal to 20.3kΩ, which corresponds to a temperature of 95°C, as the beginning of an overtemperature dimming event and starts reducing the power dissipation. The output current is scaled until the series resistance (R_S+R_{NTC}) value reaches 16.26kΩ (125°C). Beyond this temperature, the IC shuts down until the resistance (R_S+R_{NTC}) rises above 19.23kΩ. This is not a latched protection state, and the ADC keeps tracking the temperature in this state in order to clear the fault state once the temperature drops below 110°C.

When exiting reset, the chip enters startup and the ADC quickly (<5ms) tracks the external temperature to check if it is below the 110°C reference code before the controller is powered up. If this check fails, the chip will wait until this condition becomes true before initializing the rest of the system.

For example, a 14kΩ (±1% tolerance) series resistor is required to allow measurements of up to 130°C to be within the eOTP tracking range when a 100kΩ NTC with a Beta of 4275. If the temperature exceeds 95°C, thermistor R_{NTC} is approximately 6.3kΩ and series resistor R_S is 14kΩ, so the eOTP pin has a total resistance of 20.3kΩ. The eOTP pin initiates protective dimming action by reducing the power dissipation. At 125°C the thermistor R_{NTC} has 2.26kΩ plus a series resistor R_S equal to 14kΩ present a resistance of 16.26kΩ at the eOTP pin reaching the point where a thermal shutdown fault intervenes. The CS1615/16 will continue to monitor pin eOTP and once the series resistor R_S plus the thermistor R_{NTC} rises above 19.23kΩ the device will resume power conversion (see Figure 16).

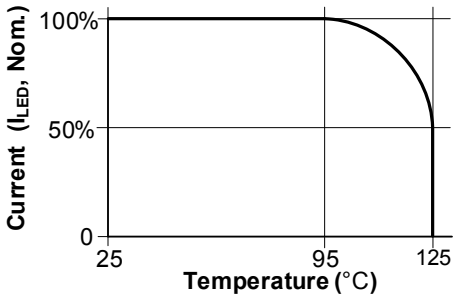
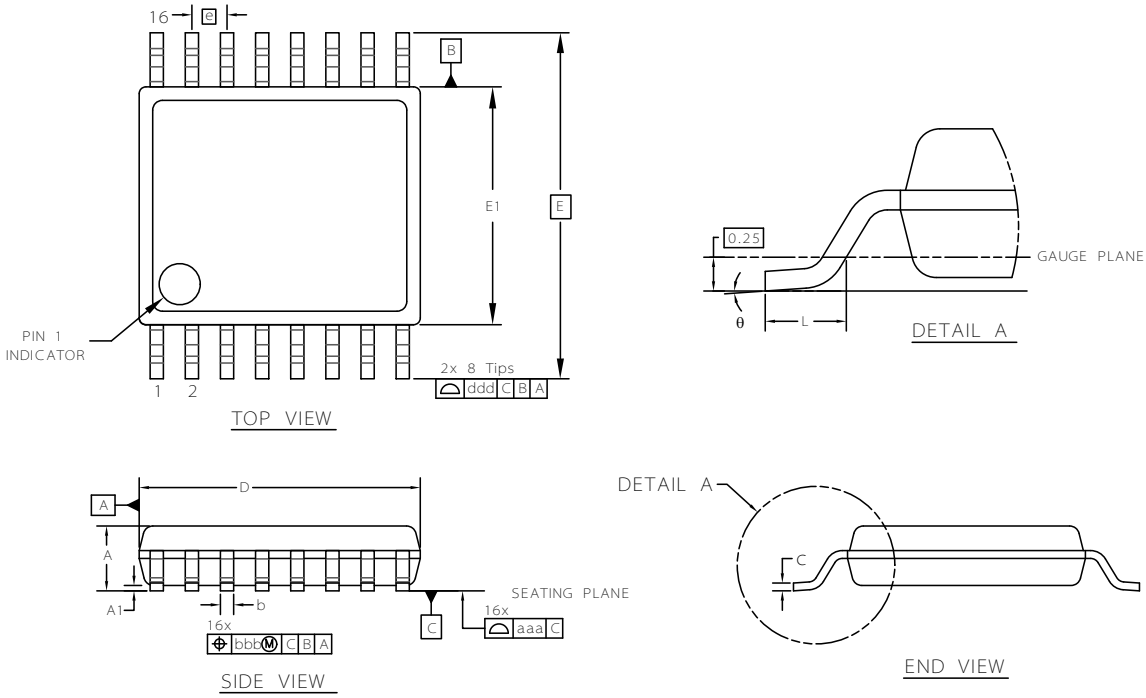


Figure 16. eOTP Temperature vs. Impedance

If the external overtemperature protection feature is not required, connect the eOTP pin to GND using a 50kΩ-to-500kΩ resistor to disable the eOTP feature.

6. PACKAGE DRAWING

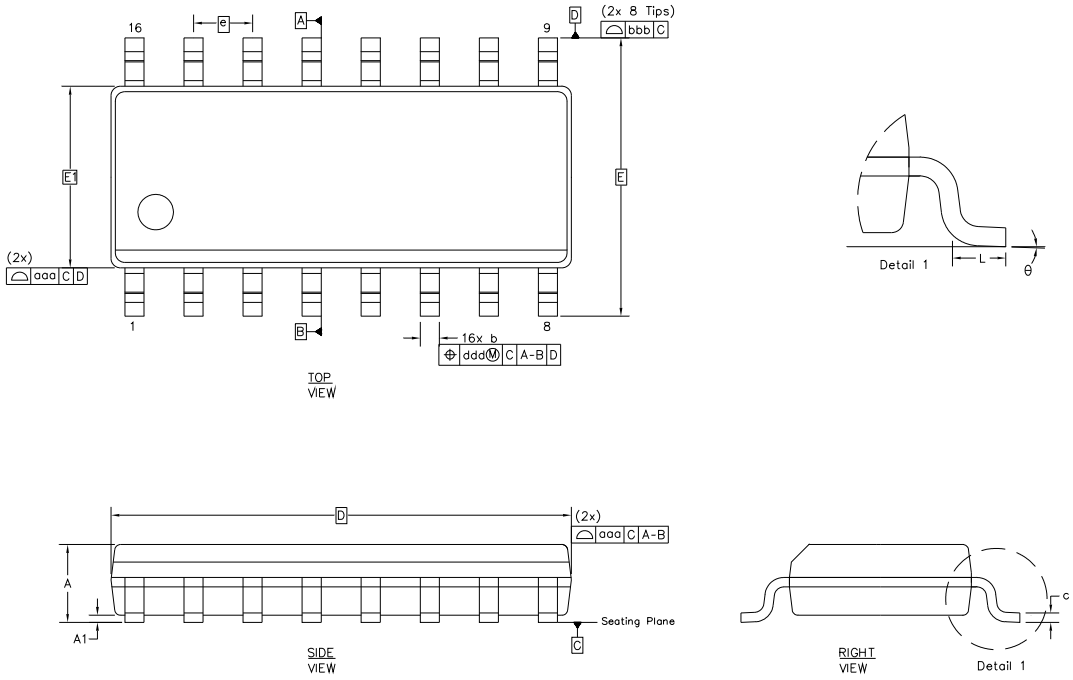
16-PIN TSSOP (173 MIL BODY)



	mm			inch		
Dimension	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	- -	- -	1.20	- -	- -	0.047
A1	0.05	- -	0.15	0.002	- -	0.006
b	0.19	- -	0.30	0.007	- -	0.012
C	0.09	- -	0.20	0.004	- -	0.008
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.40 BSC			0.252 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0°	- -	8°	0°	- -	8°
aaa	0.10			0.004		
bbb	0.10			0.004		
ddd	0.20			0.008		

1. Controlling dimensions are in millimeters.
2. Dimensioning and tolerances per ASME Y14.5M.
3. This drawing conforms to JEDEC outline MO-153, variation AB.
4. Recommended reflow profile is per JEDEC/IPC J-STD-020.

16-PIN SOICN (150 MIL BODY)



	mm			inch		
Dimension	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	- -	- -	1.75	- -	- -	0.069
A1	0.10	- -	0.25	0.004	- -	0.010
b	0.31	- -	0.51	0.012	- -	0.020
c	0.10	- -	0.25	0.004	- -	0.010
D	9.90 BSC			0.390 BSC		
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
L	0.40	- -	1.27	0.016	- -	0.050
Θ	0°	- -	8°	0°	- -	8°
aaa	0.10			0.004		
bbb	0.25			0.010		
ddd	0.25			0.010		

Notes:
1. Controlling dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M.
3. This drawing conforms to JEDEC outline MS-012, variation AC for standard 16 SOICN narrow body.
4. Recommended reflow profile is per JEDEC/IPC J-STD-020.

7. ORDERING INFORMATION

Ordering Number	Container	AC Line Voltage	Temperature	Package
CS1615-FSZ	Bulk	120VAC	-40 °C to +125 °C	16-lead SOICN, Lead (Pb) Free
CS1615-FSZR	Tape & Reel			
CS1616-FSZ	Bulk	230VAC	-40 °C to +125 °C	16-lead SOICN, Lead (Pb) Free
CS1616-FSZR	Tape & Reel			
CS1615-FZZ	Bulk	120VAC	-40 °C to +125 °C	16-lead TSSOP, Lead (Pb) Free
CS1615-FZZR	Tape & Reel			
CS1616-FZZ	Bulk	230VAC	-40 °C to +125 °C	16-lead TSSOP, Lead (Pb) Free
CS1616-FZZR	Tape & Reel			

8. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Part Number	Peak Reflow Temp	MSL Rating[a]	Max Floor Life[b]
CS1615-FSZ	260 °C	3	7 Days
CS1616-FSZ	260 °C	3	7 Days
CS1615-FZZ	260 °C	3	7 Days
CS1616-FZZ	260 °C	3	7 Days

a.MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

b.Stored at 30°C, 60% relative humidity.

REVISION HISTORY

Revision	Date	Changes
T1	JUN 2012	Initial release.
PP1	JUL 2012	Corrected typographical errors.
PP2	SEP 2012	Clarified context and corrected typographical errors.
PP3	OCT 2012	Clarified context.
PP4	JAN 2013	Buck-boost content added, and clarified context.
PP5	APR 2013	Context clarification.

Contacting Cirrus Logic Support

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