THE DATASHEET OF

STK14C88-NF35

STK14C88

32Kx8 AutoStore nvSRAM

Features

- 25, 35, 45 ns Read Access and R/W Cycle Time
- Unlimited Read/Write Endurance
- Automatic Nonvolatile STORE on Power Loss
- Nonvolatile STORE Under Hardware or Software Control
- Automatic RECALL to SRAM on Power Up
- Unlimited RECALL Cycles
- 1 Million STORE Cycles
- 100-Year Nonvolatile Data Retention
- Single 5V±10% Power Supply
- Commercial, Industrial, Military Temperatures
- 32-Pin 300 mil SOIC (RoHS-Compliant)
- 32-Pin CDIP and LCC Packages

Description

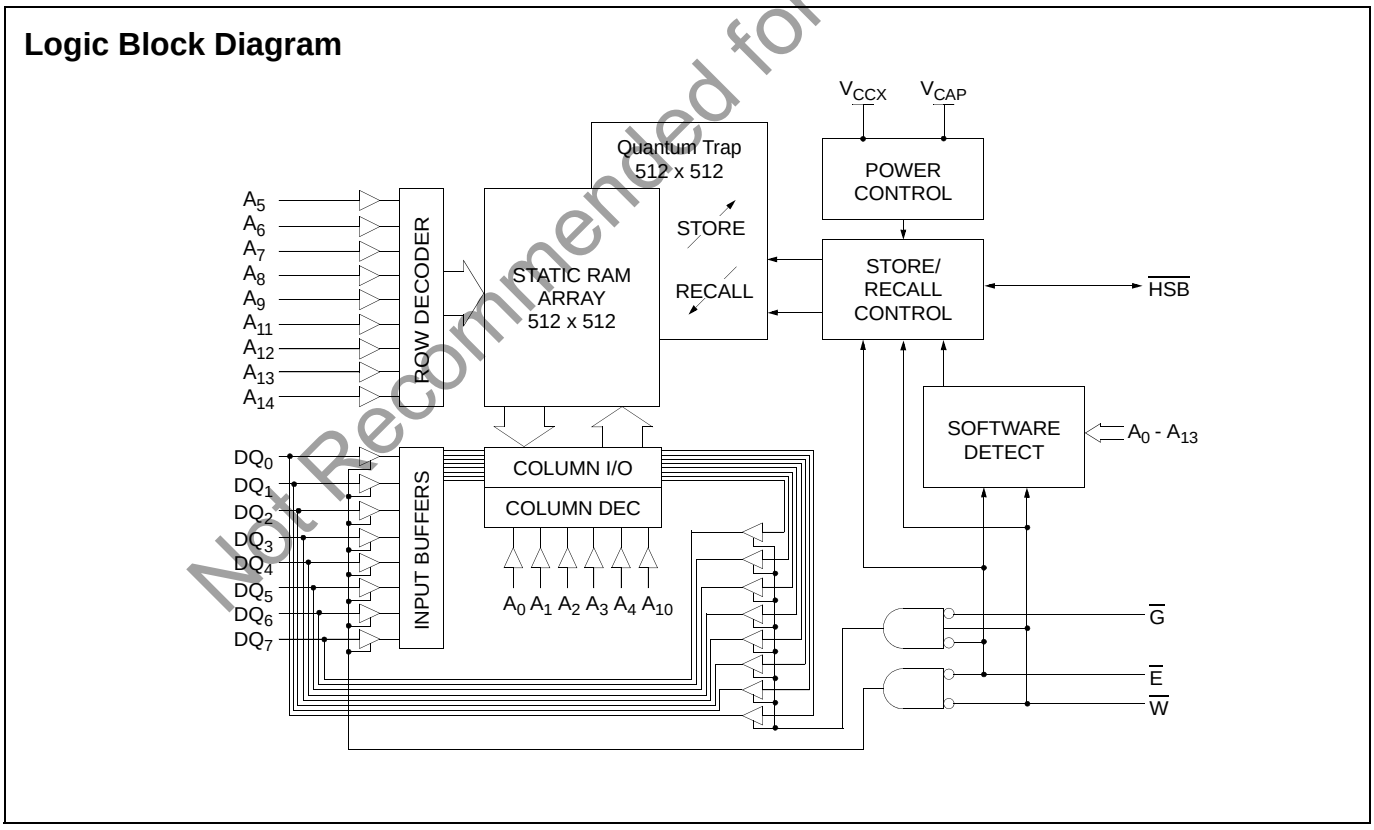
The Cypress STK14C88 is a 256 Kb fast static RAM with a nonvolatile Quantum Trap storage element included with each memory cell.

The SRAM provides the fast access and cycle times, ease of use, and unlimited read and write endurance of a normal SRAM.

Data automatically transfers to the nonvolatile storage cells when power loss is detected (the STORE operation). On power up, data is automatically restored to the SRAM (the RECALL operation). Both STORE and RECALL operations are also available under software control.

The Cypress nvSRAM is the first monolithic nonvolatile memory to offer unlimited writes and reads. It is the highest performance, most reliable nonvolatile memory available.

Logic Block Diagram



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Pin Configurations

Figure 1. Pin Diagram - 32-Pin 300 Mil SOIC/CDIP

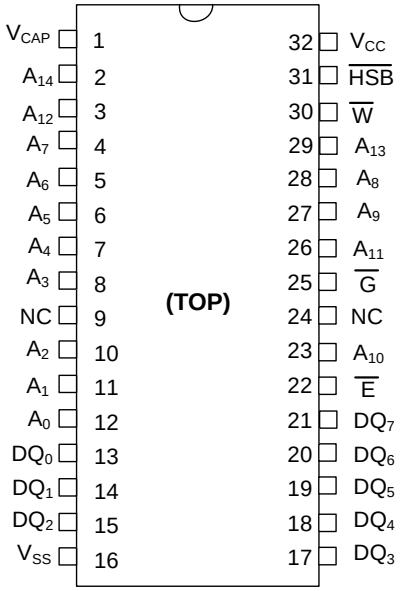
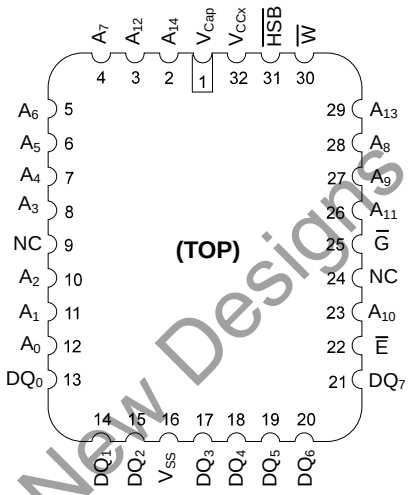


Figure 2. Pin Diagram - 32-Pin 450 Mil LCC



Pin Descriptions

Pin Name	I/O	Description
A_{14}-A_0	Input	**Address**: The 15 address inputs select one of 32,768 bytes in the nvSRAM array.
DQ_7-DQ_0	I/O	**Data**: Bi-directional 8-bit data bus for accessing the nvSRAM.
$\overline{E}$	Input	**Chip Enable**: The active low $\overline{E}$ input selects the device.
$\overline{W}$	Input	**Write Enable**: The active low $\overline{W}$ enables data on the DQ pins to be written to the address location latched by the falling edge of $\overline{E}$.
$\overline{G}$	Input	**Output Enable**: The active low $\overline{G}$ input enables the data output buffers during read cycles. De-asserting $\overline{G}$ high caused the DQ pins to tristate.
V_{CC}	Power Supply	**Power**: 5.0V, ±10%.
$\overline{HSB}$	I/O	**Hardware Store Busy**: When low this output indicates a Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak pull up resistor keeps this pin high if not connected. (optional connection).
V_{CAP}	Power Supply	**AutoStore Capacitor**: Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile storage elements.
V_{SS}	Power Supply	**Ground.**
NC	No Connect	Unlabeled pins have no internal connections.

Absolute Maximum Ratings

Voltage on Input Relative to Ground.....–0.5V to 7.0V
Voltage on Input Relative to V_{SS}.....–0.6V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} or $\overline{HSB}$ .....–0.5V to (V_{CC} + 0.5V)
Temperature under Bias ..... –55°C to 125°C
Storage Temperature ..... –65°C to 150°C
Power Dissipation..... 1W
DC Output Current (1 output at a time, 1s duration).... 15 mA

Note Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics

Over the operating range (V_{CC} = 5.0V ± 10%)[4]

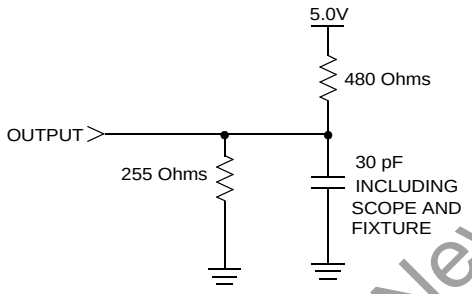
Symbol	Parameter	Commercial		Industrial/ Military		Unit	Notes
		Min	Max	Min	Max		
I_{CC1}[1]	Average V_{CC} Current		97 80 70		100 85 70	mA mA mA	t_{AVAV} = 25 ns t_{AVAV} = 35 ns t_{AVAV} = 45 ns
I_{CC2}[2]	Average V_{CC} Current during *STORE*		3		3	mA	All Inputs Don't Care, V_{CC} = max
I_{CC3}[1]	Average V_{CC} Current at t_{AVAV} = 200 ns 5V, 25°C, Typical		10		10	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I_{CC4}[2]	Average V_{CAP} Current during AutoStore Cycle		2		2	mA	All Inputs Don't Care
I_{SB1}[3]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		30 25 22		31 26 23	mA mA mA	t_{AVAV} = 25 ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 35 ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 45 ns, $\overline{E} \geq V_{IH}$
I_{SB2}[3]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		1.5		1.5	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±5		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC} + 0.5	2.2	V_{CC} +0.5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –4 mA except $\overline{HSB}$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8 mA except $\overline{HSB}$
V_{BL}	Logic "0" Voltage on $\overline{HSB}$ Output		0.4		0.4	V	I_{OUT} = 3 mA
T_A	Operating Temperature	0	70	-40/-55	85/125	°C	

Notes
1. I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
2. I_{CC2} and I_{CC4} are the average currents required for the duration of the respective STORE cycles (t_{STORE}).
3. $\overline{E} \geq V_{IH}$ does not produce standby current levels until any nonvolatile cycle in progress has timed out.
4. V_{CC} reference levels throughout this data sheet refer to V_{CC} if that is where the power supply connection is made, or V_{CAP} if V_{CC} is connected to ground.

AC Test Conditions

Input Pulse Levels ..... 0V to 3V
Input Rise and Fall Times ..... ≤5 ns
Input and Output Timing Reference Levels 1.5V
Output Load ..... See Figure 3

Figure 3. AC Output Loading



Capacitance

Parameter[5]	Description	Test Conditions	Max	Unit	Conditions
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz,	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance		7	pF	ΔV = 0 to 3V

Note
5. These parameters are guaranteed but not tested.

SRAM Read Cycles #1 and #2

(VCC = 5.0V ± 10%)[4]

NO.	Symbols		Parameter	STK14C88-25		STK14C88-35		STK14C88-45		Unit
	#1, #2	Alt.		Min	Max	Min	Max	Min	Max	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}[6], t_{ELEH}[6]	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}[7]	t_{AA}	Address Access Time		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20	ns
5	t_{AXQX}[7]	t_{OH}	Output Hold after Address Change	5		5		5		ns
6	t_{ELQX}	t_{LZ}	Address Change or Chip Enable to Output Active	5		5		5		ns
7	t_{EHQZ}[8]	t_{HZ}	Address Change or Chip Disable to Output Inactive		10		13		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}[8]	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10	t_{ELICCH}[5]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	t_{EHICCL}[5]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Figure 4. SRAM Read Cycle 1: Address Controlled [6, 7]

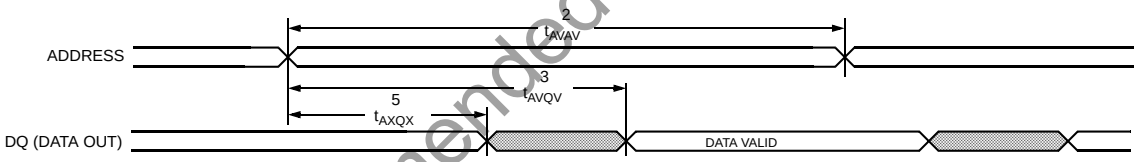
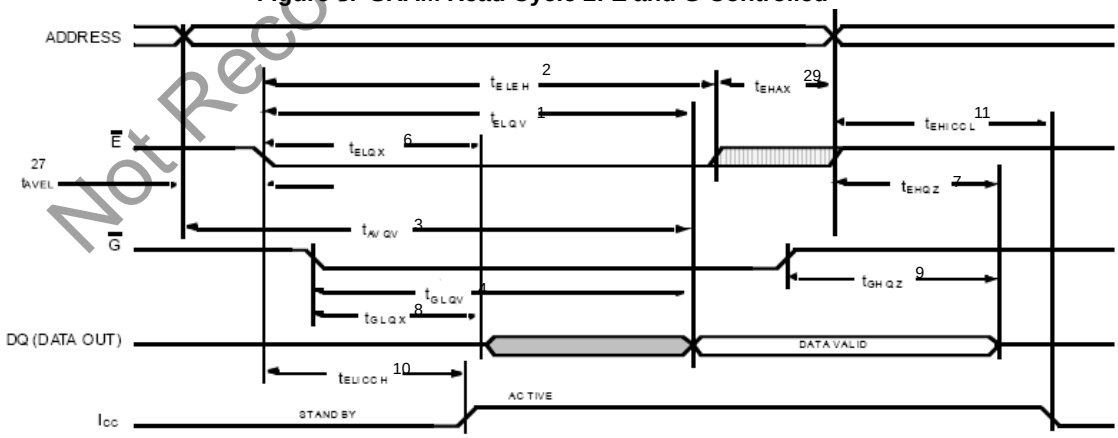


Figure 5. SRAM Read Cycle 2: $\overline{E}$ and $\overline{G}$ Controlled [6]



Notes
6. $\overline{W}$ and $\overline{HSB}$ must be high during SRAM read cycles.
7. I/O state assumes $\overline{E}$ and $\overline{G} \leq V_{IL}$ and $\overline{W} \geq V_{IH}$; device is continuously selected.
8. Measured ± 200 mV from steady state output voltage.

SRAM Write Cycle #1 and #2

(VCC = 5.0V ± 10%)[4]

NO.	Symbols			Parameter	STK14C88-25		STK14C88-35		STK14C88-45		Unit
	#1	#2	Alt.		Min	Max	Min	Max	Min	Max	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Setup to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Setup to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Setup to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns
20	t_{WLQZ}[8, 9]		t_{WZ}	Write Enable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	5		5		5		ns

Figure 6. SRAM Write Cycle 1: $\overline{W}$ Controlled [10, 11]

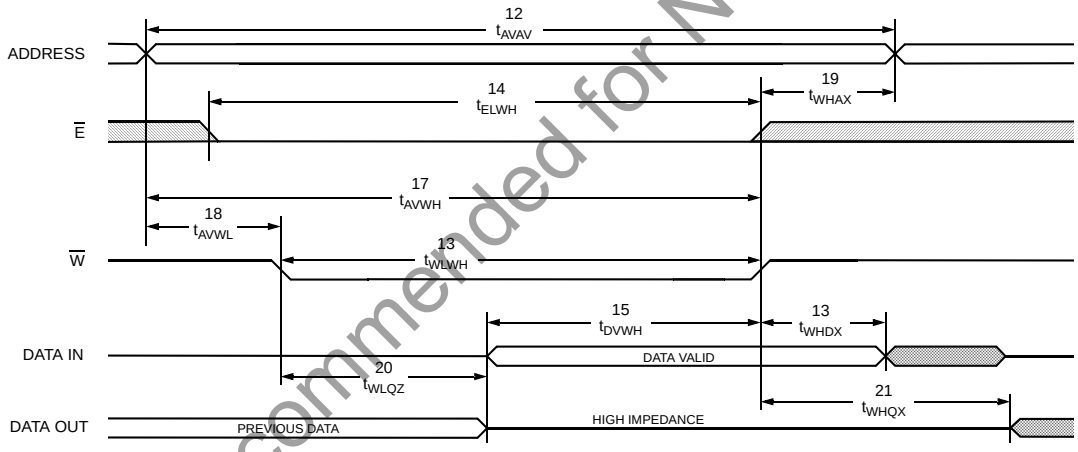
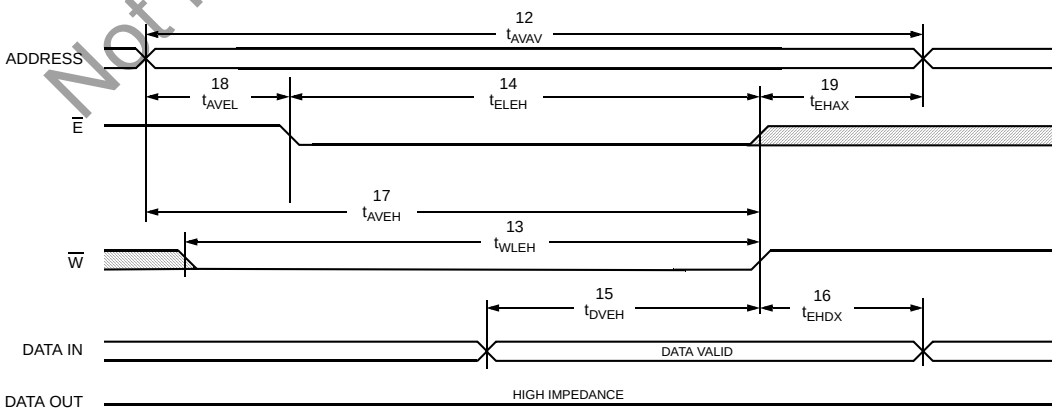


Figure 7. SRAM Write Cycle 2: $\overline{E}$ Controlled [10, 11]



Notes
9. If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
10. $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
11. $\overline{HSB}$ must be high during SRAM write cycles.

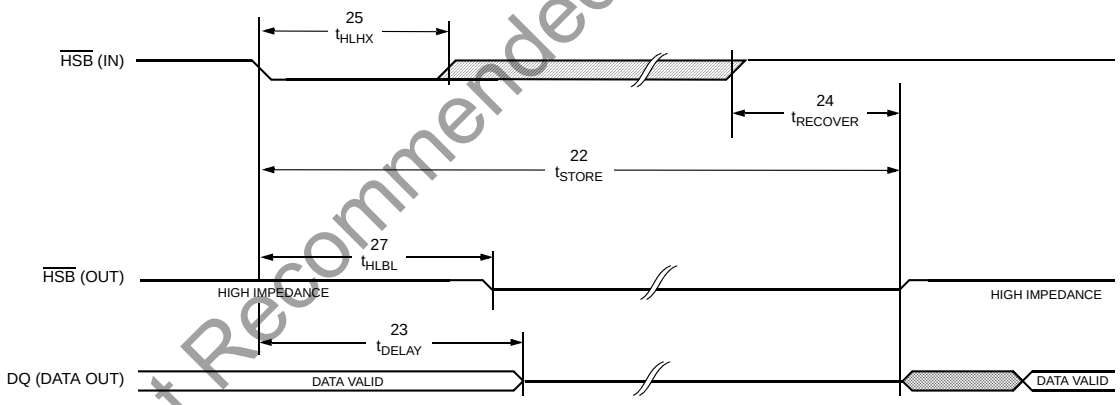
Hardware Mode Selection

$\overline{E}$	$\overline{W}$	$\overline{HSB}$	A_{13} - A_0 (hex)	Mode	I/O	Power	Notes
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	19
L	L	H	X	Write SRAM	Input Data	Active	
X	X	L	X	Nonvolatile *STORE*	Output High Z	I_{CC2}	12

Hardware STORE Cycle

No.	Symbols		Parameter	STK14C88		Units	Notes
	Standard	Alternate		Min	Max		
22	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		10	ms	13
23	t_{DELAY}	t_{HLQZ}	Time Allowed to Complete SRAM Cycle	1		µs	13
24	$t_{RECOVER}$	t_{HHQX}	Hardware *STORE* High to Inhibit Off		700	ns	13, 14
25	t_{HLHX}		Hardware *STORE* Pulse Width	15		ns	
26	t_{HLBL}		Hardware *STORE* Low to *STORE* Busy		300	ns	

Figure 8. Hardware STORE Cycle

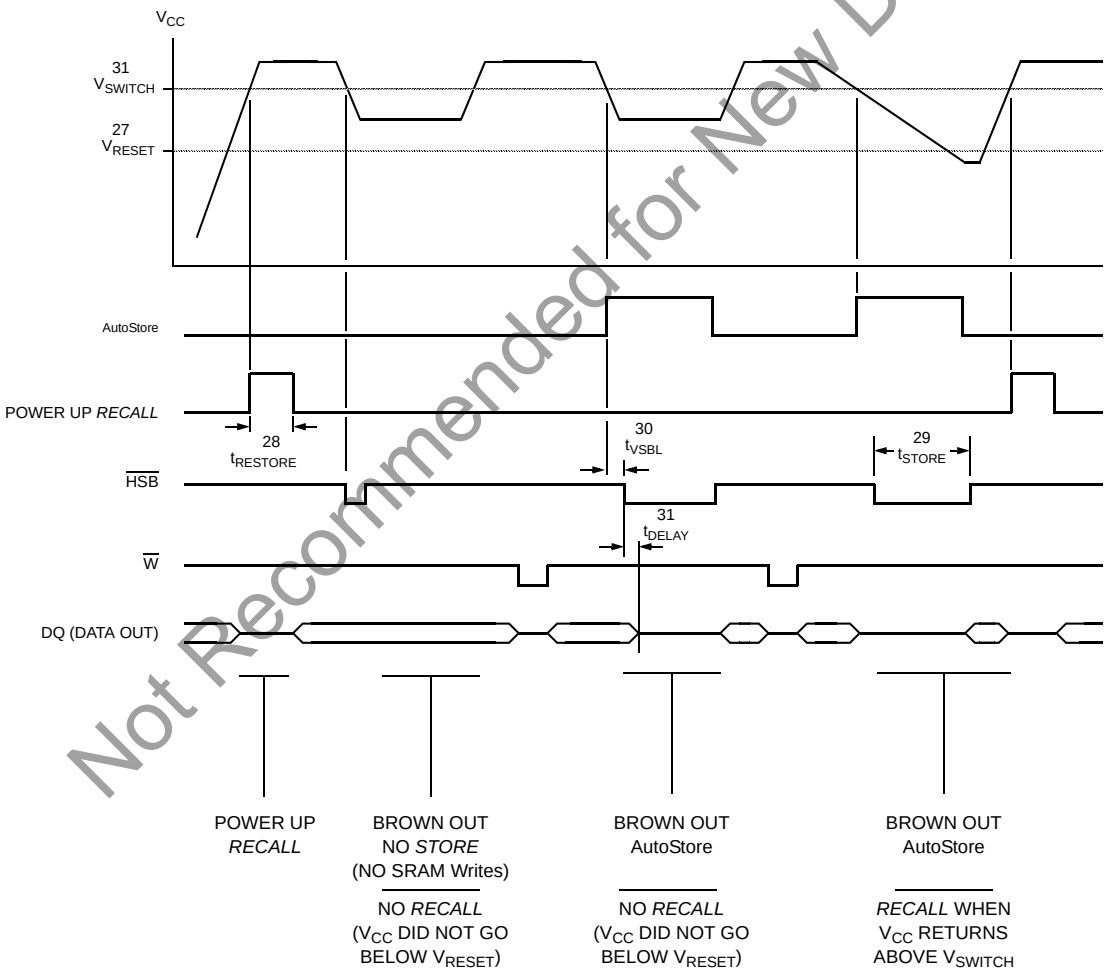


Notes
12. $\overline{HSB}$ STORE operation occurs only if an SRAM write is done since the last nonvolatile cycle. After the STORE (if any) completes, the part goes into standby mode, inhibiting all operations until HSB rises
13. $\overline{E}$ and $\overline{G}$ low, $\overline{W}$ high for output behavior.
14. $t_{RECOVER}$ is only applicable after t_{STORE} is complete.

AutoStore/Power up RECALL

NO.	Symbols		Parameter	STK14C88		Unit	Notes
	Standard	Alt.		Min	Max		
27	$t_{RESTORE}$		Power up *RECALL* Duration		550	µs	15
28	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		10	ms	13, 16
29	t_{VSBL}		Low Voltage Trigger (V_{SWITCH}) to $\overline{HSB}$ Low		300	ns	11
30	t_{DELAY}	t_{BLQZ}	Time Allowed to Complete SRAM Cycle	1		µs	13
31	V_{SWITCH}		Low Voltage Trigger Level	4.0	4.5	V	
32	V_{RESET}		Low Voltage Reset Level		3.6	V	

Figure 9. AutoStore/POWER UP RECALL



Notes
15. $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.
16. $\overline{HSB}$ is asserted low for 1µs when V_{CAP} drops through V_{SWITCH}. If an SRAM write has not taken place since the last nonvolatile cycle, $\overline{HSB}$ is released and no *STORE* takes place.

nvSRAM Operation

The STK14C88 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to nonvolatile elements (the STORE operation) or from nonvolatile elements to SRAM (the RECALL operation). In this mode, SRAM functions are disabled.

Noise Considerations

The STK14C88 is a high speed memory and so must have a high frequency bypass capacitor of approximately 0.1 µF connected between V_{CAP} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals helps to prevent noise problems.

SRAM Read

The STK14C88 performs a read cycle whenever $\overline{E}$ and $\overline{G}$ are low, and $\overline{W}$ and HSB are high. The address specified on pins A_{0-14} determines which of the 32,768 data bytes are accessed. When the read is initiated by an address transition, the outputs are valid after a delay of t_{AVQV} (Read cycle #1). If the read is initiated by $\overline{E}$ or $\overline{G}$, the outputs are valid at t_{ELQV} or at t_{GLQV}, whichever is later (Read cycle #2). The data outputs repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high, or $\overline{W}$ or HSB is brought low.

SRAM Write

A write cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low, and HSB is high. The address inputs must be stable prior to entering the write cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} are written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled write or t_{DVEH} before the end of an $\overline{E}$ controlled write.

Keep $\overline{G}$ high during the entire write cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left low, internal circuitry turns off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

Power Up RECALL

During power up, or after any low power condition (V_{CAP} < V_{RESET}), an internal RECALL request is latched. When V_{CAP} again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{RESTORE}$ to complete.

If the STK14C88 is in a write state at the end of power up RECALL, the SRAM data will be corrupted. To avoid this, a 10 KOhm resistor should be connected either between $\overline{W}$ and system V_{CC} or between $\overline{E}$ and system V_{CC}.

Software Nonvolatile STORE

The STK14C88 software STORE cycle is initiated by executing sequential $\overline{E}$ controlled read cycles from six specific address locations. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. When a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence, or the sequence will be aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following read sequence must be performed:

1. Read address 0E38 (hex) Valid READ
2. Read address 31C7 (hex) Valid READ
3. Read address 03E0 (hex) Valid READ
4. Read address 3C1F (hex) Valid READ
5. Read address 303F (hex) Valid READ
6. Read address 0FC0 (hex) Initiate STORE cycle

The software sequence must be clocked with $\overline{E}$ controlled reads.

After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. Use only read cycles in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the tSTORE cycle time is fulfilled, the SRAM is again activated for read and write operation.

Software Nonvolatile RECALL

A software RECALL cycle is initiated with a sequence of read operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{E}$ controlled read operations must be performed:

1. Read address 0E38 (hex) Valid READ
2. Read address 31C7 (hex) Valid READ
3. Read address 03E0 (hex) Valid READ
4. Read address 3C1F (hex) Valid READ
5. Read address 303F (hex) Valid READ
6. Read address 0C63 (hex) Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for read and write operations. The RECALL operation in no way alters the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

AutoStore Mode

The STK14C88 can be powered in one of three modes.

During normal AutoStore operation, the STK14C88 draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. After power up, when the voltage on the V_{CAP} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC} and initiate a STORE operation.

Figure 11 shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of between 68 µF and 220 µF (±20%) rated at 6V should be provided.

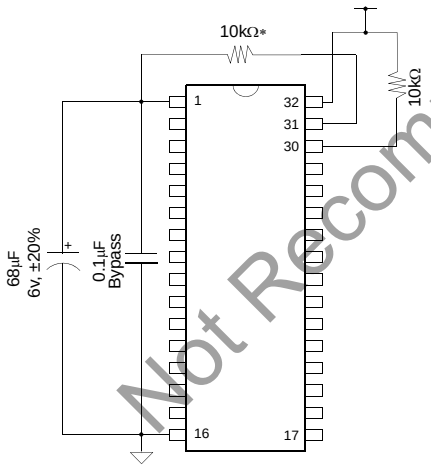
In system power mode, both V_{CC} and V_{CAP} are connected to the + 5V power supply without the 68 µF capacitor. In this mode, the AutoStore function of the STK14C88 operates on the stored system charge as power goes down. The user must, however, guarantee that V_{CC} does not drop below 3.6V during the 10 ms STORE cycle.

If an automatic STORE on power loss is not required, then V_{CC} can be tied to ground and + 5V applied to V_{CAP} (Figure 12). This is the AutoStore Inhibit mode, in which the AutoStore function is disabled. If the STK14C88 is operated in this configuration, references to V_{CC} should be changed to V_{CAP} throughout this data sheet. In this mode, STORE operations may be triggered through software control or the HSB pin. To enable or disable AutoStore using an I/O port pin, see Preventing STORES on page 12.

To prevent unneeded STORE operations, automatic STOREs and those initiated by externally driving HSB low are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place.

If the power supply drops faster than 20 ms/volt before V_{CC} reaches V_{SWITCH}, then a 2.2 ohm resistor should be inserted between V_{CC} and the system supply to avoid momentary excess of current between V_{cc} and V_{CAP}.

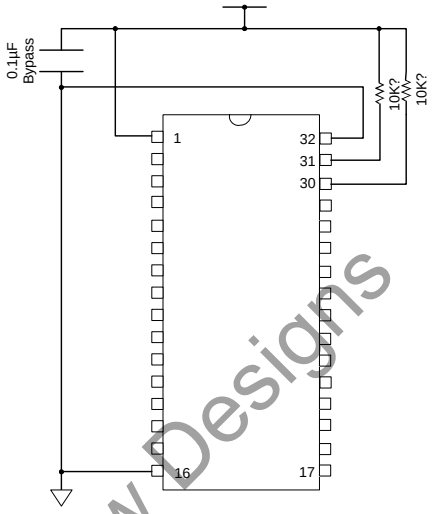
Figure 11. AutoStore Mode



AutoStore INHIBIT Mode

If an automatic STORE on power loss is not required, then V_{CC} can be tied to ground and system power applied to V_{CAP} (Figure 12). This is the AutoStore Inhibit mode, in which the AutoStore function is disabled. If the STK14C88 is operated in this configuration, references to V_{CC} should be changed to V_{CAP} throughout this data sheet. In this mode, STORE operations may be triggered through software control. It is not permissible to change between these three options “on the fly.”

Figure 12. AutoStore Inhibit Mode



HSB Operation

The STK14C88 provides the HSB pin for controlling and acknowledging the STORE operations. The HSB pin can be used to request a hardware STORE cycle. When the HSB pin is driven low, the STK14C88 conditionally initiates a STORE operation after t_{DELAY}; an actual STORE cycle only begins if a write to the SRAM took place since the last STORE or RECALL cycle. The HSB pin has a very resistive pull up and is internally driven low to indicate a busy condition when the STORE (initiated by any means) is in progress. Pull up this pin with an external 10 Kohm resistor to V_{CAP} if HSB is used as a driver.

SRAM read and write operations that are in progress when HSB is driven low by any means are given time to complete before the STORE operation is initiated. After HSB goes low, the STK14C88 continues SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM read operations may take place. If a write is in progress when HSB is pulled low it is allowed a time, tDELAY, to complete. However, any SRAM write cycles requested after HSB goes low are inhibited until HSB returns high.

The HSB pin can be used to synchronize multiple STK14C88s while using a single larger capacitor. To operate in this mode, the HSB pin should be connected together to the HSB pins from the other STK14C88s. An external pull up resistor to + 5V is required because HSB acts as an open drain pull down. The V_{CAP} pins from the other STK14C88 parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the STK14C88s detects a power loss and asserts HSB, the common HSB pin causes all parts to request a STORE cycle (a STORE takes place in those STK14C88s that are written since the last nonvolatile cycle).

During any STORE operation, regardless of how it was initiated, the STK14C88 continues to drive the HSB pin low, releasing it only when the STORE is complete. Upon completion of the STORE operation the STK14C88 remains disabled until the HSB pin returns high.

If HSB is not used, leave it unconnected.

Best Practices

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. The end product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on should always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state (such as autostore enabled). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, and so on).
- The V_{CAP} value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the max V_{CAP} value because the nvSRAM internal algorithm calculates V_{CAP} charge time based on this max V_{CAP} value. Customers who want to use a larger V_{CAP} value to make sure there is extra store charge and store time should discuss their V_{CAP} size selection with Cypress to understand any impact on the V_{CAP} voltage level at the end of a t_{RECALL} period.

Preventing STORES

The STORE function can be disabled on the fly by holding $\overline{HSB}$ high with a driver capable of sourcing 30 mA at a V_{OH} of at least 2.2V, because it must overpower the internal pull down device that drives HSB low for 20 ms at the onset of a STORE. When the STK14C88 is connected for AutoStore operation (system V_{CC} connected to V_{CC} and a 68 uF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the STK14C88 attempts to pull $\overline{HSB}$ low; if $\overline{HSB}$ does not actually get below V_{IL}, the part stops trying to pull $\overline{HSB}$ low and abort the STORE attempt.

Hardware Protect

The STK14C88 offers hardware protection against inadvertent STORE operation and SRAM writes during low voltage conditions. When V_{CAP} < V_{SWITCH}, all externally initiated STORE operations and SRAM writes are inhibited.

AutoStore can be completely disabled by tying V_{CC} to ground and applying + 5V to V_{CAP}. This is the AutoStore Inhibit mode; in this mode STOREs are only initiated by explicit request using either the software sequence or the $\overline{HSB}$ pin.

Low Average Active Power

The STK14C88 draws significantly less current when it is cycled at times longer than 50 ns. Figure 13 shows the relationship between I_{CC} and read cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 5.5V, 100% duty cycle on chip enable). Figure 14 shows the same relationship for write cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK14C88 depends on the following items:

- CMOS vs. TTL input levels
- The duty cycle of chip enable
- The overall cycle rate for accesses
- The ratio of reads to writes
- The operating temperature
- The V_{CC} level
- I/O loading

Figure 13. Icc (max) Reads

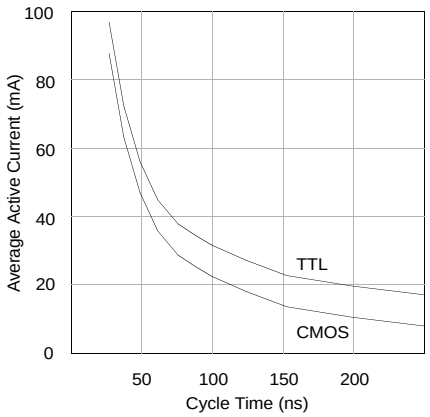
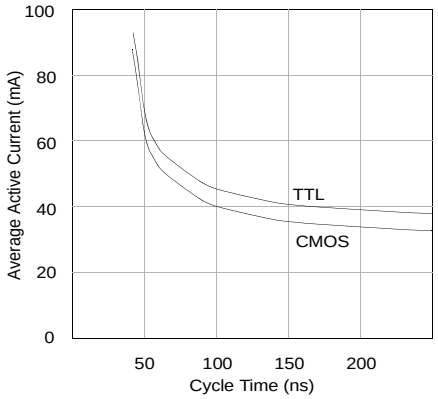
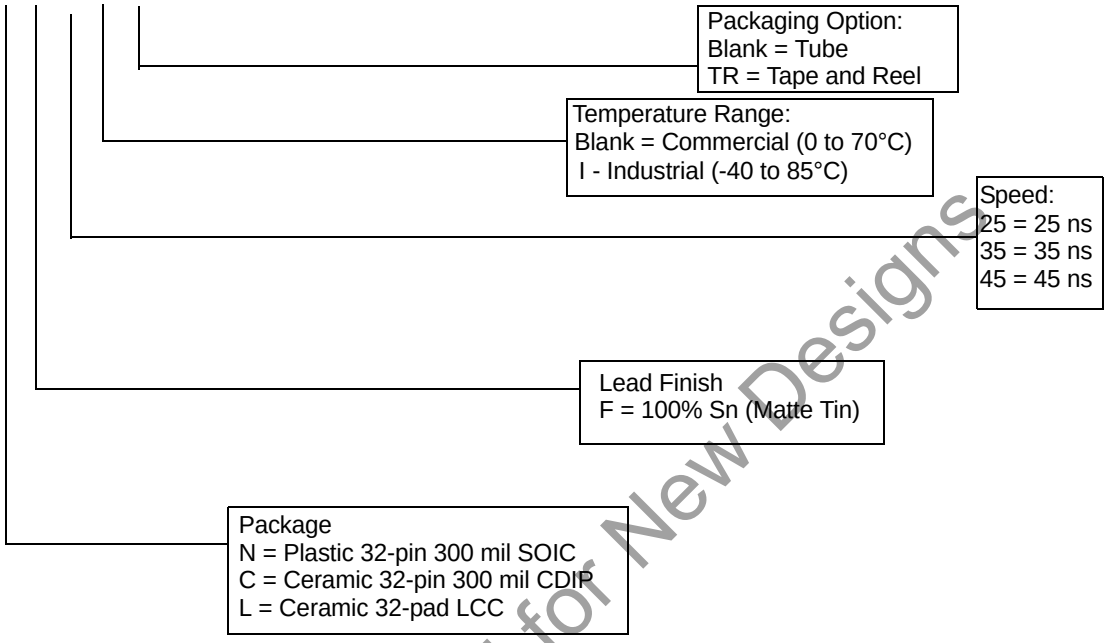


Figure 14. Icc (max) Writes



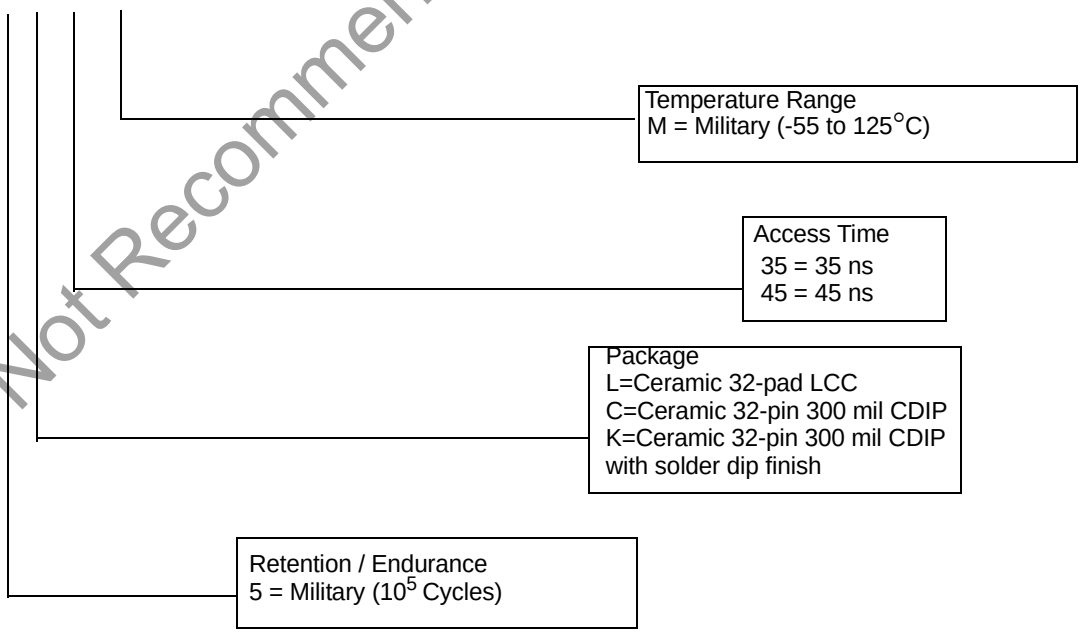
Commercial and Industrial Ordering Information

STK14C88 - N F 45 I TR



Military Ordering Information

STK14C88 - 5 C 45 M



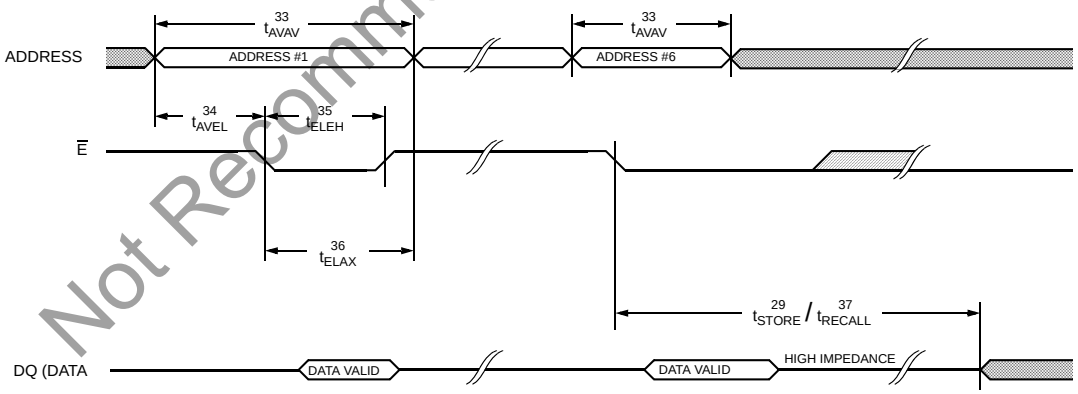
Software STORE/RECALL Mode Selection

$\overline{E}$	$\overline{W}$	A_{13} - A_0 (hex)	Mode	I/O	POWER	Notes
L	H	0E38 31C7 03E0 3C1F 303F	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM	Output Data Output Data Output Data Output Data Output Data	Active	13, 17, 18, 19
		0FC0	Nonvolatile *STORE*	Output High Z	I_{CC2}	
L	H	0E38 31C7 03E0 3C1F 303F 0C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile *RECALL*	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	13, 17, 18, 19

Software-Controlled STORE/RECALL Cycle

NO.	Symbols		Parameter	STK14C88-25		STK14C88-35		STK14C88-45		Unit	Notes
	Standard	Alt.		Min	Max	Min	Max	Min	Max		
33	t_{AVAV}	t_{RC}	STORE/RECALL Initiation Cycle Time	35		45		55		ns	13
34	t_{AVEL}	t_{AS}	Address Setup Time	0		0		0		ns	20, 21
35	t_{ELEH}	t_{CW}	Clock Pulse Width	25		30		35		ns	20, 21
36	t_{ELAX}		Address Hold Time	20		20		20		ns	20, 21
37	t_{RECALL}		RECALL Duration		20		20		20	µs	

Figure 10. $\overline{E}$ Controlled Software STORE/RECALL Cycle [21]



Notes
17. The six consecutive addresses must be in the order listed. $\overline{W}$ must be high during all six consecutive $\overline{E}$ controlled cycles to enable a nonvolatile cycle.
18. While there are 15 addresses on the STK14C88, only the lower 14 are used to control software modes.
19. I/O state assumes $\overline{G} < V_{IL}$. Activation of nonvolatile cycles does not depend on state of $\overline{G}$.
20. The software sequence is clocked on the falling edge of $\overline{E}$ controlled reads without involving $\overline{G}$ (double clocking aborts the sequence).
21. The six consecutive addresses must be in the order listed in the Software STORE/RECALL Mode Selection Table: (0E38, 31C7, 03E0, 3C1F, 303F, 0FC0) for a STORE cycle or (0E38, 31C7, 03E0, 3C1F, 303F, 0C63) for a RECALL cycle. W must be high during all six consecutive cycles.

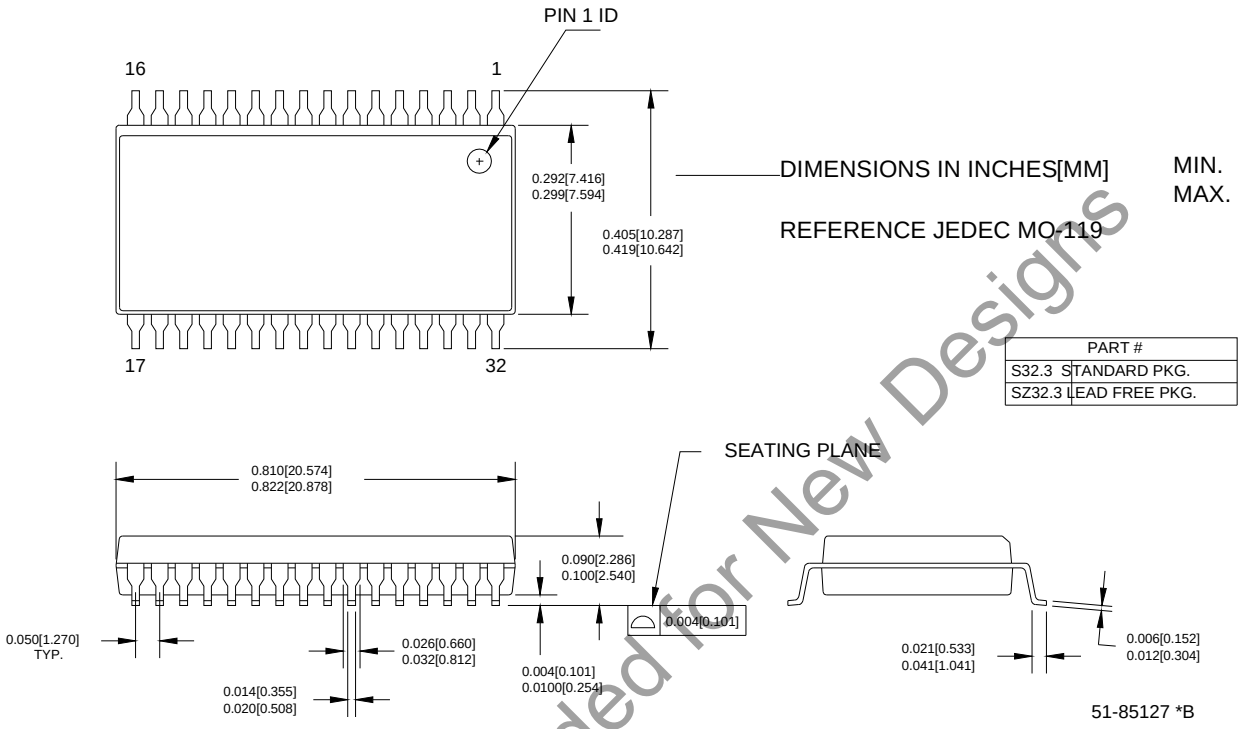
Ordering Information

These parts are not recommended for new designs.

Part Number	Description	Access Times	Temperature
STK14C88-NF25	5V 32Kx8 AutoStore nvSRAM SOIC32-300	25 ns	Commercial
STK14C88-NF35	5V 32Kx8 AutoStore nvSRAM SOIC32-300	35 ns	Commercial
STK14C88-NF45	5V 32Kx8 AutoStore nvSRAM SOIC32-300	45 ns	Commercial
STK14C88-NF25TR	5V 32Kx8 AutoStore nvSRAM SOIC32-300	25 ns	Commercial
STK14C88-NF35TR	5V 32Kx8 AutoStore nvSRAM SOIC32-300	35 ns	Commercial
STK14C88-NF45TR	5V 32Kx8 AutoStore nvSRAM SOIC32-300	45 ns	Commercial
STK14C88-NF25I	5V 32Kx8 AutoStore nvSRAM SOIC32-300	25 ns	Industrial
STK14C88-NF35I	5V 32Kx8 AutoStore nvSRAM SOIC32-300	35 ns	Industrial
STK14C88-NF45I	5V 32Kx8 AutoStore nvSRAM SOIC32-300	45 ns	Industrial
STK14C88-NF25ITR	5V 32Kx8 AutoStore nvSRAM SOIC32-300	25 ns	Industrial
STK14C88-NF35ITR	5V 32Kx8 AutoStore nvSRAM SOIC32-300	35 ns	Industrial
STK14C88-NF45ITR	5V 32Kx8 AutoStore nvSRAM SOIC32-300	45 ns	Industrial
STK14C88-C45I	5V 32Kx8 AutoStore nvSRAM CDIP32-300	45 ns	Industrial
STK14C88-5L35M	5V 32Kx8 AutoStore nvSRAM LCC32-300	35 ns	Military
STK14C88-5L45M	5V 32Kx8 AutoStore nvSRAM LCC32-300	45 ns	Military
STK14C88-5C35M	5V 32Kx8 AutoStore nvSRAM CDIP32-300	35 ns	Military
STK14C88-5C45M	5V 32Kx8 AutoStore nvSRAM CDIP32-300	45 ns	Military
STK14C88-5K35M	5V 32Kx8 AutoStore nvSRAM CDIP32-300	35 ns	Military
STK14C88-5K45M	5V 32Kx8 AutoStore nvSRAM CDIP32-300	45 ns	Military

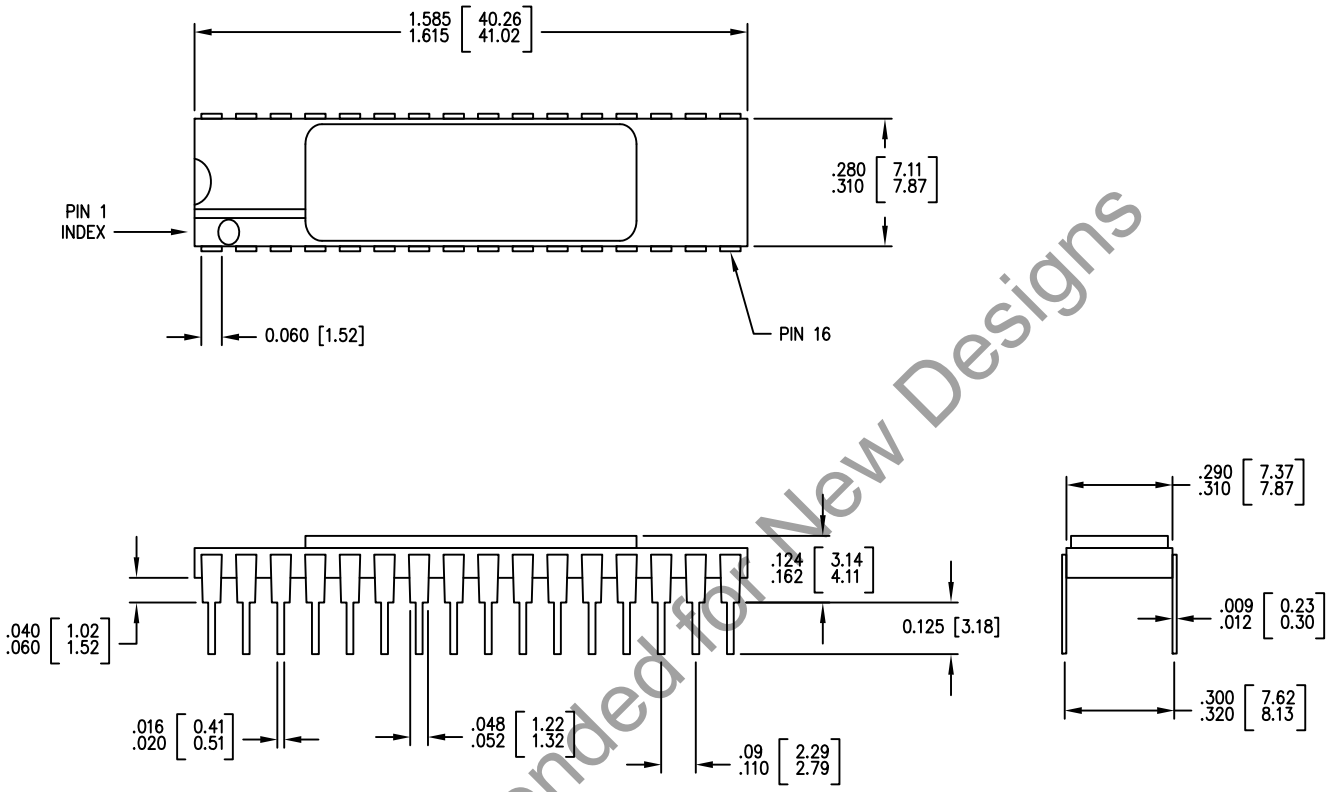
Package Diagrams

Figure 15. 32-Pin 300 mil SOIC Gull Wing (51-85127)



Package Diagrams (continued)

Figure 16. 32-Pin 300 mil Side Braze DIL (001-51694)

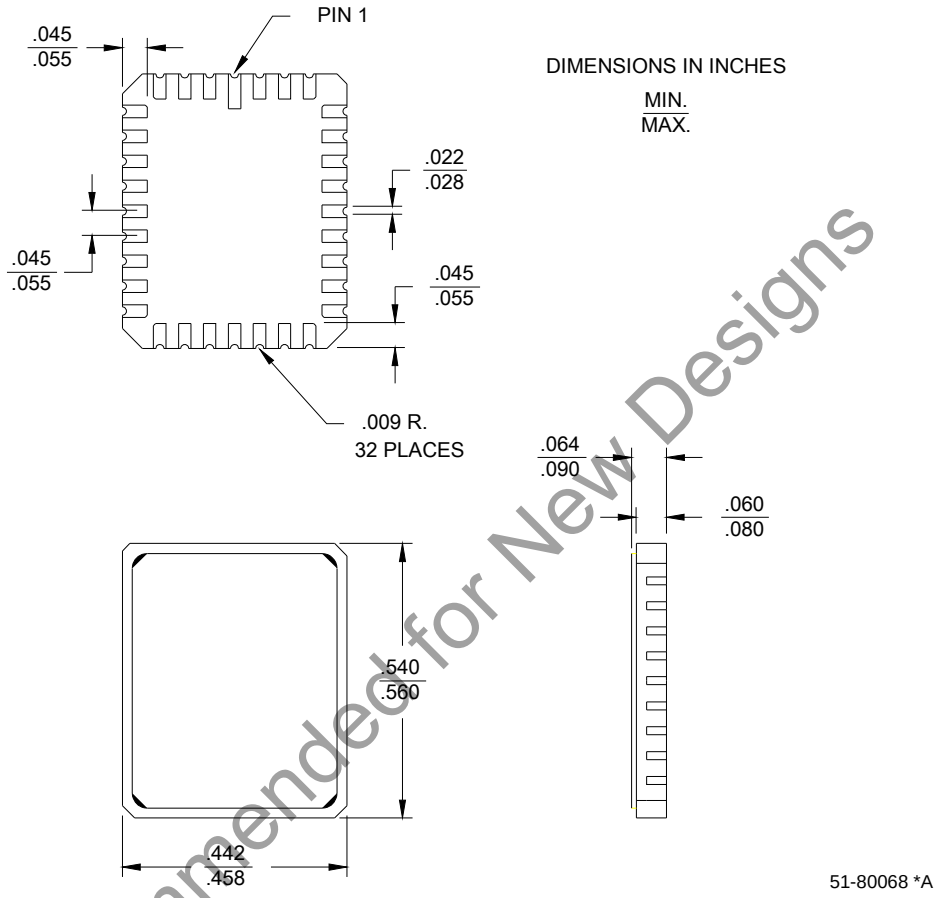


1. ALL DIMENSIONS ARE IN MILLIMETERS AND INCHS [MIN/MAX]
2. PACKAGE WEIGHT : TBD

001-51694 **

Package Diagrams (continued)

Figure 17. 32-Pin 450 mil Ceramic LCC (51-80068)



Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2668632	GVCH	03/04/2009	New data sheet
*A	2718242	GVCH	06/12/09	Ordering Information description: Corrected typo
*B	2821358	GVCH	12/04/2009	Added Note in Ordering Information mentioning that these parts are not recommended for new designs. Added “Not recommended for New Designs” watermark in the PDF. Added Contents on page 2.

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