THE DATASHEET OF

ZL30406QGG1

ZL30406

SONET/SDH Clock Multiplier PLL

Data Sheet

July 2011

Features

- Meets jitter requirements of Telcordia GR-253-CORE for OC-48, OC-12, and OC-3 rates
- Meets jitter requirements of ITU-T G.813 for STM-16, STM-4 and STM-1 rates
- Provides four LVPECL differential output clocks at 77.76 MHz
- Provides a CML differential clock programmable to 19.44 MHz, 38.88 MHz, 77.76 MHz and 155.52 MHz
- Provides a single-ended CMOS clock at 19.44 MHz
- Provides enable/disable control of output clocks
- Accepts a CMOS reference at 19.44 MHz
- 3.3 V supply

Applications

- SONET/SDH line cards
- Network Element timing cards

Ordering Information

ZL30406QGG1	64 Pin TQFP*	Trays, Bake & Drypack

*Pb Free Matte Tin

-40°C to +85°C

Description

The ZL30406 is an analog phase-locked loop (APLL) designed to provide rate conversion and jitter attenuation for SDH (Synchronous Digital Hierarchy) and SONET (Synchronous Optical Network) networking equipment. The ZL30406 generates very low jitter clocks that meet the jitter requirements of Telcordia GR-253-CORE OC-48, OC-12, OC-3, OC-1 rates and ITU-T G.813 STM-16, STM-4 and STM-1 rates.

The ZL30406 accepts a CMOS compatible reference at 19.44 MHz and generates four LVPECL differential output clocks at 77.76 MHz, a CML differential clock programmable to 19.44 MHz, 38.88 MHz, 77.76 MHz and 155.52 MHz and a single-ended CMOS clock at 19.44 MHz. The output clocks can be individually enabled or disabled.

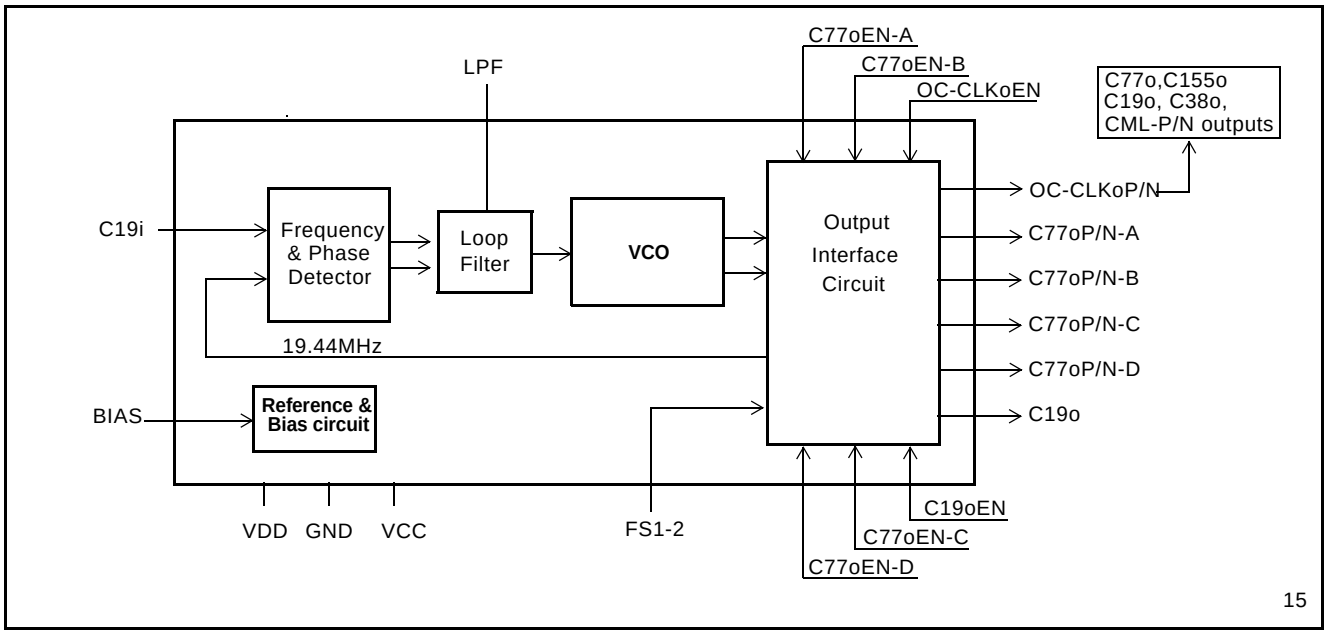


Figure 1 - Functional Block Diagram

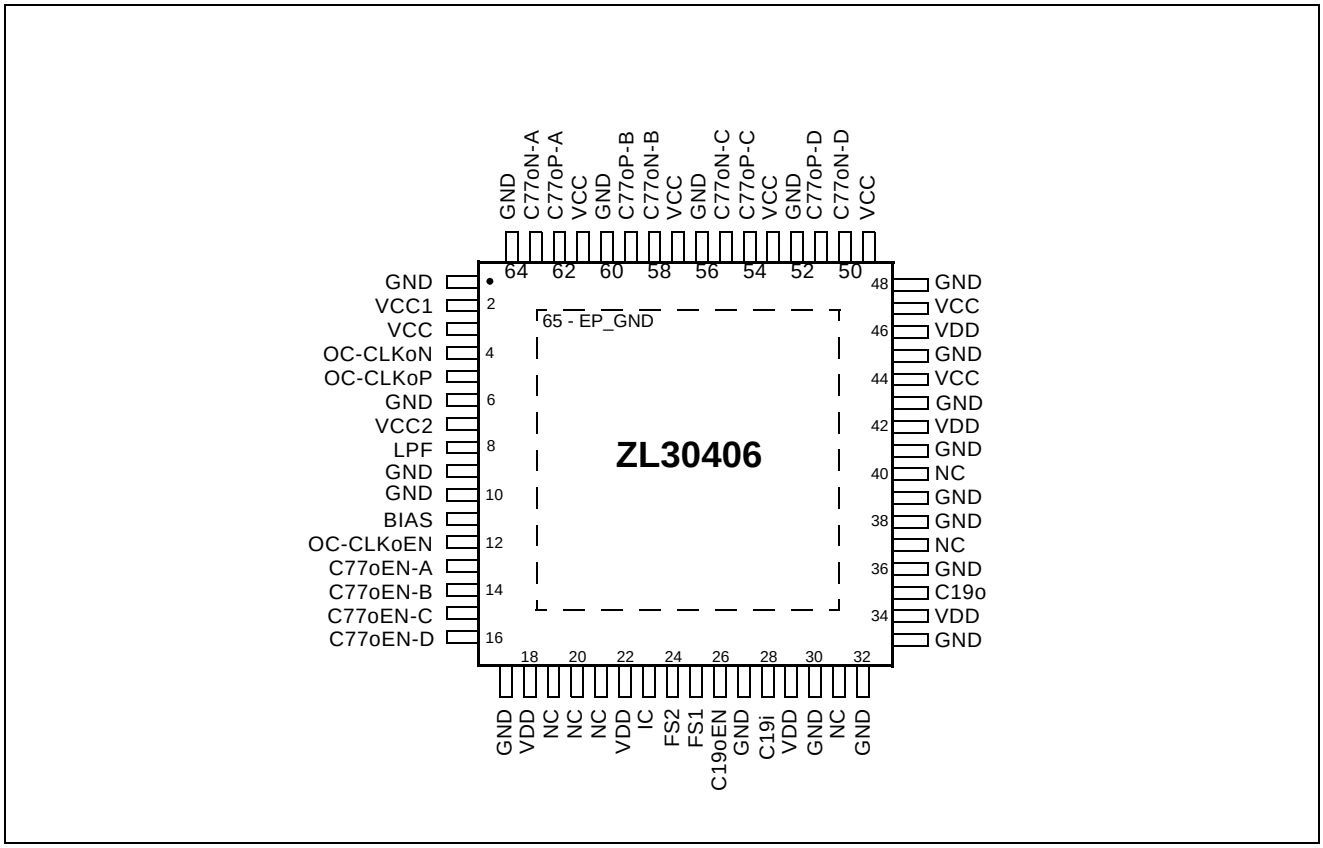


Figure 2 - TQFP 64 pin (Top View)

Change Summary

The following table captures the changes from the July 2011 issue.

Page	Item	Change
1	Ordering Information	The ZL30406QGC has been obsoleted and replaced by the ZL30406QGG1.

The following table captures the changes from the February 2005 issue.

Page	Item	Change
1		Updated Ordering Information.

Pin Description

Pin Description Table

Pin #	Name	Description
1	GND	**Ground.** 0 volt.
2	VCC1	**Positive Analog Power Supply.** +3.3 V ±10%
3	VCC	**Positive Analog Power Supply.** +3.3 V ±10%
4 5	OC-CLKoN OC-CLKoP	**SONET/SDH Clock (CML Output).** These outputs provide a programmable differential CML clock at 19.44 MHz, 38.88 MHz, 77.76 MHz and 155.52 MHz. The output frequency is selected with FS2 and FS1 pins.
6	GND	**Ground.** 0 volt
7	VCC2	**Positive Analog Power Supply.** +3.3 V ±10%
8	LPF	Low Pass Filter (Analog). Connect to this pin external RC network (R_F and C_F) for the low pass filter.
9	GND	**Ground.** 0 volt
10	GND	**Ground.** 0 volt
11	BIAS	**Bias.** See Figure 11 for the recommended bias circuit.
12	OC-CLKoEN	**SONET/SDH Clock Enable (CMOS Input).** If tied high this control pin enables the OC-CLKoP/N differential driver. Pulling this input low disables the output clock without deactivating differential drivers.
13	C77oEN-A	**C77 Clock Output Enable A (CMOS Input).** If tied high this control pin enables the C77oP/N-A output clock. Pulling this input low disables the output clock without deactivating differential drivers.
14	C77oEN-B	**C77 Clock Output Enable B (CMOS Input).** If tied high this control pin enables the C77oP/N-B output clock. Pulling this input low disables the output clock without deactivating differential drivers.
15	C77oEN-C	**C77 Clock Output Enable C (CMOS Input).** If tied high this control pin enables the C77oP/N-C output clock. Pulling this input low disables the output clock without deactivating differential drivers.
16	C77oEN-D	**C77 Clock Output Enable D (CMOS Input).** If tied high this control pin enables the C77oP/N-D output clock. Pulling this input low disables the output clock without deactivating differential drivers.
17	GND	**Ground.** 0 volt
18	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
19	NC	No internal bonding Connection. Leave unconnected.
20	NC	No internal bonding Connection. Leave unconnected.
21	NC	No internal bonding Connection. Leave unconnected.
22	VDD	**Positive Digital Power Supply.** +3.3 V ±10%

Pin Description Table (continued)

Pin #	Name	Description
23	IC	**Internal Connection.** Connect this pin to Ground (GND).
24 25	FS2 FS1	**Frequency Select 2-1 (CMOS Input)**. These inputs program the clock frequency on the OC-CLKo output. The possible output frequencies are 19.44 MHz (00), 38.88 MHz (01), 77.76 MHz (10), 155.52 MHz (11).
26	C19oEN	**C19o Output Enable (CMOS Input).** If tied high this control pin enables the C19o output clock. Pulling this pin low forces output driver into a high impedance state.
27	GND	**Ground.** 0 volt
28	C19i	**C19 Reference Input (CMOS Input).** This pin is a single-ended input reference source used for synchronization. This pin accepts 19.44 MHz.
29	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
30	GND	**Ground.** 0 volt
31	NC	No internal bonding Connection. Leave unconnected.
32	GND	**Ground.** 0 volt.
33	GND	**Ground.** 0 volt
34	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
35	C19o	**C19 Clock Output (CMOS Output)**. This pin provides a single-ended CMOS clock at 19.44 MHz.
36	GND	**Ground.** 0 volt
37	NC	No internal bonding Connection. Leave unconnected.
38	GND	**Ground.** 0 volt
39	GND	**Ground.** 0 volt
40	NC	No internal bonding Connection. Leave unconnected.
41	GND	**Ground.** 0 volt
42	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
43	GND	**Ground.** 0 volt
44	VCC	**Positive Analog Power Supply.** +3.3 V ±10%
45	GND	**Ground.** 0 volt
46	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
47	VCC	**Positive Analog Power Supply.** +3.3 V ±10%
48	GND	**Ground.** 0 volt
49	VCC	**Positive Analog Power Supply.** +3.3 V ±10%.

Pin Description Table (continued)

Pin #	Name	Description
50 51	C77oN-D C77oP-D	**C77 Clock Output (LVPECL Output)**. These outputs provide a differential LVPECL clock at 77.76 MHz. Unused LVPECL port should be left unterminated to decrease supply current.
52	GND	**Ground.** 0 volt
53	VCC	**Positive Analog Power Supply.** +3.3 V ±10%.
54 55	C77oP-C C77oN-C	**C77 Clock Output (LVPECL Output)**. These outputs provide a differential LVPECL clock at 77.76 MHz. Unused LVPECL port should be left unterminated to decrease supply current.
56	GND	**Ground.** 0 volt
57	VCC	**Positive Analog Power Supply.** +3.3 V ±10%.
58 59	C77oN-B C77oP-B	**C77 Clock Output (LVPECL Output)**. These outputs provide a differential LVPECL clock at 77.76 MHz. Unused LVPECL port should be left unterminated to decrease supply current.
60	GND	**Ground.** 0 volt
61	VCC	**Positive Analog Power Supply.** +3.3 V ±10%.
62 63	C77oP-A C77oN-A	**C77 Clock Output (LVPECL Output)**. These outputs provide a differential LVPECL clock at 77.76 MHz. Unused LVPECL port should be left unterminated to decrease supply current.
64	GND	**Ground.** 0 volt
65	EP_GND	**Exposed die Pad Ground.** 0 volt (connect to GND)

1.0 Functional Description

The ZL30406 is an analog phased-locked loop which provides rate conversion and jitter attenuation for SONET/SDH OC-48/STM-16, OC-12/STM-4 and OC-3/STM-1 applications. A functional block diagram of the ZL30406 is shown in Figure 1 and a brief description is presented in the following sections.

1.1 Frequency/Phase Detector

The Frequency/Phase Detector compares the frequency/phase of the input reference signal with the feedback signal from the Frequency Divider circuit and provides an error signal corresponding to the frequency/phase difference between the two. This error signal is passed to the Loop Filter circuit and averaged to control the VCO frequency.

1.2 Loop Filter

The Loop Filter is a low pass filter. This low pass filter ensures that the network jitter requirements are met for an input reference frequency of 19.44 MHz. The corner frequency of the Loop Filter is configurable with an external capacitor and resistor connected to the LPF pin and ground as shown below.

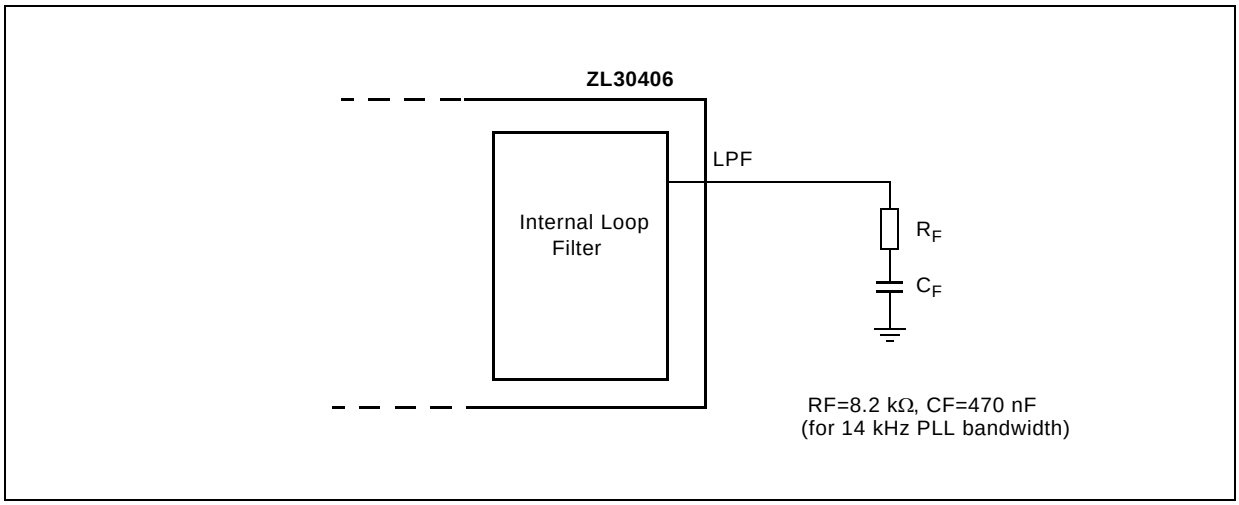


Figure 3 - External Loop Filter

1.3 VCO

The voltage-controlled oscillator (VCO) receives the filtered error signal from the Loop Filter, and based on the voltage of the error signal, generates a primary frequency. The VCO output is connected to the Output Interface Circuit that divides VCO frequency and buffers generated clocks.

1.4 Output Interface Circuit

The output of the VCO is used by the Output Interface Circuit to provide four LVPECL differential clocks at 77.76 MHz, one programmable CML differential clock (19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz) controlled with FS1-2 pins and a single-ended 19.44 MHz output clock. This block provides also a 19.44 MHz feedback clock that closes PLL loop. Each output clock can be enabled or disabled individually with the associated Output Enable pin.

Output Clocks	Output Enable Pins
C77oP/N-A	C77oEN-A
C77oP/N-B	C77oEN-B
C77oP/N-C	C77oEN-C
C77oP/N-D	C77oEN-D
OC-CLKoP/N	OC-CLKoEN
C19o	C19oEN

Table 1 - Output Enable Control

To reduce power consumption and achieve the lowest possible intrinsic jitter the unused output clocks must be disabled. If any of the LVPECL outputs are disabled they must be left open without any terminations.

The output clock frequency of the OC-CLKo CML differential output clock is selected with FS1-2 pins as shown in the following table.

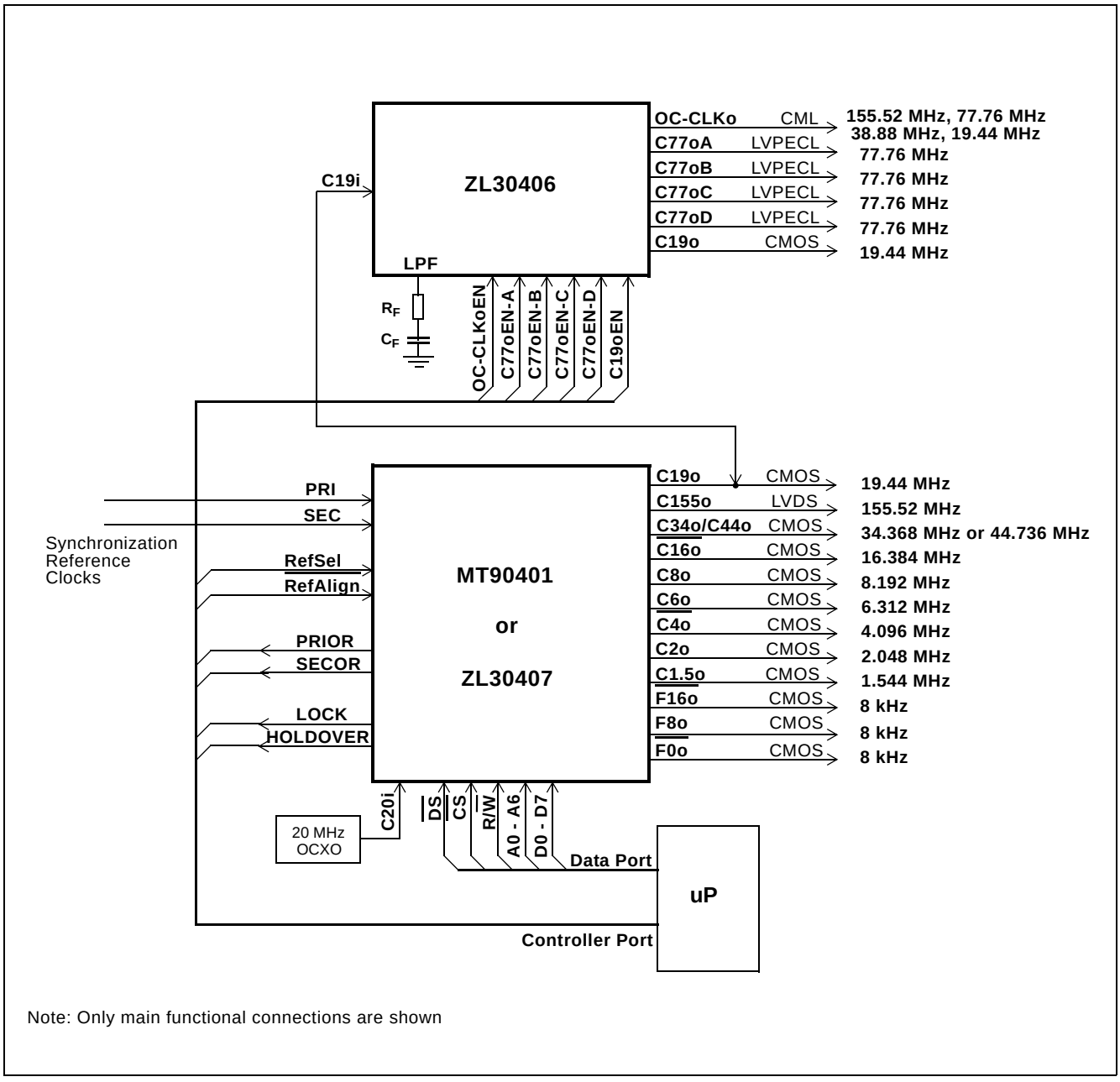
FS2	FS1	OC-CLKo Frequency
0	0	19.44 MHz
0	1	38.88 MHz
1	0	77.76 MHz
1	1	155.52 MHz

Table 2 - OC-CLKo Clock Frequency Selection

2.0 Applications

2.1 Ultra-Low Jitter SONET/SDH Equipment Clocks

The ZL30406 functionality and performance complements the entire family of the Zarlink's advanced network synchronization PLLs. Its superior jitter filtering characteristics exceed requirements of SONET/SDH optical interfaces operating at OC-48/STM-16 rate (2.5 Gbit/s). The ZL30406 in combination with the MT90401 or the ZL30407 (SONET/SDH Network Element PLLs) provides the core building blocks for high quality equipment clocks suitable for network synchronization (see Figure 4).



Note: Only main functional connections are shown

Figure 4 - SONET/SDH Equipment Timing Card

The ZL30406 in combination with the MT9046 provides an optimum solution for SONET/SDH line cards (see Figure 5).

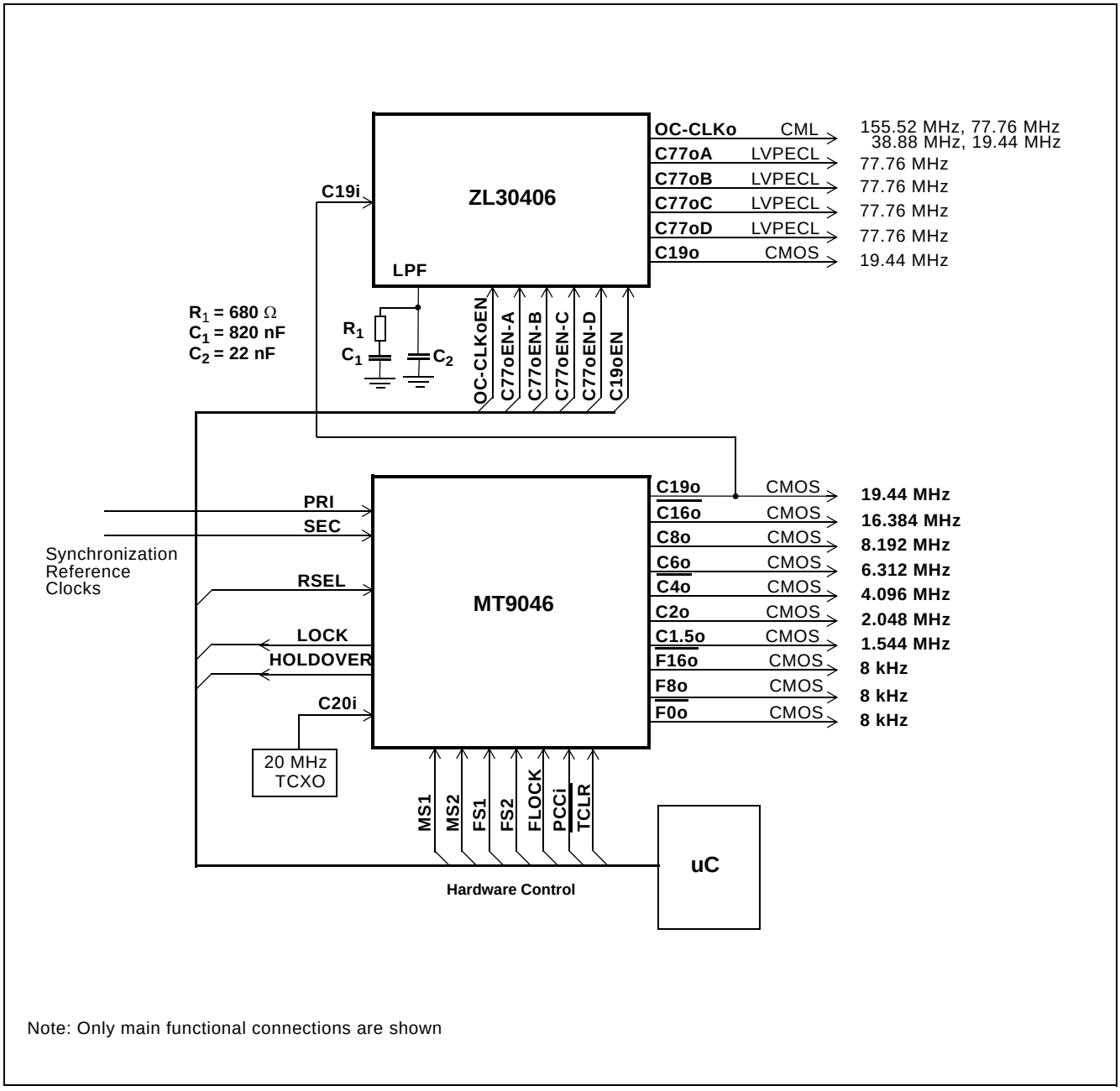


Figure 5 - SONET/SDH Line Card

2.2 Recommended Interface Circuit

2.2.1 LVPECL to LVPECL Interface

The C77oP/N-A, C77oP/N-B, C77oP/N-B, and C77oP/N-D outputs provide differential LVPECL clocks at 77.76 MHz. The LVPECL output drivers require a 50 Ω termination connected to the VCC-2V source for each output terminal at the terminating end as shown below. The terminating resistors should be placed as close as possible to the LVPECL receiver.

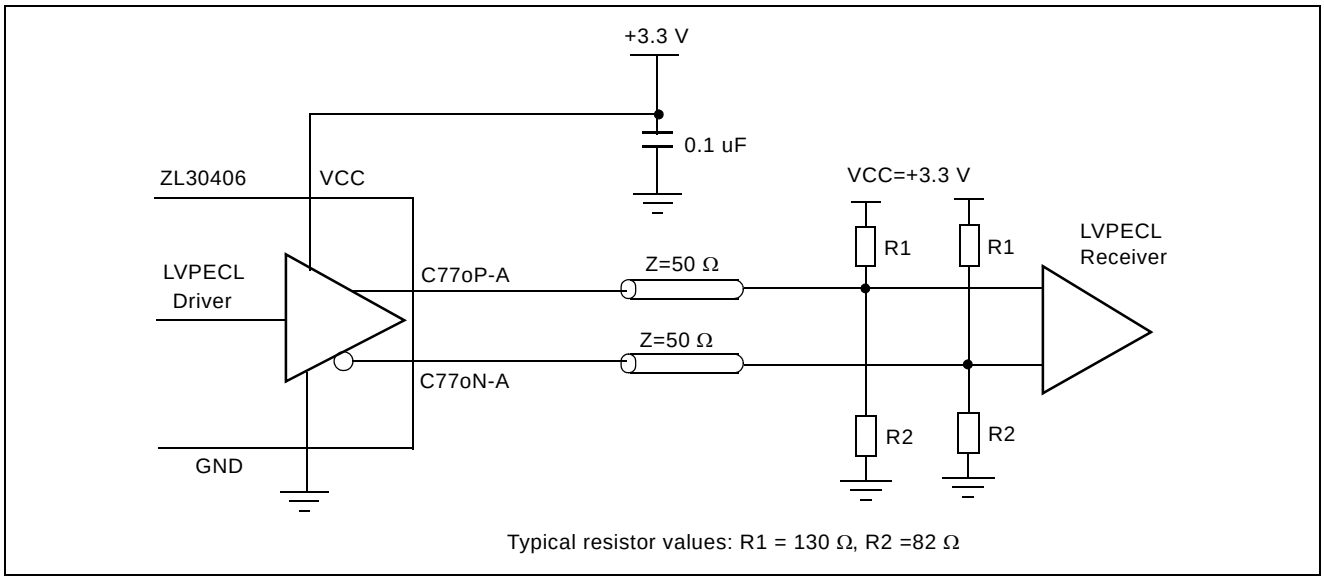


Figure 6 - LVPECL to LVPECL Interface

2.2.2 CML to CML Interface

The CMLP/N output provides a differential CML/LVDS compatible clock at 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz selected with FS1-2 pins. The output drivers require a 50 Ω load at the terminating end if the receiver is CML type.

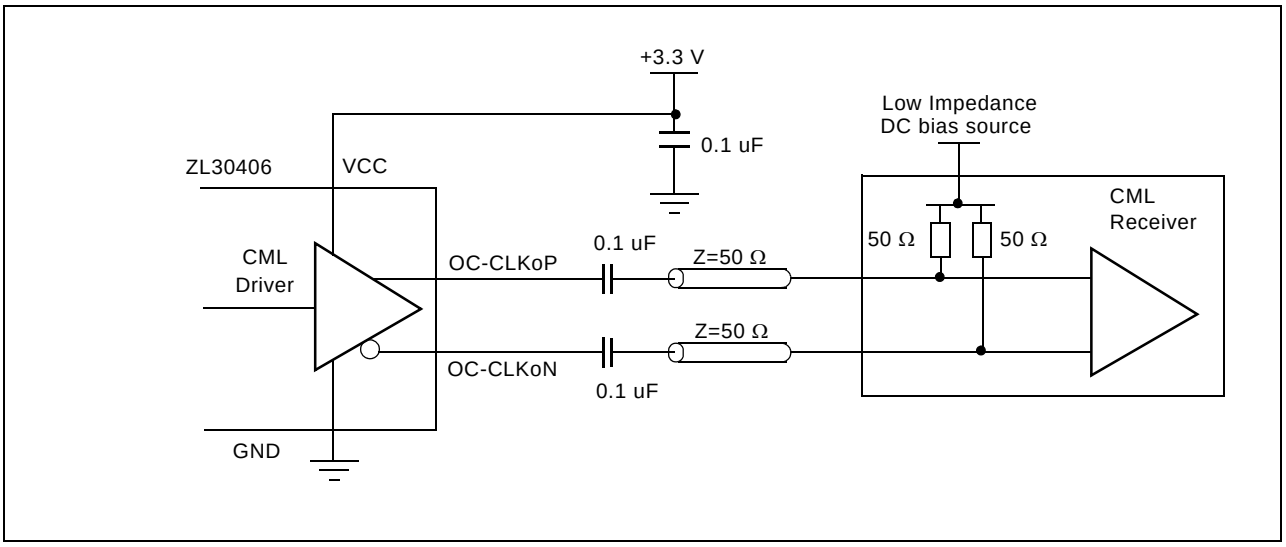


Figure 7 - CML to CML Interface

2.2.3 CML to LVDS Interface

To configure the driver as an LVDS driver, external biasing resistors are required to set up the common mode voltage as specified by ANSI/TIA/EIA-644 LVDS standard. The standard specifies the V_{CM} (common mode voltage) as minimum 1.125 V, typical 1.2 V, and maximum 1.375 V. The following figure provides a recommendation for LVDS applications.

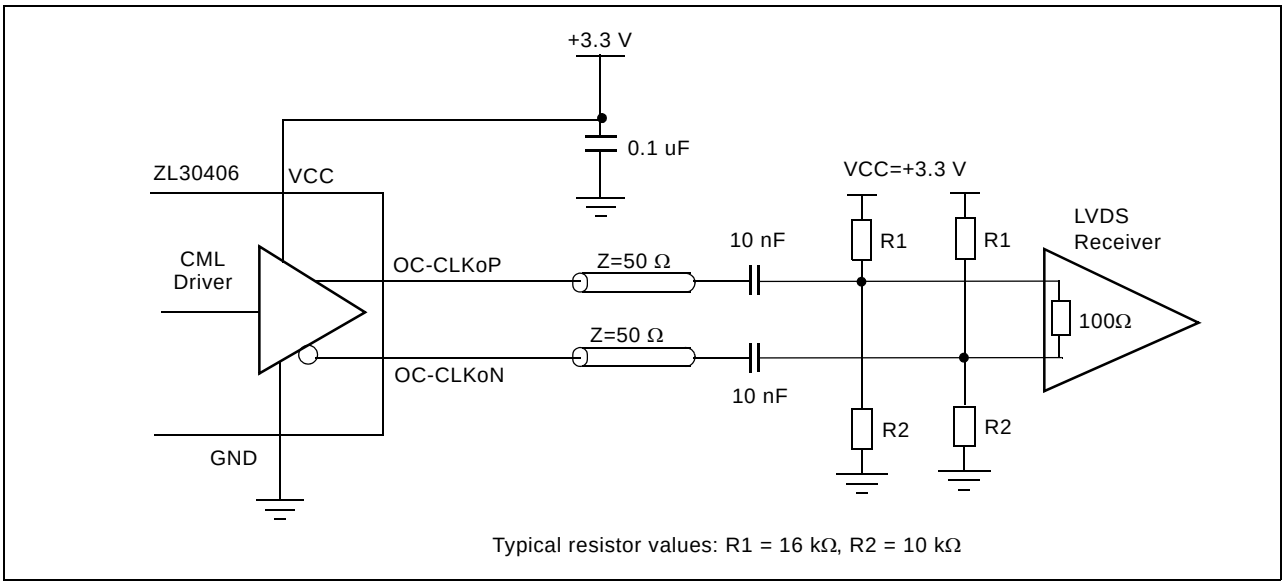


Figure 8 - LVDS Termination

2.2.4 CML to LVPECL Interface

In the case when more than four 77.76 MHz clocks are required to drive LVPECL receivers then the unused OC-CLKo clock (CML output) can be configured to output the 77.76 MHz clock and interface to the LVPECL receiver as is shown in the Figure 9. The terminating resistors should be placed as close as possible to the LVPECL receiver.

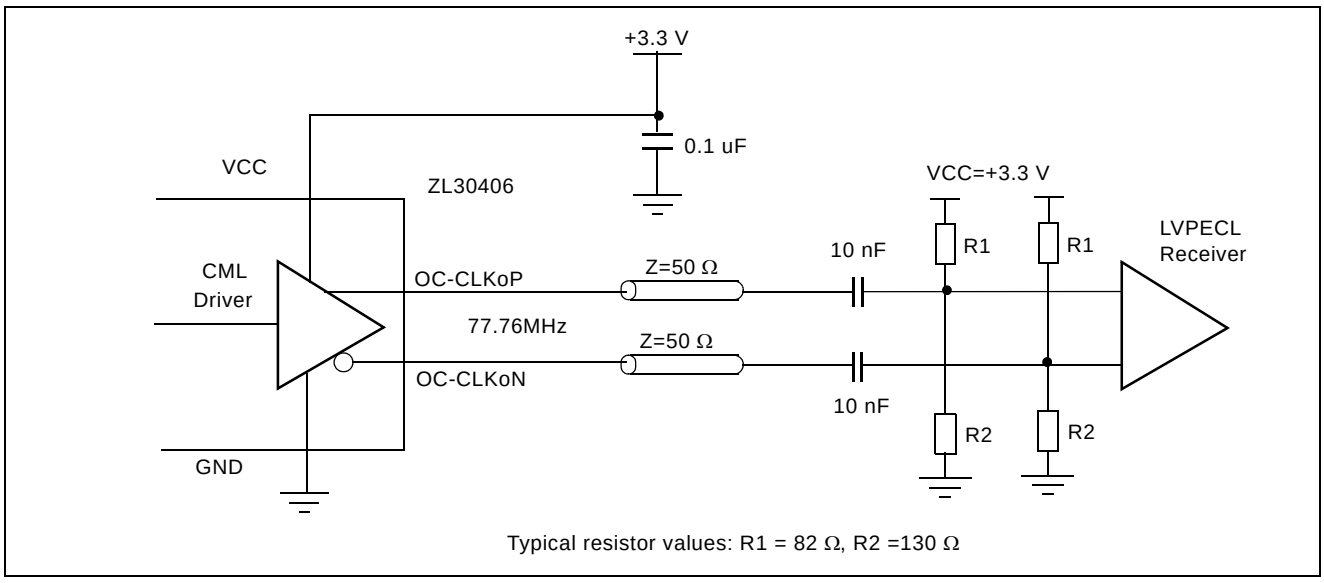


Figure 9 - CML to LVPECL Interface

2.3 Tristating LVPECL Outputs

The ZL30406 has four differential 77.76 MHz LVPECL outputs, which can be used to drive four different OC-3/OC-12/OC-48 devices such as framers, mappers and SERDES. In the case where fewer than four clocks are required, a user can disable unused LVPECL outputs on the ZL30406 by pulling the corresponding enable pins low. When disabled, voltage at the both pins of the differential LVPECL output will be pulled up to Vcc - 0.7 V.

For applications requiring the LVPECL outputs to be in a tri-state mode, external AC coupling capacitors can be used as shown in Figure 10. Typically this might be required in hot swappable applications.

Resistors R1 and R2 are required for DC bias of the LVPECL driver. Capacitors C1 and C2 are used as AC coupling capacitors. During disable mode (C77oEN pin pulled low) those capacitors present infinite impedance to the DC signal and to the receiving device this looks like a tristated (High-Z) output. Resistors R3, R4, R5 and R6 are used to terminate the transmission line with 50 ohm impedance and to generate DC bias voltage for the LVPECL receiver. If the LVPECL receiver has an integrated 50 ohm termination and bias source, resistors R3, R4, R5 and R6 should not be populated.

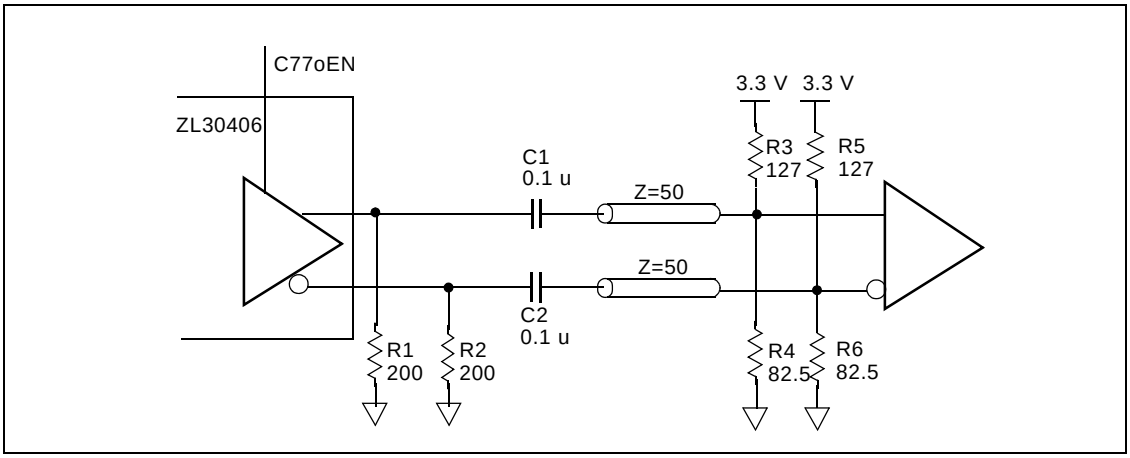
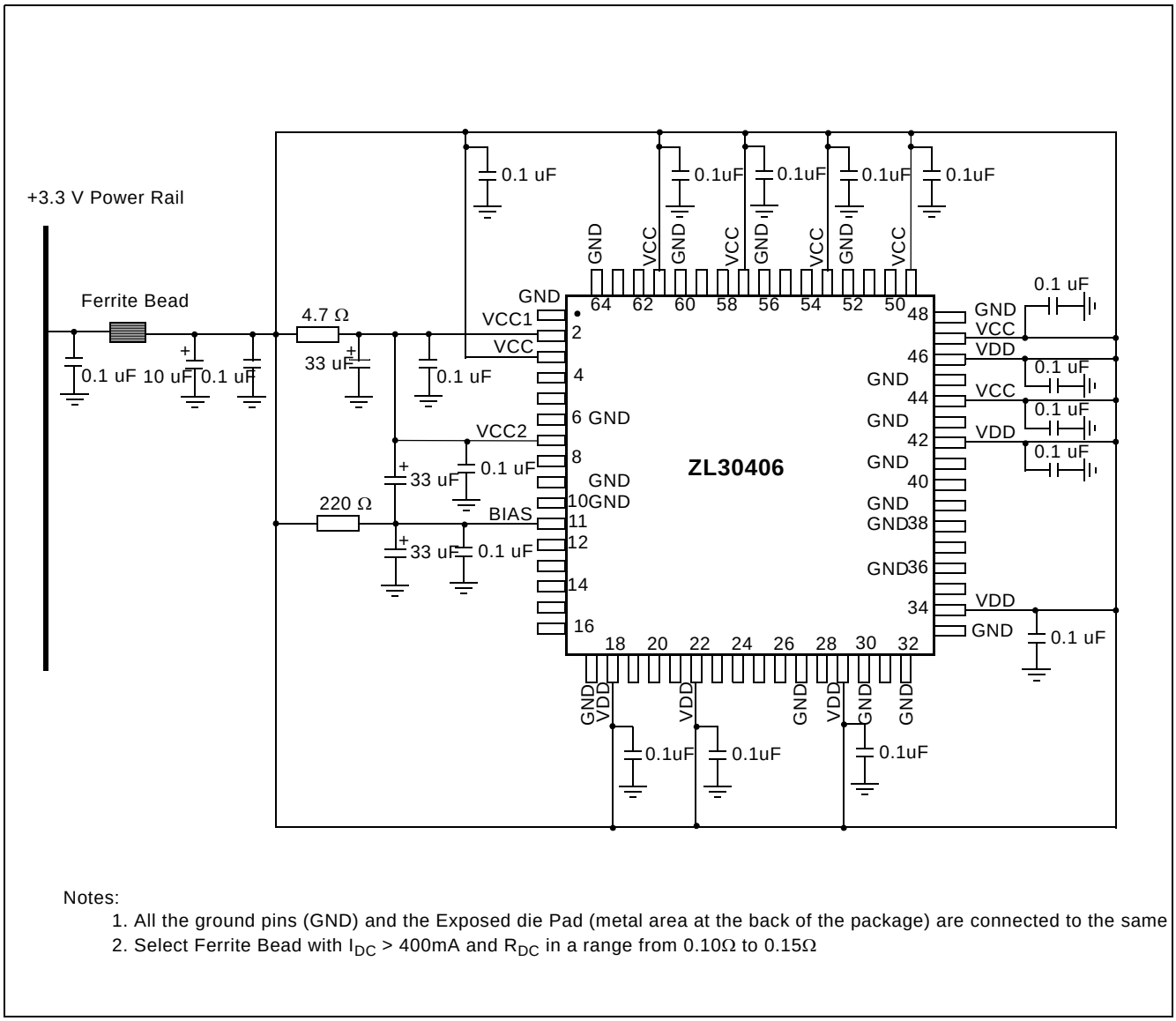


Figure 10 - Tristatable LVPECL Outputs

2.4 Power Supply and BIAS Circuit Filtering Recommendations

Figure 11 presents a complete filtering arrangement that is recommended for applications requiring maximum jitter performance. The level of required filtering is subject to further optimization and simplification. Please check Zarlink's web site for updates.



Notes:

1. All the ground pins (GND) and the Exposed die Pad (metal area at the back of the package) are connected to the same
2. Select Ferrite Bead with I_{DC} > 400mA and R_{DC} in a range from 0.10Ω to 0.15Ω

Figure 11 - Power Supply and BIAS circuit filtering

3.0 Characteristics

Absolute Maximum Ratings†

	Characteristics	Sym	Min.‡	Max.‡	Units
1	Supply voltage	V_{DDR}, V_{CCR}	TBD	TBD	V
2	Voltage on any pin	V_{PIN}	-0.5	V_{CC} + 0.5 V_{DD} + 0.5	V
3	Current on any pin	I_{PIN}	-0.5	30	mA
4	ESD Rating	V_{ESD}		1500	V
5	Storage temperature	T_{ST}	-55	125	°C
6	Package power dissipation	P_{PD}		1.8	W

† Voltages are with respect to ground unless otherwise stated.
‡ Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions†

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Operating Temperature	T_{OP}	-40	25	+85	°C	
2	Positive Supply	V_{DD}, V_{CC} V_{CC_VCO}	3.0	3.3	3.6	V	

† Voltages are with respect to ground unless otherwise stated.
‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.
‡

DC Electrical Characteristics†

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Supply Current	I_{DD}+I_{CC}		140	155	mA	LVPECL, CML drivers disabled and unterminated
2	Incremental Supply Current to single LVPECL driver (driver enabled and terminated, see Figure 6)	I_{LVPECL}		40		mA	Note 1,2
3	Incremental Supply Current to CML driver (driver enabled and terminated, see Figure 7)	I_{CML}		24		mA	Note 3
4	CMOS: High-level input voltage	V_{IH}	0.7V_{DD}		V_{DD}	V	
5	CMOS: Low-level input voltage	V_{IL}	0		0.3V_{DD}	V	
6	CMOS: Input leakage current, C19i	I_{IL}		1		uA	V_I = V_{DD} or 0V

DC Electrical Characteristics† (continued)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
7	CMOS: Input bias current for pulled-down inputs: FS1, FS2, C77oEN-A, C77oEN-C, C77oEN-D, OC-CLKoEN	I_{B-PU}		300		uA	$V_I = V_{DD}$
8	CMOS: Input bias current for pulled-up inputs: , C77oEN-B, C19o_EN	I_{B-PD}		90		uA	V_I = 0V
9	CMOS: High-level output voltage	V_{OH}	2.4			V	I_{OH} = 8 mA
10	CMOS: Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
11	CMOS: C19o output rise time (18pF)	T_R		1.8	3.3	ns	18 pF load
12	CMOS: C19o output fall time (18pF)	T_F		1.1	1.4	ns	18 pF load
13	LVPECL: Differential output voltage	$IV_{OD\_LVPECL}I$		1.30		V	Note 2
14	LVPECL: Offset voltage	V_{OS_LVPECL}	Vcc-1.38	Vcc-1.27	Vcc-1.15	V	Note 2
15	LVPECL: Output rise/fall times	T_{RF}		260		ps	Note 2
16	CML: Differential output voltage	$IV_{OD\_CML}I$		0.70		V	Note 3
17	CML: Offset voltage (Also referred to as common mode voltage)	V_{OS_CML}	Vcc-0.58	Vcc-0.54	Vcc-0.50	V	Note 3
18	CML: Output rise/fall times	T_{RF}		120		ps	Note 3

† : Voltages are with respect to ground unless otherwise stated.

‡ :Typical figures are for design aid only: not guaranteed and not subject to production testing.

Note: Supply voltage and operating temperature are as per Recommended Operating Conditions

Note 1: The I_{LVPECL} current is determined by termination network connected to LVPECL outputs. More than 25% of this current flows outside the chip and it does not contribute to the internal power dissipation.

Note 2: LVPECL outputs terminated with Z_T = 50 Ω resistors biased to V_{CC}-2V (see Figure 6)

Note 3: CML outputs terminated with Z_T = 50 Ω resistors connected to low impedance DC bias voltage source (see Figure 7)

AC Electrical Characteristics† - Output Timing Parameters Measurement Voltage Levels

	Characteristics	Sym	CMOS‡	LVPECL	CML	Units
1	Threshold Voltage	$V_{T\text{-}CMOS}$ $V_{T\text{-}LVPECL}$ $V_{T\text{-}CML}$	$0.5V_{DD}$	$0.5V_{OD\_LVPECL}$	$0.5V_{OD\_CML}$	V
2	Rise and Fall Threshold Voltage High	V_{HM}	$0.7V_{DD}$	$0.8V_{OD\_LVPECL}$	$0.8V_{OD\_CML}$	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD}$	$0.2V_{OD\_LVPECL}$	$0.2V_{OD\_CML}$	V

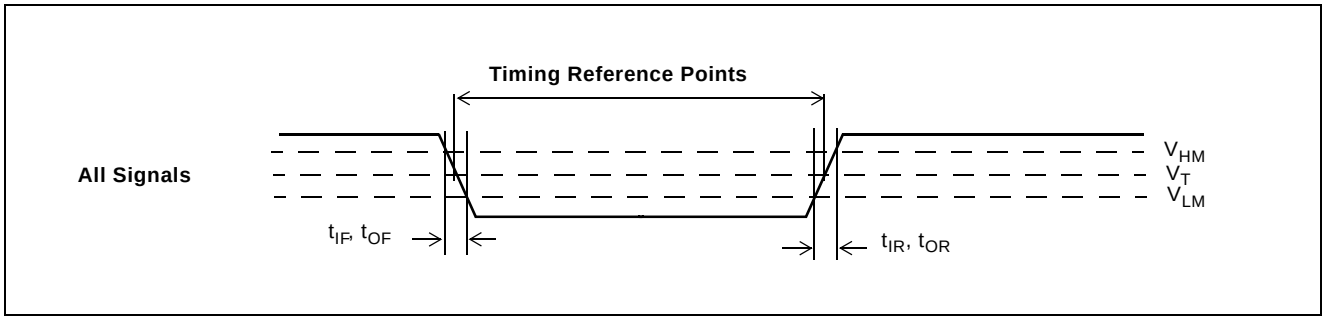
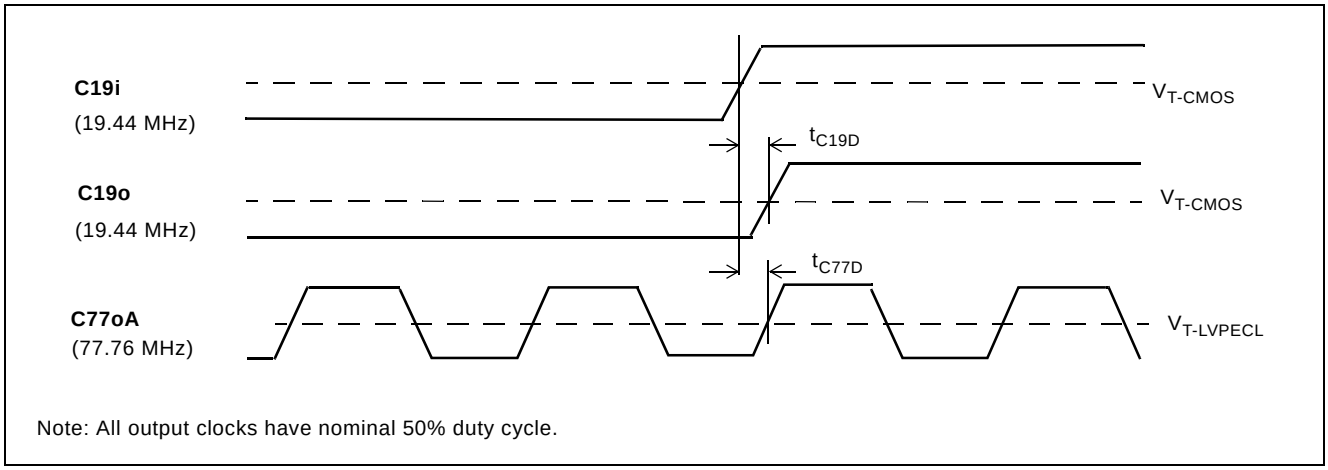


Figure 12 - Output Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics† - C19i Input to C19o and C77o Output Timing

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	C19i to C19o delay	t_{C19D}		6.7		ns	
2	C19i to C77oA delay	t_{C77D}		-4		ns	

† Supply voltage and operating temperature are as per Recommended Operating Conditions.
‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.



Note: All output clocks have nominal 50% duty cycle.

Figure 13 - C19i Input to C19o and C77o Output Timing

AC Electrical Characteristics† - C19i Input to OC-CLKo Output Delay Timing (CML)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	C19i to OC-CLKo(19) delay	$t_{OC-CLK19D}$		3.2		ns	
2	C19i to OC-CLKo(38) delay	$t_{OC-CLK38D}$		3.0		ns	
3	C19i to OC-CLKo(77) delay	$t_{OC-CLK77D}$		2.7		ns	
4	C19i to OC-CLKo(155) delay	$t_{OC-CLK155D}$		2.4		ns	

† Supply voltage and operating temperature are as per Recommended Operating Conditions.

‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.

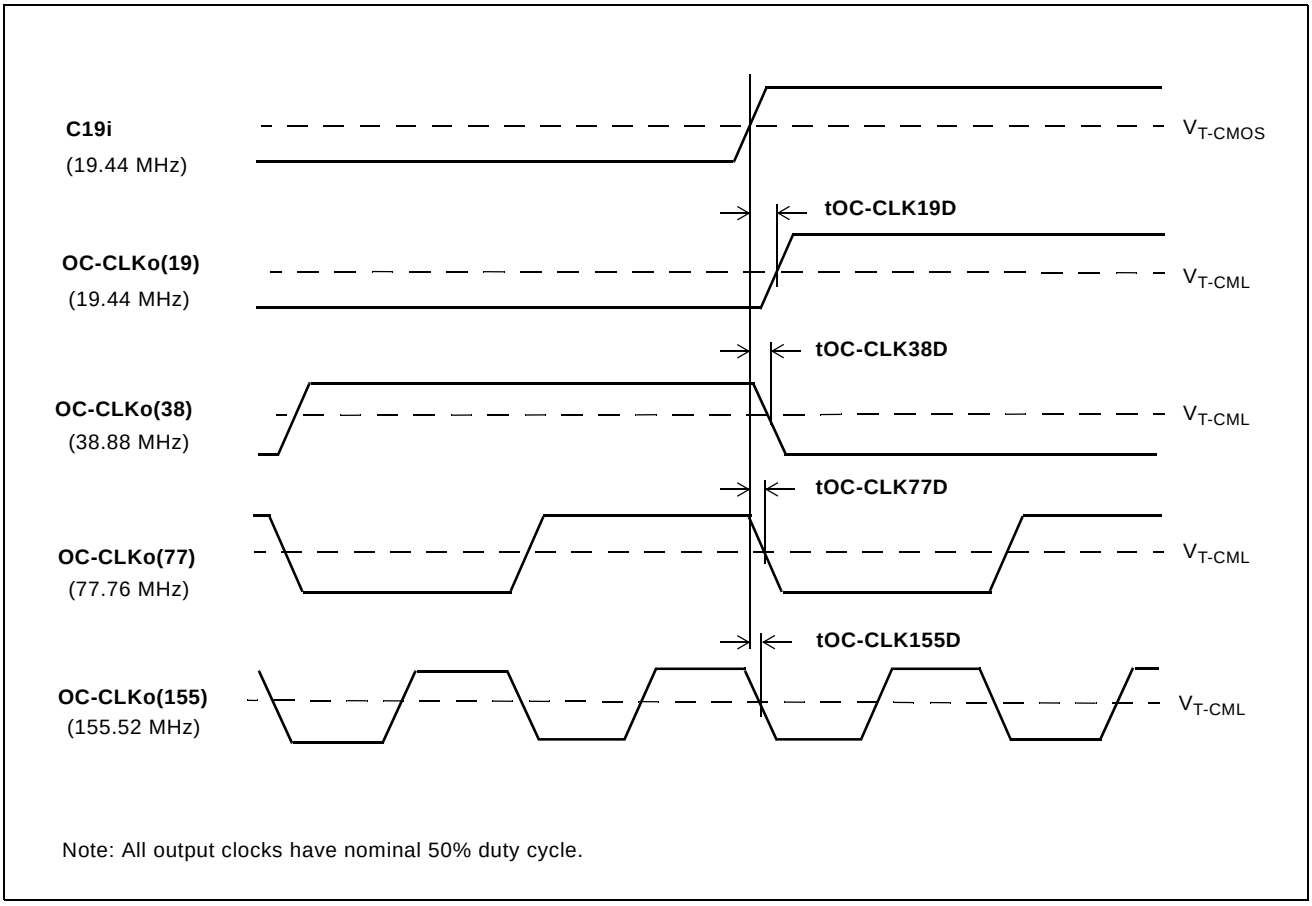


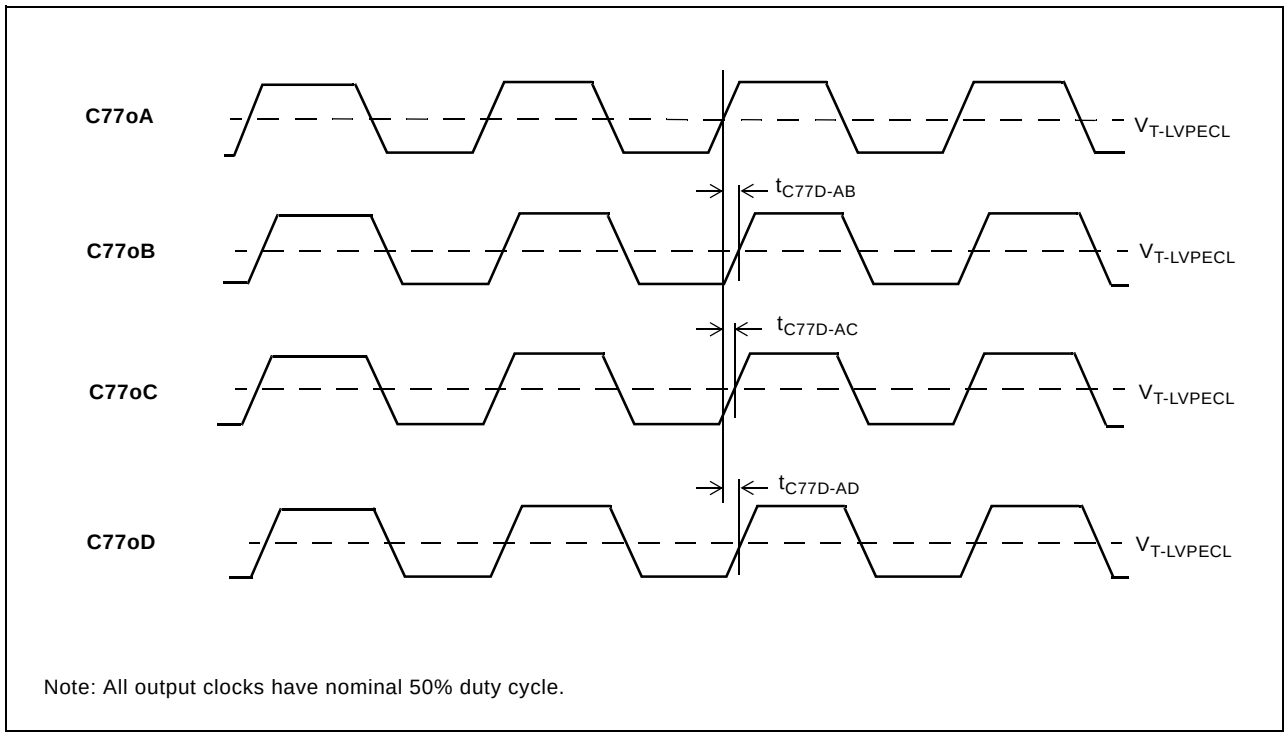
Figure 14 - C19i Input to OC-CLKo Output Timing

AC Electrical Characteristics† - C77 Clocks Output Timing

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	C77oA to C77oB	$t_{C77D-AB}$		100		ps	
2	C77oA to C77oC	$t_{C77D-AC}$		100		ps	
3	C77oA to C77oD	$t_{C77D-AD}$		100		ps	

† Supply voltage and operating temperature are as per Recommended Operating Conditions.

‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.



Note: All output clocks have nominal 50% duty cycle.

Figure 15 - C77oB, C77oC, C77oD Outputs Timing

Performance Characteristics - Functional- (V_{CC} = 3.3V ±10%; T_A = -40 to 85°C)

	Characteristics	Min.	Max.	Units	Notes
1	Pull-in range	±1000		ppm	
2	Lock Time		300	ms	

Performance Characteristics: Output Jitter Generation - GR-253-CORE conformance - (V_{CC} = 3.3V ±10%; T_A = -40 to 85°C)

GR-253-CORE Jitter Generation Requirements				ZL30406 Jitter Generation Performance			
	Interface (Category II)	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**Typ.†**	**Max.‡**	**Units**
1	OC-48 STS-48	12 kHz - 20 MHz	0.1 UIpp	40.2	-	16.9	ps_{P-P}
			$0.01UI_{RMS}$	4.02	1.3	2.1	ps_{RMS}
2	OC-12 STS-12	12 kHz - 5 MHz	0.1 UIpp	161	-	9.0	ps_{P-P}
			$0.01UI_{RMS}$	16.1	0.7	1.3	ps_{RMS}

† Typical figures are for design aid only: not guaranteed and not subject to production testing.

‡ Loop Filter components: R_F=8.2 kΩ, C_F=470 nF

Performance Characteristics: Output Jitter Generation - ETSI EN 300 462-7-1 conformance - (V_{CC} = 3.3V ±10%; T_A = -40 to 85°C)

EN 300 462-7-1 Jitter Generation Requirements				ZL30406 Jitter Generation Performance			
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**Typ.†**	**Max.‡**	**Units**
1	STM-16	1 MHz to 20 MHz	0.1 UIpp	40.2	-	12.6	ps_{P-P}
			-	-	1.0	1.5	ps_{RMS}
		5 kHz to 20 MHz	0.5UIpp	201	-	17.1	ps_{P-P}
			-	-	1.3	2.2	ps_{RMS}
2	STM-4	250 kHz to 5 MHz	0.1 UIpp	161	-	5.8	ps_{P-P}
			-	-	0.46	0.9	ps_{RMS}
		1 kHz to 5 MHz	0.5 UIpp	804	-	29.8	ps_{P-P}
			-	-	2.4	3.2	ps_{RMS}

† Typical figures are for design aid only: not guaranteed and not subject to production testing.

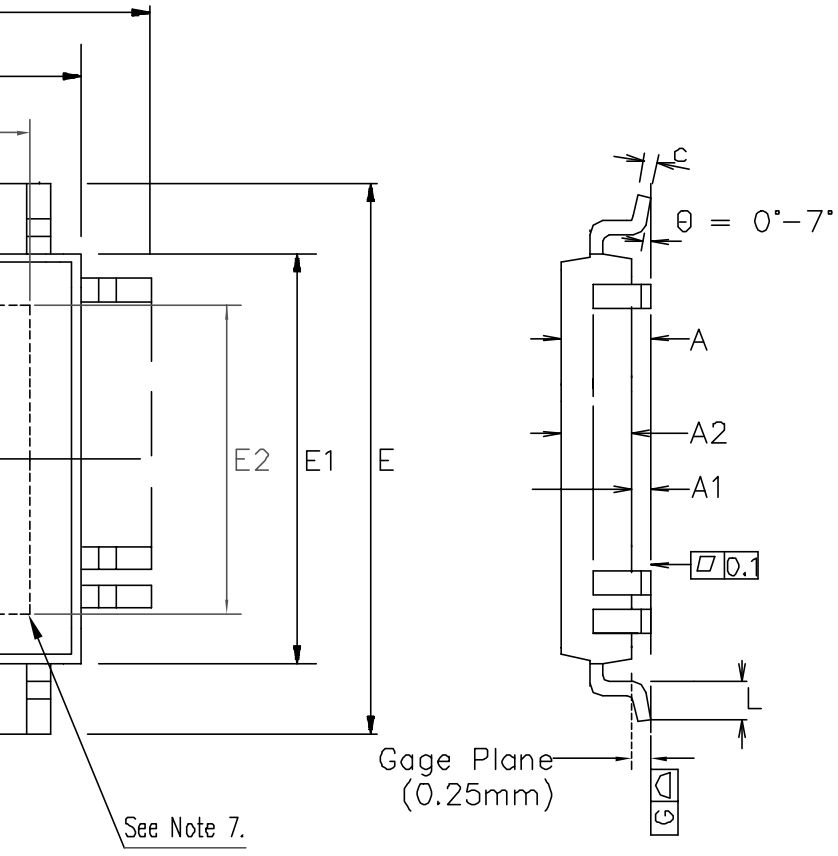
‡ Loop Filter components: R_F=8.2 kΩ, C_F=470 nF

Performance Characteristics: Output Jitter Generation - G.813 conformance (Option 1 and 2) - (V_{CC} = 3.3V ±10%; T_A = -40 to 85°C)

G.813 Jitter Generation Requirements				ZL30406 Jitter Generation Performance			
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**Typ.†**	**Max.‡**	**Units**
Option 1							
1	STM-16	1 MHz to 20 MHz	0.1 UIpp	40.2	-	12.6	ps_{P-P}
			-	-	1.0	1.5	ps_{RMS}
		5 kHz to 20 MHz	0.5 UIpp	201	-	17.1	ps_{P-P}
			-	-	1.3	2.2	ps_{RMS}
2	STM-4	250 kHz to 5 MHz	0.1 UIpp	161	-	5.8	ps_{P-P}
			-	-	0.46	0.9	ps_{RMS}
		1 kHz to 5 MHz	0.5 UIpp	804	-	29.8	ps_{P-P}
			-	-	2.4	3.2	ps_{RMS}
Option 2							
3	STM-16	12 kHz - 20 MHz	0.1 UIpp	40.2	-	16.9	ps_{P-P}
			-	-	1.3	2.1	ps_{RMS}
4	STM-4	12 kHz - 5 MHz	0.1 UIpp	161	-	9.0	ps_{P-P}
			-	-	0.7	1.3	ps_{RMS}

† Typical figures are for design aid only: not guaranteed and not subject to production testing.

‡ Loop Filter components: R_F=8.2 kΩ, C_F=470 nF



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	1.20		---	0.047
A1	0.05	0.15		0.002	0.006
A2	0.95	1.05		0.037	0.041
D	12.00 BSC			0.472 BSC	
D1	10.00 BSC			0.394 BSC	
D2	6.74	7.5		0.265	0.295
E	12.00 BSC			0.472 BSC	
E1	10.00 BSC			0.394 BSC	
E2	6.74	7.5		0.265	0.295
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	64				
ND	16				
NE	16				
NOTE	SQUARE				

Conforms to JEDEC MS-026 ACD Iss. C

oth.

he bottom package body size by a max. of 0.15 mm.
ion.

.08 mm max.

nils on straight edge, and upto 50mils at corner.

	Package Code QD/QG
Previous package codes N/A	Package Outline for 64 Lead e-Pad TQFP 10x10x1.0mm, +2.0mm (footprint) with 7.5mm DAP (Die Attach Pad)
	113400

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