THE DATASHEET OF

AD8016ARBZ

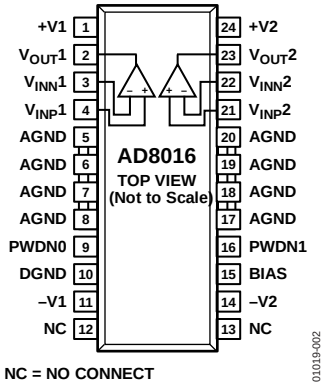
Low Power, High Output Current xDSL Line Driver

Data Sheet **AD8016**

FEATURES

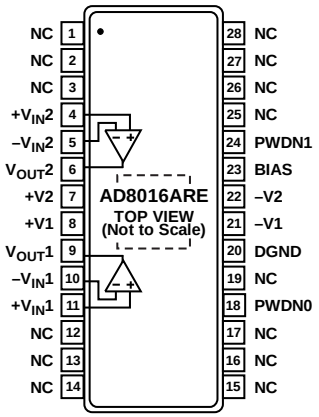
- xDSL line driver that features full ADSL central office (CO)
  - Performance on ±12 V supplies
- Low power operation
  - ±5 V to ±12 V voltage supply
  - 12.5 mA/amp (typical) total supply current
  - Power reduced keep alive current of 4.5 mA/amp
- High output voltage and current drive
  - I_{OUT} = 600 mA
  - 40 V p-p differential output voltage R_L = 50 Ω, V_S = ±12 V
- Low single-tone distortion
  - –75 dBc @ 1 MHz SFDR, R_L = 100 Ω, V_{OUT} = 2 V p-p
- MTPR = –75 dBc, 26 kHz to 1.1 MHz, Z_{LINE} = 100 Ω,
  - P_{LINE} = 20.4 dBm
- High Speed
  - 78 MHz bandwidth (–3 dB), G = +5
  - 40 MHz gain flatness
  - 1000 V/µs slew rate

PIN CONFIGURATIONS



NC = NO CONNECT

Figure 1. 24-Lead SOIC_W_BAT (RB-24)



NOTES
1. THE EXPOSED PADDLE IS FLOATING, NOT ELECTRICALLY CONNECTED INTERNALLY.
2. NC = NO CONNECT.

Figure 2. 28-Lead TSSOP_EP (RE-28-1)

GENERAL DESCRIPTION

The AD8016 high output current dual amplifier is designed for the line drive interface in Digital Subscriber Line systems such as ADSL, HDSL2, and proprietary xDSL systems. The drivers are capable, in full-bias operation, of providing 24.4 dBm output power into low resistance loads, enough to power a 20.4 dBm line, including hybrid insertion loss.

The AD8016 is available in a low cost 24-lead SOIC_W_BAT and a 28-lead TSSOP_EP with an exposed lead frame (ePAD). Operating from ±12 V supplies, the AD8016 requires only 1.5 W of total power dissipation (refer to the Power Dissipation section for details) while driving 20.4 dBm of power downstream using the xDSL hybrid in Figure 35 and Figure 36. Two digital bits (PWDN0, PWDN1) allow the driver to be capable of full performance, an output keep-alive state, or two intermediate bias states. The keep-alive state biases the output transistors enough to provide a low impedance at the amplifier outputs for back termination.

The low power dissipation, high output current, high output voltage swing, flexible power-down, and robust thermal packaging enable the AD8016 to be used as the central office (CO) terminal driver in ADSL, HDSL2, VDSL, and proprietary xDSL systems.

Rev. C

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11/03—Rev. A to Rev. B

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Updated Outline Dimensions ... 19-20

SPECIFICATIONS

@ 25°C, V_S = ±12 V, R_L = 100 Ω, PWDN0, PWDN1 = (1, 1), T_{MIN} = −40°C, T_{MAX} = +85°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, R_F = 1.5 kΩ, V_{OUT} = 0.2 V p-p		380		MHz
	G = +5, R_F = 499 Ω, V_{OUT} < 0.5 V p-p	69	78		MHz
Bandwidth for 0.1 dB Flatness	G = +5, R_F = 499 Ω, V_{OUT} = 0.2 V p-p	16	38		MHz
Large Signal Bandwidth	V_{OUT} = 4 V p-p		90		MHz
Peaking	V_{OUT} = 0.2 V p-p < 50 MHz		0.1		dB
Slew Rate	V_{OUT} = 4 V p-p, G = +2		1000		V/µs
Rise and Fall Time	V_{OUT} = 2 V p-p		2		ns
Settling Time	0.1%, V_{OUT} = 2 V p-p		23		ns
Input Overdrive Recovery Time	V_{OUT} = 12.5 V p-p		350		ns
NOISE/DISTORTION PERFORMANCE					
Distortion, Single-Ended	V_{OUT} = 2 V p-p, G = +5, R_F = 499 Ω				
Second Harmonic	f_C = 1 MHz, R_L = 100 Ω/25 Ω	−75/−62	−77/−64		dBc
Third Harmonic	f_C = 1 MHz, R_L = 100 Ω/25 Ω	−88/−74	−93/−76		dBc
Multitone Power Ratio[1]	26 kHz to 1.1 MHz, Z_{LINE} = 100 Ω, P_{LINE} = 20.4 dBm		−75		dBc
IMD	500 kHz, Δf = 10 kHz, R_L = 100 Ω/25 Ω	−84/−80	−88/−85		dBc
IP3	500 kHz, R_L = 100 Ω/25 Ω	42/40	43/41		dBm
Voltage Noise (RTI)	f = 10 kHz		2.6	4.5	nV/√Hz
Input Current Noise	f = 10 kHz		18	21	pA√Hz
INPUT CHARACTERISTICS					
RTI Offset Voltage		−3.0	1.0	+3.0	mV
+Input Bias Current		−45		+45	µA
−Input Bias Current		−75	4	+75	µA
Input Resistance			400		kΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range		−10		+10	V
Common-Mode Rejection Ratio		58	64		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Single-ended, R_L = 100 Ω	−11		+11	V
Linear Output Current	G = 5, R_L = 10 Ω, f_1 = 100 kHz, −60 dBc SFDR	400	600		mA
Short-Circuit Current			2000		mA
Capacitive Load Drive			80		pF
POWER SUPPLY					
Operating Range		±3		±13	V
Quiescent Current	PWDN1, PWDN0 = (1, 1)		12.5	13.2	mA/Amp
	PWDN1, PWDN0 = (1, 0)		8	10	mA/Amp
	PWDN1, PWDN0 = (0, 1)		5	8	mA/Amp
	PWDN1, PWDN0 = (0, 0)		4	6	mA/Amp
Recovery Time	To 95% of I_Q		25		µs
Shutdown Current	250 µA out of bias pin		1.5	4.0	mA/Amp
Power Supply Rejection Ratio	ΔV_S = ±1 V	63	75		dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

[1] See Figure 48, R20, R21 = 0 Ω, R1 = open.

@ 25°C, V_S = ±6 V, R_L = 100 Ω, PWDN0, PWDN1 = (1, 1), T_{MIN} = −40°C, T_{MAX} = +85°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, R_F = 1.5 kΩ, V_{OUT} = 0.2 V p-p		320		MHz
	G = +5, R_F = 499 Ω, V_{OUT} < 0.5 V p-p	70	71		MHz
Bandwidth for 0.1 dB Flatness	G = +5, R_F = 499 Ω, V_{OUT} = 0.2 V p-p	10	15		MHz
Large Signal Bandwidth	V_{OUT} = 1 V rms		80		MHz
Peaking	V_{OUT} = 0.2 V p-p < 50 MHz		0.7	1.0	dB
Slew Rate	V_{OUT} = 4 V p-p, G = +2		300		V/µs
Rise and Fall Time	V_{OUT} = 2 V p-p		2		ns
Settling Time	0.1%, V_{OUT} = 2 V p-p		39		ns
Input Overdrive Recovery Time	V_{OUT} = 6.5 V p-p		350		ns
NOISE/DISTORTION PERFORMANCE					
Distortion, Single-Ended	G = +5, V_{OUT} = 2 V p-p, R_F = 499 Ω				
Second Harmonic	f_C = 1 MHz, R_L = 100 Ω/25 Ω	−73/61	−75/−63		dBc
Third Harmonic	f_C = 1 MHz, R_L = 100 Ω/25 Ω	−80/−68	−82/−70		dBc
Multitone Power Ratio[1]	26 kHz to 138 kHz, Z_{LINE} = 100 Ω, P_{LINE} = 13 dBm		−68		dBc
IMD	500 kHz, Δf = 110 kHz, R_L = 100 Ω/25 Ω	−87/−82	−88/−83		dBc
IP3	500 kHz	42/39	42/39		dBm
Voltage Noise (RTI)	f = 10 kHz		4	5	nV/√Hz
Input Current Noise	f = 10 kHz		17	20	pA√Hz
INPUT CHARACTERISTICS					
RTI Offset Voltage		−3.0	0.2	+3.0	mV
+Input Bias Current		−25	10	+25	µA
−Input Bias Current		−30	10	+30	µA
Input Resistance			400		kΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range		−4		+4	V
Common-Mode Rejection Ratio		60	66		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Single-Ended, R_L = 100 Ω	−5		+5	V
Linear Output Current	G = +5, R_L = 5 Ω, f = 100 kHz, −60 dBc SFDR	300	420		mA
Short-Circuit Current			830		mA
Capacitive Load Drive	R_S = 10 Ω		50		pF
POWER SUPPLY					
Quiescent Current	PWDN1, PWDN0 = (1, 1)		8	9.7	mA/Amp
	PWDN1, PWDN0 = (1, 0)		6	6.9	mA/Amp
	PWDN1, PWDN0 = (0, 1)		4	5.0	mA/Amp
	PWDN1, PWDN0 = (0, 0)		3	4.1	mA/Amp
Recovery Time	To 95% of I_Q		23		µs
Shutdown Current	250 µA out of bias pin		1.0	2.0	mA/Amp
Power Supply Rejection Ratio	ΔV_S = ±1 V	63	80		dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

[1]See Figure 48, R20, R21 = 0 Ω, R1 = open.

LOGIC INPUTS (CMOS COMPATIBLE LOGIC)

PWDN0, PWDN1, V_{CC} = ±12 V or ±6 V; full temperature range.

Table 3.

Parameter	Min	Typ	Max	Unit
Logic 1 Voltage	2.2		V_{CC}	V
Logic 0 Voltage	0		0.8	V

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	26.4 V
Internal Power Dissipation	
SOIC_W_BAT Package[1]	1.4 W
TSSOP_EP Package[2]	1.4 W
Input Voltage (Common-Mode)	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Output Short-Circuit Duration	Observe power derating curves
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C

[1] Specification is for device on a 4-layer board with 10 inches^2 of 1 oz copper at 85°C 24-lead SOIC_W_BAT package: θ_{JA} = 28°C/W.
2 Specification is for device on a 4-layer board with 9 inches^2 of 1 oz copper at 85°C 28-lead (TSSOP_EP) package: θ_{JA} = 29°C/W.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8016 is limited by the associated rise in junction temperature. The maximum safe junction temperature for a plastic encapsulated device is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package.

The output stage of the AD8016 is designed for maximum load current capability. As a result, shorting the output to common can cause the AD8016 to source or sink 2000 mA. To ensure proper operation, it is necessary to observe the maximum power derating curves. Direct connection of the output to either power supply rail can destroy the device.

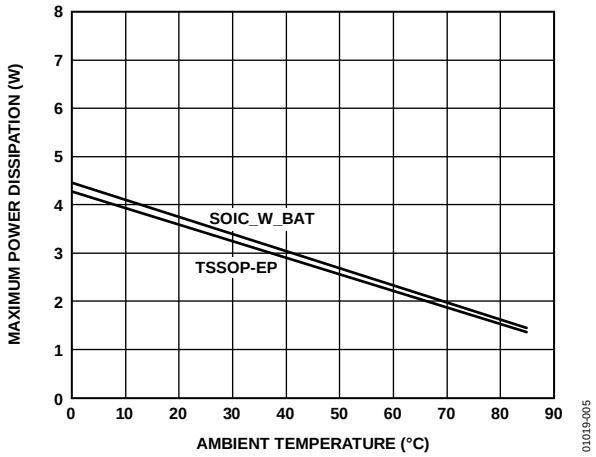

Figure 3. Maximum Power Dissipation vs. Temperature for AD8016 for T_J = 125 °C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

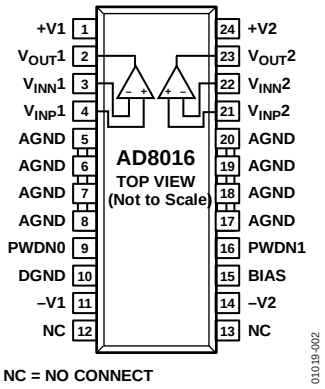

Figure 4. 24-Lead SOIC_W_BAT (RB-24)

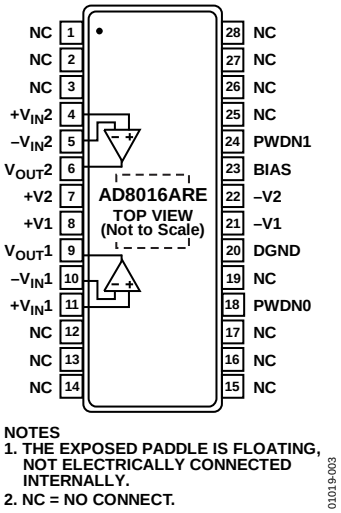

Figure 5. 28-Lead TSSOP_EP (RE-28-1)

Table 5. Pin Function Descriptions

Pin No.			
SOIC_W_BAT	**TSSOP_EP**	**Mnemonic**	**Description**
1	8	+V1	Positive Power Supply, Amp 1.
2	9	$V_{OUT}1$	Output Signal, Amp 1.
3		$V_{INN}1$	Negative Input Signal, Amp 1.
4		$V_{INP}1$	Positive Input Signal, Amp1.
5 to 8, 17 to 20		AGND	Analog Ground.
9	18	PWDN0	Power-Down Input 0.
10	20	DGND	Digital Ground.
11	21	–V1	Negative Power Supply, Amp1.
12, 13	1 to 3, 12 to 17, 19, 25 to 28	NC	This pin is not connected internally (see Figure 4 and Figure 5).
14	22	–V2	–V Power Supply, Amp 2.
15	23	BIAS	Quiescent Current Adjust.
16	24	PWDN1	Power-Down Input 1.
21		$V_{INP}2$	Positive Input Signal, Amp 2.
22		$V_{INN}2$	Negative Input Signal, Amp 2.
23	6	$V_{OUT}2$	Output Signal, Amp 2.
24	7	+V2	Positive Power Supply, Amp 2.
	4	$+V_{IN}2$	Positive Input Signal, Amp 2.
	5	$-V_{IN}2$	Negative Input Signal, Amp 2.
	10	$-V_{IN}1$	Negative Input Signal, Amp 1.
	11	$+V_{IN}1$	Positive Input Signal, Amp 1.
	EP	EPAD	Exposed Pad. The exposed paddle is floating, not electrically connected internally.

TYPICAL PERFORMANCE CHARACTERISTICS

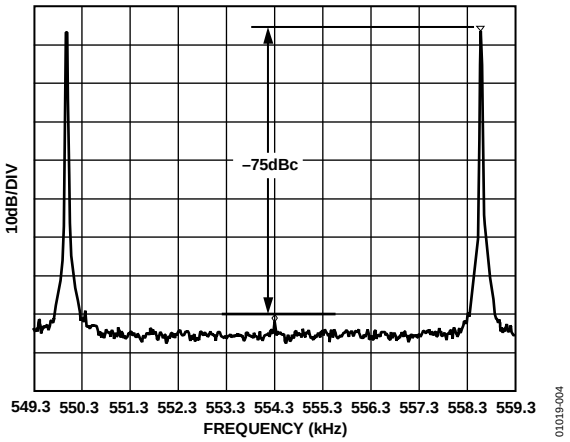

Figure 6. Multitone Power Ratio; V_S = ±12 V, 20.4 dBm Output Power into 100 Ω, Downstream

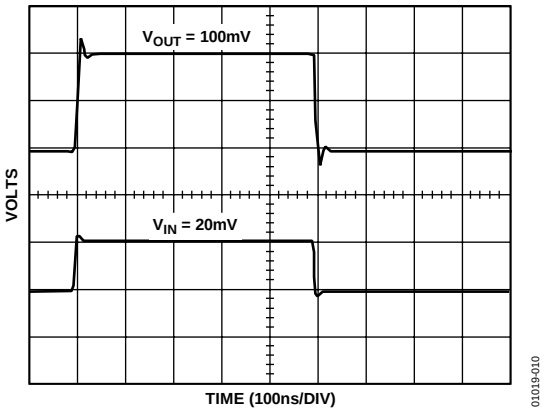

Figure 9. 100 mV Step Response; G = +5, V_S = ±12 V, R_L = 25 Ω, Single-Ended

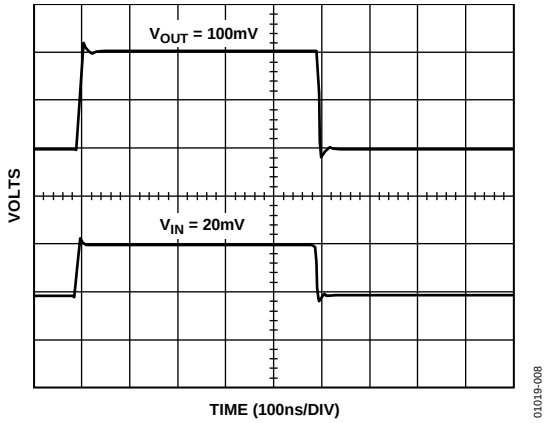

Figure 7. 100 mV Step Response; G = +5, V_S = ±6 V, R_L = 25 Ω, Single-Ended

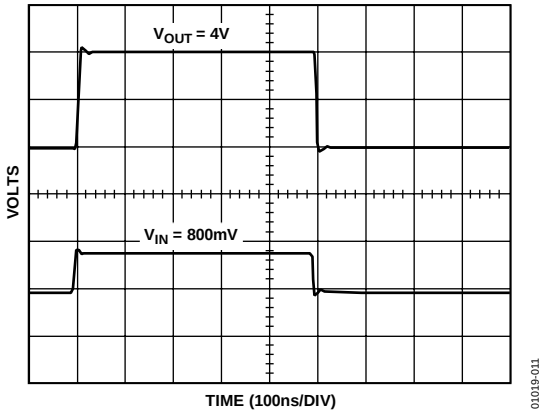

Figure 10. 4 V Step Response; G = +5, V_S = ±12 V, R_L = 25 Ω, Single-Ended

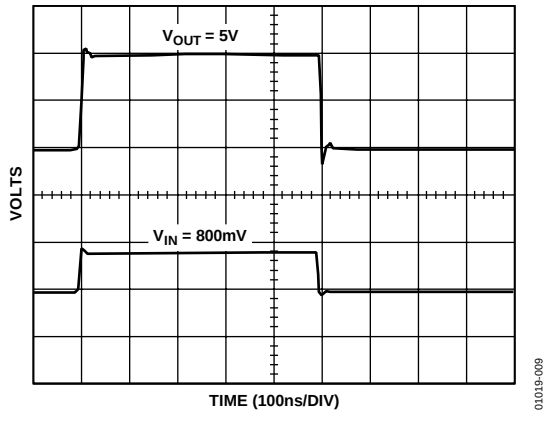

Figure 8. 4 V Step Response; G = +5, V_S = ±6 V, RL = 25 Ω, Single-Ended

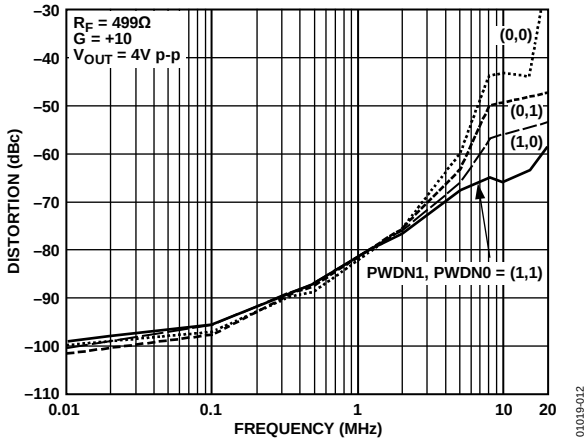

Figure 11. Distortion vs. Frequency; Second Harmonic, V_S = ±12 V, R_L = 50 Ω, Differential

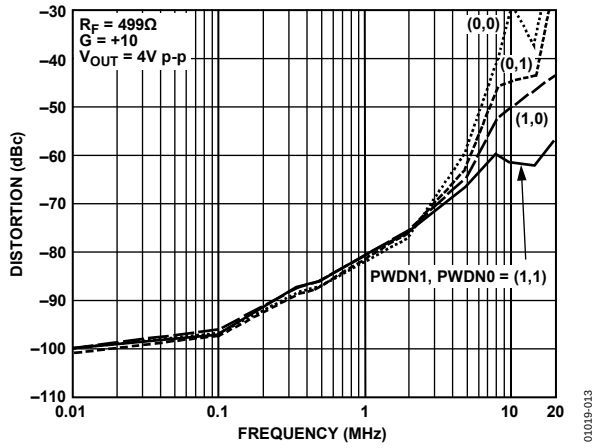

Figure 12. Distortion vs. Frequency; Second Harmonic, V_S = ±6 V, R_L = 50 Ω

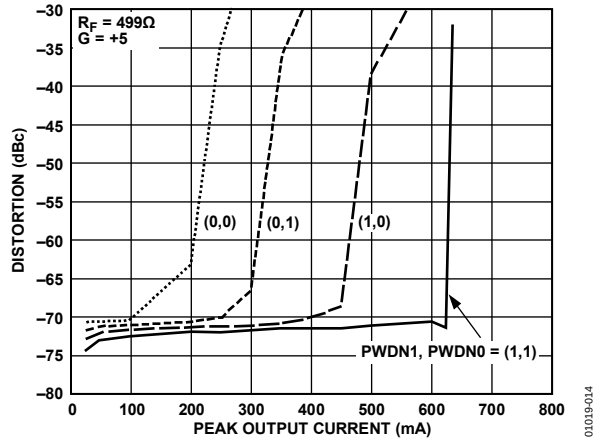

Figure 13. Distortion vs. Peak Output Current; Second Harmonic, V_S = ±12 V, R_L = 10 Ω, f = 100 kHz, Single-Ended

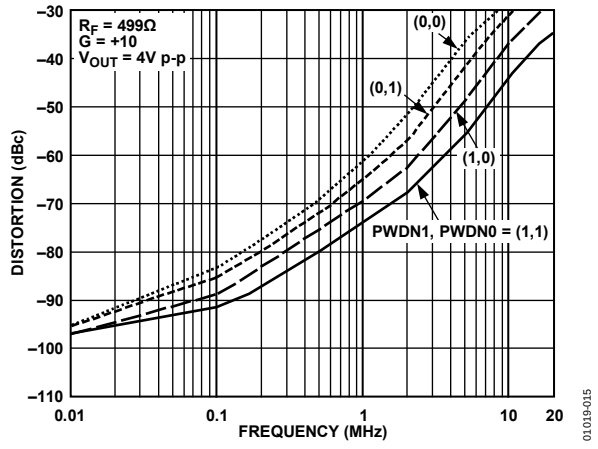

Figure 14. Distortion vs. Frequency; Third Harmonic, V_S = ±12 V, R_L = 50 Ω, Differential

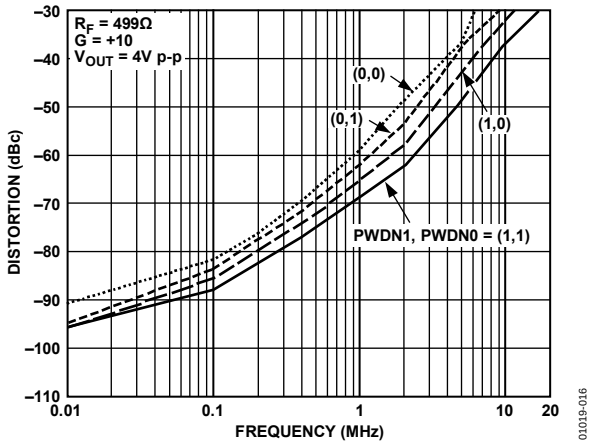

Figure 15. Distortion vs. Frequency; Third Harmonic, V_S = ±6 V, R_L = 50 Ω, Differential

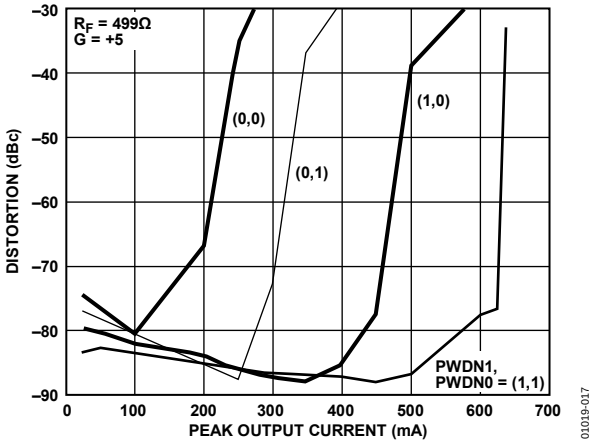

Figure 16. Distortion vs. Peak Output Current, Third Harmonic; V_S = ±12 V, R_L = 10 Ω, G = +5, f = 100 kHz, Single-Ended

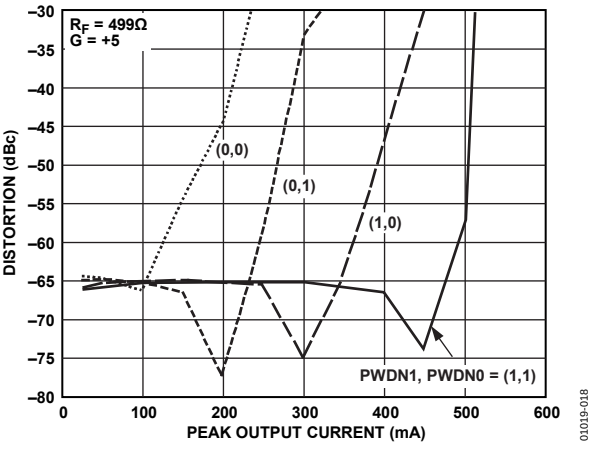

Figure 17. Distortion vs. Peak Output Current; Second Harmonic, V_S = ±6 V, R_L = 5 Ω, f = 100 kHz, Single-Ended

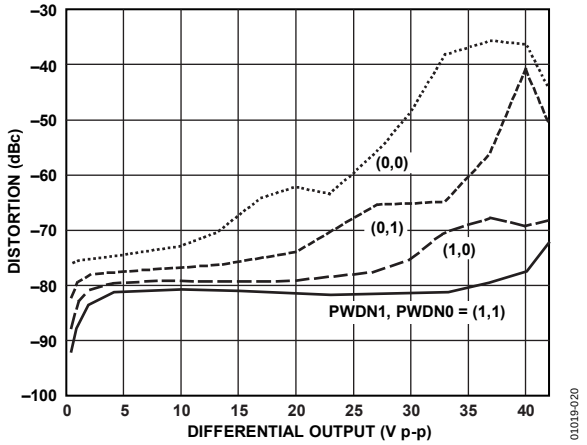

Figure 18. Distortion vs. Output Voltage; Second Harmonic, $V_S = \pm 12$ V, $G = +10$, $f = 1$ MHz, $R_L = 50\ \Omega$, Differential

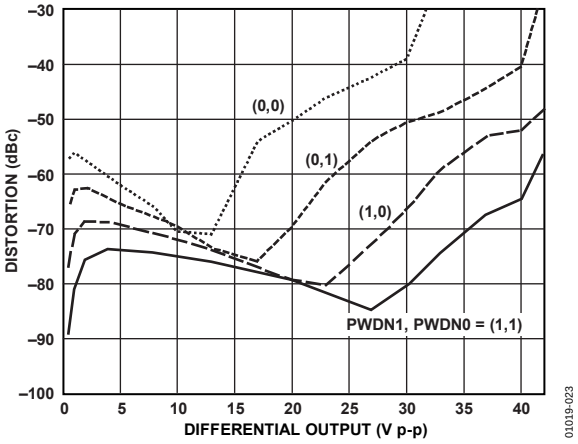

Figure 21. Distortion vs. Output Voltage; Third Harmonic, $V_S = \pm 12$ V, $G = +10$, $f = 1$ MHz, $R_L = 50\ \Omega$, Differential

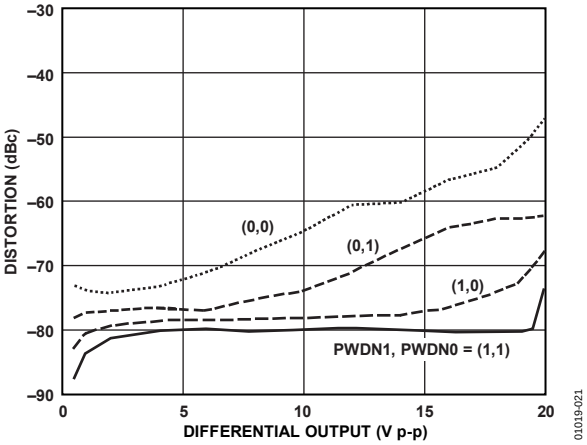

Figure 19. Distortion vs. Output Voltage; Second Harmonic, $V_S = \pm 6$ V, $G = +10$, $f = 1$ MHz, $R_L = 50\ \Omega$, Differential

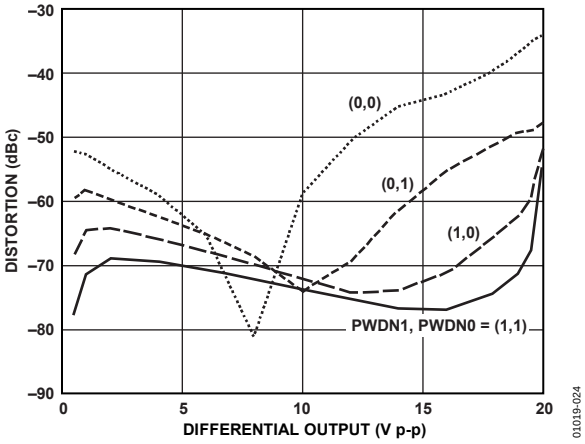

Figure 22. Distortion vs. Output Voltage, Third Harmonic, $V_S = \pm 6$ V, $G = +10$, $f = 1$ MHz, $R_L = 50\ \Omega$, Differential

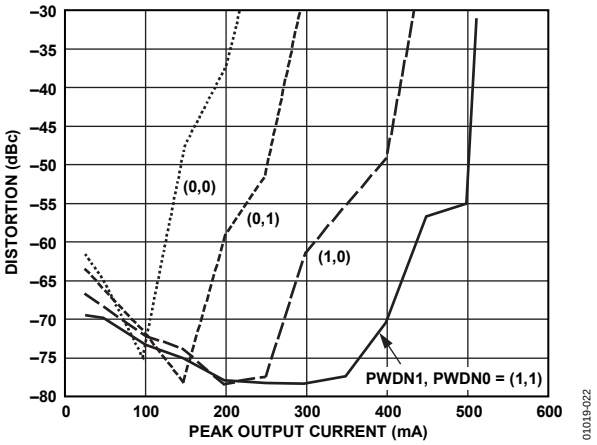

Figure 20. Distortion vs. Peak Output Current; Third Harmonic, $V_S = \pm 6$ V, $G = +5$, $R_L = 5\ \Omega$, $f = 100$ kHz, Single-Ended

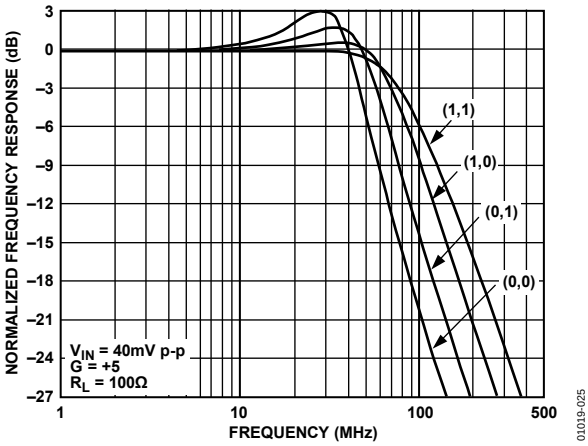

Figure 23. Frequency Response; $V_S = \pm 12$ V, @ PWDN1, PWDN0 Codes

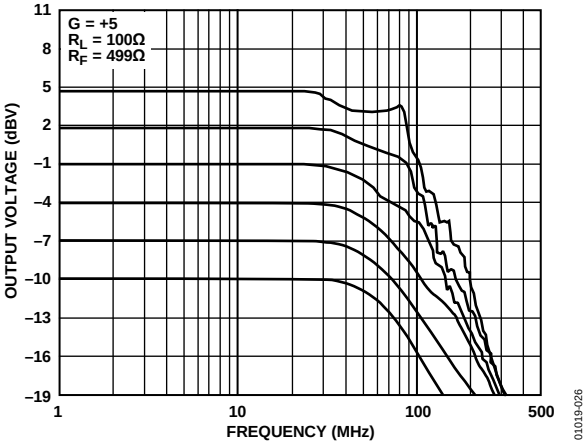

Figure 24. Output Voltage vs. Frequency; V_S = ±12 V

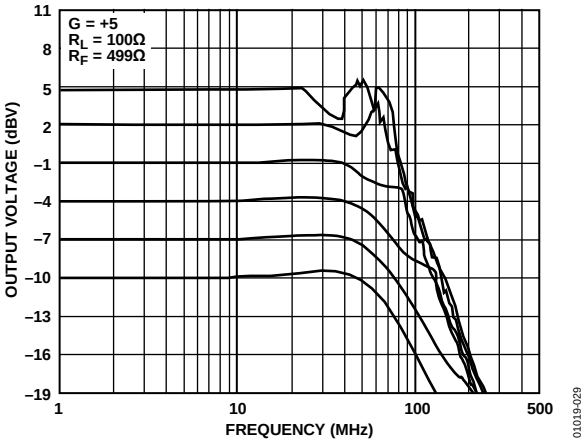

Figure 27. Output Voltage vs. Frequency; V_S = ±6 V

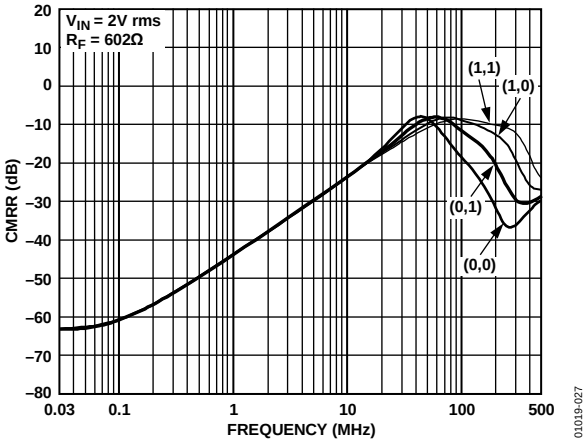

Figure 25. CMRR vs. Frequency; V_S = ±12 V @ PWDN1, PWDN0 Codes

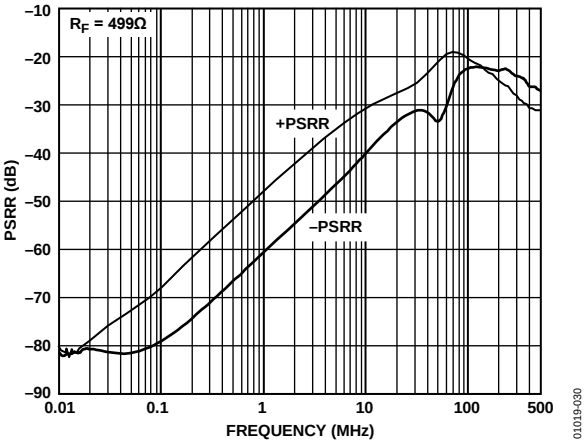

Figure 28. PSRR vs. Frequency; V_S = ±12 V

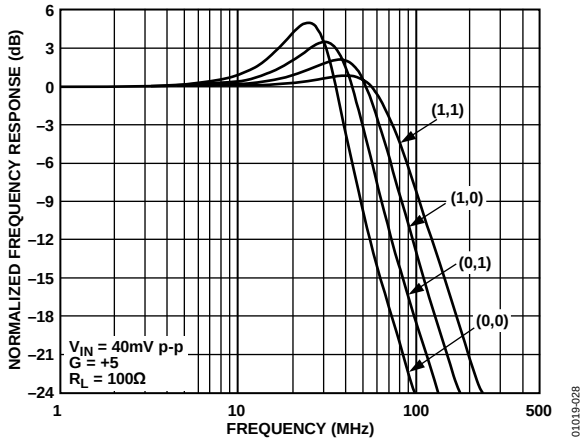

Figure 26. Frequency Response; V_S = ±6 V, @ PWDN1, PWDN0 Codes

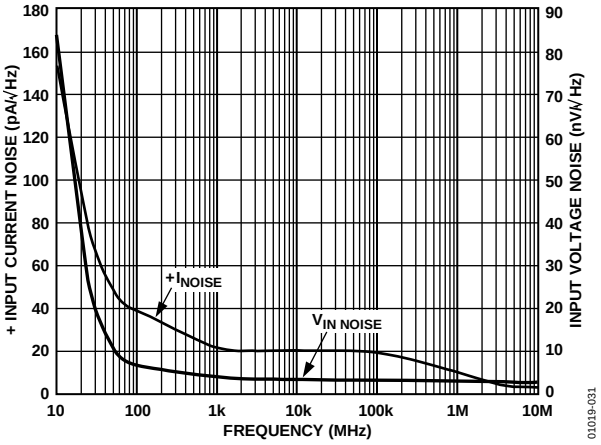

Figure 29. Noise vs. Frequency

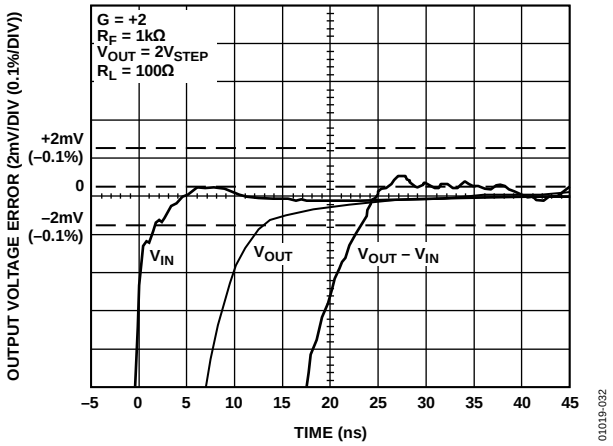

Figure 30. Settling Time 0.1%; V_S = ±12 V

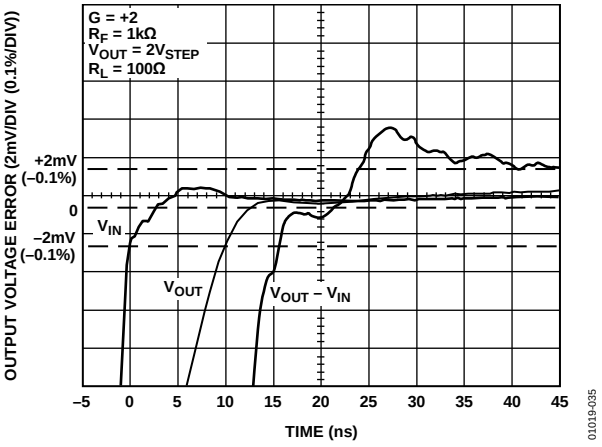

Figure 33. Settling Time 0.1%; V_S = ±6 V

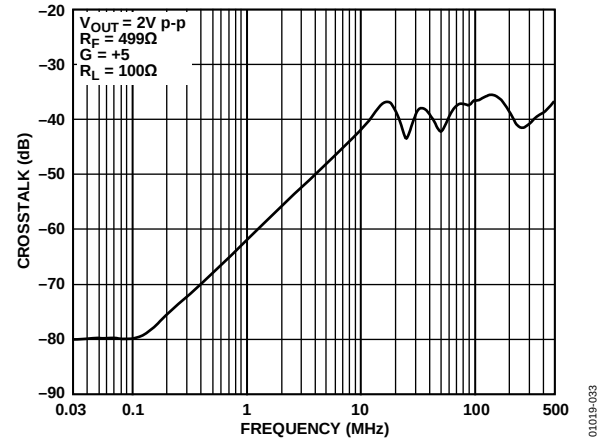

Figure 31. Output Crosstalk vs. Frequency

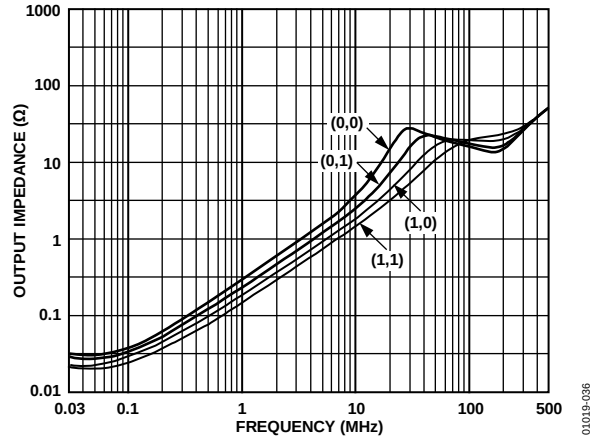

Figure 34. Output Impedance vs. Frequency @ PWDN1, PWDN0 Codes

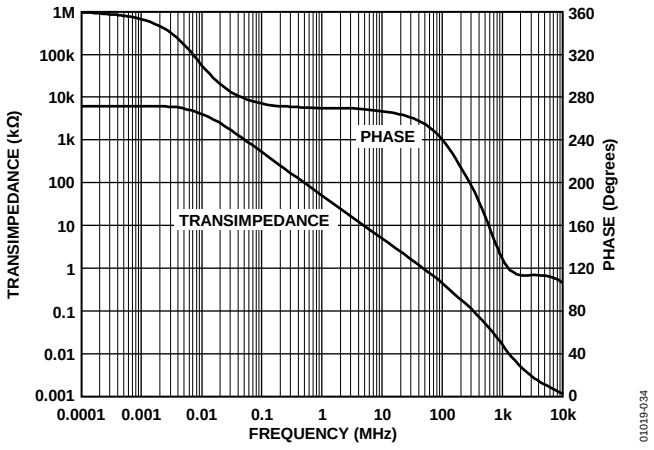

Figure 32. Open-Loop Transimpedance and Phase vs. Frequency

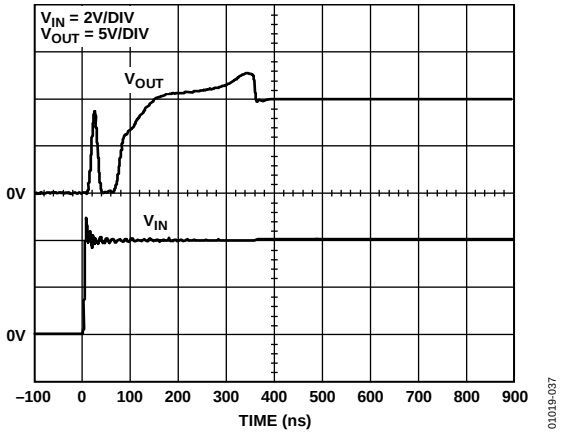

Figure 35. Positive Overdrive Recovery; V_S = ±12 V, G = +5, R_L = 100 Ω

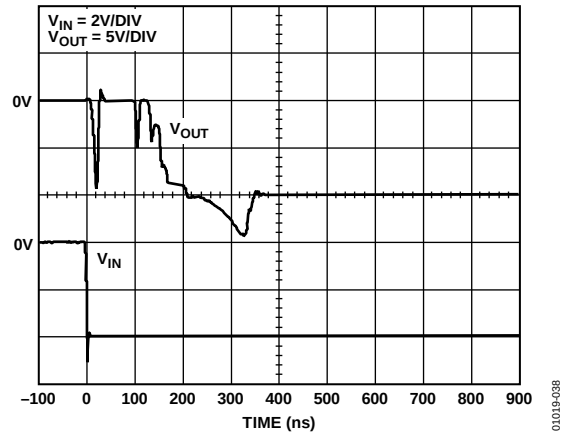

Figure 36. Negative Overdrive Recovery; V_S = ±12 V, G = +5, R_L = 100 Ω

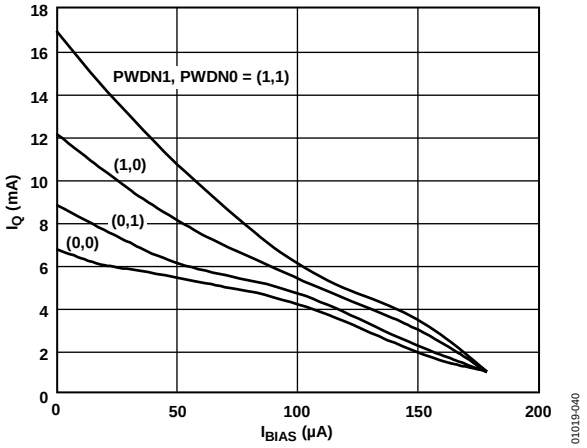

Figure 38. I_Q vs. I_{BIAS} Current; V_S = ±6 V

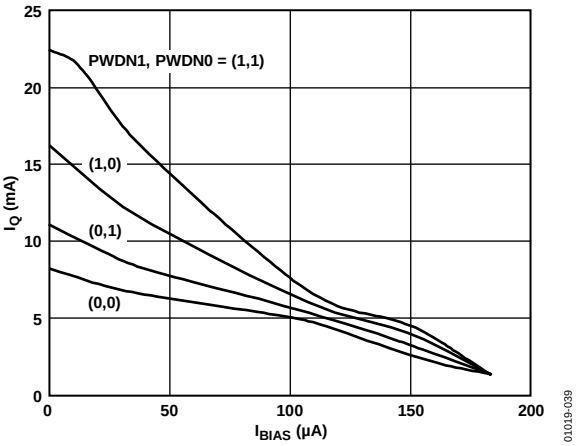

Figure 37. I_Q vs. I_{BIAS} Current; V_S = ±12 V

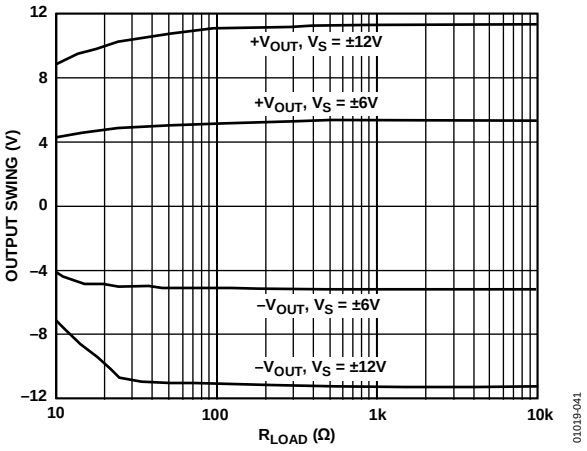

Figure 39. Output Voltage vs. R_{LOAD}

TEST CIRCUTS

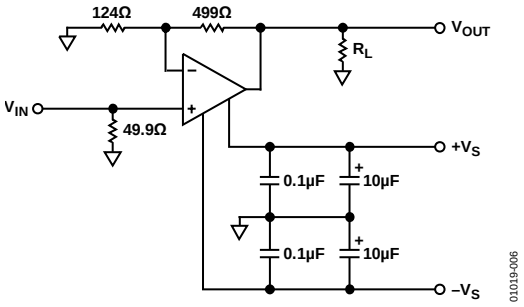

Figure 40. Single-Ended Test Circuit; G = +5

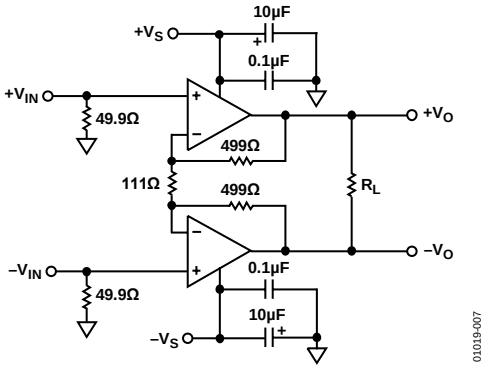

Figure 41. Differential Test Circuit; G = +10

THEORY OF OPERATION

The AD8016 is a current feedback amplifier with high (500 mA) output current capability. With a current feedback amplifier, the current into the inverting input is the feedback signal and the open-loop behavior is that of a transimpedance, dV_{OUT}/dI_{IN} or T_Z. The open-loop transimpedance is analogous to the open-loop voltage gain of a voltage feedback amplifier. Figure 42 shows a simplified model of a current feedback amplifier. Because R_{IN} is proportional to $1/g_m$, the equivalent voltage gain is just $T_Z \times g_m$, where g_m is the transconductance of the input stage. Basic analysis of the follower with gain circuit yields

$$\frac{V_{OUT}}{V_{IN}} = G \times \frac{T_Z(S)}{T_Z(S) + G \times R_{IN} + R_F}$$

where:

$$G = 1 + \frac{R_F}{R_G}$$

$$R_{IN} = \frac{1}{g_m} \approx 25\,\Omega$$

Recognizing that $G \times R_{IN} << R_F$ for low gains, the familiar result of constant bandwidth with gain for current feedback amplifiers is evident, the 3 dB point being set when $|T_Z| = R_F$. Of course, for a real amplifier there are additional poles that contribute excess phase and there is a value for R_F below which the amplifier is unstable. Tolerance for peaking and desired flatness determines the optimum R_F in each application.

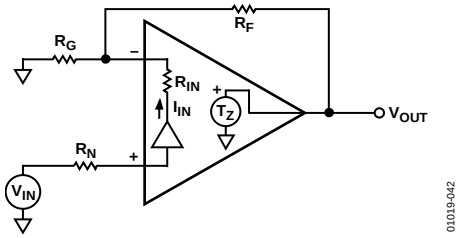

Figure 42. Simplified Block Diagram

The AD8016 is the first current feedback amplifier capable of delivering 400 mA of output current while swinging to within 2 V of either power supply rail. This enables full CO ADSL performance on only 12 V rails, an immediate 20% power saving. The AD8016 is also unique in that it has a power management system included on-chip. It features four user programmable power levels (all of which provide a low output impedance of the driver), as well as the provision for complete shutdown (high impedance state). Also featured is a thermal shutdown with alarm signal.

POWER SUPPLY AND DECOUPLING

The AD8016 should be powered with a good quality (that is, low noise) dual supply of ±12 V for the best distortion and multitone power ratio (MTPR) performance. Careful attention must be paid to decoupling the power supply pins. A 10 µF capacitor located in near proximity to the AD8016 is required to provide good decoupling for lower frequency signals. In addition, 0.1 µF decoupling capacitors should be located as close to each of the four power supply pins as is physically possible. All ground pins should be connected to a common low impedance ground plane.

FEEDBACK RESISTOR SELECTION

In current feedback amplifiers, selection of feedback and gain resistors has an impact on the MTPR performance, bandwidth, and gain flatness. Take care in selecting these resistors so that optimum performance is achieved. Table 6 below shows the recommended resistor values for use in a variety of gain settings. These values are suggested as a good starting point when designing for any application.

Table 6. Resistor Selection Guide

Gain	R_F (Ω)	R_G (Ω)
+1	1000	∞
−1	500	500
+2	650	650
+5	750	187
+10	1000	111

BIAS PIN AND PWDN FEATURES

The AD8016 is designed to cover both central office (CO) and customer premise equipment (CPE) ends of an xDSL application. It offers full versatility in setting quiescent bias levels for the particular application from full on to reduced bias (in three steps) to full off (via BIAS pin). This versatility gives the modem designer the flexibility to maximize efficiency while maintaining reasonable levels of MTPR performance. Optimizing driver efficiency while delivering the required DMT power is accomplished with the AD8016 through the use of on-chip power management features. Two digitally programmable logic pins, PWDN1 and PWDN0, may be used to select four different bias levels: 100%, 60%, 40%, and 25% of full quiescent power (see Table 7).

Table 7. PWDN Code Selection Guide

PWDN1 Code	PWDN0 Code	Quiescent Bias Level
1	1	100% (full on)
1	0	60%
0	1	40%
0	0	25% (low Z_{OUT} but not off)
X	X	Full off (high Z_{OUT} via 250 µA pulled out of BIAS pin)

The bias level can be controlled with TTL logic levels (high = 1) applied to the PWDN1 and PWDN0 pins alone or in combination with the BIAS control pin. The DGND or digital ground pin is the logic ground reference for the PWDN1 and PWDN0 pins. In typical ADSL applications where ±12 V or ±6 V supplies (also single supplies) are used, the DGND pin is connected to analog ground.

The BIAS control pin by itself is a means to continuously adjust the AD8016 internal biasing and, thus, quiescent current I_Q. By pulling out a current of 0 µA (or open) to approximately200 µA, the quiescent current can be adjusted from 100% (full on) to a full off condition. The full off condition yields a high output impedance. Because of an on-chip resistor variation of up to ±20%, the actual amount of current required to fully shut down the AD8016 can vary. To institute a full chip shutdown, a pull-down current of 250 µA is recommended. See Figure 43 for the logic drive circuit for complete amplifier shutdown. Figure 37 and Figure 38 show the relationship between current pulled out of the BIAS pin (I_{BIAS}) and the supply current (I_Q). A typical shutdown I_Q is less than 1 mA total. Alternatively, an external pull-down resistor to ground or a current sink attached to the BIAS pin can be used to set I_Q to lower levels (see Figure 44). The BIAS pin may be used in combination with the PWDN1 and PWDN0 pins; however, diminished MTPR performance may result when I_Q is lowered too much. Current pulled away from the BIAS pin shunts away a portion of the internal bias current. Setting PWDN1 or PWDN0 to Logic 0 also shunts away a portion of the internal bias current. The reduction of quiescent bias levels due to the use of PWDN1 and PWDN0 is consistent with the percentages established in Table 7. When PWDN0 alone is set to Logic 0, and no other means of reducing the internal bias currents is used, full-rate ADSL signals may be driven while maintaining reasonable levels of MTPR.

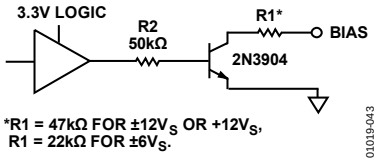

Figure 43. Logic Drive of BIAS Pin for Complete Amplifier Shutdown

THERMAL SHUTDOWN

The AD8016 ARB is designed to incorporate shutdown protection against accidental thermal overload. In the event of thermal overload, the AD8016 was designed to shut down at a junction temperature of 165°C and return to normal operation at a junction temperature 140°C. The AD8016 continues to operate, cycling on and off, as long as the thermal overload condition remains. The frequency of the protection cycle depends on the ambient environment, severity of the thermal overload condition, the power being dissipated, and the thermal mass of the PCB beneath the AD8016. When the AD8016 begins to cycle due to thermal stress, the internal shutdown circuitry draws current out of the node connected in common with the BIAS pin, while the voltage at the BIAS pin goes to the negative rail. When the junction temperature returns to 140°C, current is no longer drawn from this node, and the BIAS pin voltage returns to the positive rail. Under these circumstances, the BIAS pin can be used to trip an alarm indicating the presence of a thermal overload condition.

Figure 44 also shows three circuits for converting this signal to a standard logic level.

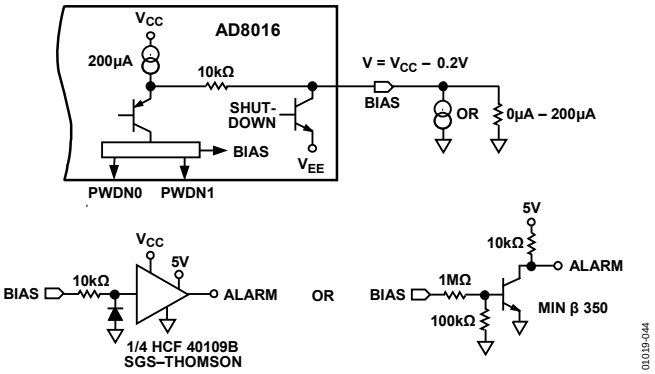

Figure 44. Shutdown and Alarm Circuit

APPLICATIONS INFORMATION

The AD8016 dual amplifier forms an integrated single-channel ADSL line driver. The AD8016 may be applied in driving modulated signals including discrete multitone (DMT) in either direction; upstream from CPE to the CO and downstream from CO to CPE. The most significant thermal management challenge lies in driving downstream information from CO sites to the CPE. Driving xDSL information downstream suggests the need to locate many xDSL modems in a single CO site. The implication is that several modems will be placed onto a single printed circuit board residing in a card cage located in a variety of ambient conditions. Environmental conditioners such as fans or air conditioning may or may not be available, depending on the density of modems and the facilities contained at the CO site. To achieve long-term reliability and consistent modem performance, designers of CO solutions must consider the wide array of ambient conditions that exist within various CO sites.

MULTITONE POWER RATIO (MTPR)

ADSL systems rely on discrete multitone modulation to carry digital data over phone lines. DMT modulation appears in the frequency domain as power contained in several individual frequency subbands, sometimes referred to as tones or bins, each of which is uniformly separated in frequency. (See Figure 6 for an example of downstream DMT signals used in evaluating MTPR performance.) A uniquely encoded, quadrature amplitude modulation (QAM) signal occurs at the center frequency of each subband or tone. Difficulties arise when decoding these subbands if a QAM signal from one subband is corrupted by the QAM signal(s) from other subbands, regardless of whether the corruption comes from an adjacent subband or harmonics of other subbands. Conventional methods of expressing the output signal integrity of line drivers, such as spurious-free dynamic range (SFDR), single-tone harmonic distortion or THD, two-tone intermodulation distortion (IMD), and third-order intercept (IP3) become significantly less meaningful when amplifiers are required to drive DMT and other heavily modulated waveforms. A typical xDSL downstream DMT signal may contain as many as 256 carriers (subbands or tones) of QAM signals. MTPR is the relative difference between the measured power in a typical subband (at one tone or carrier) vs. the power at another subband specifically selected to contain no QAM data. In other words, a selected subband (or tone) remains open or void of intentional power (without a QAM signal), yielding an empty frequency bin. MTPR, sometimes referred to as the empty bin test, is typically expressed in dBc, similar to expressing the relative difference between single-tone fundamentals and second or third harmonic distortion components.

See Figure 6 for a sample of the ADSL downstream spectrum showing MTPR results while driving 20.4 dBm of power onto a 100 Ω line. Measurements of MTPR are typically made at the output (line side) of ADSL hybrid circuits. MTPR can be affected by the components contained in the hybrid circuit, including the quality of the capacitor dielectrics, voltage ratings, and the turns ratio of the selected transformers. Other components aside, an ADSL driver hybrid containing the AD8016 can be optimized for the best MTPR performance by selecting the turns ratio of the transformers. The voltage and current demands from the differential driver changes, depending on the transformer turns ratio. The point on the curve indicating maximum dynamic headroom is achieved when the differential driver delivers both the maximum voltage and current while maintaining the lowest possible distortion. Below this point, the driver has reserve current-driving capability and experiences voltage clipping. Above this point, the amplifier runs out of current drive capability before the maximum voltage drive capability is reached. Because a transformer reflects the secondary load impedance back to the primary side by the square of the turns ratio, varying the turns ratio changes the load across the differential driver. The following equation may be used to calculate the load impedance across the output of the differential driver, reflected by the transformers, from the line side of the xDSL driver hybrid.

$$Z' \equiv \frac{Z_2}{(2 \times N)^2}$$

where:
Z' is the primary side impedance as seen by the differential driver.
Z_2 is the line impedance.
N is the transformer turns ratio.

Figure 45 shows the dynamic headroom in each subband of a downstream DMT waveform vs. turns ratio running at 100% and 60% of the quiescent power while maintaining −65 dBc of MTPR at V_S = ±12 V.

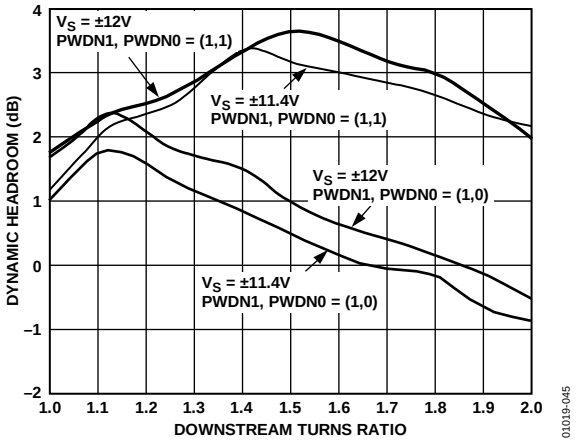

Figure 45. Dynamic Headroom vs. XFMR Turns Ratio, V_S = ±12 V

Once an optimum turns ratio is determined, the amplifier has an MTPR performance for each setting of the power-down pins. Table 8 demonstrates the effects of reducing the total power dissipated by using the PWDN pins on MTPR performance when driving 20.4 dBm downstream onto the line with a transformer turns ratio of 1:1.4.

Table 8. Dynamic Power Dissipation of Downstream Transmission

PWDN1	PWDN0	PD (W)	MTPR
1	1	1.454	−78 dBc
1	0	1.262	−75.3 dBc
0	1	1.142	−57.2 dBc
0[1]	0	0.120	N/A

[1] This mode is quiescent power dissipation.

GENERATING DMT

At this time, DMT modulated waveforms are not typically menu selectable items contained within arbitrary waveform generators. Even using AWG software to generate DMT signals, AWGs that are available today may not deliver DMT signals sufficient in performance with regard to MTPR due to limitations in the DAC and output drivers used by AWG manufacturers. Similar to evaluating single-tone distortion performance of an amplifier, MTPR evaluation requires a DMT signal generator capable of delivering MTPR performance better than that of the driver under evaluation.

POWER DISSIPATION

To properly size the heat sinking area for the user's application, it is important to consider the total power dissipation of the AD8016. The dc power dissipation for V_{IN} = 0 V is I_Q (V_{CC} − V_{EE}), or 2 × I_Q × V_S.

For the AD8016 powered on +12 V and −12 V supplies (±V_S), the number is 0.6 W. In a differential driver circuit (Figure 41), one can use symmetry to simplify the computation for a dc input signal.

$$P_D = 2 \times I_Q \times V_S + 4 \times (V_S - V_{OUT}) \frac{V_{OUT}}{R_L}$$

where:
V_{OUT} is the peak output voltage of an amplifier.

This formula is slightly pessimistic due to the fact that some of the quiescent supply current is commutated during sourcing or sinking current into the load. For a sine wave source, integration over a half cycle yields

$$P_D = 2 \times I_Q \times V_S + 2\left(\frac{4V_{OUT}V_S}{\pi R_L} - \frac{{V_{OUT}}^2}{R_L}\right)$$

The situation is more complicated with a complex modulated signal. In the case of a DMT signal, taking the equivalent sine wave power overestimates the power dissipation by ~23%. For example:

P_{OUT} = 23.4 dBm = 220 mW

V_{OUT} @ 50 Ω = 3.31 V rms

V_{OUT} = 2.354 V

at each amplifier output, which yields a P_D of 1.81 W.

Through measurement, a DMT signal of 23.4 dBm requires 1.47 W of power to be dissipated by the AD8016. Figure 46 shows the results of calculation and actual measurements detailing the relationship between the power dissipated by the AD8016 vs. the total output power delivered to the back termination resistors and the load combined. A 1:2 transformer turns ratio was used in the calculations and measurements.

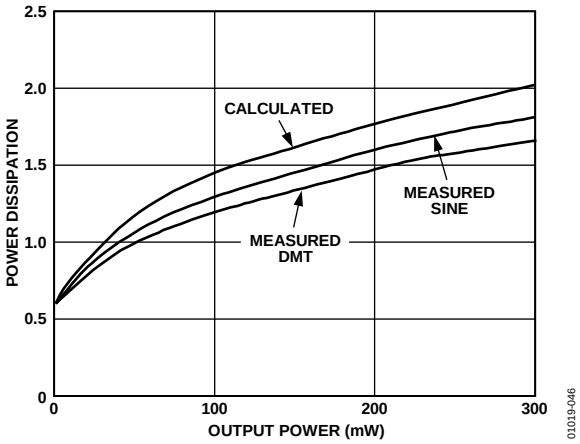

Figure 46. Power Dissipation vs. Output Power (Including Back Terminations), See Figure 9 for Test Circuit

THERMAL ENHANCEMENTS AND PCB LAYOUT

There are several ways to enhance the thermal capacity of the CO solution. Additional thermal capacity can be created using enhanced PCB layout techniques such as interlacing (sometimes referred to as stitching or interconnection) of the layers immediately beneath the line driver. This technique serves to increase the thermal mass or capacity of the PCB immediately beneath the driver. The AD8016 in a TSSOP_EP (ARE model) package can be designed to operate in the CO solution using prudent measures to manage the power dissipation through careful PCB design. The ARE package is available for use in designing the highest density CO solutions. Maximum heat transfer to the PCB can be accomplished using the ARE package when the thermal slug is soldered to an exposed copper pad directly beneath the AD8016. Optimum thermal performance can be achieved in the ARE package only when the back of the package is soldered to a PCB designed for maximum thermal capacity (see Figure 48). Thermal experiments with the ARE package were conducted without soldering the heat slug to the PCB. Heat transfer was through physical contact only. The following offers some insight into the AD8016 power dissipation and relative junction temperature, as well as the effects of PCB size and composition on the junction-to-air thermal resistance or θ_{JA}.

THERMAL TESTING

A wind tunnel study was conducted to determine the relationship between thermal capacity (that is, printed circuit board copper area), air flow, and junction temperature. Junction-to-ambient thermal resistance, θ_{JA}, was also calculated for the AD8016 ARE and AD8016 ARB packages. The AD8016 was operated in a noninverting differential driver configuration, typical of an xDSL application yet isolated from any other modem components. Testing was conducted using a 1 oz. copper board in an ambient temperature of ~24°C over air flows of 200, 150, 100, and 50 linear feet per minute (LFM) (0.200 and 400 for AD8016 ARE) and for the ARB packages as well as in still air. The 4-layer PCB was designed to maximize the area of copper on the outer two layers of the board, while the inner layers were used to configure the AD8016 in a differential driver circuit. The PCB measured 3 inches × 4 inches in the beginning of the study and was progressively reduced in size to approximately 2 inches × 2 inches. The testing was performed in a wind tunnel to control airflow in units of LFM. The tunnel is approximately 11 inches in diameter.

AIR FLOW TEST CONDITIONS

DUT Power

A typical DSL DMT signal produces about 1.5 W of power dissipation in the AD8016 package. The fully biased (PWDN0 and PWDN1 = Logic 1) quiescent current of the AD8016 is ~25 mA. A 1 MHz differential sine wave at an amplitude of 8 V p-p/amplifier into an R_{LOAD} of 100 Ω differential (50 Ω per side) produces the 1.5 W of power typical in the AD8016 device. (See the Power Dissipation section for details.)

Thermal Resistance

The junction-to-case thermal resistance (θ_{JC}) of the AD8016 ARB or SOIC_W_BAT package is 8.6°C/W and for the AD8016 ARE or TSSOP_EP it is 5.6°C/W. These package specifications were used in this study to determine junction temperature based on the measured case temperature.

PCB Dimensions of a Differential Driver Circuit

Several components are required to support the AD8016 in a differential driver circuit. The PCB area necessary for these components (that is, feedback and gain resistors, ac-coupling and decoupling capacitors, termination and load resistors) dictated the area of the smallest PCB in this study, 4.7 square inches. Further reduction in PCB area, although possible, has consequences in terms of the maximum operating junction temperature method of thermal enhancement.) A cooling fan that draws moving air over the PCB and xDSL drivers, while not always required, may be useful in reducing the operating temperature.

EXPERIMENTAL RESULTS

The experimental data suggests that for both packages, and a PCB as small as 4.7 square inches, reasonable junction temperatures can be maintained even in the absence of air flow. The graph in Figure 47 shows junction temperature vs. airflow for various dimensions of 1 oz. copper PCBs at an ambient temperature of 24°C in the ARB package. For the worst-case package, the AD8016 ARB and the worst-case PCB at 4.7 square inches, the extrapolated junction temperature for an ambient environment of 85°C would be approximately 132°C with 0 LFM of airflow. If the target maximum junction temperature of the AD8016 ARB is 125°C, a 4-layer PCB with 1 oz. copper covering the outer layers and measuring 9 square inches is required with 0 LFM of air flow.

Note that the AD8016 ARE is targeted at xDSL applications other than full-rate CO ADSL. The AD8016 ARE is targeted at g.lite and other xDSL applications where reduced power dissipation can be achieved through a reduction in output power. Extreme temperatures associated with full-rate ADSL using the AD8016 ARE should be avoided whenever possible.

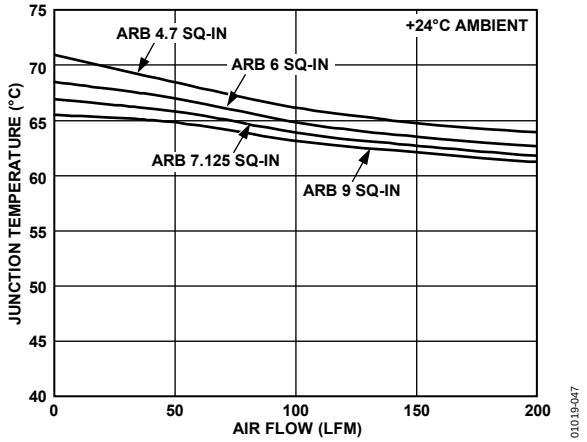

Figure 47. Junction Temperature vs. Air Flow

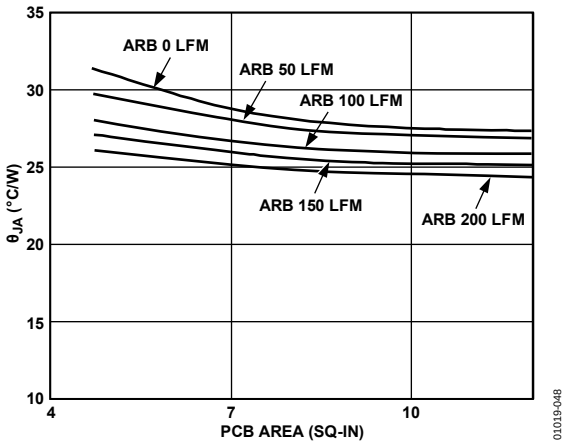

Figure 48. Junction-to-Ambient Thermal Resistance vs. PCB Area

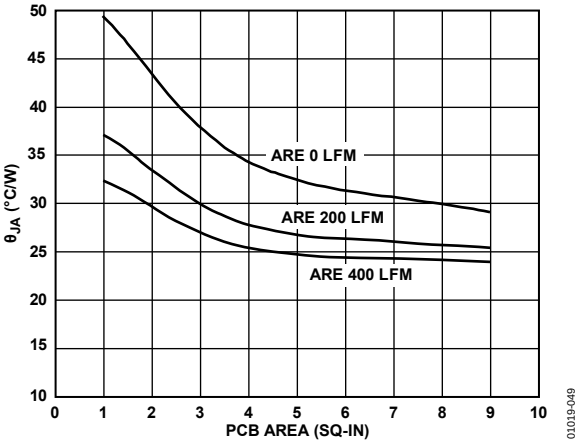

Figure 49. Junction-to-Ambient Thermal Resistance vs. PCB Area

OUTLINE DIMENSIONS

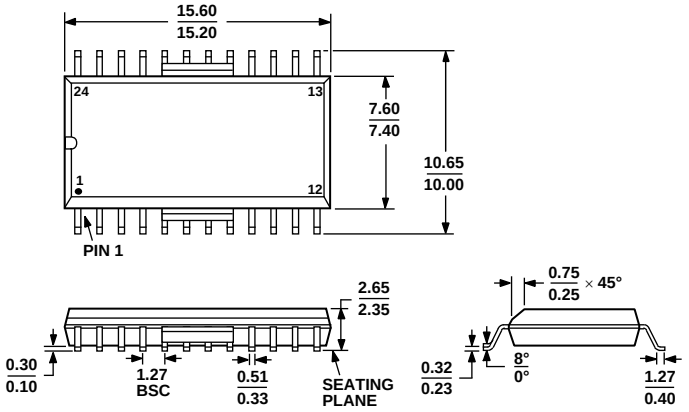

Figure 50. 24-Lead Batwing SOIC, Thermally Enhanced w/Fused Leads [SOIC_W_BAT]
(RB-24)
Dimensions shown in millimeters

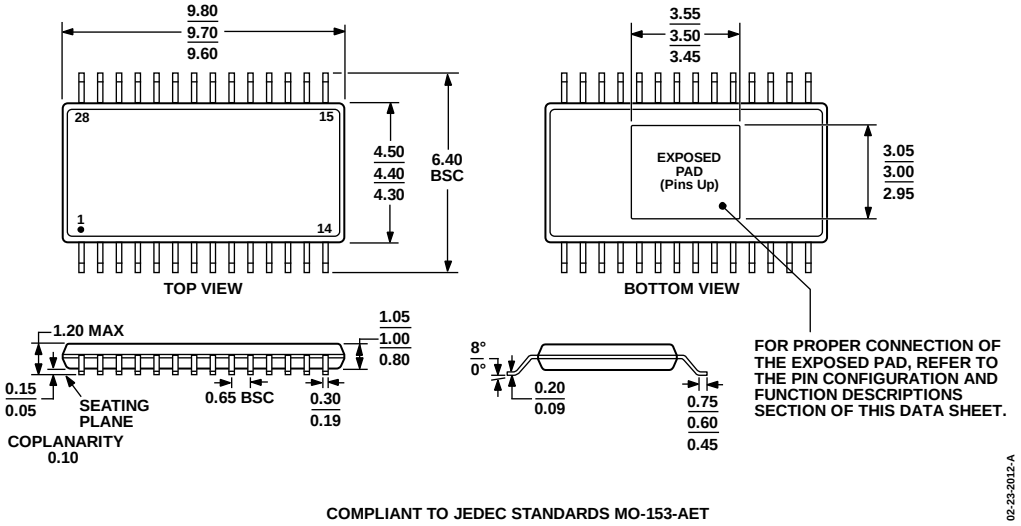

Figure 51. 28-Lead Thin Shrink Small Outline With Exposed Pad [TSSOP_EP]
(RE-28-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8016ARBZ	−40°C to +85°C	24-Lead SOIC_W_BAT	RB-24
AD8016ARBZ-REEL	−40°C to +85°C	24-Lead SOIC_W_BAT	RB-24
AD8016AREZ	−40°C to +85°C	28-Lead TSSOP_EP	RE-28-1
AD8016AREZ-REEL	−40°C to +85°C	28-Lead TSSOP_EP	RE-28-1
AD8016AREZ-REEL7	−40°C to +85°C	28-Lead TSSOP_EP	RE-28-1

[1] Z = RoHS Compliant Part.

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