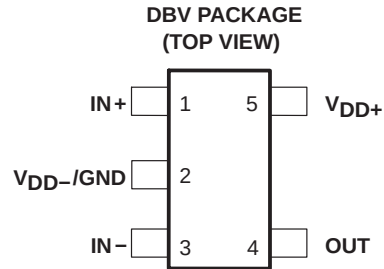




THE DATASHEET OF TLV2221IDBVT

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Single-Supply 3-V and 5-V Operation**
- **Very Low Power . . . 110 μA Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Wide Supply Voltage Range 2.7 V to 10 V**
- **Macromodel Included**



description

The TLV2221 is a single low-voltage operational amplifier available in the SOT-23 package. It offers a compromise between the ac performance and output drive of the TLV2231 and the micropower TLV2211.

It consumes only 150 μA (max) of supply current and is ideal for battery-powered applications. The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLV2221 is fully characterized at 3 V and 5 V and is optimized for low-voltage applications.

The TLV2221, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs).

With a total area of 5.6mm², the SOT-23 package only requires one third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pick-up from long PCB traces. TI has also taken special care to provide a pinout that is optimized for board layout (see Figure 1). Both inputs are separated by GND to prevent coupling or leakage paths. The OUT and IN– terminals are on the same end of the board to provide negative feedback. Finally, gain setting resistors and decoupling capacitor are easily placed around the package.

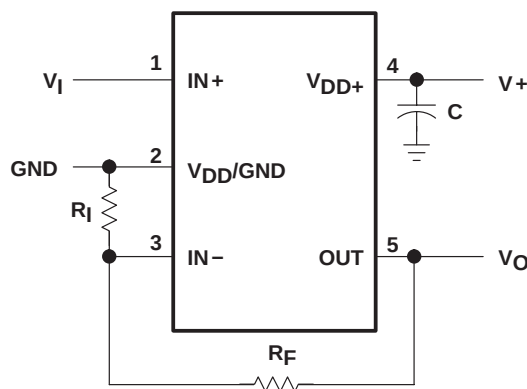


Figure 1. Typical Surface Mount Layout for a Fixed-Gain Noninverting Amplifier



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TLV2221, TLV2221Y

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

SLOS157B – JUNE1996 – REVISED APRIL 2005

AVAILABLE OPTIONS

T_A	V_{IOmax} AT 25°C	PACKAGED DEVICES	SYMBOL	CHIP FORM [‡] (Y)
		SOT-23 (DBV) [†]		
0°C to 70°C	3 mV	TLV2221CDBV	VADC	TLV2221Y
–40°C to 85°C	3 mV	TLV2221IDBV	VADI	

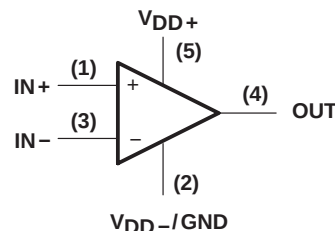
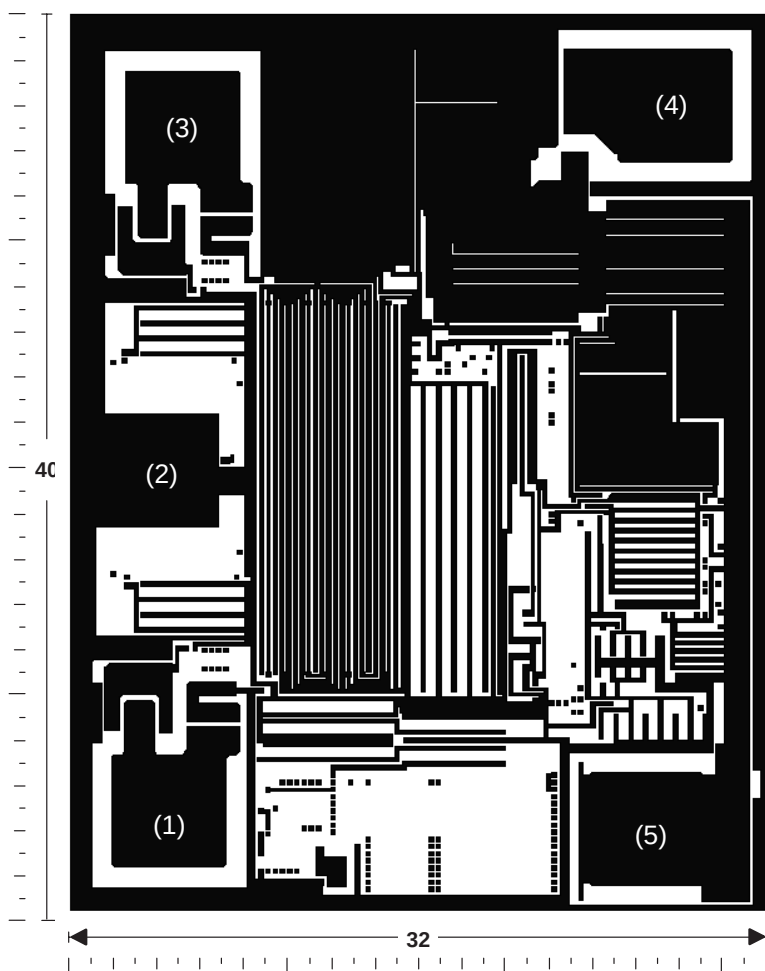
[†] The DBV package available in tape and reel only.

[‡] Chip forms are tested at $T_A = 25^\circ\text{C}$ only.

TLV2221Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2221C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4×4 MILS MINIMUM

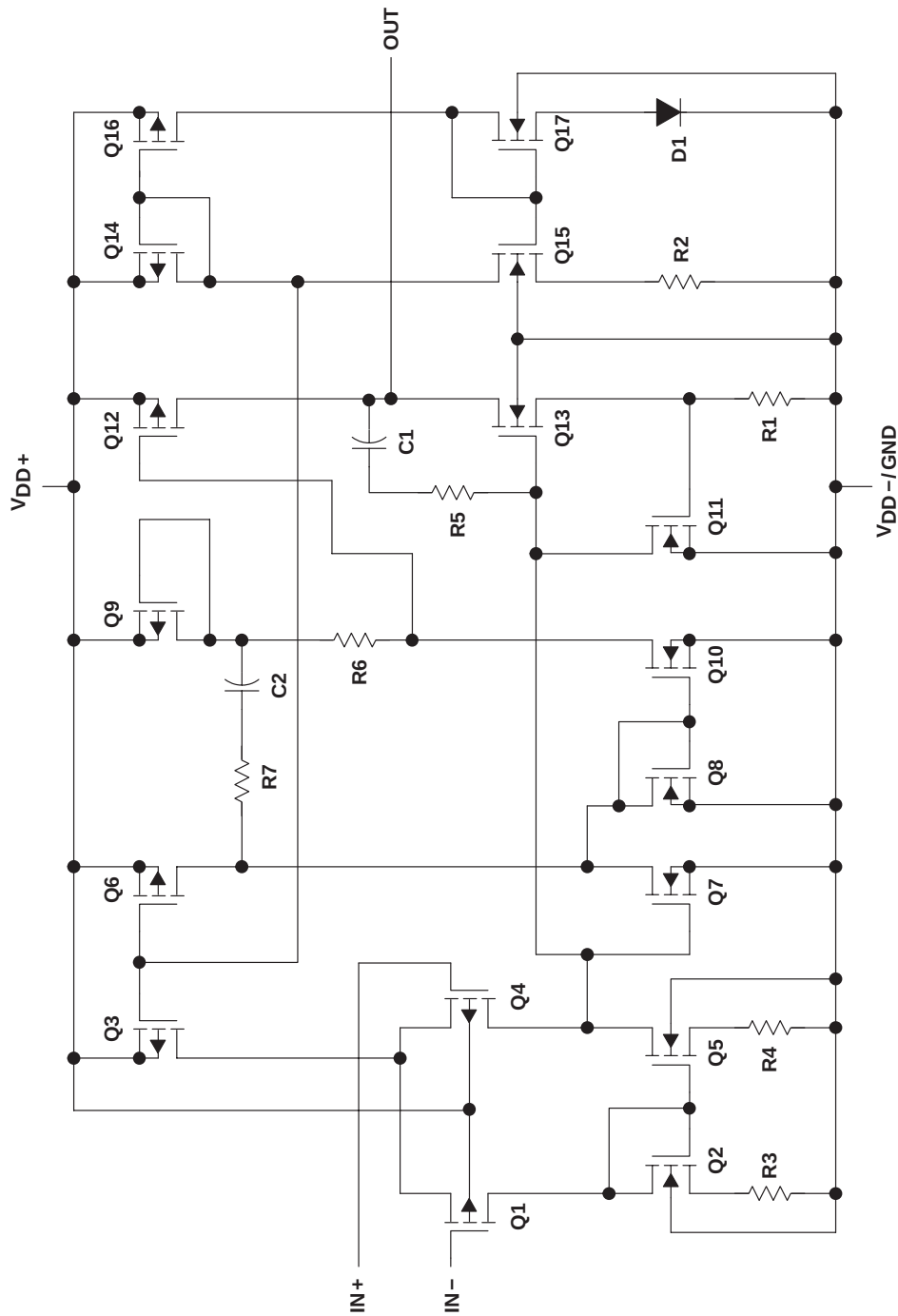
$T_{jmax} = 150^\circ\text{C}$

TOLERANCES ARE $\pm 10\%$.

ALL DIMENSIONS ARE IN MILS.

PIN (2) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic



COMPONENT COUNT†	
Transistors	23
Diodes	5
Resistors	11
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

TLV2221, TLV2221Y

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

SLOS157B – JUNE 1996 – REVISED APRIL 2005

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	12 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1)	-0.3 V to V_{DD}
Input current, I_I (each input)	± 5 mA
Output current, I_O	± 50 mA
Total current into V_{DD+}	± 50 mA
Total current out of V_{DD-}	± 50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : TLV2221C	0°C to 70°C
TLV2221I	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV package	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-} .
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD-} - 0.3$ V.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DBV	150 mW	1.2 mW/°C	96 mW	78 mW

recommended operating conditions

	TLV2221C		TLV2221I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD} (see Note 1)	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	0	70	-40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-} .

TLV2221, TLV2221Y
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS
SLOS157B – JUNE 1996 – REVISED APRIL 2005

electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2221C			TLV2221I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD} ± = ±1.5 V, V _{IC} = 0, V _O = 0, R _S = 50 Ω		Full range	0.62		3	0.62		3	mV
α _{VIO}	Temperature coefficient of input offset voltage				1		1		μV/°C		
	Input offset voltage long-term drift (see Note 4)			25°C	0.003		0.003		μV/mo		
I _{IO}	Input offset current			25°C	0.5		0.5		pA		
				Full range	150		150				
I _{IB}	Input bias current			25°C	1		1		pA		
		Full range	150		150						
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤5 mV		25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2	V	
				Full range	0 to 1.7		0 to 1.7				
V _{OH}	High-level output voltage	I _{OH} = −100 μA		25°C	2.97		2.97		V		
		I _{OH} = −400 μA		25°C	2.88		2.88				
				Full range	2.5		2.5				
V _{OL}	Low-level output voltage	V _{IC} = 1.5 V, I _{OL} = 50 μA		25°C	15		15		mV		
		V _{IC} = 1.5 V, I _{OL} = 500 μA		25°C	150		150				
				Full range	500		500				
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 1.5 V, V _O = 1 V to 2 V	R _L = 2 kΩ‡	25°C	2	3	2	3	V/mV		
				Full range	1		1				
			R _L = 1 MΩ‡	25°C	250		250				
r _{id}	Differential input resistance			25°C	10 ¹²		10 ¹²		Ω		
r _{ic}	Common-mode input resistance			25°C	10 ¹²		10 ¹²		Ω		
c _{ic}	Common-mode input capacitance	f = 10 kHz		25°C	6		6		pF		
z _O	Closed-loop output impedance	f = 10 kHz, A _V = 10		25°C	90		90		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 1.7 V, V _O = 1.5 V, R _S = 50 Ω		25°C	70	82	70	82	dB		
				Full range	65		65				
k _{SVR}	Supply voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 2.7 V to 8 V, V _{IC} = V _{DD} /2, No load		25°C	80	95	80	95	dB		
				Full range	80		80				
I _{DD}	Supply current	V _O = 1.5 V, No load		25°C	100	150	100	150	μA		
				Full range	200		200				

† Full range for the TLV2221C is 0°C to 70°C. Full range for the TLV2221I is -40°C to 85°C.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2221, TLV2221Y

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

SLOS157B – JUNE 1996 – REVISED APRIL 2005

operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER		TEST CONDITIONS	T_A †	TLV2221C			TLV2221I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.1\text{ V to }1.9\text{ V}, R_L = 2\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C	0.1	0.18		0.1	0.18		V/ μs
			Full range	0.05			0.05			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		120			120		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	25°C		20			20		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		680			680		nV
		$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		860			860		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD+N	Total harmonic distortion plus noise	$V_O = 1\text{ V to }2\text{ V}, f = 20\text{ kHz}, R_L = 2\text{ k}\Omega^\ddagger$	25°C		$A_V = 1$			2.52%		
					$A_V = 10$			7.01%		
		$V_O = 1\text{ V to }2\text{ V}, f = 20\text{ kHz}, R_L = 2\text{ k}\Omega^\S$	25°C		$A_V = 1$			0.076%		
					$A_V = 10$			0.147%		
	Gain-bandwidth product	$f = 1\text{ kHz}, R_L = 2\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C		480			480		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}, R_L = 2\text{ k}\Omega^\ddagger, A_V = 1, C_L = 100\text{ pF}^\ddagger$	25°C		30			30		kHz
t_s	Settling time	$A_V = -1, \text{Step} = 1\text{ V to }2\text{ V}, R_L = 2\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C		To 0.1%			4.5		μs
			25°C		To 0.01%			6.8		μs
ϕ_m	Phase margin at unity gain	$R_L = 2\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C		51°			51°		
	Gain margin		25°C		12			12		dB

† Full range is -40°C to 85°C .

‡ Referenced to 1.5 V

§ Referenced to 0 V

TLV2221, TLV2221Y
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS
SLOS157B – JUNE 1996 – REVISED APRIL 2005

electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2221C			TLV2221I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD±} = ±2.5 V, V _{IC} = 0, V _O = 0, R _S = 50 Ω		Full range	0.61 3			0.61 3			mV
α _{VIO}	Temperature coefficient of input offset voltage				1			1			μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.003			0.003			μV/mo
I _{IO}	Input offset current			25°C	0.5			0.5			pA
				Full range	150			150			
I _{IB}	Input bias current			25°C	1			1			pA
		Full range	150			150					
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤ 5 mV		25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2	V	
				Full range	0 to 3.5			0 to 3.5			
V _{OH}	High-level output voltage	I _{OH} = −500 μA I _{OH} = −1 mA		25°C	4.75	4.88		4.75	4.88	V	
					4.5	4.76		4.5	4.76		
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 50 μA		25°C	12			12			mV
		V _{IC} = 2.5 V, I _{OL} = 500 μA		25°C	120			120			
				Full range	500			500			
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V	R _L = 2 kΩ‡	25°C	3	5		3	5	V/mV	
				Full range	1			1			
			R _L = 1 MΩ‡	25°C	800			800			
r _{id}	Differential input resistance			25°C	10 ¹²			10 ¹²			Ω
r _{ic}	Common-mode input resistance			25°C	10 ¹²			10 ¹²			Ω
c _{ic}	Common-mode input capacitance	f = 10 kHz		25°C	6			6			pF
z _o	Closed-loop output impedance	f = 10 kHz, A _V = 10		25°C	70			70			Ω
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 2.7 V, V _O = 1.5 V, R _S = 50 Ω		25°C	70	85		70	85	dB	
				Full range	65			65			
k _{SVR}	Supply voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 4.4 V to 8 V, V _{IC} = V _{DD} /2, No load		25°C	80	95		80	95	dB	
				Full range	80			80			
I _{DD}	Supply current	V _O = 2.5 V, No load		25°C	110 150			110 150			μA
				Full range	200			200			

† Full range for the TLV2221C is 0°C to 70°C. Full range for the TLV2221I is -40°C to 85°C.

‡ Referenced to 2.5 V

NOTE 5: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2221, TLV2221Y

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

SLOS157B – JUNE 1996 – REVISED APRIL 2005

operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2221C			TLV2221I			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew rate at unity gain	V _O = 1.5 V to 3.5 V, R _L = 2 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.1	0.18		0.1	0.18		V/μs	
				Full range	0.05			0.05				
V _n	Equivalent input noise voltage	f = 10 Hz f = 1 kHz		25°C	90			90			nV/√Hz	
				25°C	19			19				
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz f = 0.1 Hz to 10 Hz		25°C	800			800			nV	
				25°C	960			960				
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz	
THD+N	Total harmonic distortion plus noise	V _O = 1.5 V to 3.5 V, f = 20 kHz, R _L = 2 kΩ [‡]	A _V = 1	25°C	2.45%			2.45%				
			A _V = 10		5.54%			5.54%				
		V _O = 1.5 V to 3.5 V, f = 20 kHz, R _L = 2 kΩ [§]	A _V = 1	25°C	0.142%			0.142%				
			A _V = 10		0.257%			0.257%				
	Gain-bandwidth product	f = 1 kHz, R _L = 2 kΩ [‡] , C _L = 100 pF [‡]		25°C	510			510			kHz	
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 1 V, R _L = 2 kΩ [‡]		A _V = 1, C _L = 100 pF [‡]	25°C	40			40			kHz
t _s	Settling time	A _V = -1, Step = 1.5 V to 3.5 V, R _L = 2 kΩ [‡] , C _L = 100 pF [‡]	To 0.1%	25°C	6.8			6.8			μs	
			To 0.01%	25°C	9.2			9.2				
φ _m	Phase margin at unity gain	R _L = 2 kΩ [‡] , C _L = 100 pF [‡]		25°C	52°			52°				
	Gain margin			25°C	12			12			dB	

† Full range is –40°C to 85°C.

‡ Referenced to 2.5 V

§ Referenced to 0 V

electrical characteristics at $V_{DD} = 3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLV2221Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} = \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$		620		μV
I_{IO} Input offset current			0.5		pA
I_{IB} Input bias current			1		pA
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$		-0.3 to 2.2		V
V_{OH} High-level output voltage	$I_{OH} = -100\ \mu\text{A}$		2.97		V
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$		15		mV
	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$		150		
A_{VD} Large-signal differential voltage amplification	$V_O = 1\text{ V to } 2\text{ V}$	$R_L = 2\text{ k}\Omega^\dagger$	3		V/mV
		$R_L = 1\text{ M}\Omega^\dagger$	250		
r_{id} Differential input resistance			10^{12}		Ω
r_{ic} Common-mode input resistance			10^{12}		Ω
c_{ic} Common-mode input capacitance	$f = 10\text{ kHz}$		6		pF
z_o Closed-loop output impedance	$f = 10\text{ kHz}$, $A_V = 10$		90		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 1.7\text{ V}$, $V_O = 0$, $R_S = 50\ \Omega$		82		dB
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to } 8\text{ V}$, $V_{IC} = 0$, No load		95		dB
I_{DD} Supply current	$V_O = 0$, No load		100		μA

† Referenced to 1.5 V

electrical characteristics at $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLV2221Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} = \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$		610		μV
I_{IO} Input offset current			0.5		pA
I_{IB} Input bias current			1		pA
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$		-0.3 to 4.2		V
V_{OH} High-level output voltage	$I_{OH} = -500\ \mu\text{A}$		4.88		V
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$		12		mV
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$		120		
A_{VD} Large-signal differential voltage amplification	$V_O = 1\text{ V to } 4\text{ V}$	$R_L = 2\text{ k}\Omega^\dagger$	5		V/mV
		$R_L = 1\text{ M}\Omega^\dagger$	800		
r_{id} Differential input resistance			10^{12}		Ω
r_{ic} Common-mode input resistance			10^{12}		Ω
c_{ic} Common-mode input capacitance	$f = 10\text{ kHz}$		6		pF
z_o Closed-loop output impedance	$f = 10\text{ kHz}$, $A_V = 10$		70		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 1.7\text{ V}$, $V_O = 0$, $R_S = 50\ \Omega$		85		dB
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to } 8\text{ V}$, $V_{IC} = 0$, No load		95		dB
I_{DD} Supply current	$V_O = 0$, No load		110		μA

† Referenced to 2.5 V

TLV2221, TLV2221Y
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

SLOS157B – JUNE 1996 – REVISED APRIL 2005

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode input voltage	2, 3 4, 5
α_{VIO}	Input offset voltage temperature coefficient	Distribution	6, 7
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	8
V_I	Input voltage	vs Supply voltage vs Free-air temperature	9 10
V_{OH}	High-level output voltage	vs High-level output current	11, 14
V_{OL}	Low-level output voltage	vs Low-level output current	12, 13, 15
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	16
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	17 18
V_O	Output voltage	vs Differential input voltage	19, 20
A_{VD}	Differential voltage amplification	vs Load resistance	21
A_{VD}	Large signal differential voltage amplification	vs Frequency vs Free-air temperature	22, 23 24, 25
z_o	Output impedance	vs Frequency	26, 27
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	28 29
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	30, 31 32
I_{DD}	Supply current	vs Supply voltage	33
SR	Slew rate	vs Load capacitance vs Free-air temperature	34 35
V_O	Inverting large-signal pulse response	vs Time	36, 37
V_O	Voltage-follower large-signal pulse response	vs Time	38, 39
V_O	Inverting small-signal pulse response	vs Time	40, 41
V_O	Voltage-follower small-signal pulse response	vs Time	42, 43
V_n	Equivalent input noise voltage	vs Frequency	44, 45
	Input noise voltage (referred to input)	Over a 10-second period	46
THD + N	Total harmonic distortion plus noise	vs Frequency	47
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	48 49
ϕ_m	Phase margin	vs Frequency vs Load capacitance	22, 23 52, 53
	Gain margin	vs Load capacitance	50, 51
B_1	Unity-gain bandwidth	vs Load capacitance	54, 55

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2211
INPUT OFFSET VOLTAGE**

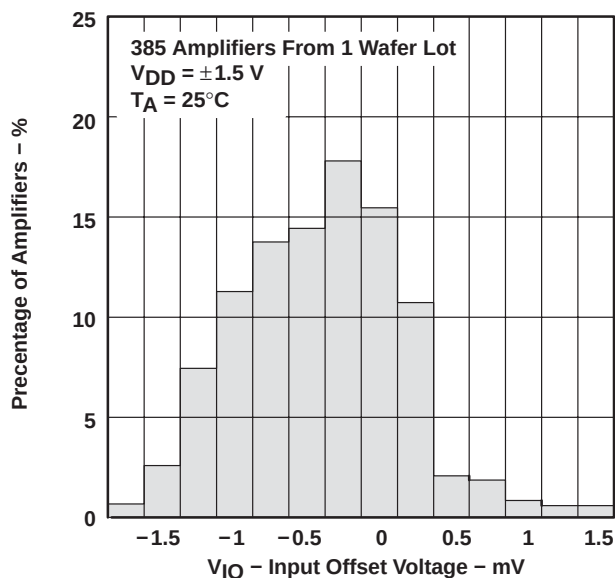


Figure 2

**DISTRIBUTION OF TLV2211
INPUT OFFSET VOLTAGE**

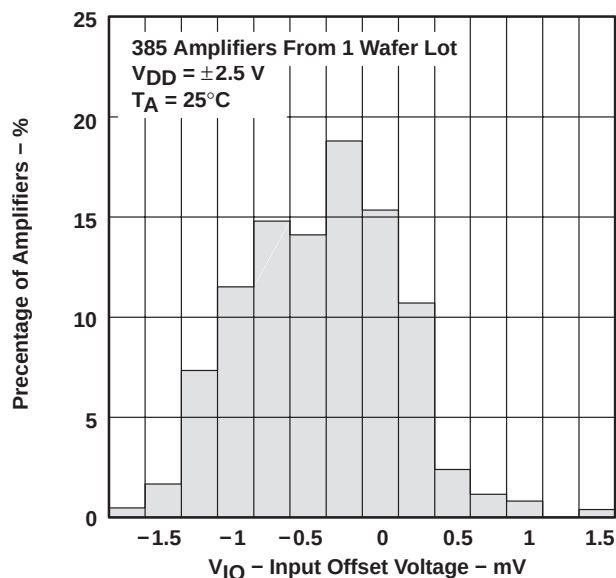


Figure 3

**INPUT OFFSET VOLTAGE[†]
vs
COMMON-MODE INPUT VOLTAGE**

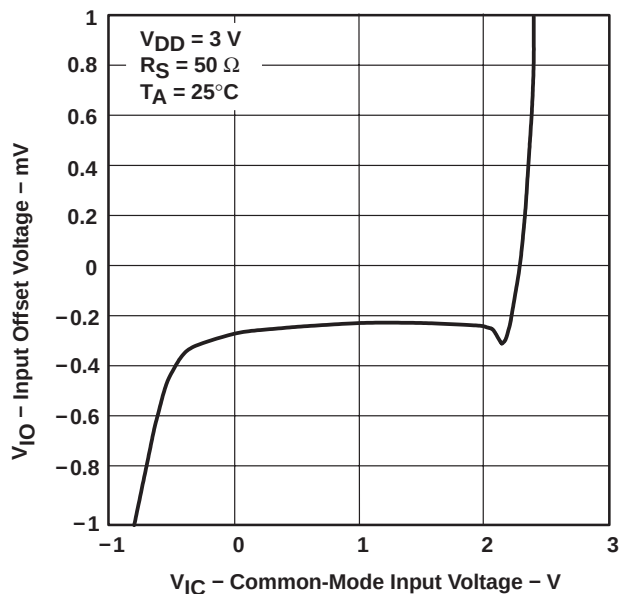


Figure 4

**INPUT OFFSET VOLTAGE[†]
vs
COMMON-MODE INPUT VOLTAGE**

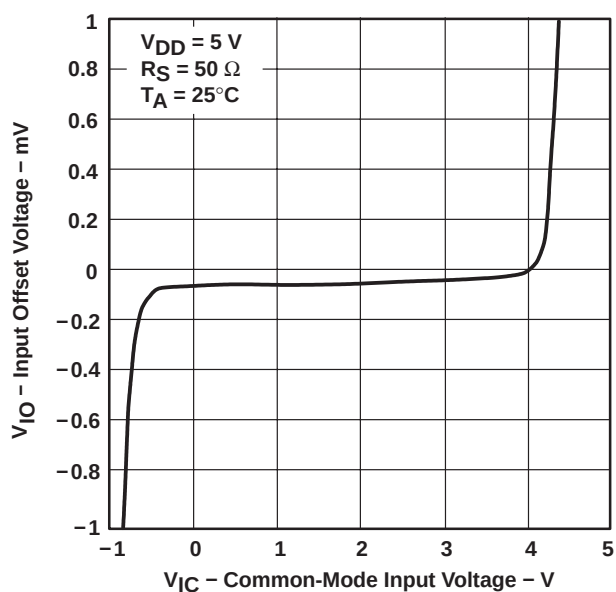


Figure 5

[†] For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.

TLV2221, TLV2221Y

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

SLOS157B – JUNE 1996 – REVISED APRIL 2005

TYPICAL CHARACTERISTICS

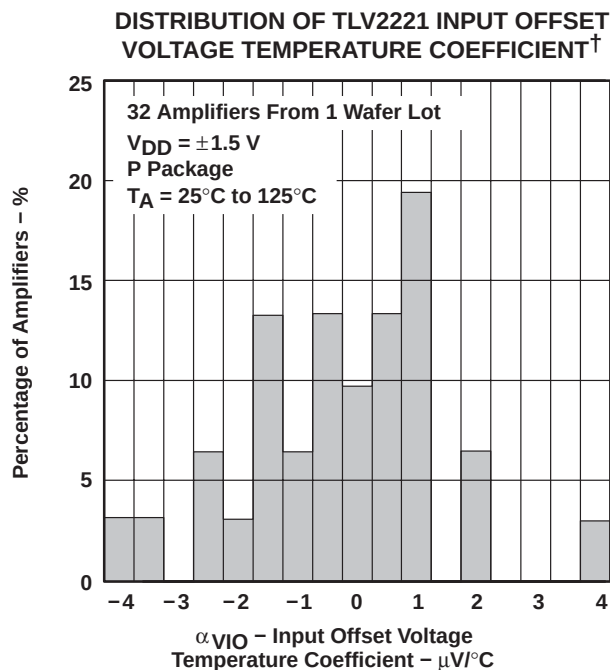


Figure 6

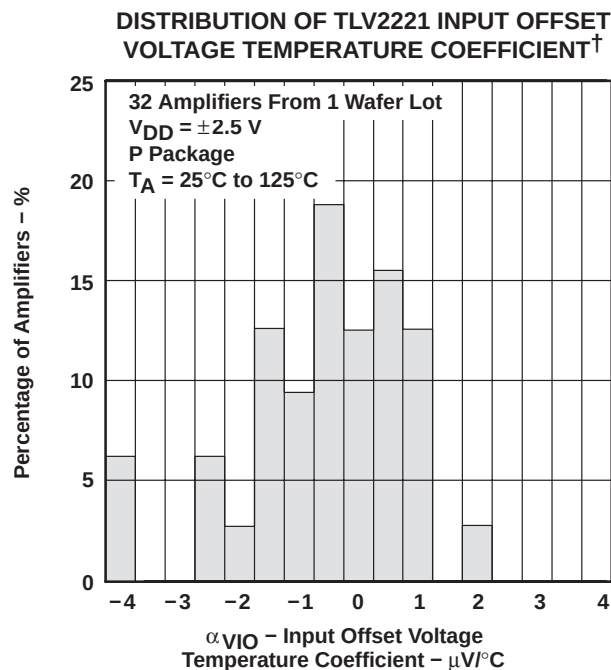


Figure 7

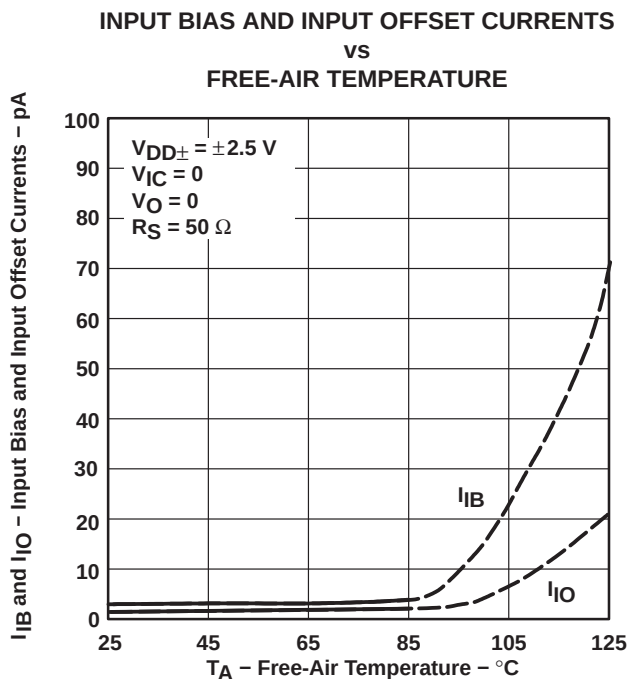


Figure 8

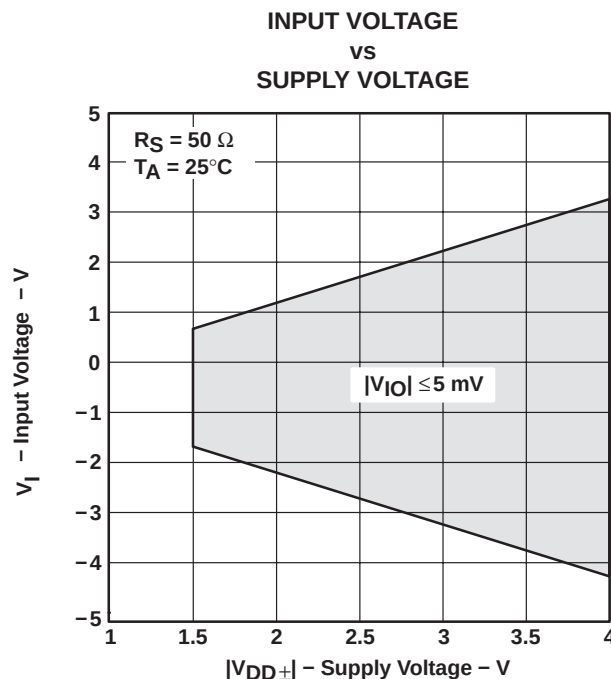
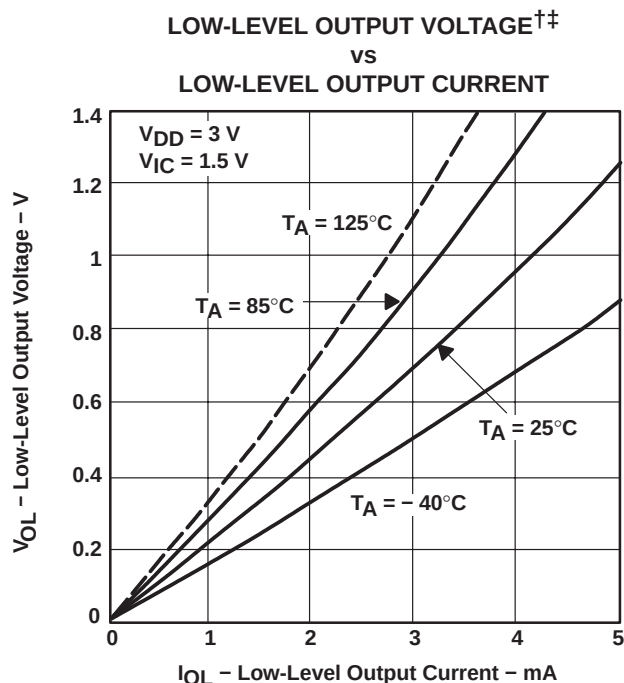
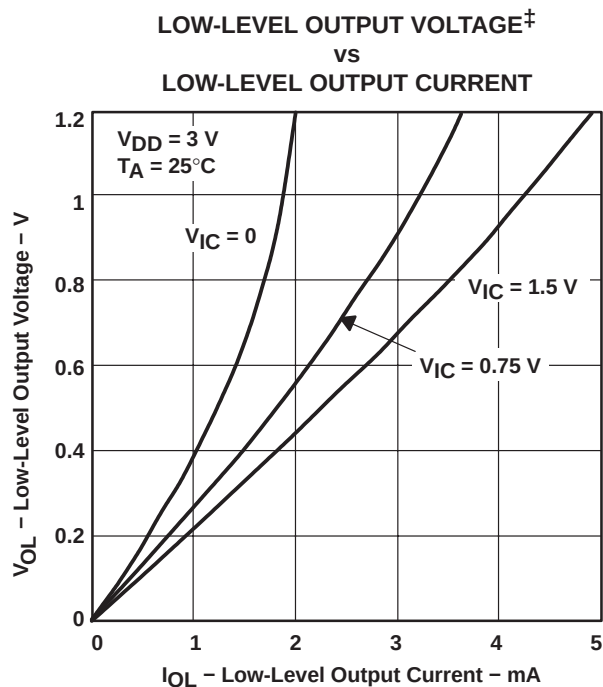
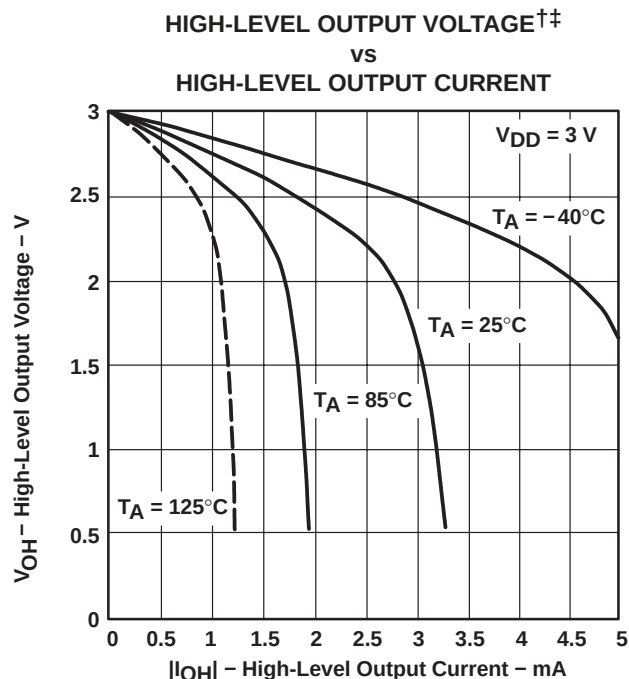
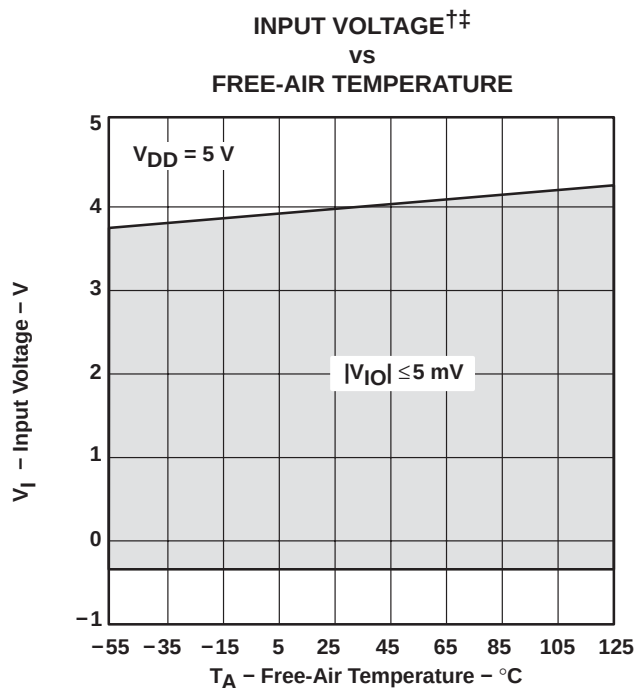


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

TLV2221, TLV2221Y

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

SLOS157B – JUNE 1996 – REVISED APRIL 2005

TYPICAL CHARACTERISTICS

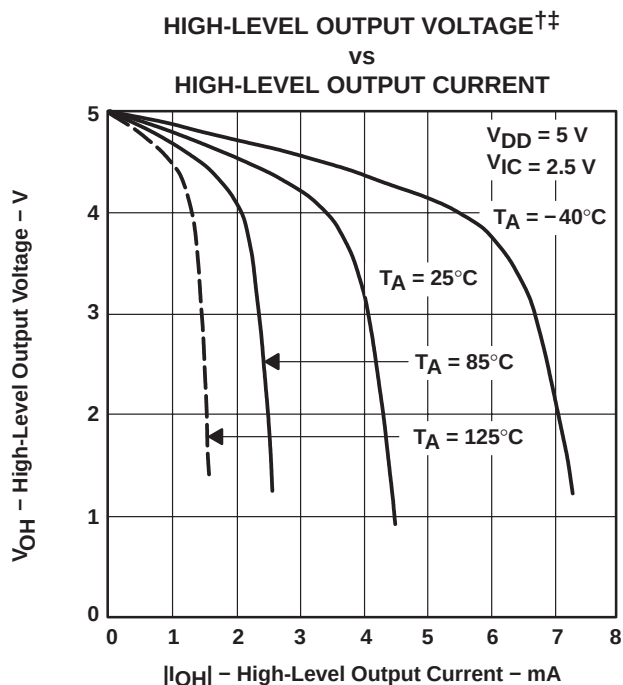


Figure 14

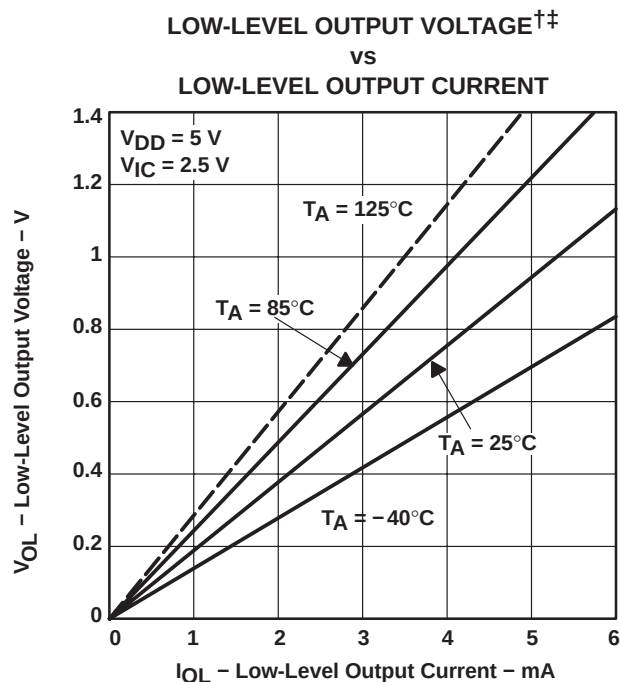


Figure 15

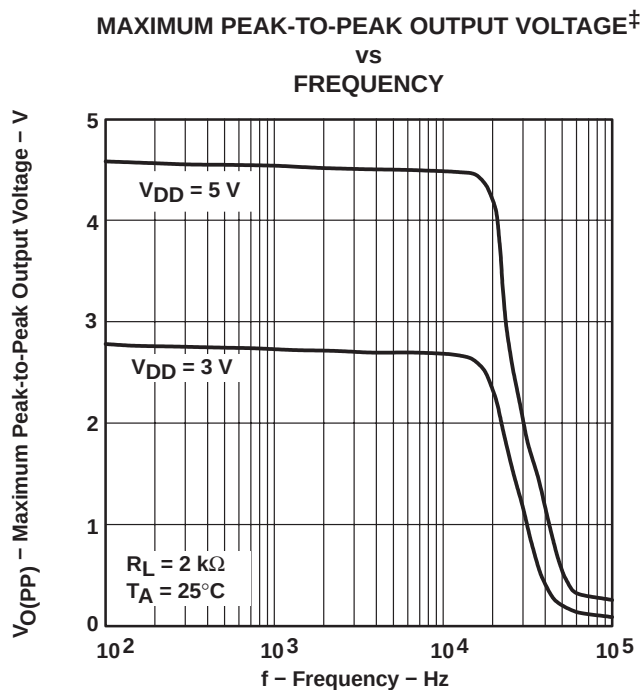


Figure 16

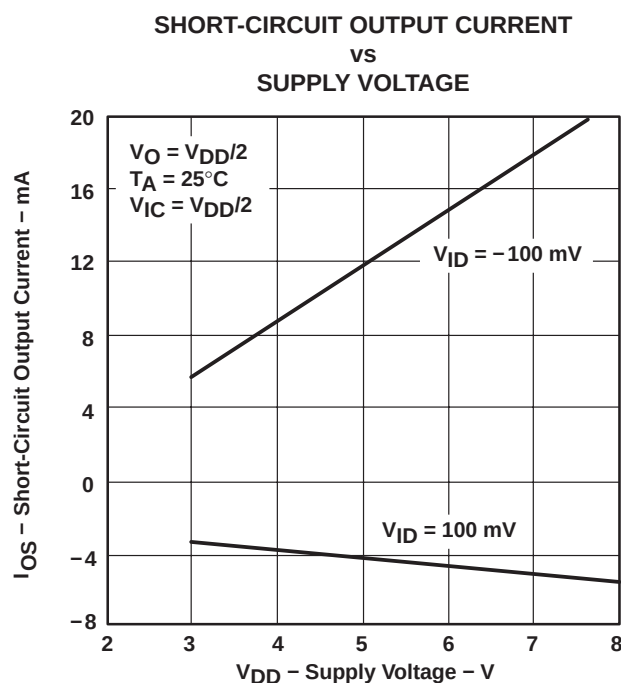
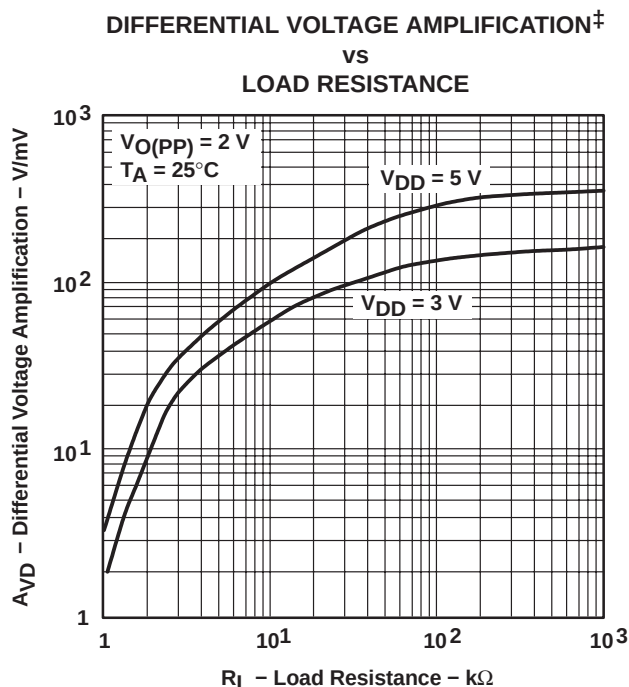
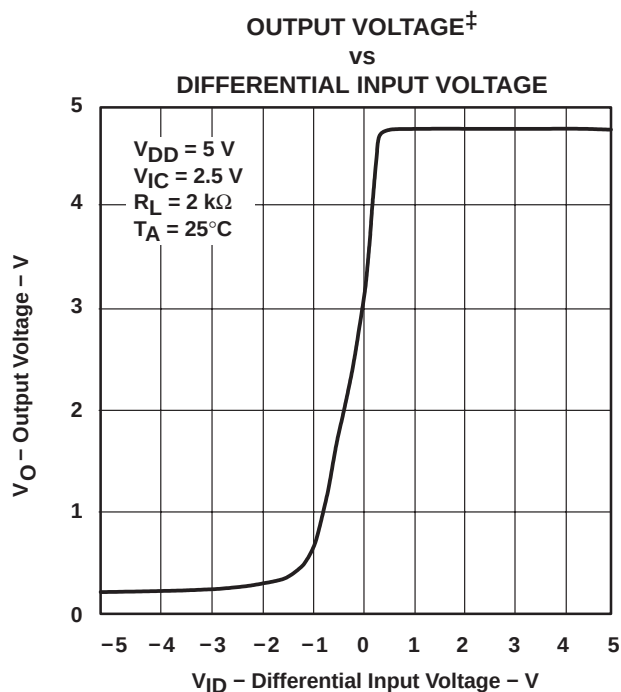
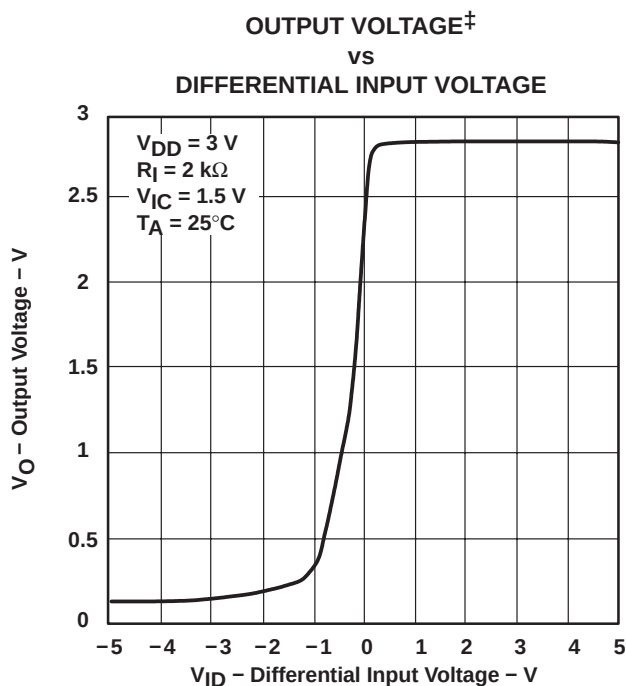
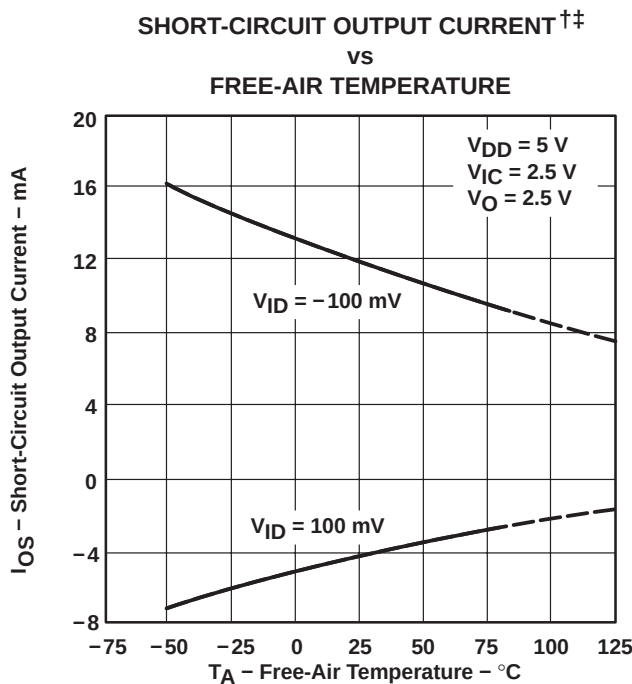


Figure 17

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

TLV2221, TLV2221Y
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

SLOS157B – JUNE 1996 – REVISED APRIL 2005

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE[†]
AMPLIFICATION AND PHASE MARGIN
VS
FREQUENCY

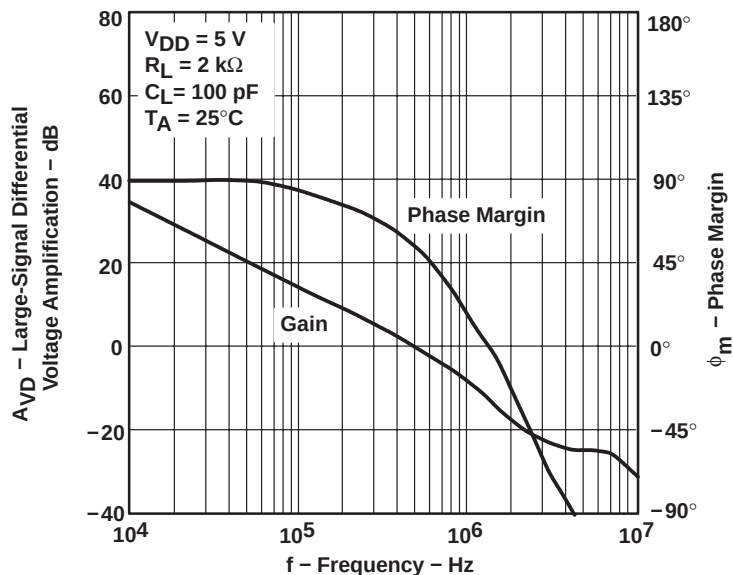


Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN[†]
VS
FREQUENCY

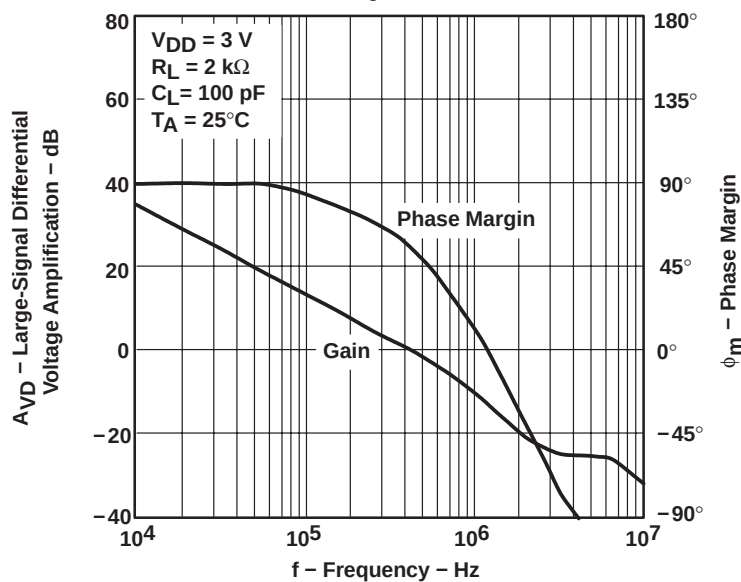


Figure 23

[†] For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

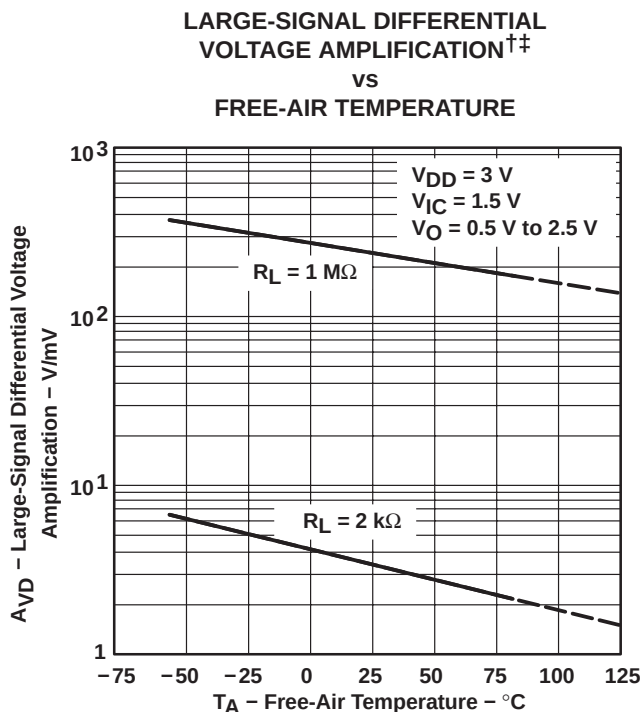


Figure 24

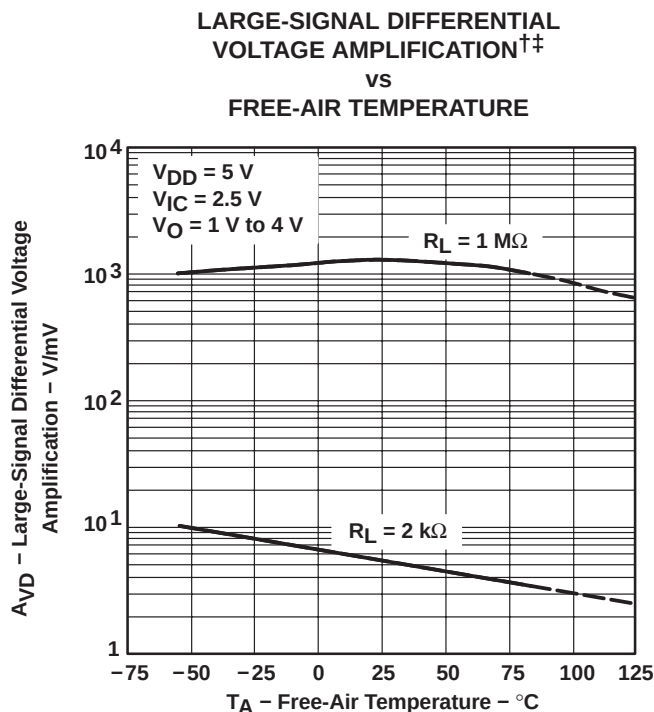


Figure 25

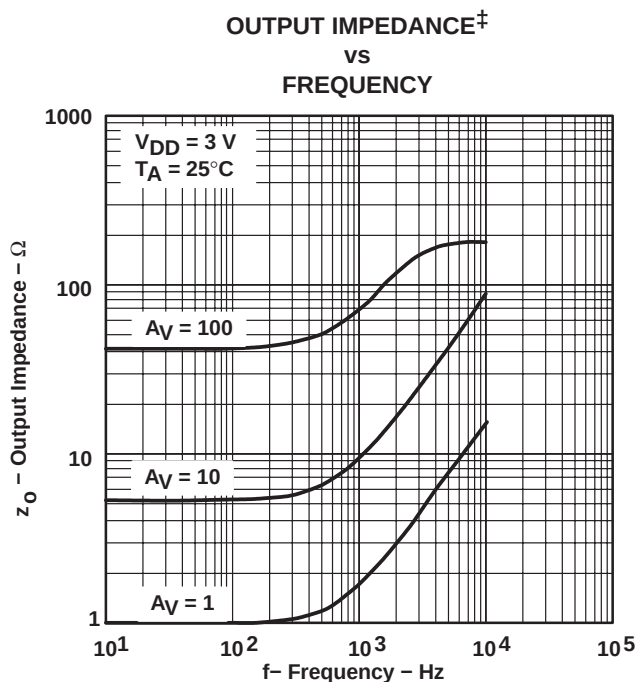


Figure 26

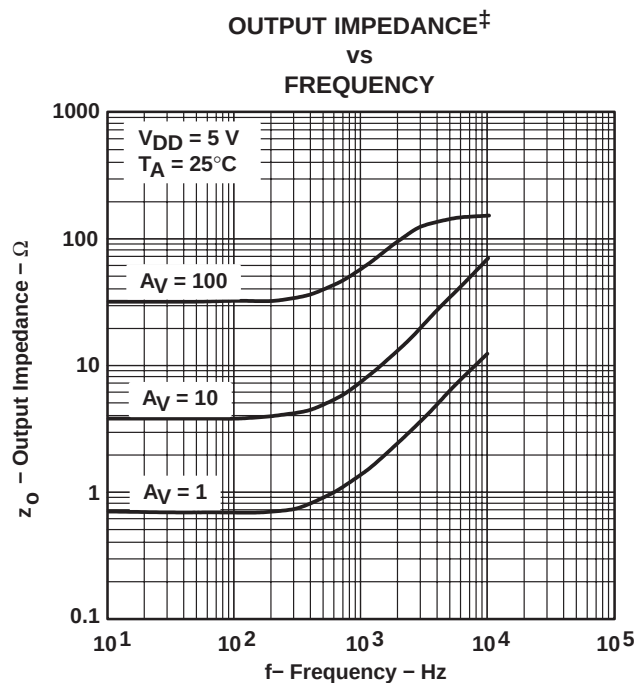


Figure 27

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TLV2221, TLV2221Y

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

SLOS157B – JUNE 1996 – REVISED APRIL 2005

TYPICAL CHARACTERISTICS

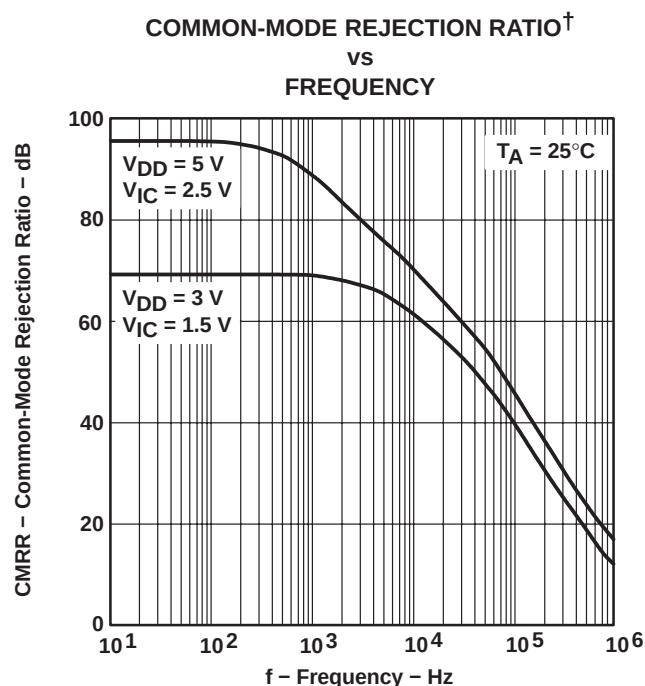


Figure 28

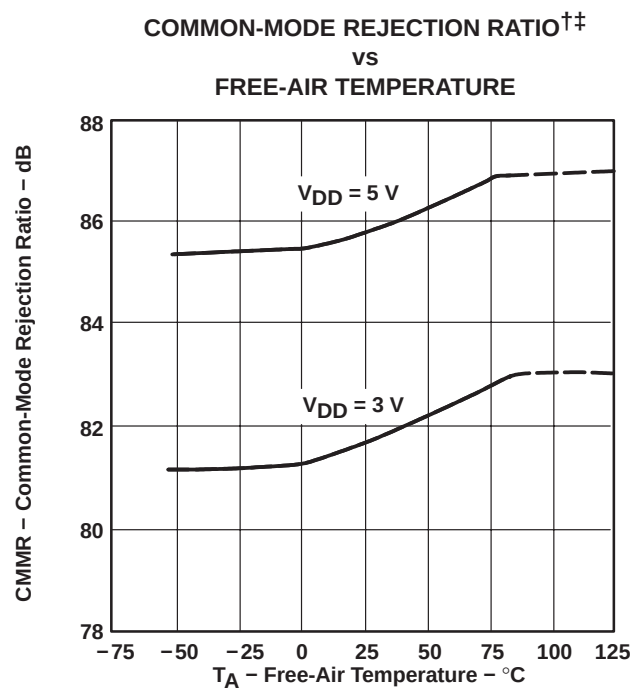


Figure 29

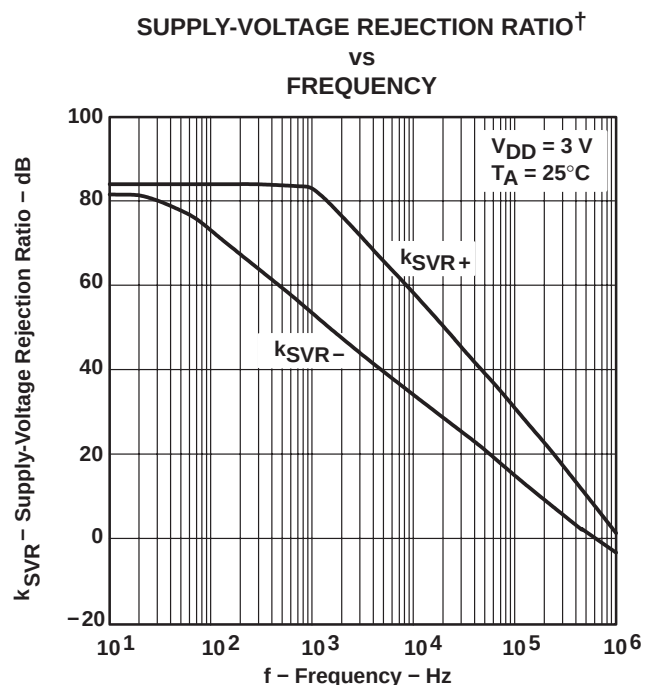


Figure 30

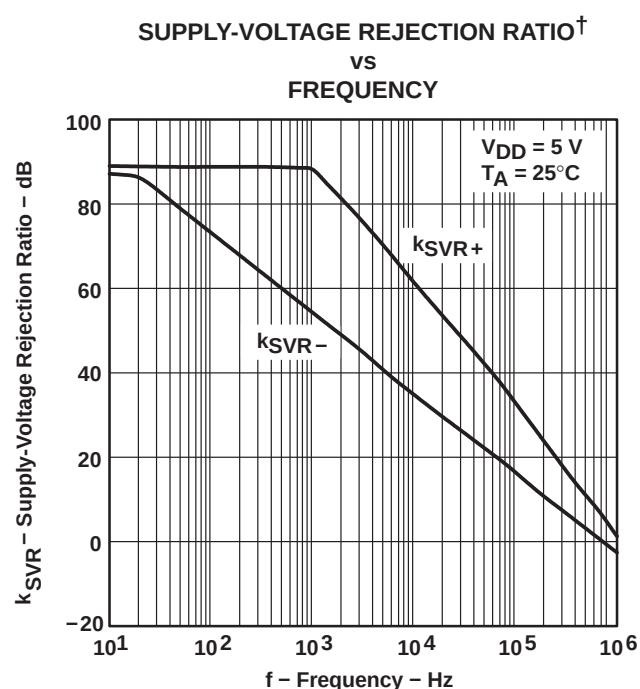


Figure 31

[†] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

[‡] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

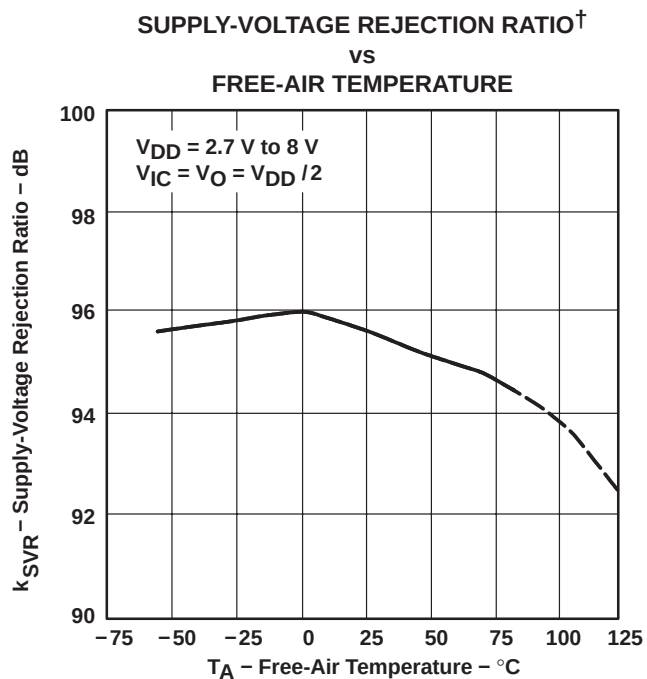


Figure 32

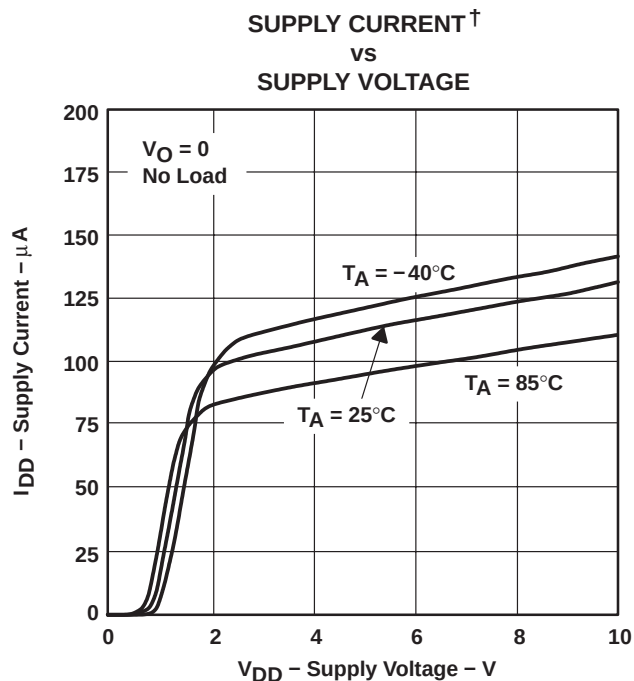


Figure 33

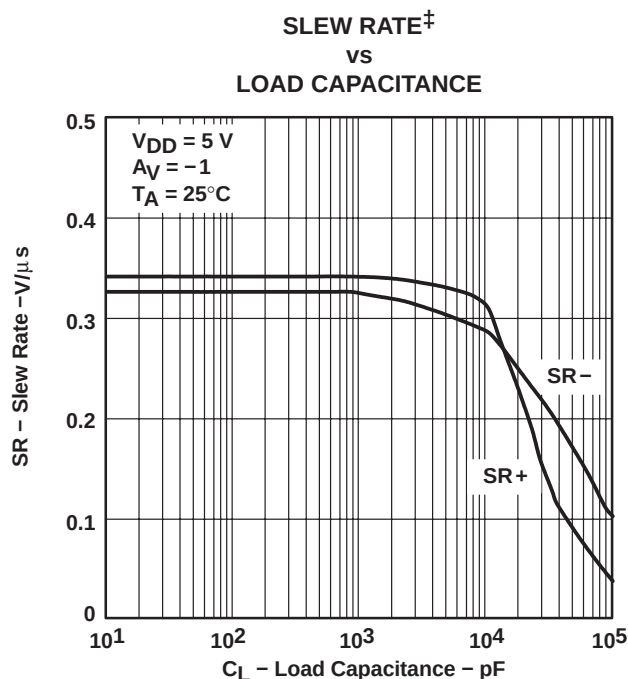


Figure 34

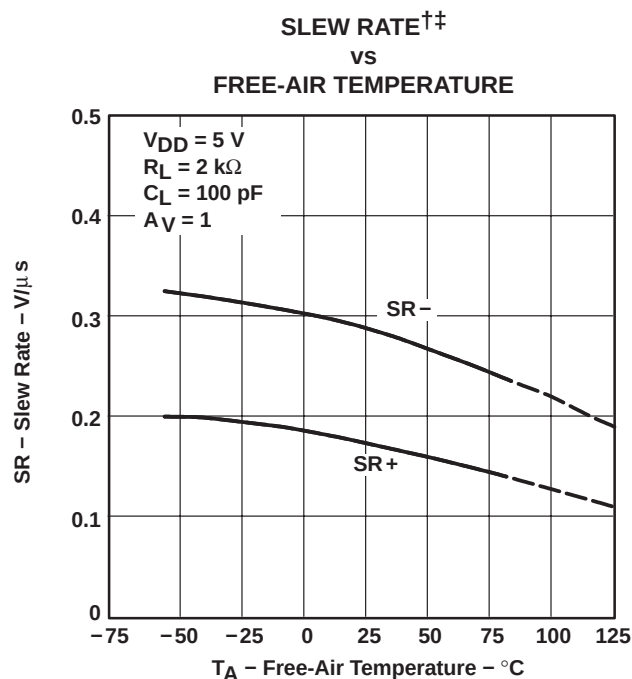


Figure 35

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.

TLV2221, TLV2221Y
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

SLOS157B – JUNE 1996 – REVISED APRIL 2005

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE†

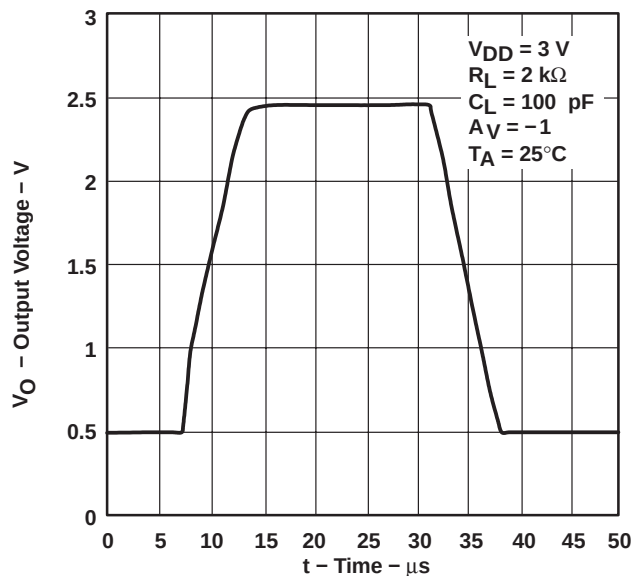


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE†

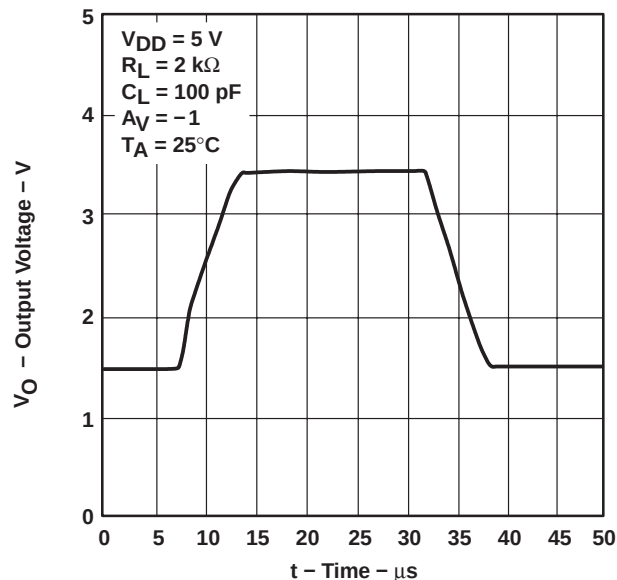


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

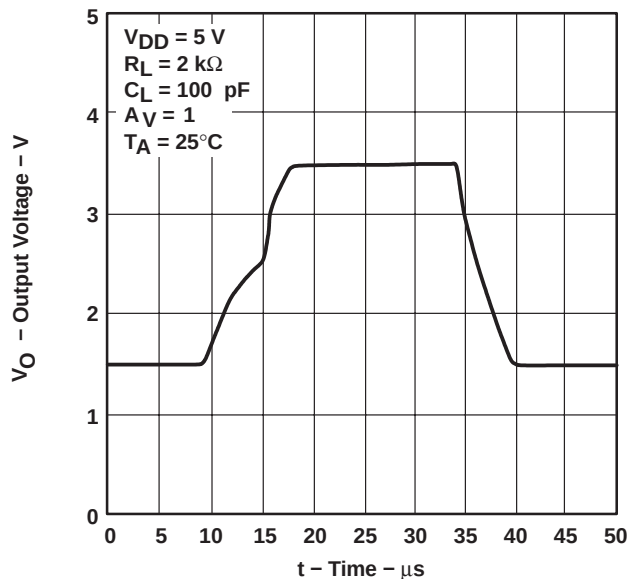


Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

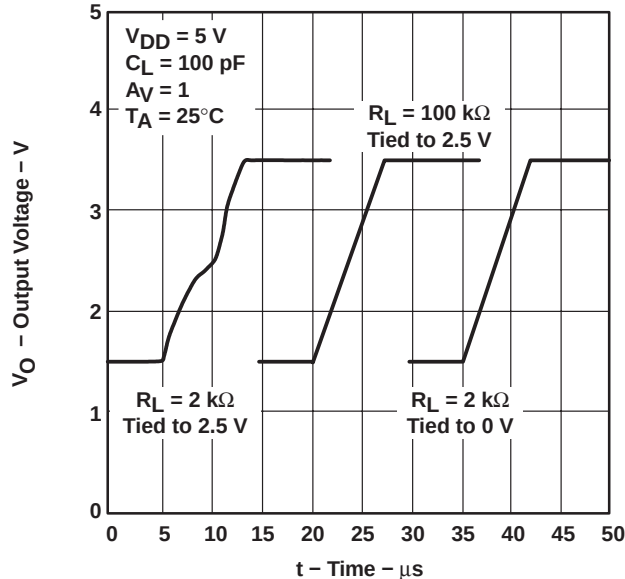


Figure 39

† For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

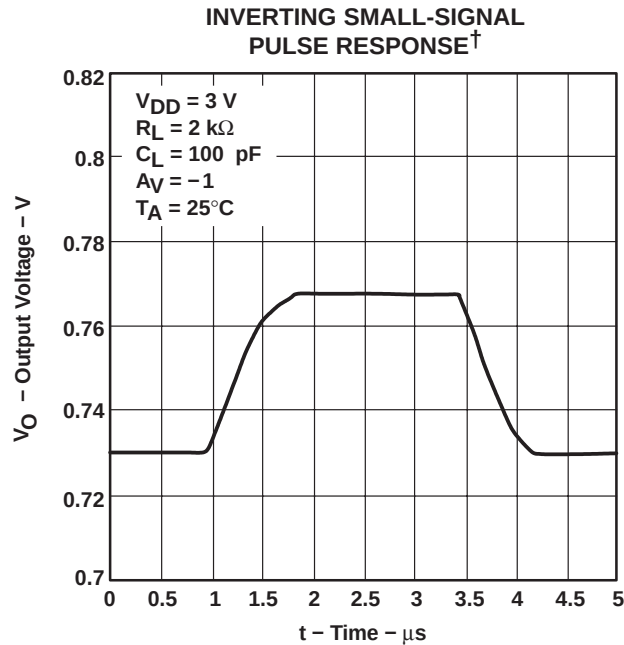


Figure 40

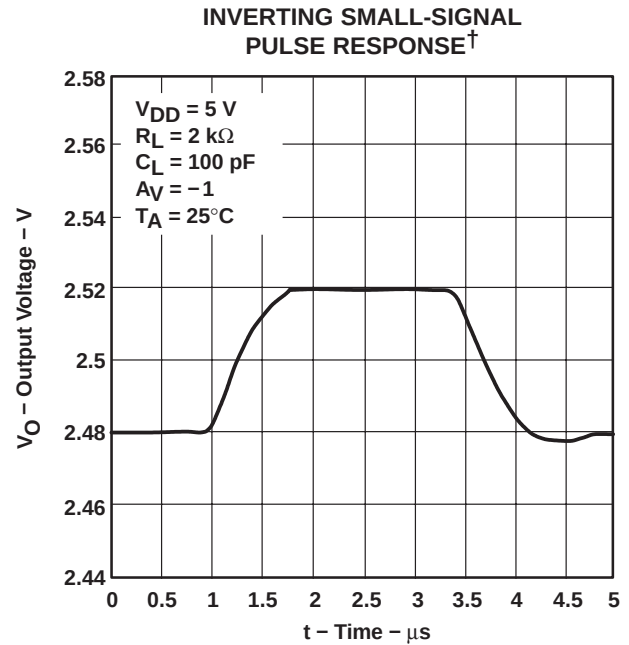


Figure 41

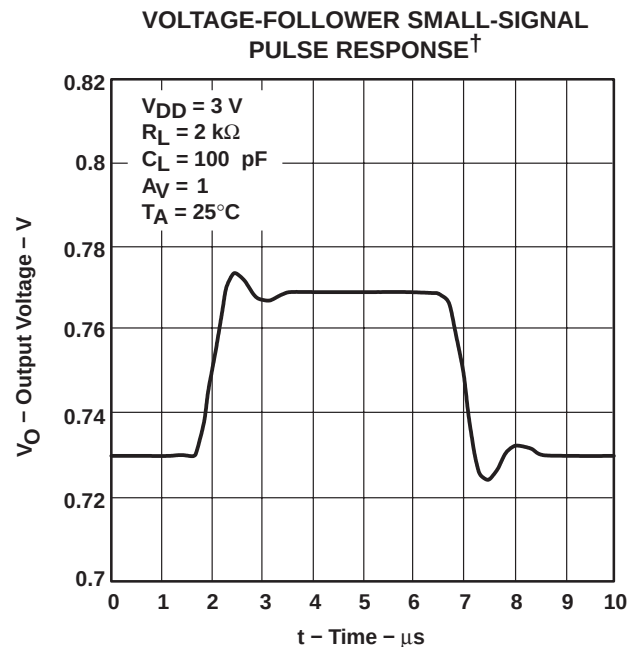


Figure 42

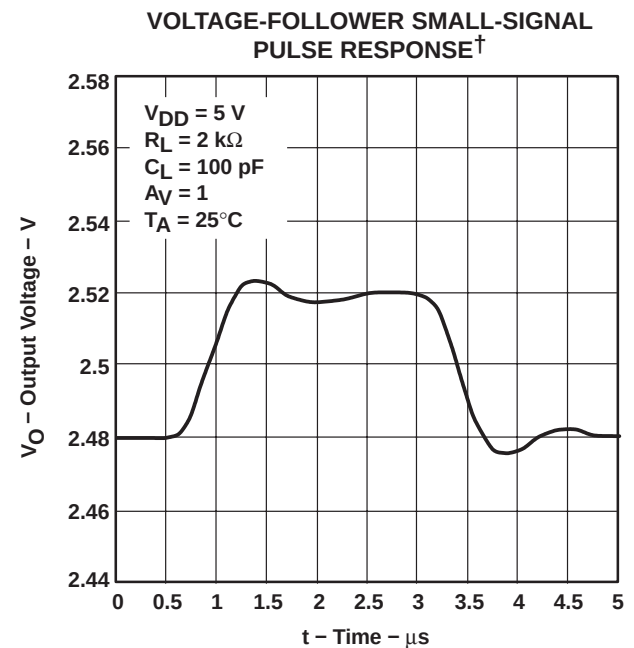


Figure 43

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TLV2221, TLV2221Y

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

SLOS157B – JUNE 1996 – REVISED APRIL 2005

TYPICAL CHARACTERISTICS

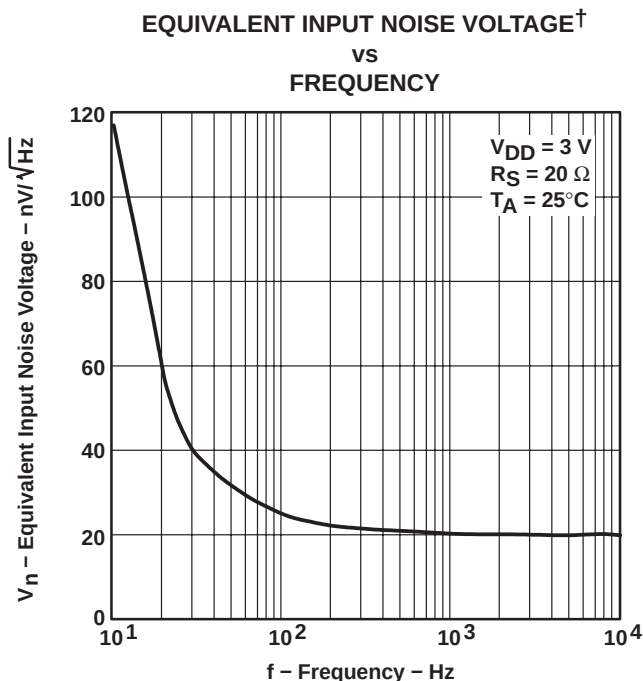


Figure 44

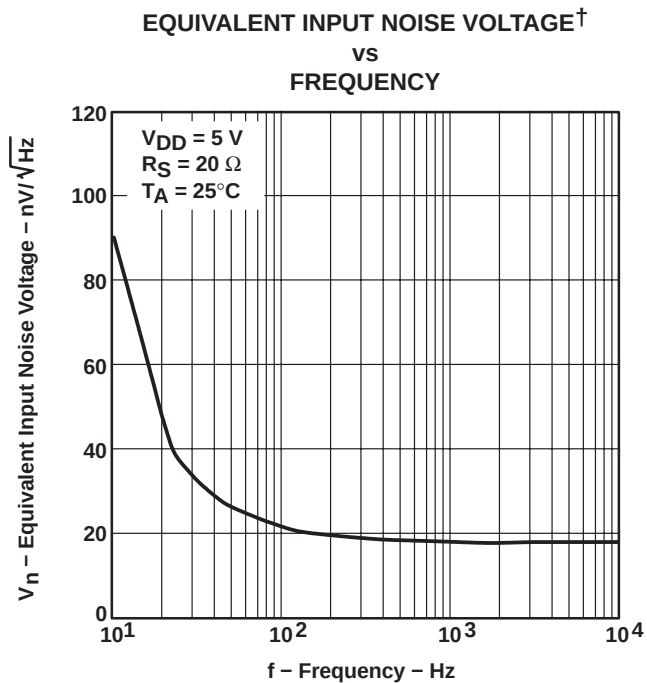


Figure 45

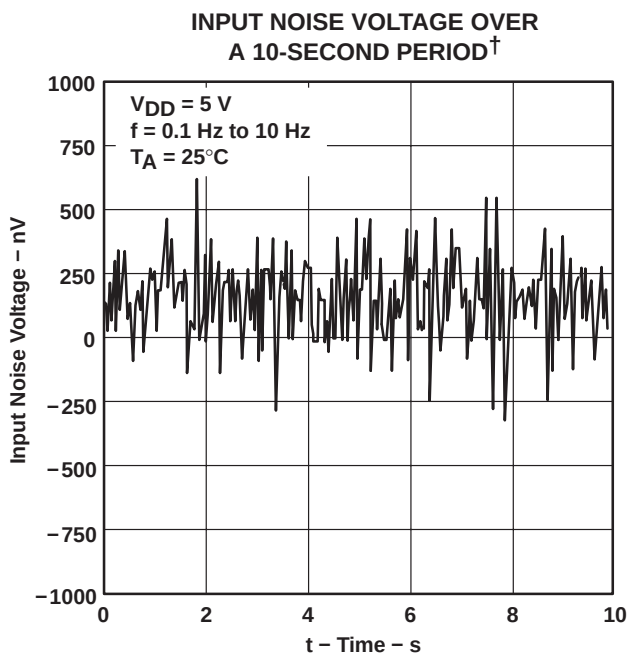


Figure 46

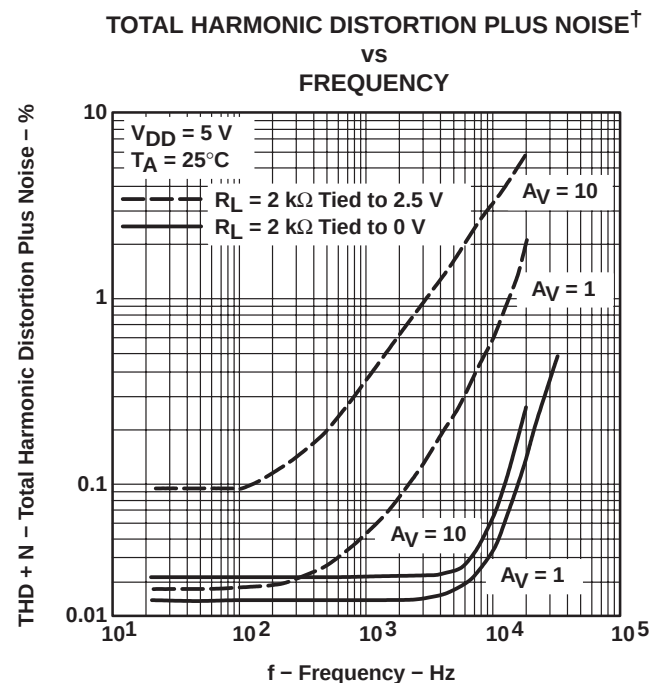


Figure 47

[†] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

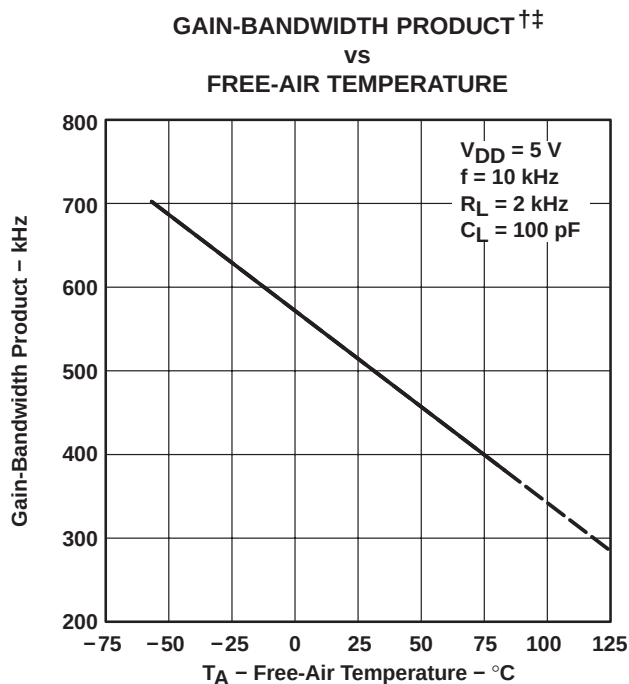


Figure 48

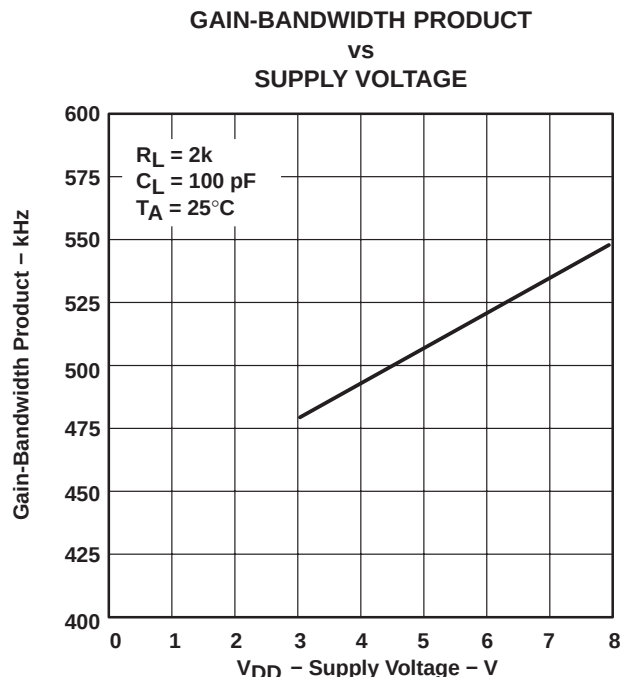


Figure 49

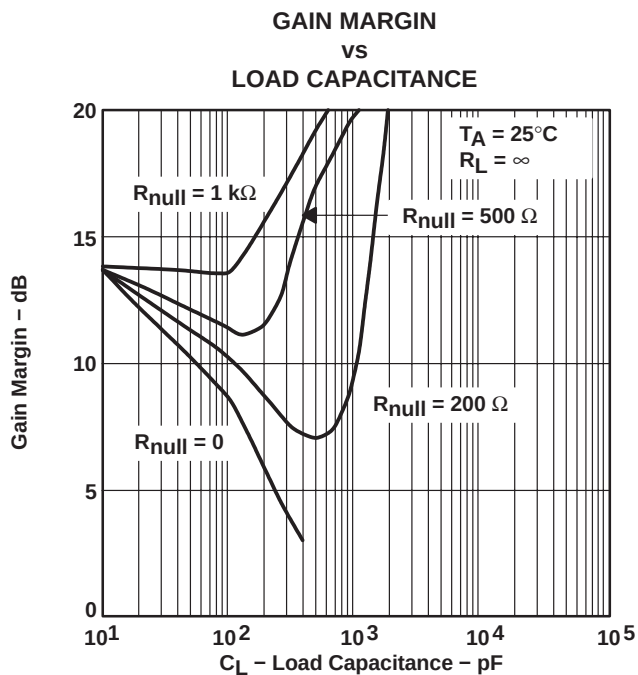


Figure 50

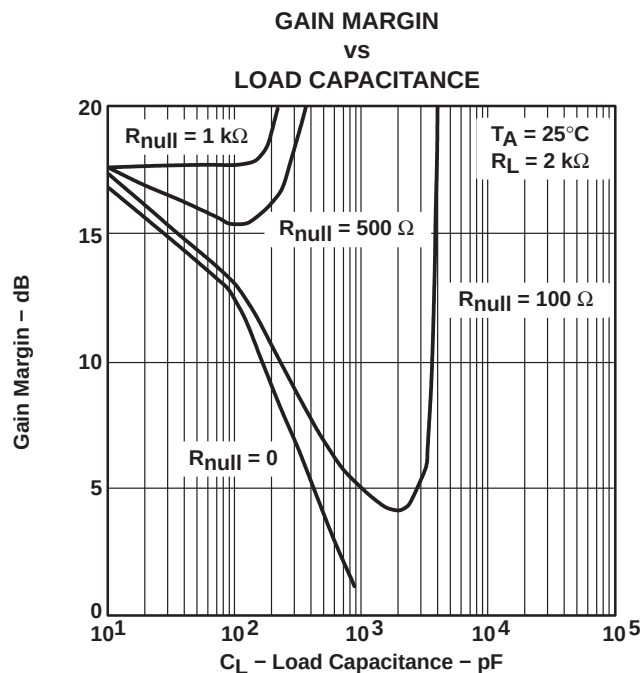
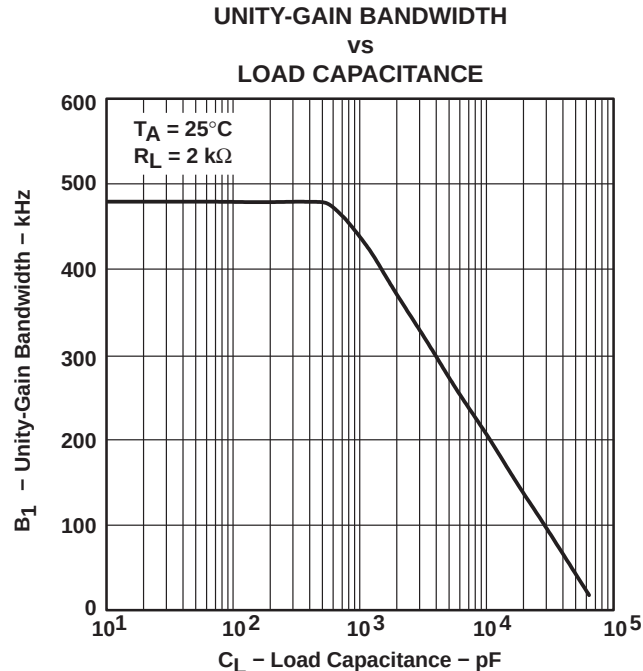
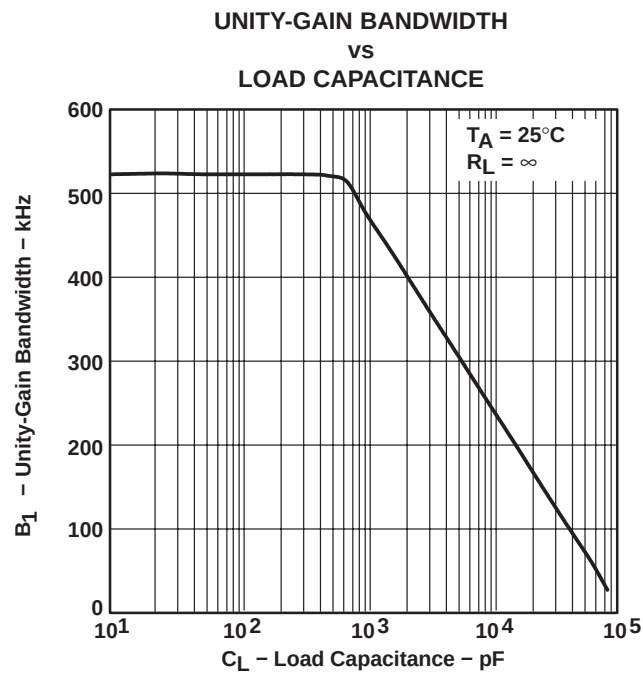
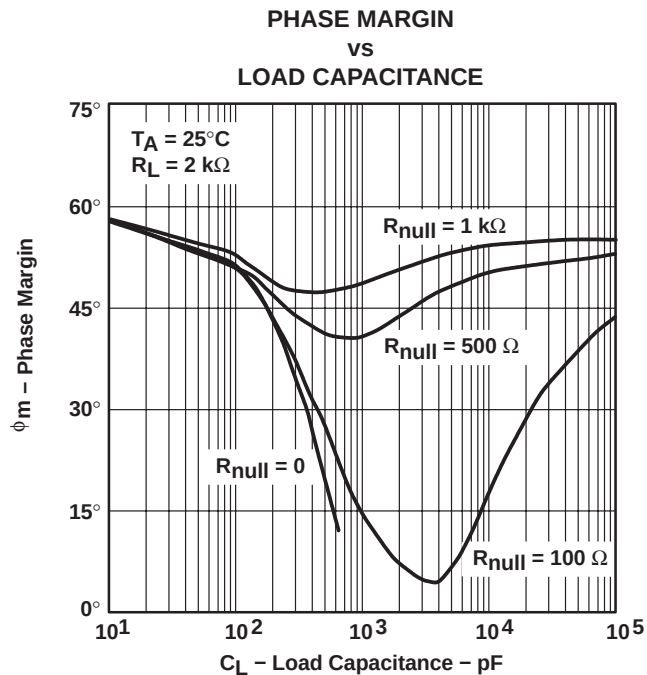
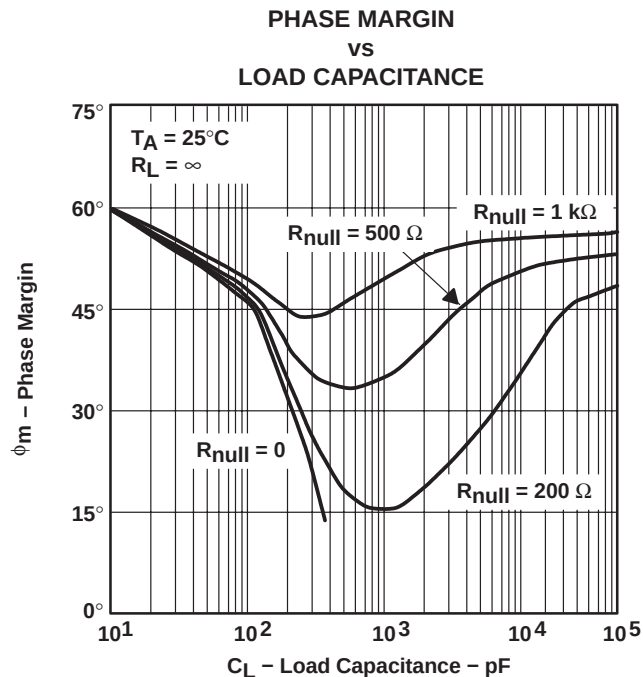


Figure 51

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



APPLICATION INFORMATION

driving large capacitive loads

The TLV2221 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 50 through Figure 55 illustrate its ability to drive loads greater than 100 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A small series resistor (R_{null}) at the output of the device (Figure 56) improves the gain and phase margins when driving large capacitive loads. Figure 50 through Figure 53 show the effects of adding series resistances of 100 Ω , 200 Ω , 500 Ω , and 1 k Ω . The addition of this series resistor has two effects: the first effect is that it adds a zero to the transfer function and the second effect is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the approximate improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \quad (1)$$

where :

$\Delta\phi_{m1}$ = improvement in phase margin

UGBW = unity-gain bandwidth frequency

R_{null} = output series resistance

C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (Figure 54 and Figure 55). To use equation 1, UGBW must be approximated from Figure 54 and Figure 55.

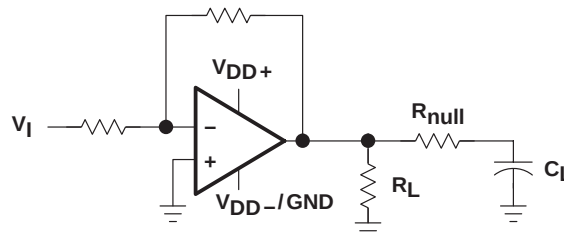


Figure 56. Series-Resistance Circuit

The TLV2221 is designed to provide better sinking and sourcing output currents than earlier CMOS rail-to-rail output devices. This device is specified to sink 500 μA and source 1 mA at $V_{DD} = 5\text{ V}$ at a maximum quiescent I_{DD} of 200 μA . This provides a greater than 80% power efficiency.

When driving heavy dc loads, such as 2 k Ω , the positive edge under slewing conditions can experience some distortion. This condition can be seen in Figure 38. This condition is affected by three factors:

- Where the load is referenced. When the load is referenced to either rail, this condition does not occur. The distortion occurs only when the output signal swings through the point where the load is referenced. Figure 39 illustrates two 2-k Ω load conditions. The first load condition shows the distortion seen for a 2-k Ω load tied to 2.5 V. The third load condition in Figure 39 shows no distortion for a 2-k Ω load tied to 0 V.
- Load resistance. As the load resistance increases, the distortion seen on the output decreases. Figure 39 illustrates the difference seen on the output for a 2-k Ω load and a 100-k Ω load with both tied to 2.5 V.
- Input signal edge rate. Faster input edge rates for a step input result in more distortion than with slower input edge rates.

TLV2221, TLV2221Y

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

SLOS157B – JUNE 1996 – REVISED APRIL 2005

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 57 are generated using the TLV2221 typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

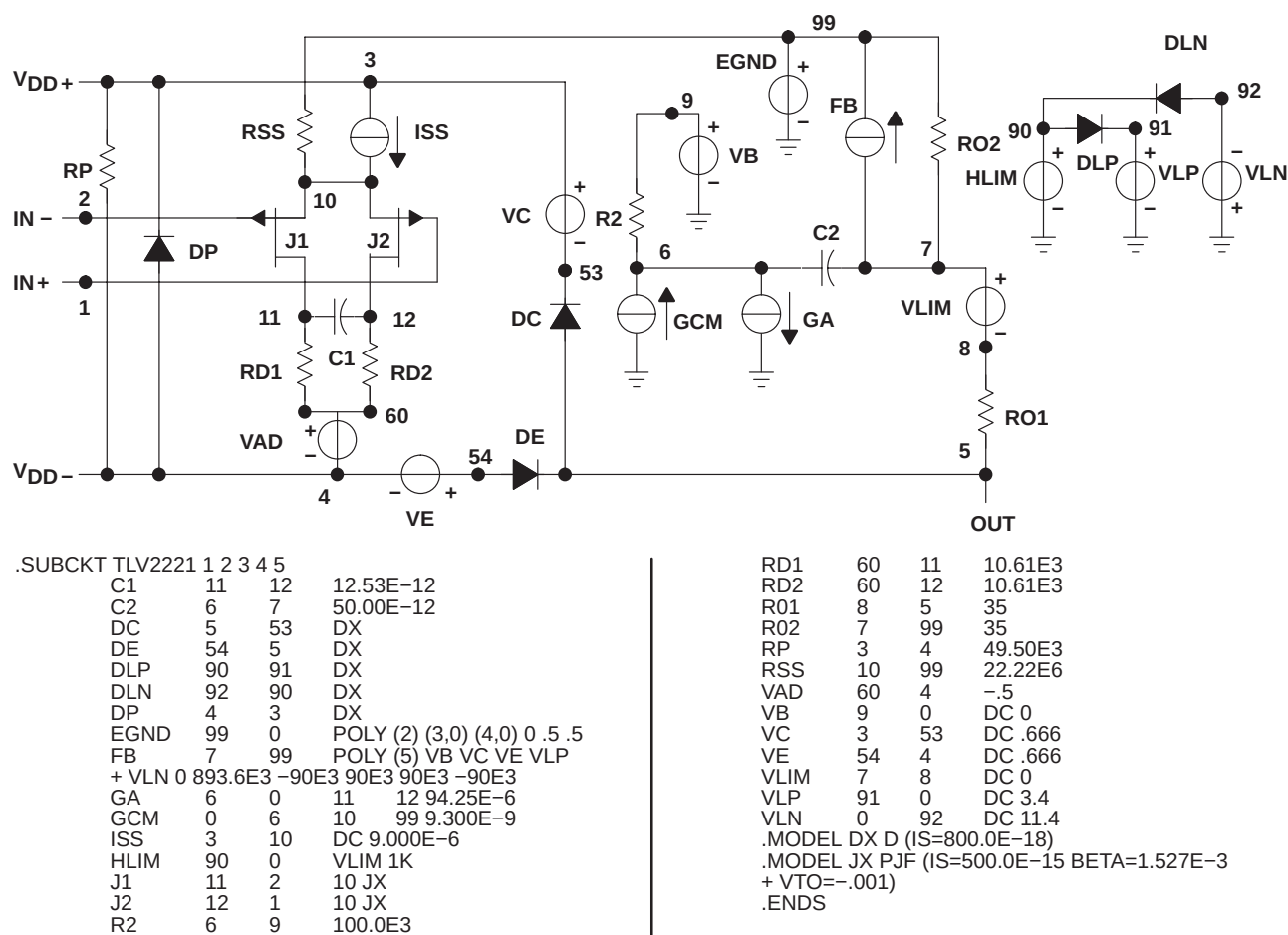


Figure 57. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademark of MicroSim Corporation.

Macromodels, simulation models, or other models provided by TI, directly or indirectly, are not warranted by TI as fully representing all of the specification and operating characteristics of the semiconductor product to which the model relates.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2221CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VADC	Samples
TLV2221CDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VADC	Samples
TLV2221CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VADC	Samples
TLV2221IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VADI	Samples
TLV2221IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VADI	Samples
TLV2221IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		VADI	Samples
TLV2221IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		VADI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

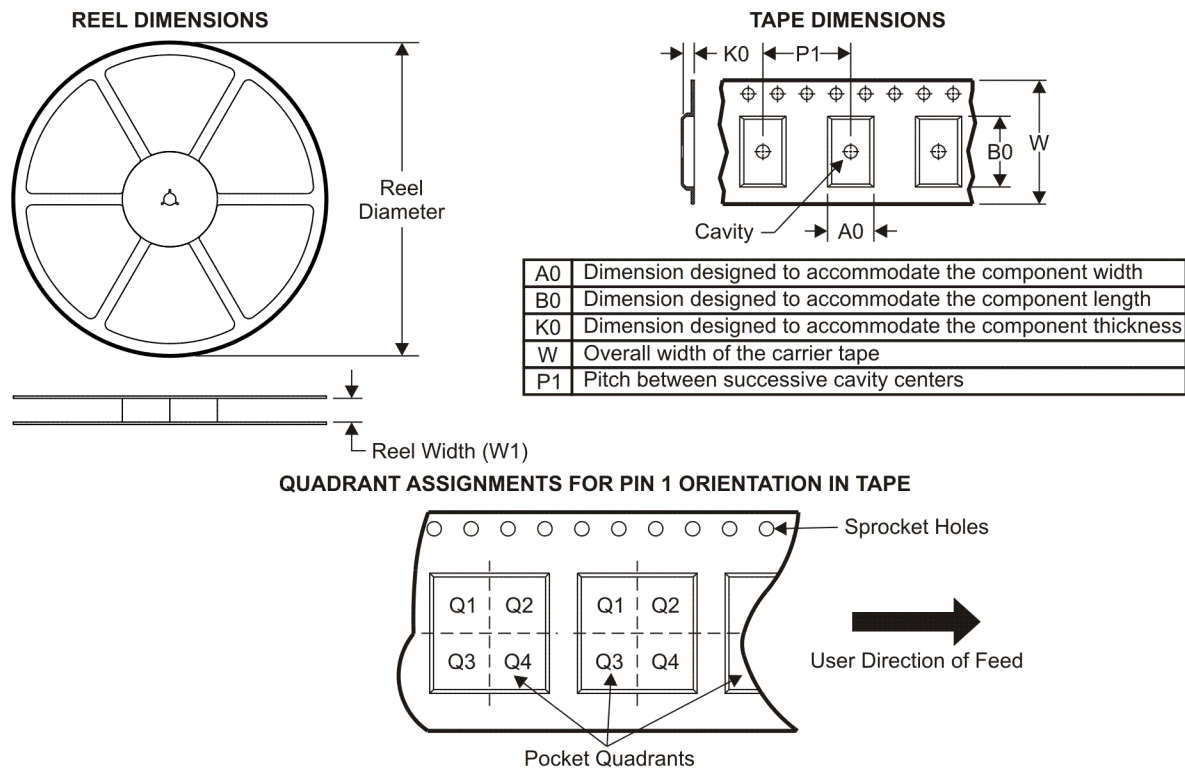
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

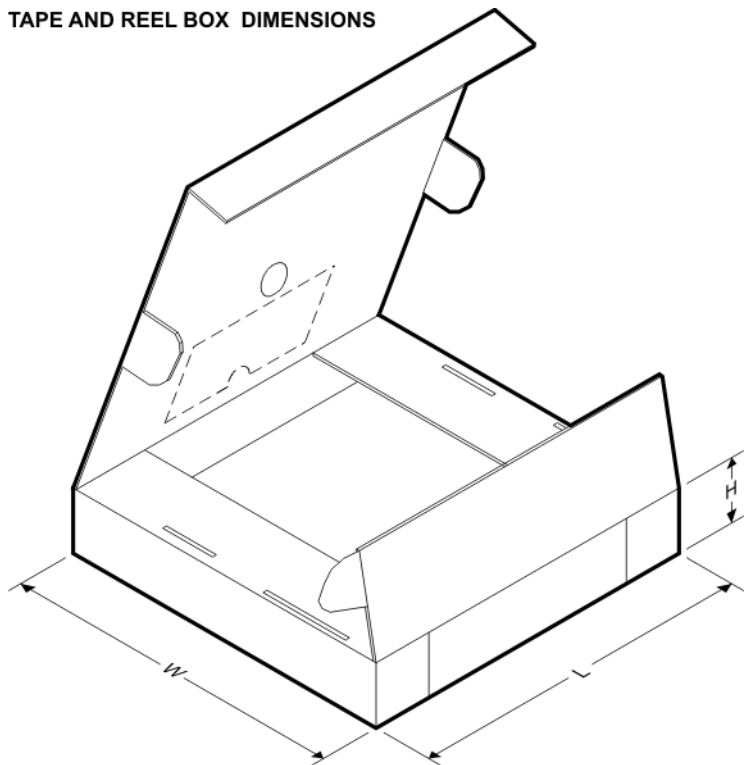
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2221CDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2221CDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2221IDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2221IDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2221CDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2221CDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV2221IDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2221IDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0

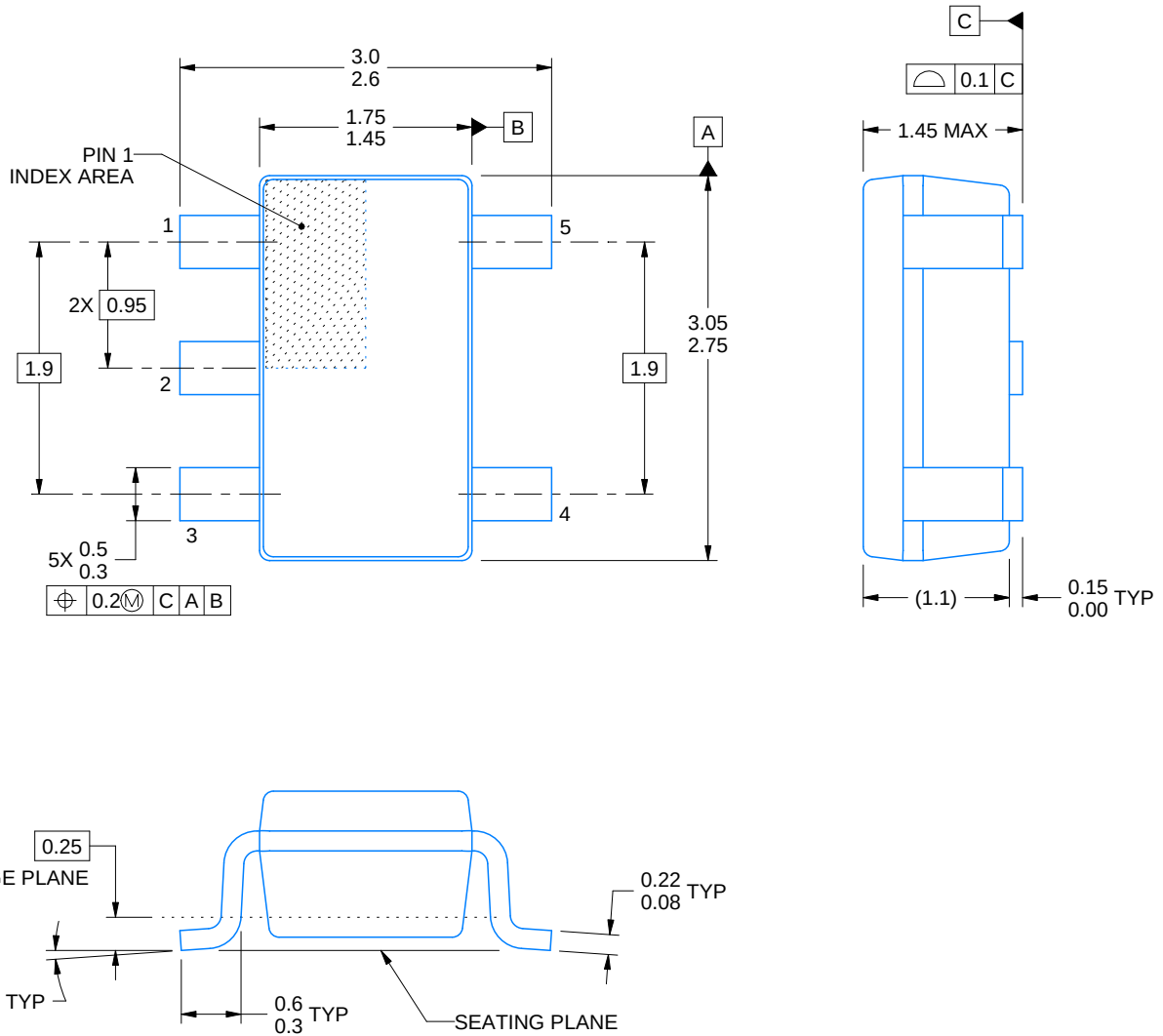


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

NOTES:

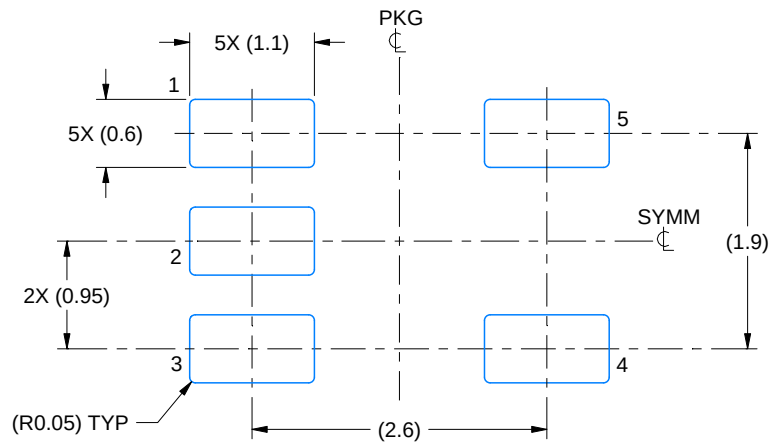
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

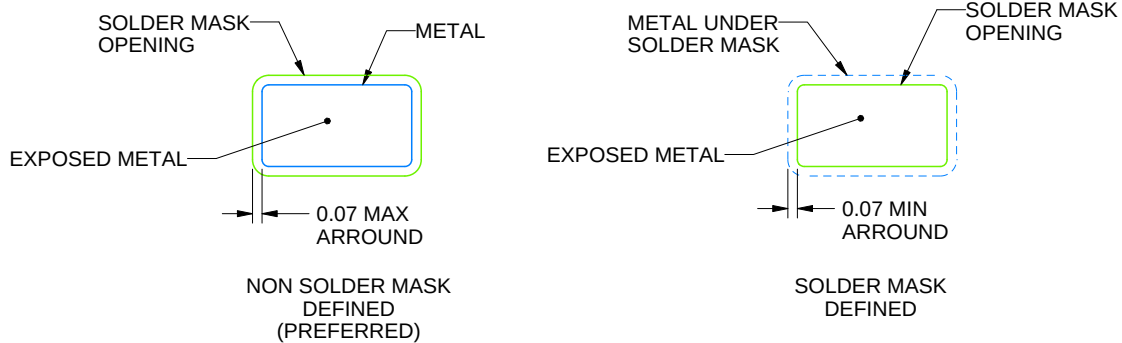
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

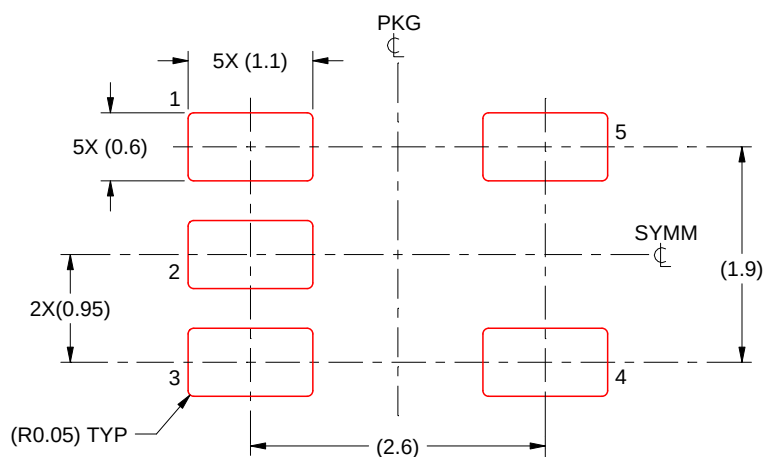
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

⊖ View [TLV2221IDBVT](#) on WIN SOURCE

⊖ [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management