



HEX D FLIP-FLOP

SY100S351

FEATURES

- Max. toggle frequency of 700MHz
- Clock to Q max. of 1200ps
- IEE min. of -98mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 50% faster than Fairchild 300K
- Better than 20% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

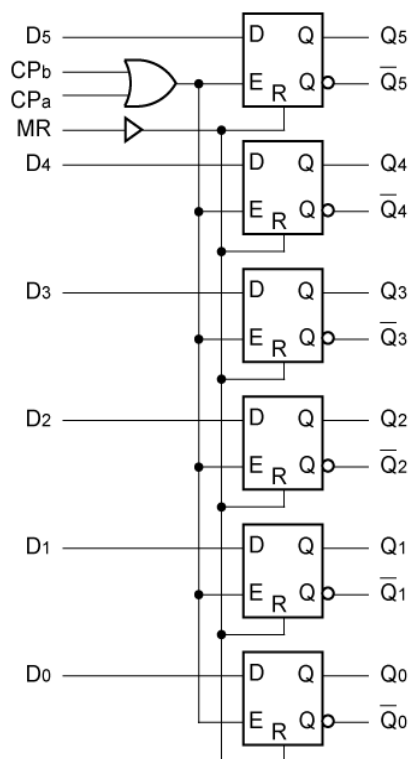
DESCRIPTION

The SY100S351 offers six D-type, edge-triggered, master/slave flip-flops with differential outputs, and is designed for use in high-performance ECL systems. The flip-flops are controlled by the signal from the logical OR operation on a pair of common clock signals (CP_a, CP_b). Data enters the master when both CP_a and CP_b are LOW and transfers to the slave when either CP_a or CP_b (or both) go to a logic HIGH. The Master Reset (MR) input overrides all other inputs and takes the Q outputs to a logic LOW. The inputs on this device have 75kΩ pull-down resistors.

PIN NAMES

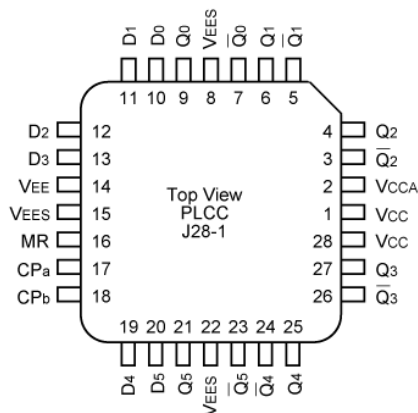
Pin	Function
D ₀ — D ₅	Data Inputs
CP _a , CP _b	Common Clock Inputs
MR	Asynchronous Master Reset Input
Q ₀ — Q ₅	Data Outputs
\bar{Q}_0 — \bar{Q}_5	Complementary Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION

Ordering Information



28-Pin PLCC (J28-1)

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S351JC	J28-1	Commercial	SY100S351JC	Sn-Pb
SY100S351JCTR ⁽¹⁾	J28-1	Commercial	SY100S351JC	Sn-Pb
SY100S351JZ ⁽²⁾	J28-1	Commercial	SY100S351JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S351JZTR ^(1,2)	J28-1	Commercial	SY100S351JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S351JY ⁽¹⁾	J28-1	Industrial	SY100S351JY with Pb-Free bar-line indicator	Matte-Sn
SY100S351JYTR ^(1,2)	J28-1	Industrial	SY100S351JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

TRUTH TABLES

Asynchronous Operation ⁽¹⁾				
Inputs				Outputs
D _n	CP _a	CP _b	MR	Q _n (t+1)
X	X	X	H	L

NOTE:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
t = Time before CP Positive Transition
t+1 = Time after CP Positive Transition
u = LOW-to-HIGH Transition

Synchronous Operation ⁽¹⁾				
Inputs				Outputs
D _n	CP _a	CP _b	MR	Q _n (t+1)
L	u	L	L	L
H	u	L	L	H
L	L	u	L	L
H	L	u	L	H
X	H	u	L	Q _n (t)
X	u	H	L	Q _n (t)
X	L	L	L	Q _n (t)

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

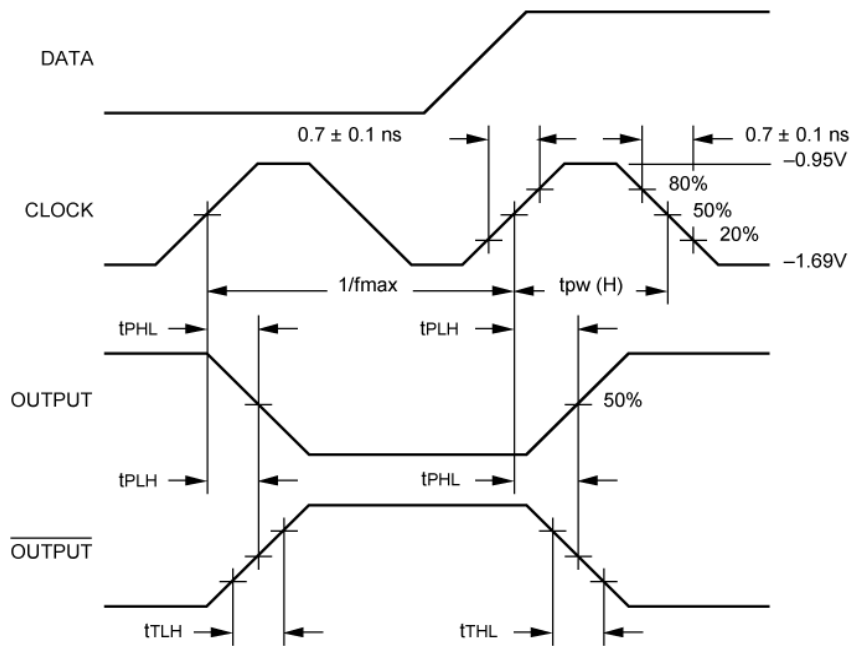
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	270	μA	$V_{IN} = V_{IH} (Max.)$
	MR	—	—	200		
	D ₀ – D ₅	—	—	300		
	CP _a , CP _b	—	—	300		
I_{EE}	Power Supply Current	-98	-71	-49	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = -40^{\circ}C$		$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Toggle Frequency	700	—	700	—	700	—	700	—	MHz	
t_{PLH} t_{PHL}	Propagation Delay CP _a , CP _b to Output	—	1200	—	1200	—	1200	—	1200	ps	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	—	1200	—	1200	—	1200	—	1200	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	300	900	ps	
t_s	Set-up Time D ₀ –D ₅ MR (Release Time)	500 1000	— —	500 1000	— —	500 1000	— —	500 1000	— —	ps	
t_H	Hold Time, D ₀ –D ₅	550	—	550	—	550	—	550	—	ps	
$t_{PW} (H)$	Pulse Width HIGH CP _a , CP _b , MR	1000	—	1000	—	1000	—	1000	—	ps	

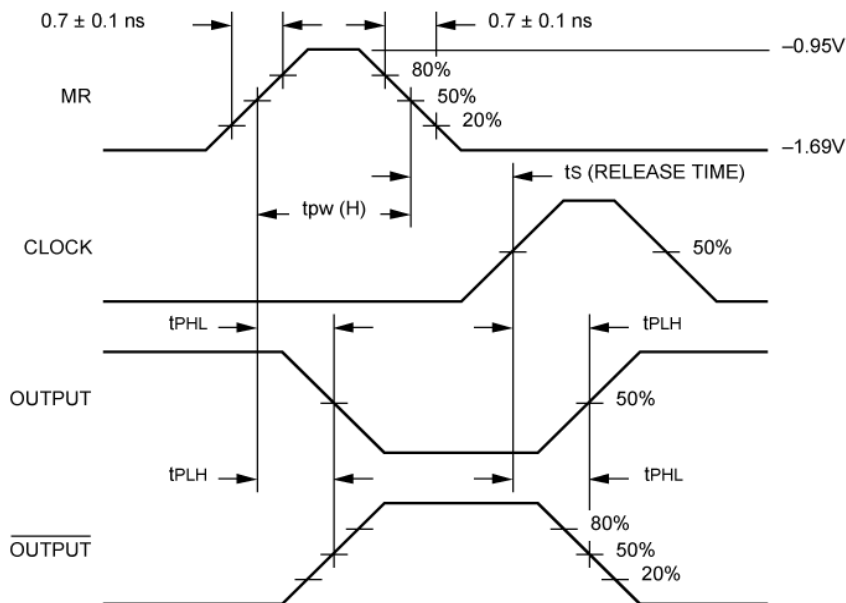
TIMING DIAGRAMS



Propagation Delay (Clock) and Transition Times

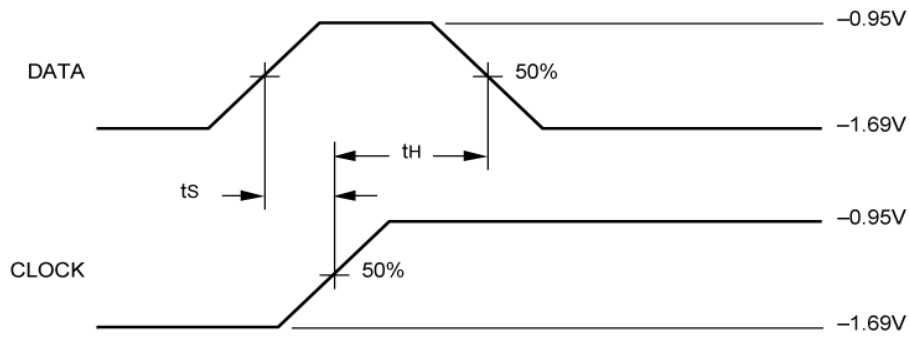
NOTE:

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND



Propagation Delay (Resets)

TIMING DIAGRAMS

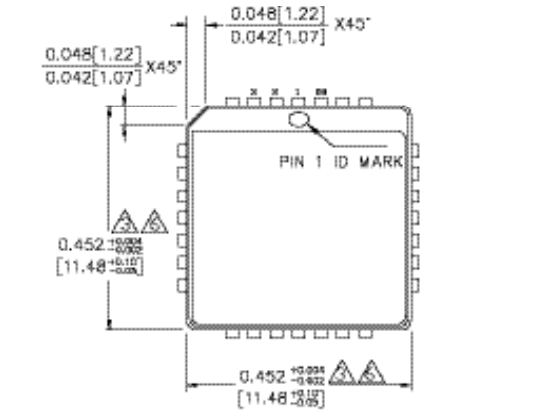


Data Set-up and Hold Time

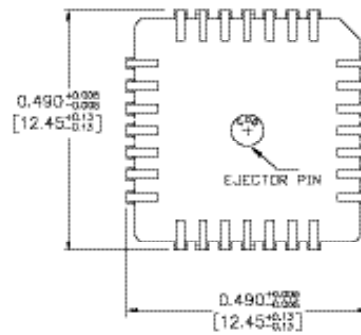
Notes:

1. $V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$
2. t_s is the minimum time before the transition of the clock that information must be present at the data input.
3. t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input.

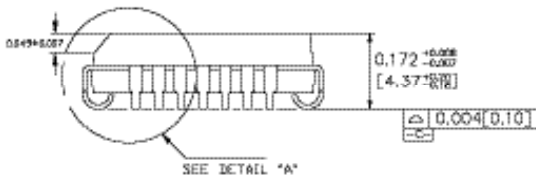
28-PIN PLCC (J28-1)



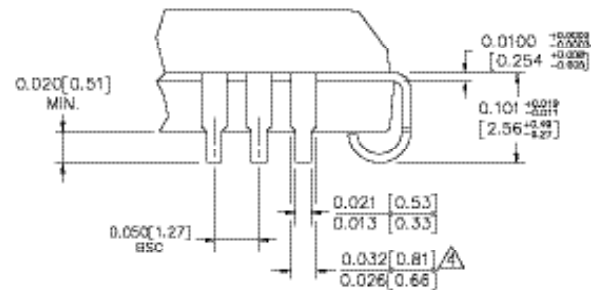
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL "A"

NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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