THE DATASHEET OF

IRS21850SPBF

Aug 25, 2008

International IOR Rectifier

IRS21850S

SINGLE HIGH SIDE DRIVER IC

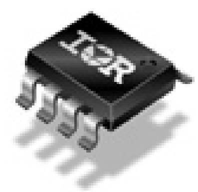
IC Features

- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for V_{BS} and V_{CC}
- 3.3 V and 5 V input logic compatible
- Tolerant to negative transient voltage
- Matched propagation delays for all channels
- RoHS compliant

Product Summary

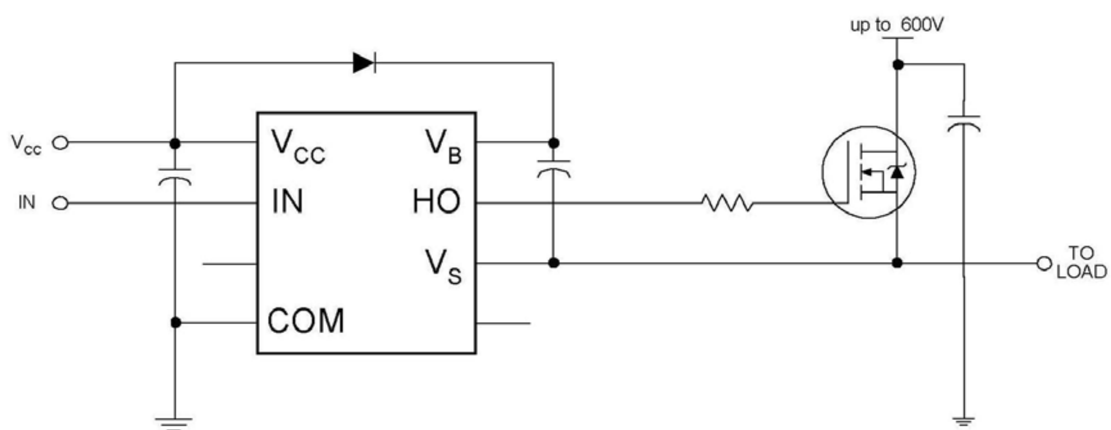
Topology	Single High Side
V_{OFFSET}	600 V
V_{OUT}	10V - 20V
I_{O+} & I_{O-} (typical)	4A / 4A
ton & toff (typical)	160ns & 160ns

Package Types



8-Lead SOIC

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

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Description

The IRS21850 is a high voltage, high speed power MOSFET and IGBT single high-side driver with propagation delay matched output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The floating logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic and can be operated up to 600 V above the ground. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFETor IGBT in the high-side configuration, which operates up to 600 V.

Qualification Information[†]

Qualification Level		Industrial[††]	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC8	MSL2[†††] 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class C (per JEDEC standard EIA/JESD22-A115)	
	Human Body Model	Class 2 (per EIA/JEDEC standard JESD22-A114)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under boardmounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_{CC}	Low-side supply y voltage	-0.3	20†	V
V_{IN}	Low-side output voltage (HIN)	COM -0.3	V_{CC} + 0.3	
V_B	High-side floating well supply voltage	-0.3	620†	
V_S	High-side floating well supply return voltage	V_B -20	V_B + 0.3	
V_{HO}	Floating gate drive output voltage	V_S -0.3	V_B + 0.3	
dV_S/dt	Allowable VS offset supply transient relative to COM	---	50	V/ns
P_D	Maximum Power Dissipation @ TA ≤ +25ºC	---	1.25	W
Rth_{JA}	Thermal resistance, junction to ambient	---	100	ºC/W
T_J	Junction temperature	-55	150	ºC
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	---	300	

† All supplies are fully tested at 25 V. An internal 20 V clamp exists for each supply.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The offset rating are tested with supplies of (VCC-COM)= (VB-VS)=15 V.

Symbol	Definition	Min.	Max.	Units
V_{CC}	Low-side supply voltage	10	20	V
VI_N	HIN input voltage	COM	V_{CC}	
V_B	High-side floating well supply voltage	V_S + 10	V_S + 20	
V_S	High-side floating well supply offset voltage	Note 2	600	
V_{HO}	Floating gate drive output voltage	V_S	V_B	
T_A	Ambient temperature	-40	125	ºC

†† Logic operational for VS of -5 V to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

(V_{CC}-COM)= (V_B-VS) =15 V, T_A = 25 ºC. C_L = 1000 pF unless otherwise specified. All parameters are referenced to COM.

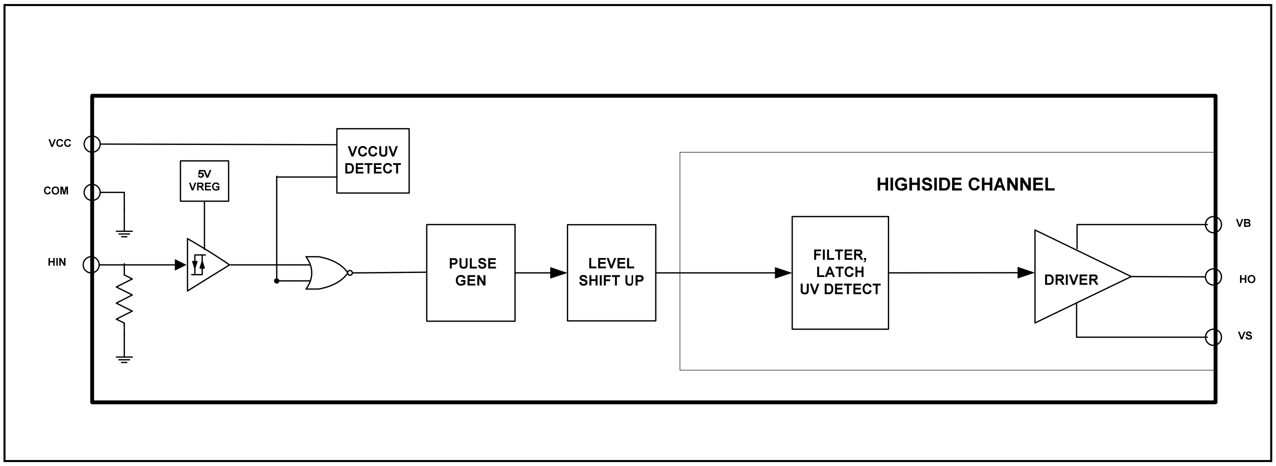
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
ton	Turn-on propagation delay	---	160	210	ns	(V_S-COM)= 0 V
toff	Turn-off propagation delay	---	160	210		(V_S-COM)= 600 V
tr	Turn-on rise time	---	15	40		
tf	Turn-off fall time	---	15	40		

Static Electrical Characteristics

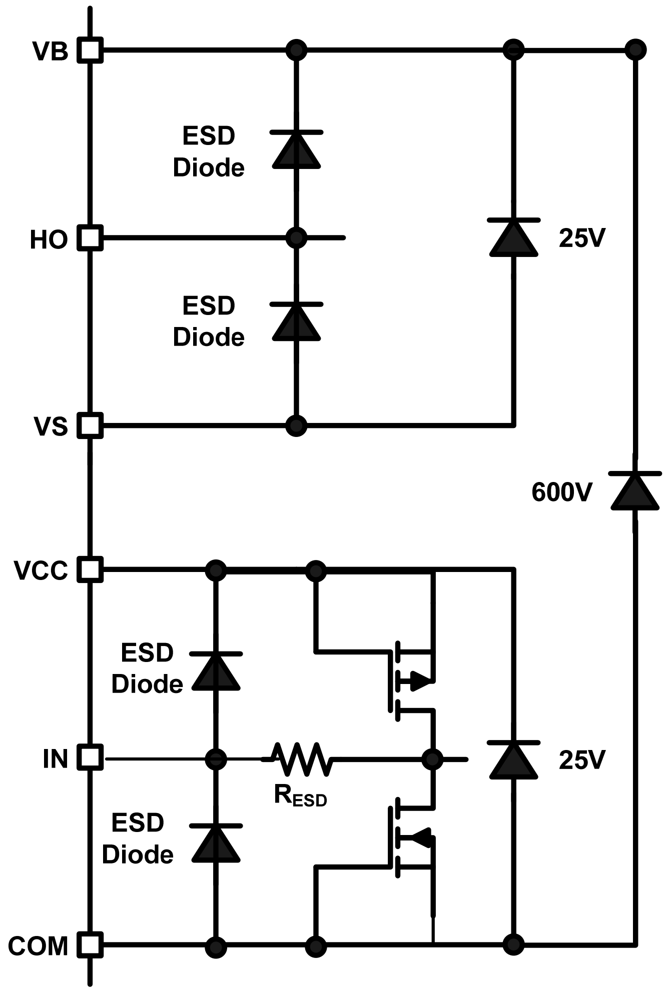
(V_{CC}-COM)= (V_B-V_S) =15 V. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced respective VS and are applicable to the respective output leads HO. The V_{CC} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{CCUV}+	V_{CC} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV}-	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{BSUV}+	V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8		
V_{BSUV}-	V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
I_{LK}	High-side floating well offset supply leakage current	—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	80	150		HIN = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	—	120	240		
V_{IH}	Logic "1" input voltage	2.5	—	—	V	
V_{IL}	Logic "0" input voltage	—	—	0.8		
$V_{OH,\ HO}$	HO high level output voltage, V_{BIAS} – V_O	—	20	60	mV	I_O = 2 mA
$V_{OL,\ HO}$	HO low level output voltage, V_O	—	10	30		
I_{IN}+	Logic "1" input bias current	—	10	20	µA	V_{HIN} = 5 V
I_{IN}-	Logic "0" input bias current	—	0	5		V_{HIN} = 0 V
I_O+, HO	Output high short circuit pulsed current HO	—	4	—	A	V_O = 0 V, V_{IN} = 0V PW ≤ 10 µs
I_O-, HO	Output low short circuit pulsed current HO	—	4	—		V_O = 15 V, V_{IN} = 15V PW ≤ 10 µs

Functional Block Diagram



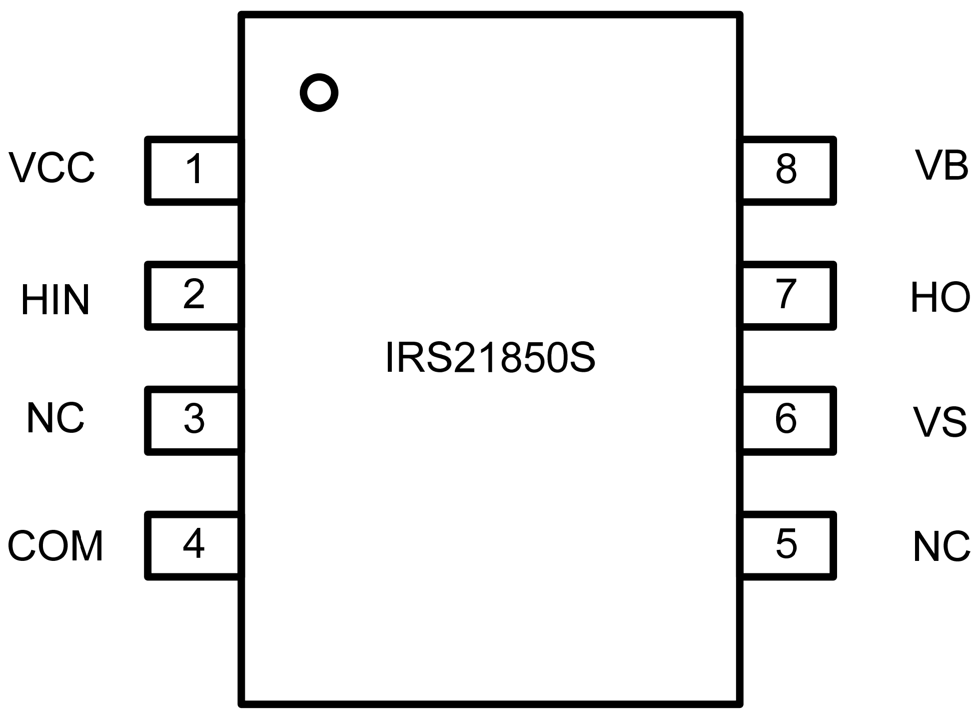
I/O Pin Equivalent Circuit Diagrams



Lead Definitions

Pin #	Symbol	Description
1	VCC	Low-side supply voltage
2	HIN	Logic inputs for high-side gate driver output (in phase)
3	NC	No Connect
4	COM	Ground
5	NC	No Connect
6	VS	High voltage floating supply return
7	HO	High-side driver outputs
8	VB	High-side drive floating supply

Lead Assignments



Waveform definitions

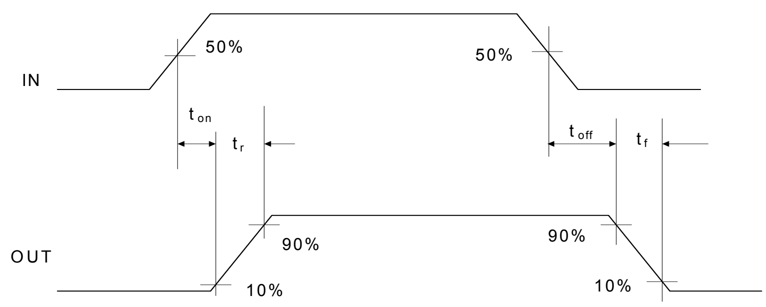


Figure 1 Switching Time Waveforms

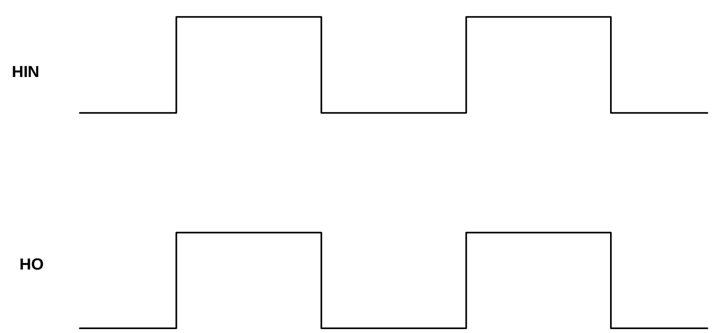


Figure 2 Input/Output Timing Diagram

Parameter Temperature Trends

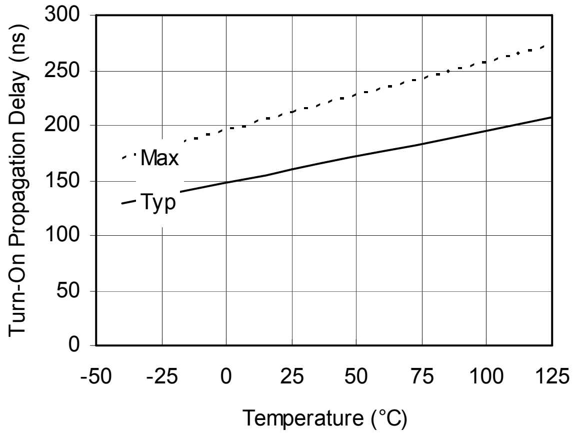


Figure 3A. Turn-On Propagation Delay vs. Temperature

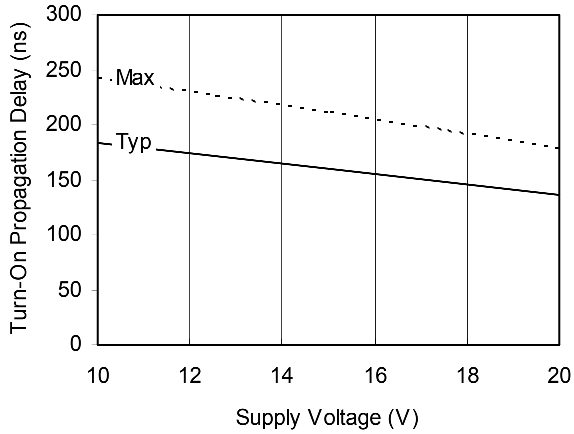


Figure 3B. Turn-On Propagation Delay vs. Supply Voltage

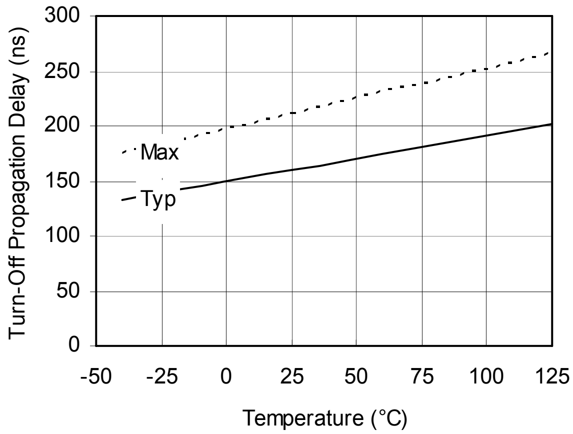


Figure 4A. Turn-Off Propagation Delay vs. Temperature

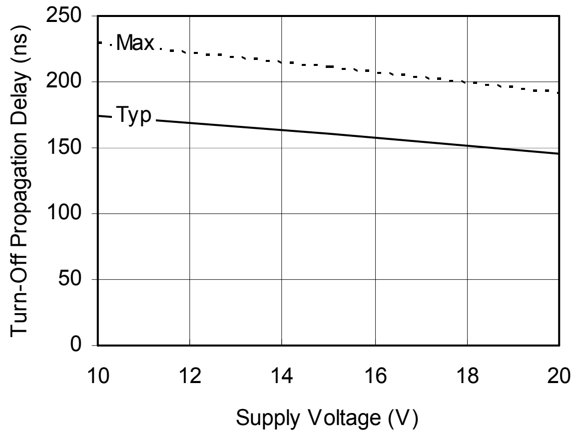


Figure 4B. Turn-Off Propagation Delay vs. Supply Voltage

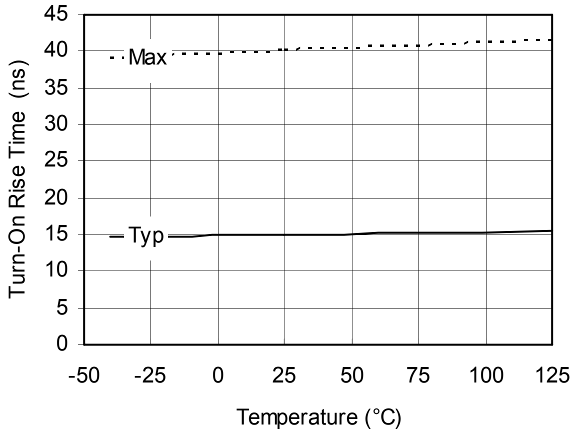


Figure 5A. Turn-On Rise Time vs. Temperature

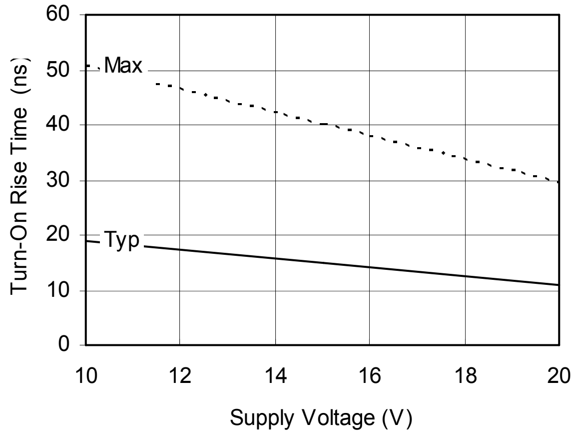


Figure 5B. Turn-On Rise Time vs. Supply Voltage

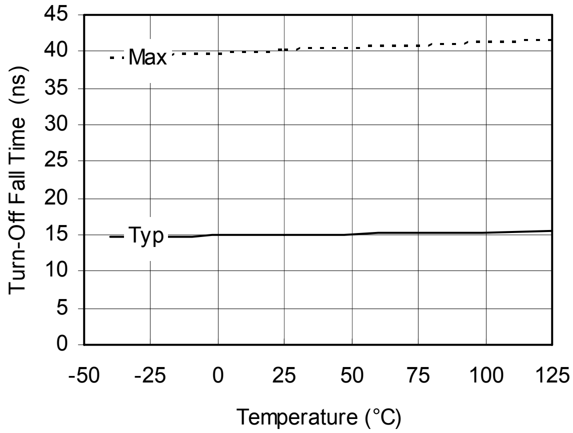


Figure 6A. Turn-Off Fall Time vs. Temperature

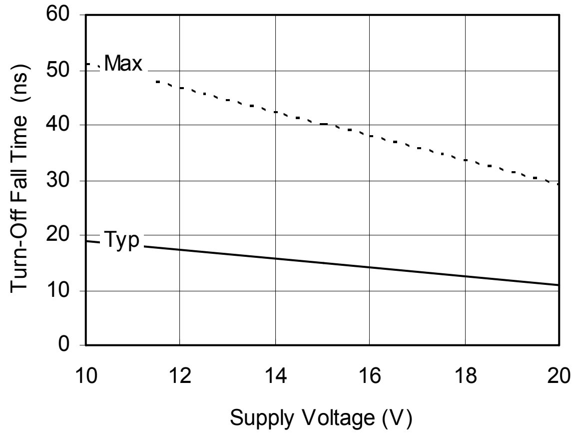


Figure 6B. Turn-Off Fall Time vs. Supply Voltage

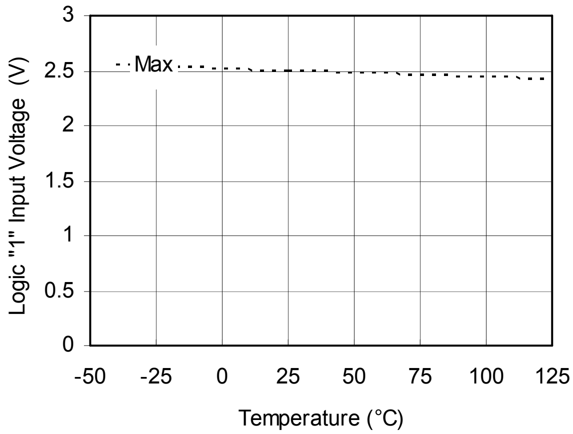


Figure 7A. Logic "1" Input Voltage vs. Temperature

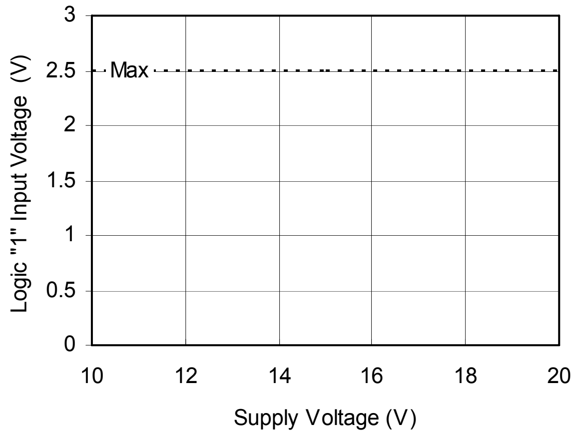


Figure 7B. Logic "1" Input Voltage vs. Supply Voltage

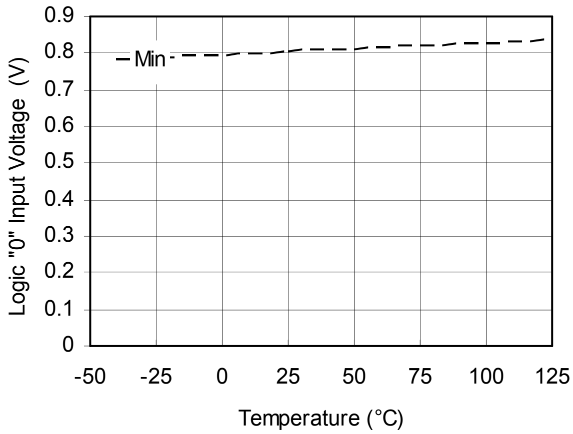


Figure 8A. Logic "0" Input Voltage vs. Temperature

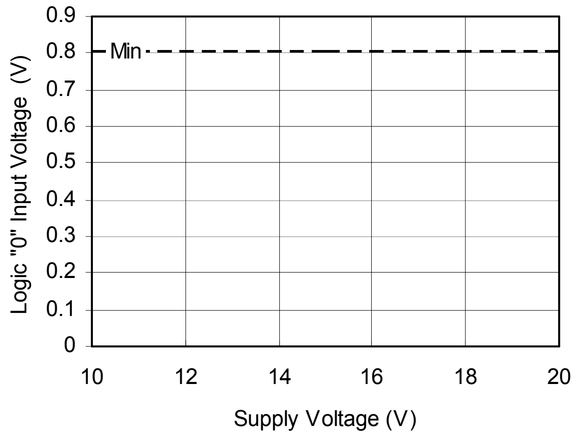


Figure 8B. Logic "0" Input Voltage vs. Supply Voltage

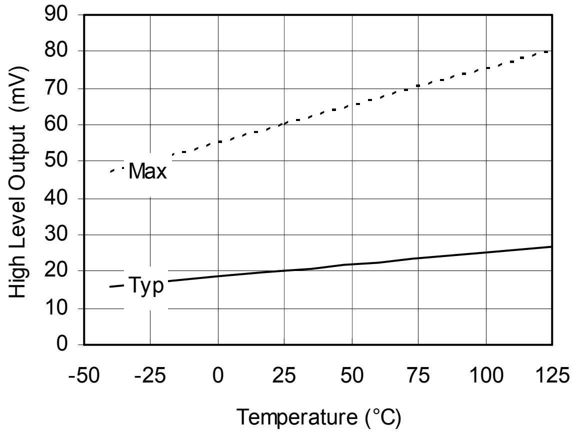


Figure 9A. High Level Output vs. Temperature (Io = 2mA)

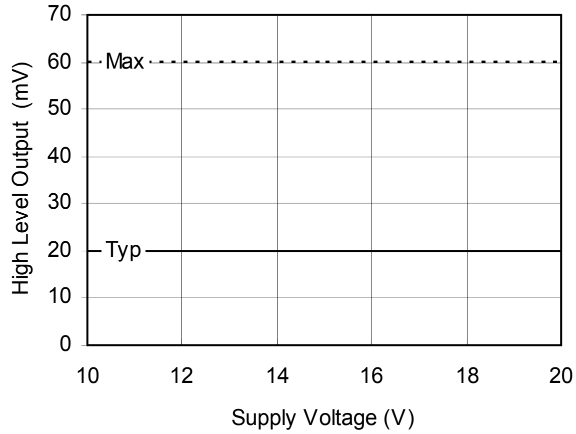


Figure 9B. High Level Output vs. Supply Voltage (Io = 2mA)

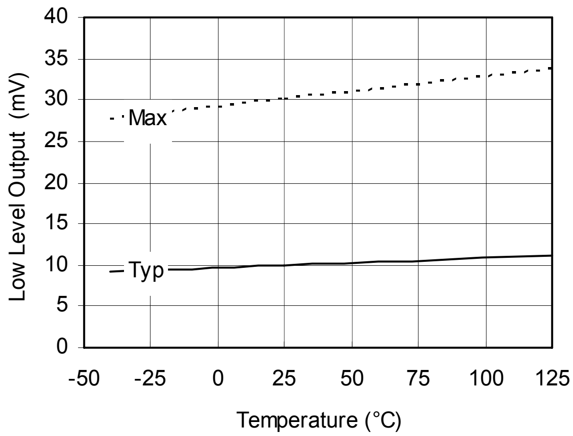


Figure 10A. Low Level Output vs. Temperature (Io = 2mA)

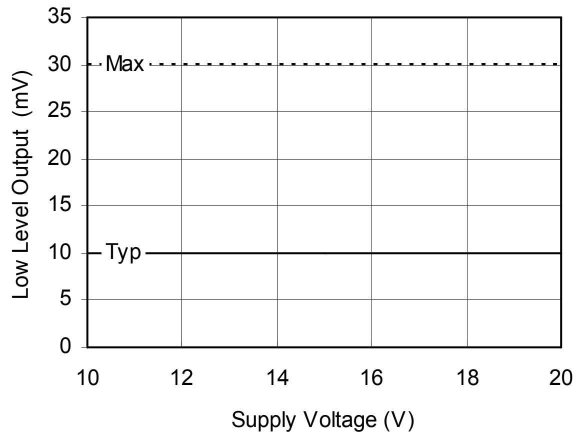


Figure 10B. Low Level Output vs. Supply Voltage (Io = 2mA)

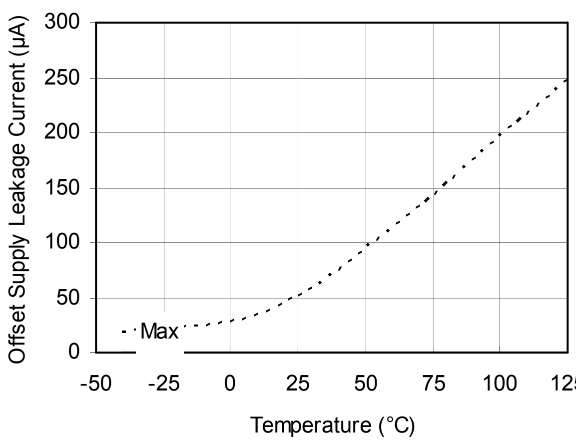


Figure 11A. Offset Supply Leakage Current vs. Temperature

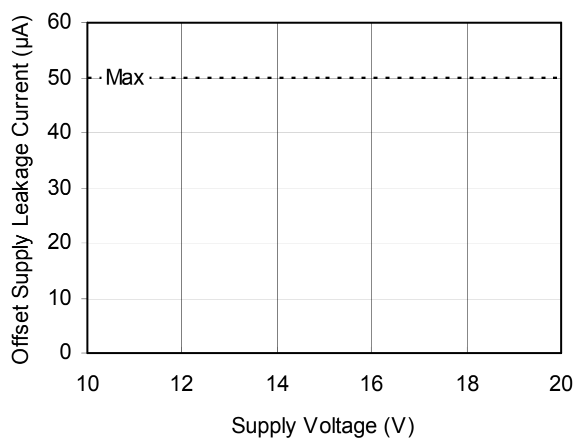


Figure 11B. Offset Supply Leakage Current vs. Supply Voltage

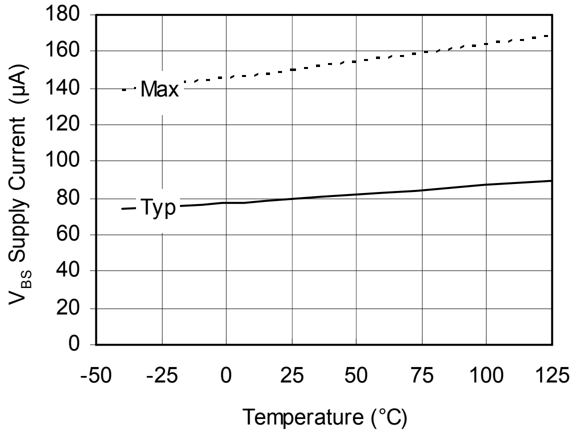


Figure 12A. V_{BS} Supply Current vs. Temperature

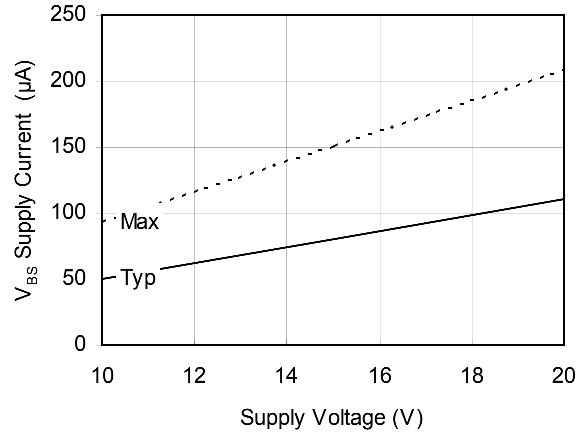


Figure 12B. V_{BS} Supply Current vs. Supply Voltage

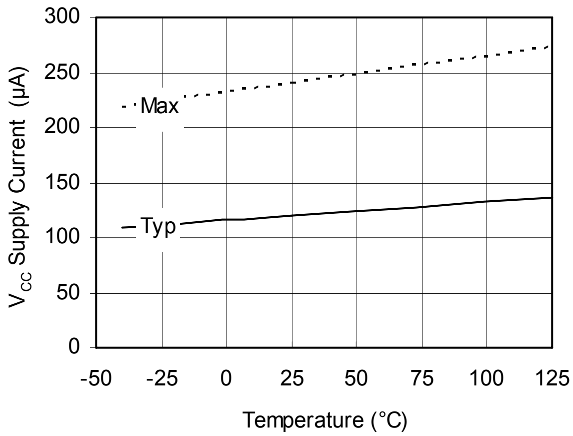


Figure 13A. V_{CC} Supply Current vs. Temperature

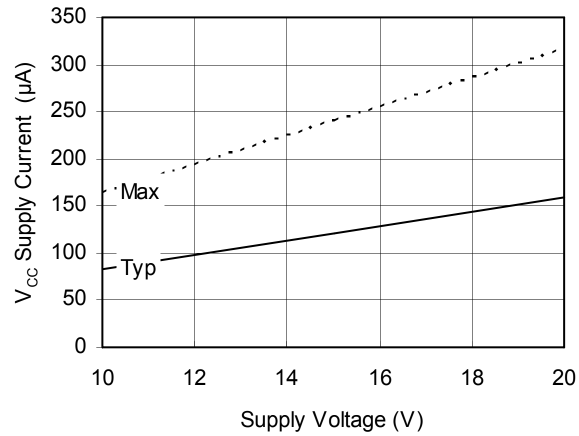


Figure 13B. V_{CC} Supply Current vs. Supply Voltage

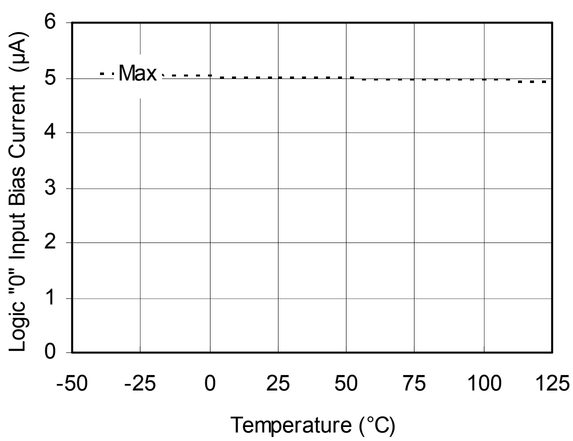


Figure 14A. Logic "0" Input Bias Current vs. Temperature

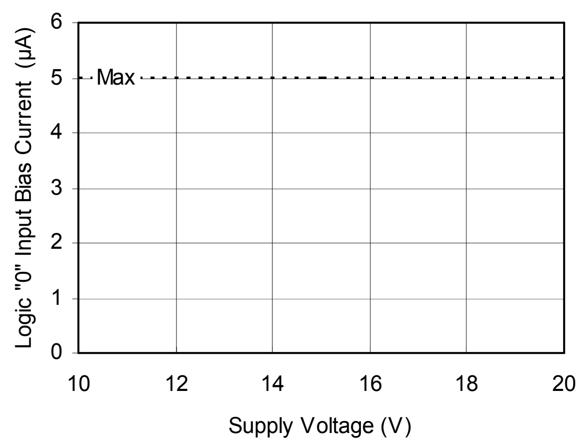


Figure 14B. Logic "0" Input Bias Current vs. Supply Voltage

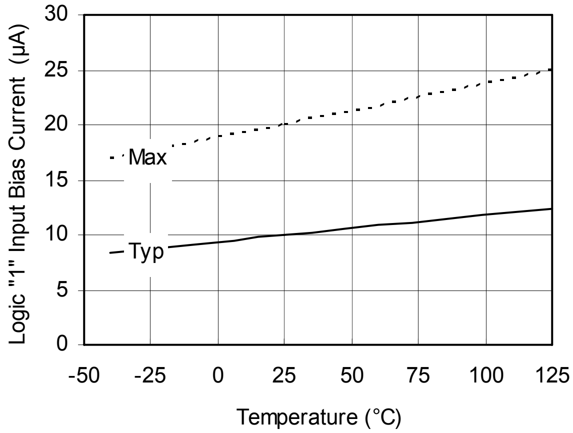


Figure 15A. Logic "1" Input Bias Current vs. Temperature

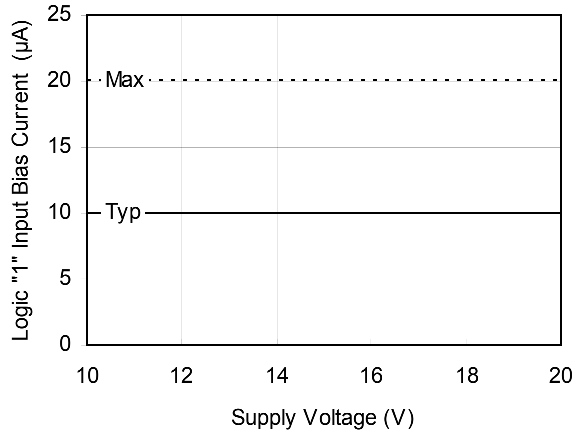


Figure 15B. Logic "1" Input Bias Current vs. Supply Voltage

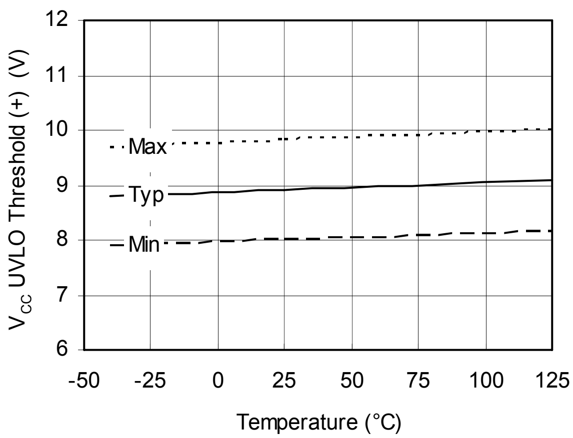


Figure 16. V_{CC} Undervoltage Threshold (+) vs. Temperature

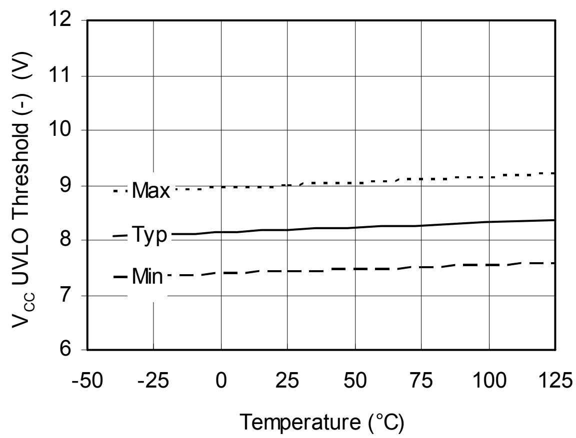


Figure 17. V_{CC} Undervoltage Threshold (-) vs. Temperature

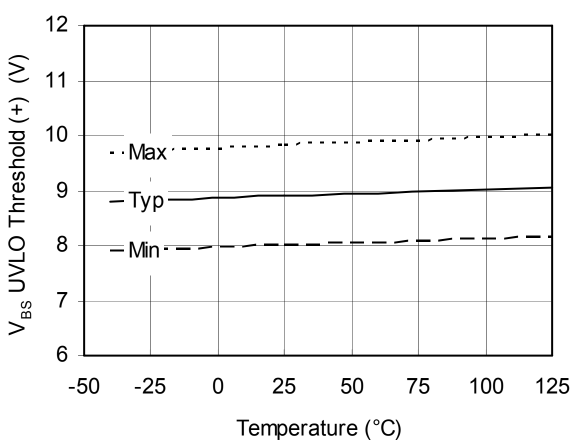


Figure 18. V_{BS} Undervoltage Threshold (+) vs. Temperature

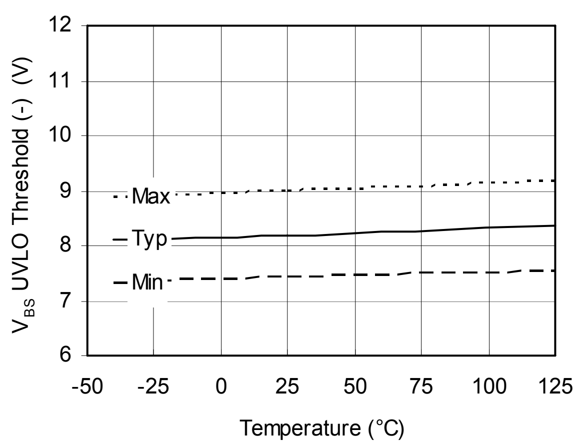


Figure 19. V_{BS} Undervoltage Threshold (-) vs. Temperature

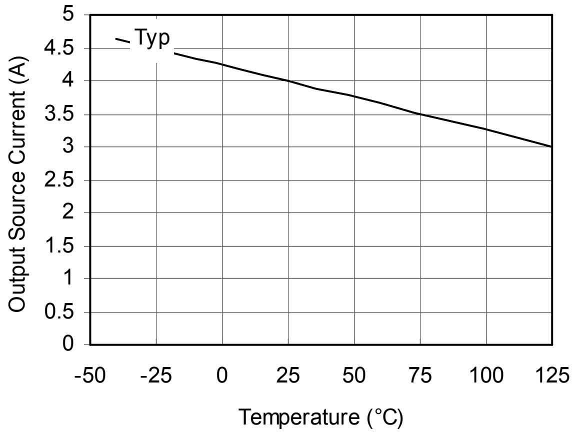


Figure 20A. Output Source Current vs. Temperature

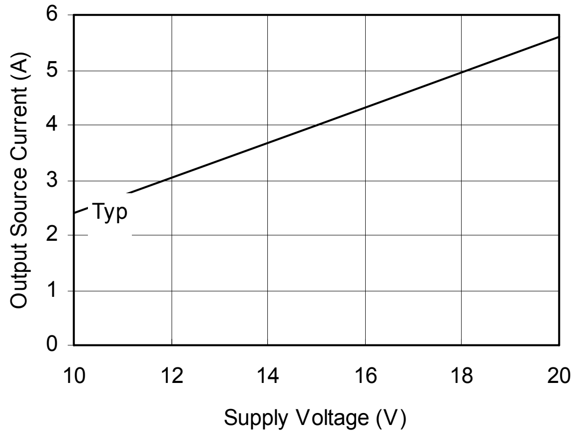


Figure 20B. Output Source Current vs. Supply Voltage

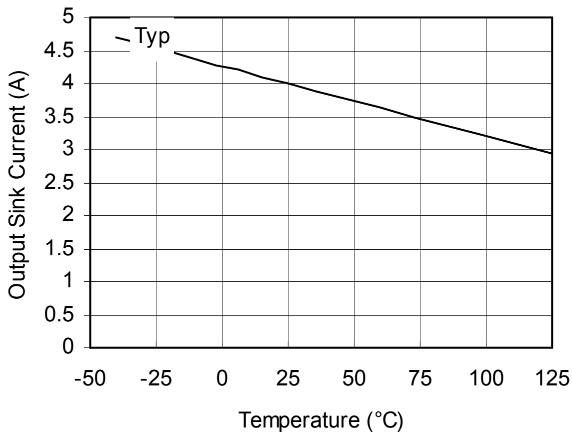


Figure 21A. Output Sink Current vs. Temperature

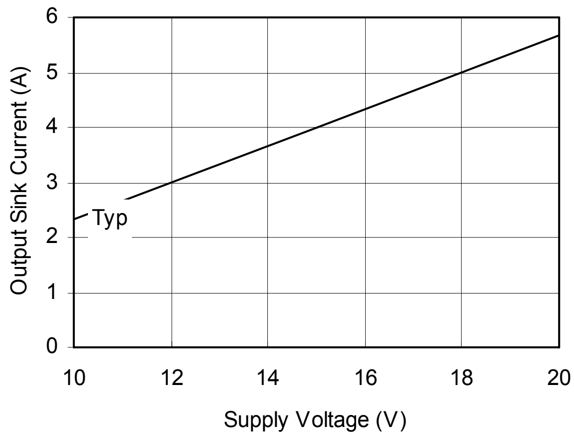
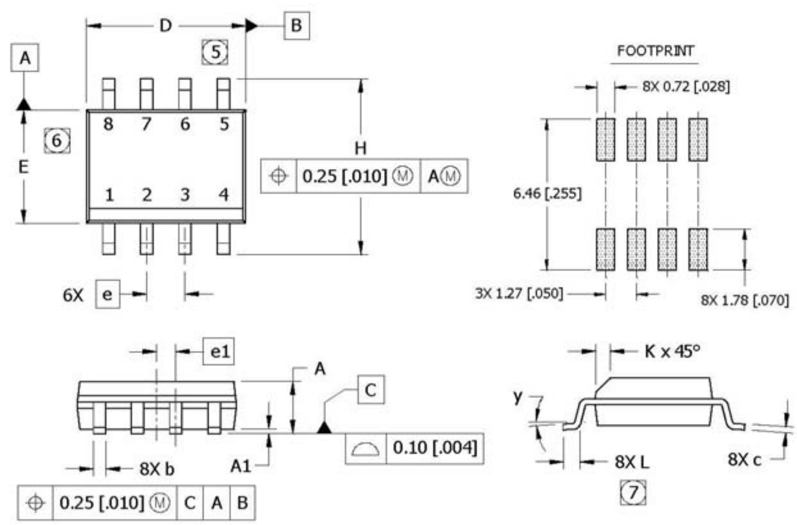


Figure 21B. Output Sink Current vs. Supply Voltage

Package Details, SOIC8N



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

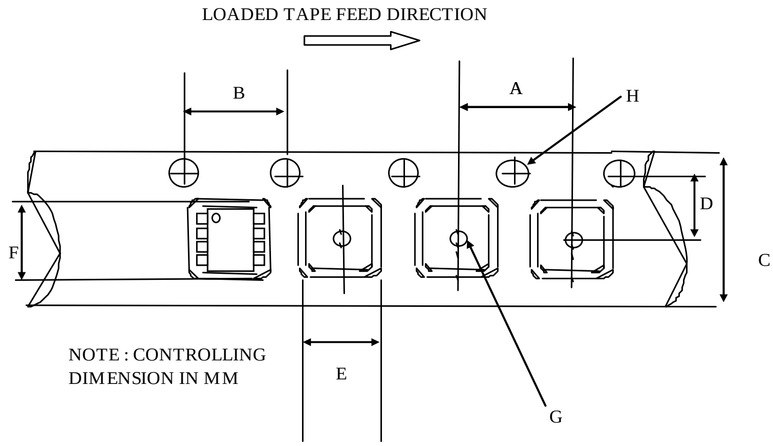
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

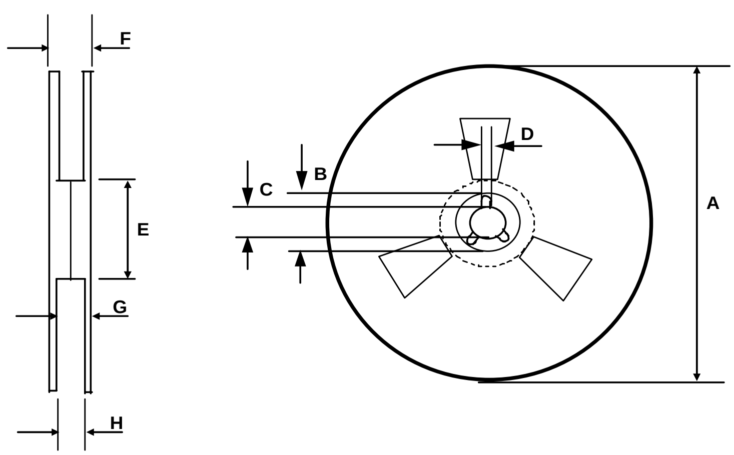
8 Lead SOIC

Package Details: SOIC8N, Tape and Reel



CARRIER TAPE DIMENSION FOR 8SOICN

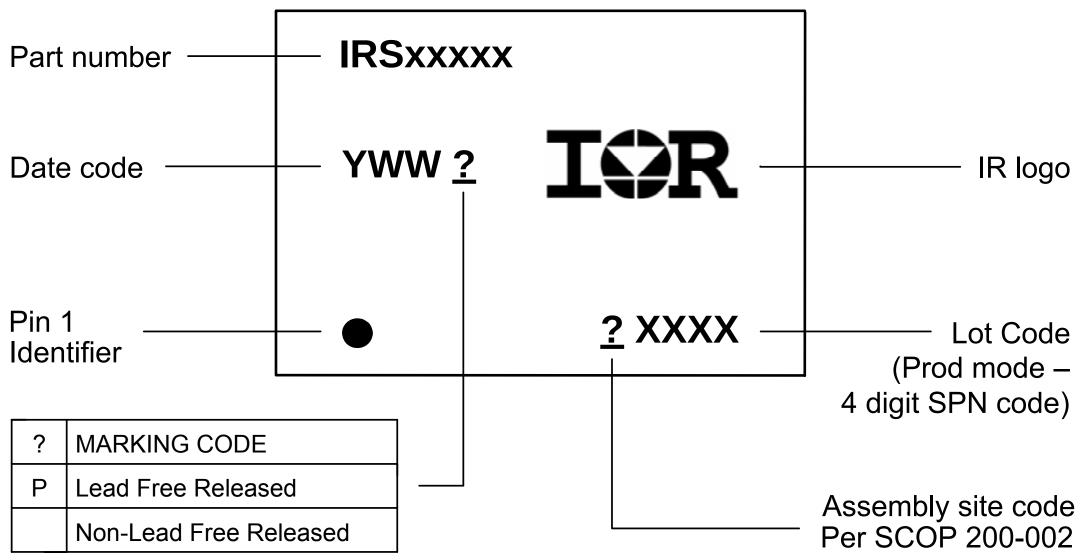
	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS21850SPBF	SOIC8N	Tube/Bulk	95	IRS21850SPBF
		Tape and Reel	2500	IRS21850STRPBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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