# THE DATASHEET OF

# ESD8106MUTAG

# ESD8106

*Product Preview*

# Transient Voltage Suppressors

## Low Capacitance ESD Protection for USB 3.0 Interface

The ESD8106 transient voltage suppressor is specifically designed to protect USB 3.0 interfaces by integrating two Superspeed pairs, D+ and D− lines into a single protection product. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow−through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines.

### Features

- Low Capacitance (0.35 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
  IEC 61000−4−2 Level 4
- UL Flammability Rating of 94 V−0
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- USB 3.0

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Operating Junction Temperature Range | $T_J$ | −55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |
| Lead Solder Temperature − Maximum (10 Seconds) | $T_L$ | 260 | °C |
| IEC 61000−4−2 Contact (ESD)<br>IEC 61000−4−2 Air (ESD) | ESD<br>ESD | ±15<br>±15 | kV<br>kV |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

See Application Note AND8308/D for further description of survivability specs.

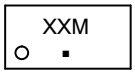
This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

**ON Semiconductor®**

**http://onsemi.com**


**UDFN14**
**CASE 517CQ**

**MARKING DIAGRAM**




XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| ESD8106MUTAG | UDFN14 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

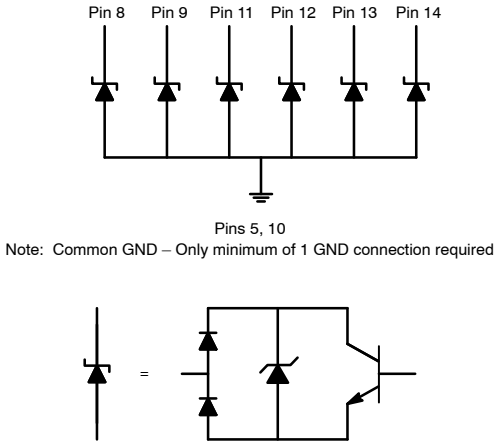



**Figure 1. Pin Schematic**

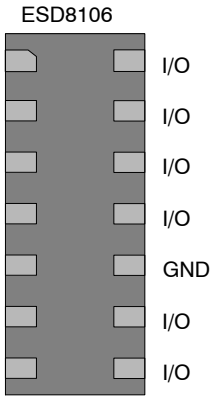



**Figure 2. Pin Configuration**

Note: Pins 5, 10 are connected internally as a common ground.

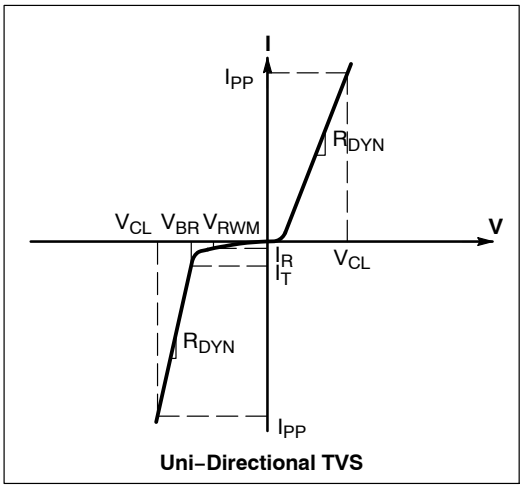
Pins 1, 2, 3, 4, 6, and 7 are not internally connected but should be connected to the opposite pin with PCB trace in order to maintain a flow through routing scheme.

## ELECTRICAL CHARACTERISTICS

($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter |
|---|---|
| $I_{PP}$ | Maximum Peak Pulse Current |
| $V_C$ | Clamping Voltage @ $I_{PP}$ |
| $V_{RWM}$ | Working Peak Reverse Voltage |
| $I_R$ | Maximum Reverse Leakage Current @ $V_{RWM}$ |
| $V_{BR}$ | Breakdown Voltage @ $I_T$ |
| $I_T$ | Test Current |
| $R_{DYN}$ | Dynamic Resistance |

*See Application Note AND8308/D for detailed explanations of datasheet parameters.




**Uni−Directional TVS**

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Reverse Working Voltage | $V_{RWM}$ | I/O Pin to GND | | | 3.3 | V |
| Breakdown Voltage | $V_{BR}$ | $I_T$ = 1 mA, I/O Pin to GND | 4.0 | 5.0 | | V |
| Reverse Leakage Current | $I_R$ | $V_{RWM}$ = 3.3 V, I/O Pin to GND | | | 1.0 | μA |
| Clamping Voltage (Note 1) | $V_C$ | IEC61000−4−2, ±8 kV Contact | See Figures 3 and 4 | | | V |
| Clamping Voltage TLP (Note 2) See Figures 7 through 10 | $V_C$ | $I_{PP}$ = 8 A, $I_{PP}$ = −8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±4 kV Air) | | 8.5<br>−4.5 | | V |
| | | $I_{PP}$ = 16 A, $I_{PP}$ = −16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±15 kV Air) | | 11.4<br>−8.0 | | |
| Dynamic Resistance | $R_{DYN}$ | I/O Pin to GND<br>GND to I/O Pin | | 0.36<br>0.44 | | Ω |
| Junction Capacitance | $C_J$ | $V_R$ = 0 V, f = 1 MHz between I/O Pins and GND<br>$V_R$ = 0 V, f = 1 MHz between I/O Pins<br>$V_R$ = 0 V, f = 1 MHz, $T_A$ = 65°C between I/O Pins and GND | | 0.30<br>0.15<br>0.37 | 0.35<br>0.20<br>0.45 | pF |

1. For test procedure see Figures 5 and 6 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 4 ns, averaging window; $t_1$ = 30 ns to $t_2$ = 60 ns.

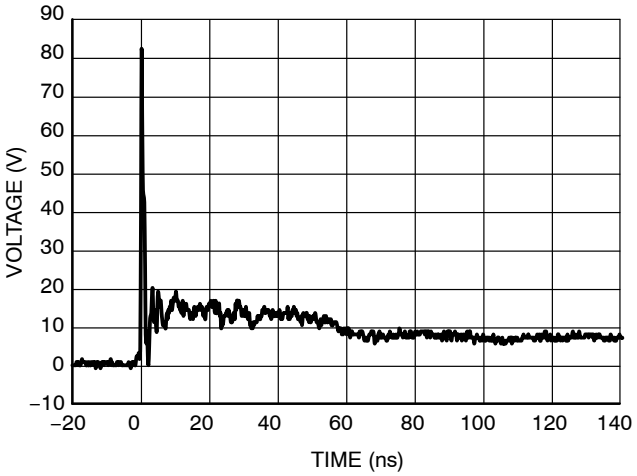



**Figure 3. IEC61000−4−2 +8 kV Contact Clamping Voltage**

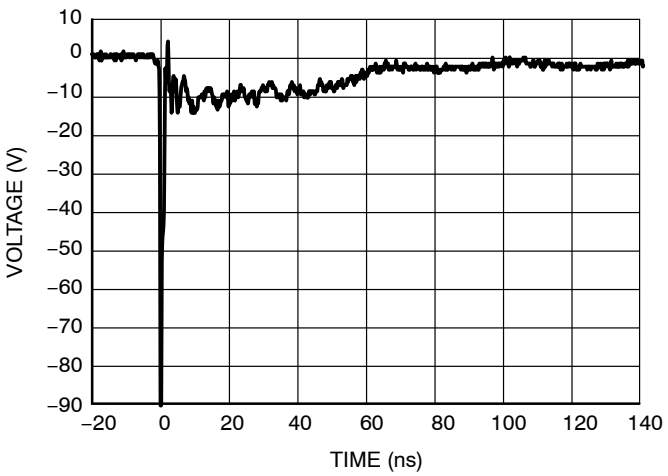



**Figure 4. IEC61000−4−2 −8 kV Contact Clamping Voltage**

**IEC 61000−4−2 Spec.**

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|---|---|---|---|---|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

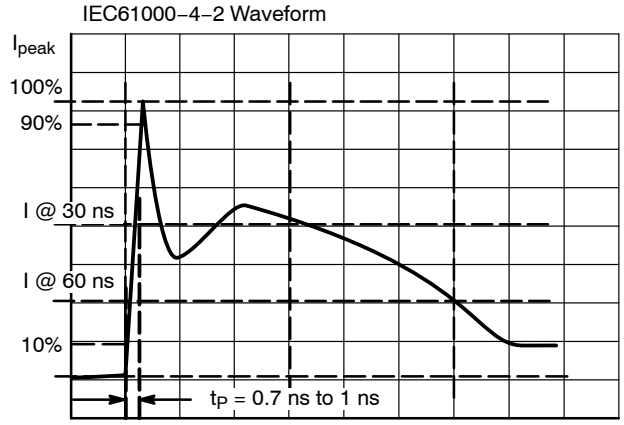



**Figure 5. IEC61000−4−2 Spec**

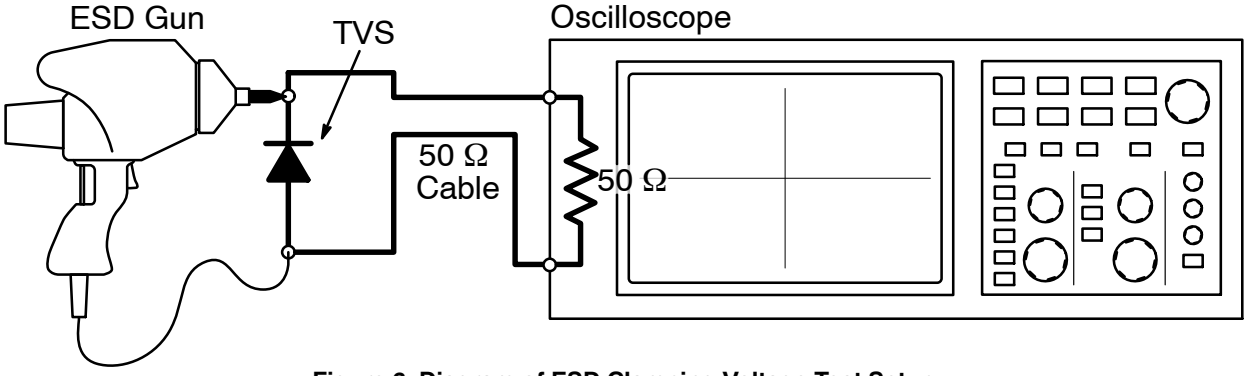



**Figure 6. Diagram of ESD Clamping Voltage Test Setup**

**The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.**

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

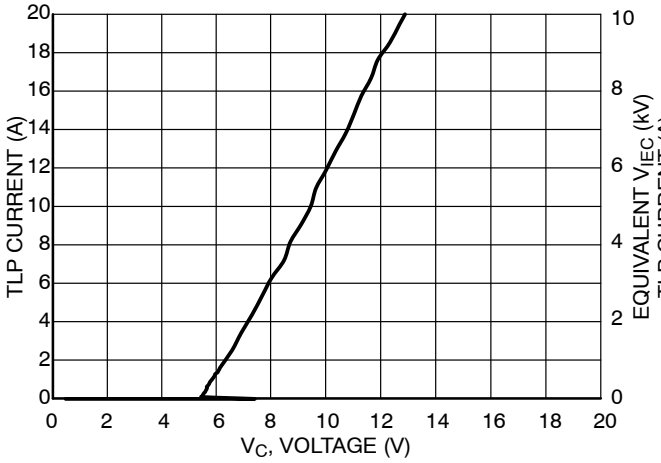



**Figure 7. Positive TLP I−V Curve**

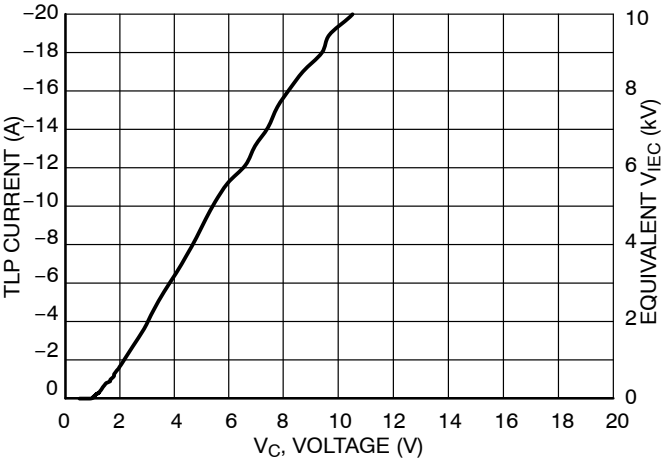



**Figure 8. Negative TLP I−V Curve**

NOTE: TLP parameter: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 300 ps, averaging window: $t_1$ = 30 ns to $t_2$ = 60 ns. $V_{IEC}$ is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000−4−2 waveform at t = 30 ns with 2 A/kV. See TLP description below for more information.

### Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 9. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 10 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

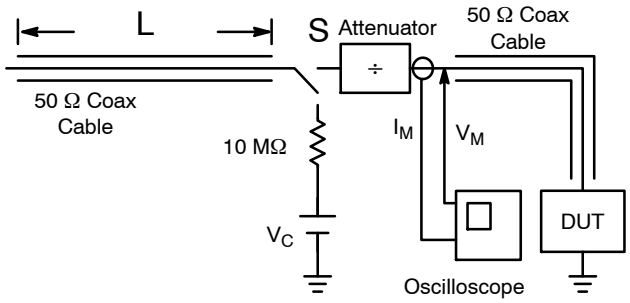



**Figure 9. Simplified Schematic of a Typical TLP System**

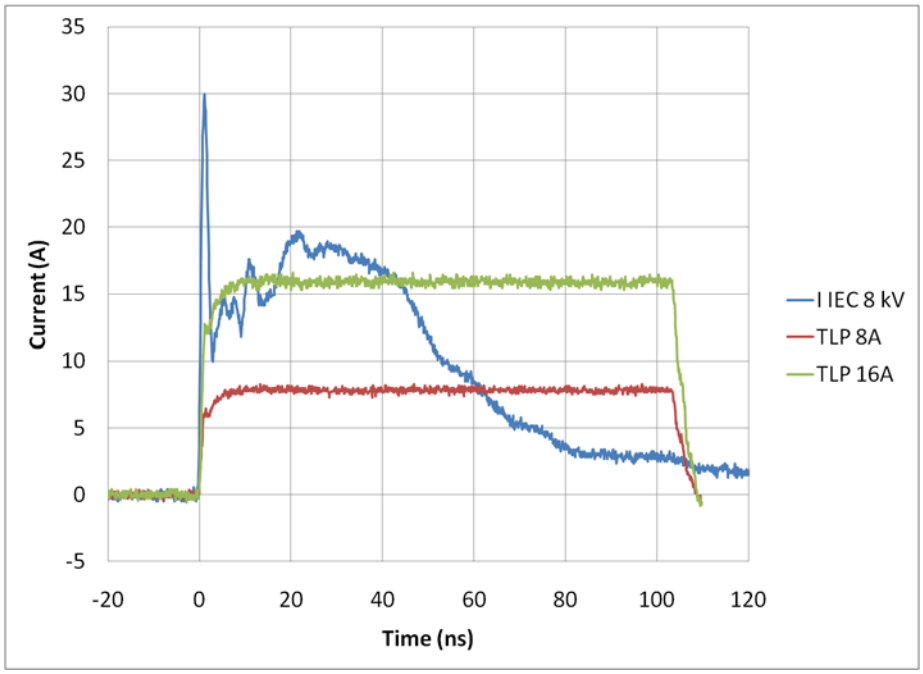



**Figure 10. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms**

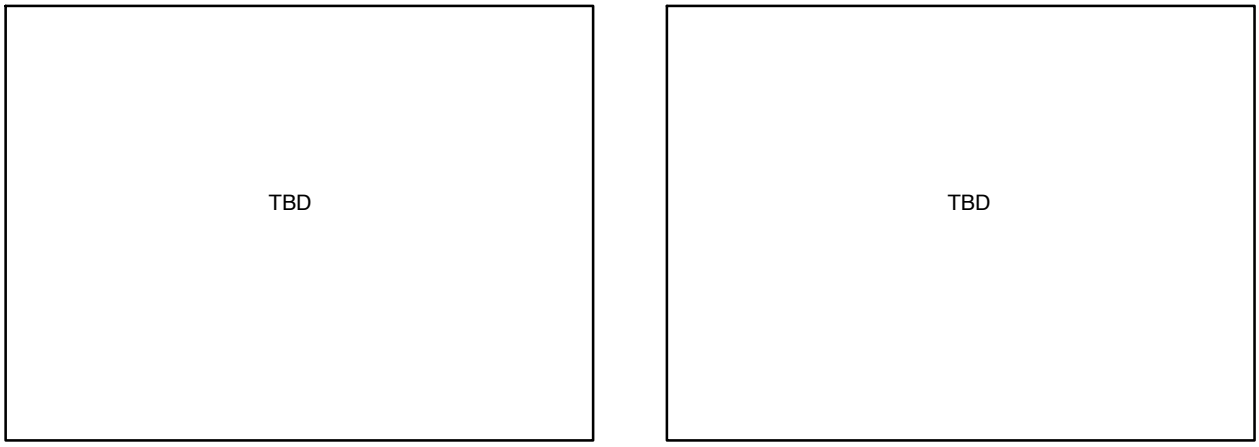
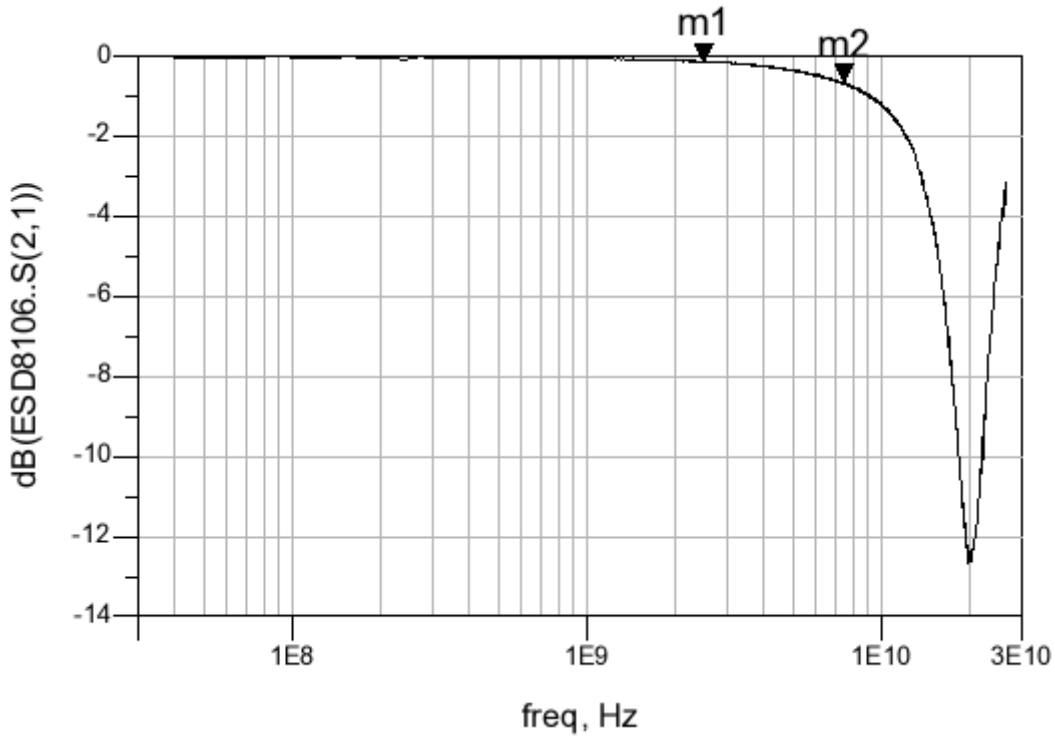



**Figure 11. USB 3.0 Eye Diagram with and without ESD8106. 5.0 Gb/s, 400 $mV_{PP}$**




| Interface | Data Rate (Gb/s) | Fundamental Frequency (GHz) | 3rd Harmonic Frequency (GHz) | ESD8106 Insertion Loss (dB) |
|---|---|---|---|---|
| USB 3.0 | 5 | 2.5 (m1) | 7.5 (m2) | m1 = 0.128<br>m2 = 0.659 |

**Figure 12. ESD8106 Insertion Loss**

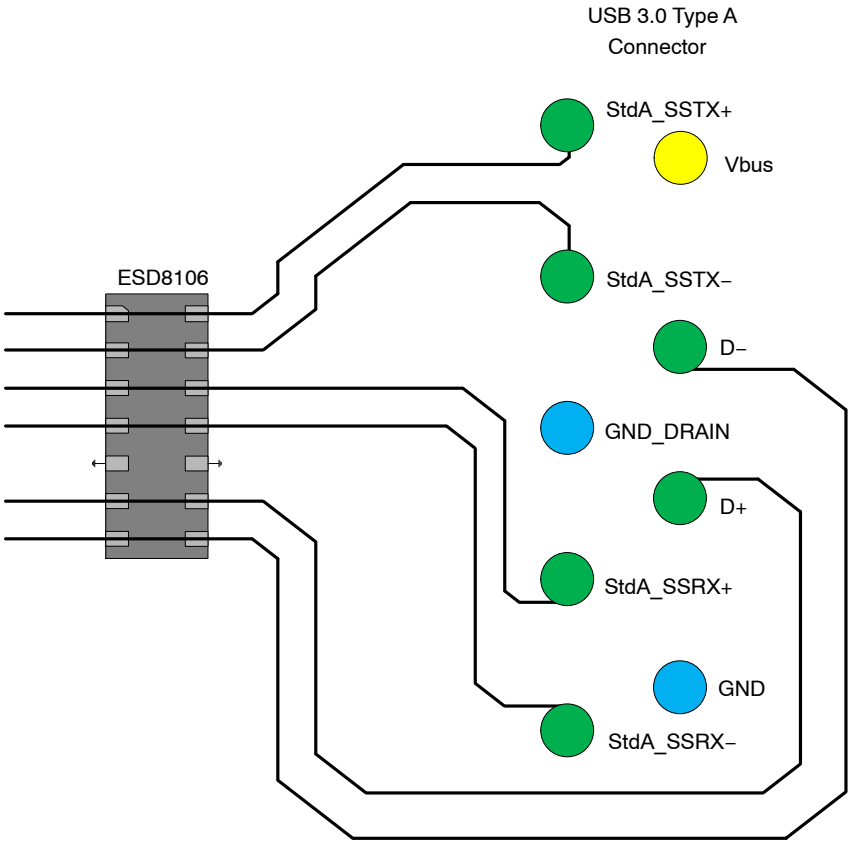



**Figure 13. USB 3.0 Layout Diagram**

### PCB Layout Guidelines

Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

- Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.
  - In USB 3.0 applications, the ESD protection device should be placed between the AC coupling capacitors and the I/O connector on the TX differential lanes as shown in Figure 14.
- Make sure to use differential design methodology and impedance matching of all high speed signal traces.
  - Use curved traces when possible to avoid unwanted reflections.
  - Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.
  - Place grounds between high speed pairs and keep as much distance between pairs as possible to reduce crosstalk.

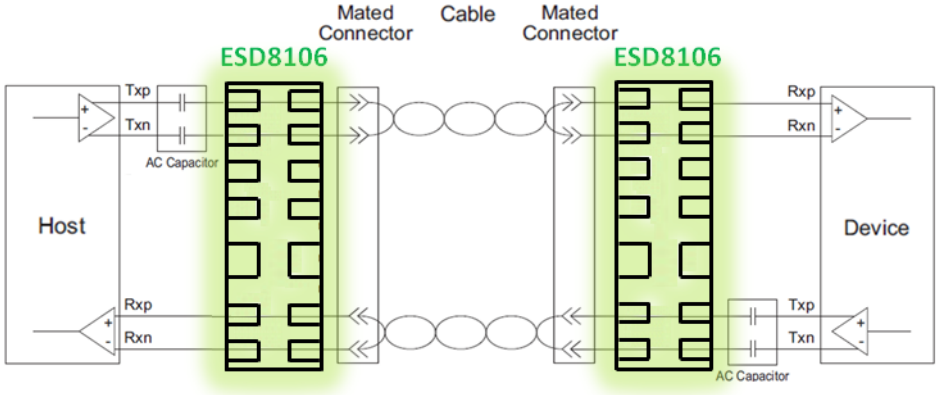



**Figure 14. USB 3.0 Connection Diagram**

### ESD Protection Device Technology

ON Semiconductor's portfolio contains three main technologies for low capacitance ESD protection device which are highlighted below and in Figure 15.

- ESD7000 series: Zener diode based technology. This technology has a higher breakdown voltage (VBR) limiting it to protecting chipsets with larger geometries.
- ESD8000 series: Silicon controlled rectifier (SCR) type technology. The key advatange for this technology is a low holding voltage (VH) which produces a deeper snapback that results in lower voltage over high currents as shown in the TLP results in Figure 16. This technology provides optimized protection for chipsets with small geometries against thermal failures resulting in chipset damage (also known as "hard failures").
- ESD8100 series: Low voltage punch through (LVPT) technology. The key advatange for this technology is a very low turn-on voltage as shown in Figure 17. This technology provides optimized protection for chipsets with small geometries against recoverable failures due to voltage peaks (also known as "soft failures").

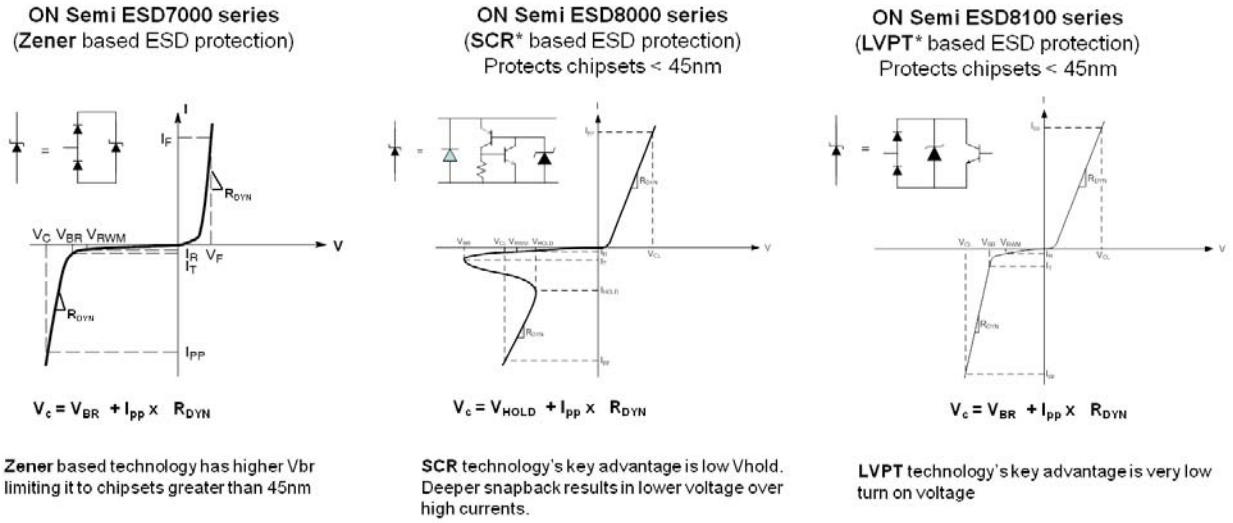



**Figure 15. ON Semiconductor's Low-cap ESD Technology Portfolio**

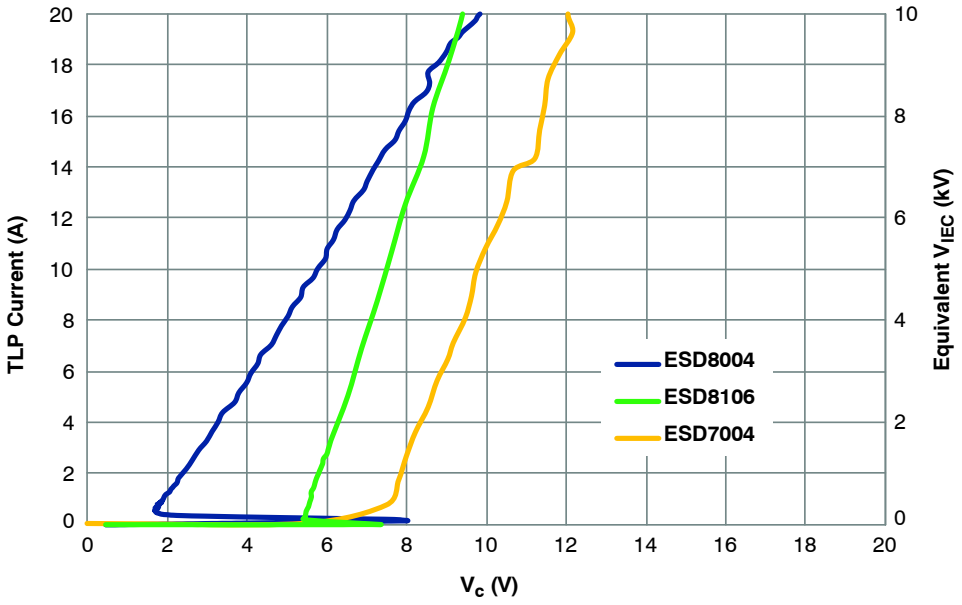



**Figure 16. High Current, TLP, IV Characteristic of Each Technology**

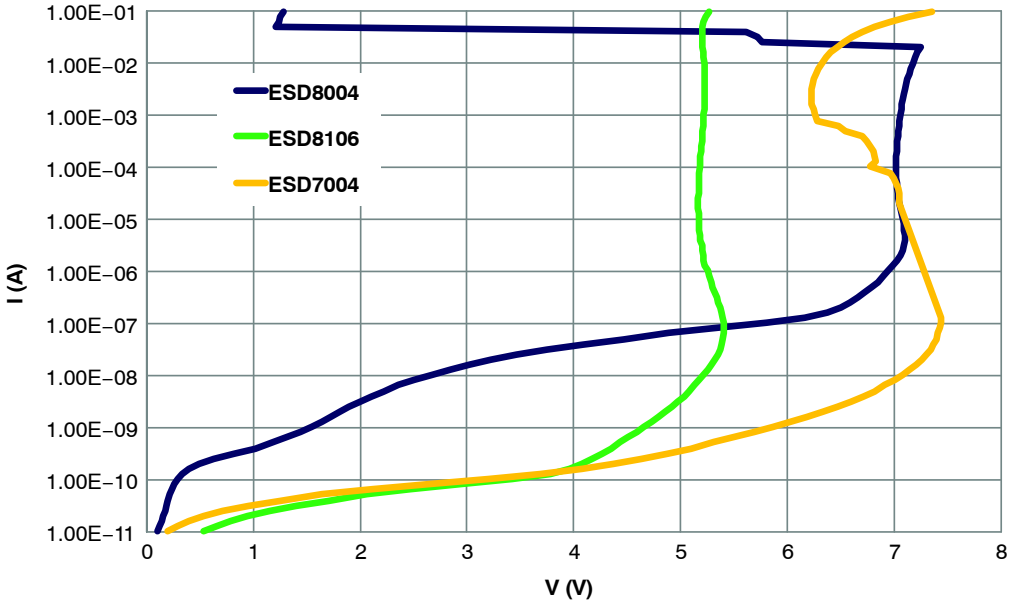
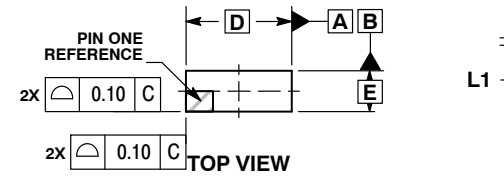


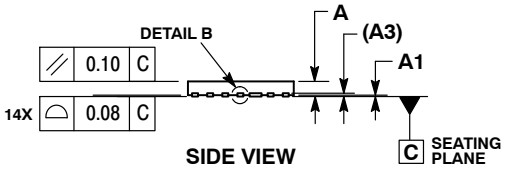

**Figure 17. Low Current, DC, IV Characteristic of Each Technology**

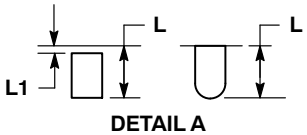
# ESD8106

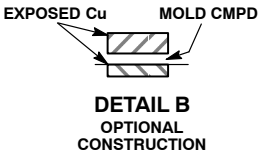
## PACKAGE DIMENSIONS

**UDFN14, 3.5x1.35, 0.5P**
CASE 517CQ
ISSUE O



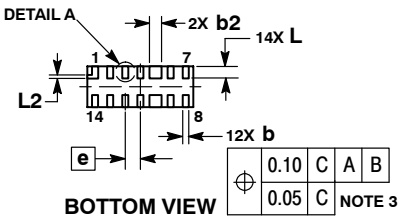



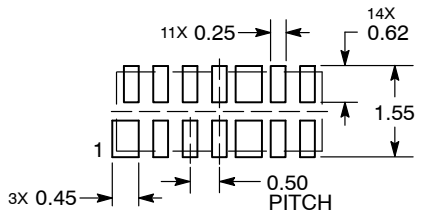




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.13 REF | |
| b | 0.15 | 0.25 |
| b2 | 0.35 | 0.45 |
| D | 3.50 BSC | |
| E | 1.35 BSC | |
| e | 0.50 BSC | |
| L | 0.30 | 0.50 |
| L1 | 0.00 | 0.15 |
| L2 | 0.20 REF | |




### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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