

iceLynx-Micro IEEE 1394a-2000 Consumer Electronics Solution

FEATURES

- **1394 Features**
 - Integrated 400 Mbps 3-port PHY
 - Compliant with IEEE 1394-1995 and IEEE 1394a-2000 standards
 - Supports bus manager functions and automatic 1394 self-ID verification.
 - Separate Async Ack FIFO decreases the ack-tracking burden on in-CPU and ex-CPU
- **DTLA Encryption Support for MPEG2-DVB, DSS, DV, and Audio (TSB43CA43A and TSB43CA42 Only)**
 - Two M6 baseline ciphers (one per HSDI port)
 - Content key generation from exchange key
 - AKE acceleration features in hardware
 - Random Number Generator
 - Secure Hash Algorithm, Revision 1 (SHA-1)
 - Other AKE acceleration features
 - Elliptical curve digital signature algorithm (EC-DCA) both signature and verification
 - Elliptical curve Diffie-Hellman (EC-DH), first phase value and shared secret calculation
 - 160-bit math functions
- **High Speed Data Interface (HSDI)**
 - Two configurable high speed data interfaces support the following audio and video modes:
 - MPEG2-DVB interface
 - MPEG2-DSS interface
 - DV codec interface
 - IEC60958 interface
 - Audio DAC interface
 - SACD interface
- **External CPU Interface**
 - 16-bit parallel asynchronous I/O-type
 - 16-bit parallel synchronous I/O-type
 - 16-bit parallel synchronous memory type
- **Internal ARM7**
 - 50-MHz operating frequency
 - 32-bit and thumb (16-bit) mode support
 - UART included for communication
 - 256K bytes of program memory included on chip
 - ARM JTAG included for software debug
- **Data Buffers**
 - Large 16.5K byte total FIFO
 - Programmable data/space available indicators for buffer flow control
- **Hardware Packet Formatting for the Following Standards**
 - DVB MPEG2 transport stream (IEC61883-4)
 - DSS MPEG2 transport stream per standard
 - DV Stream (IEC 61883-2) SD-DV
 - Audio over 1394 (IEC 61883-6)
 - Audio Music Protocol (version 1.0 and enhancements)
 - Asynchronous and asynchronous stream (as defined by IEEE 1394)
- **Additional Features**
 - PID filtering for transmit function (up to 16 separate PIDs per HSDI)
 - Packet insertion – two insertion buffers per HSDI
 - 11 general-purpose inputs/outputs (GPIOs)
 - Interrupt driven to minimize CPU polling.
 - Single 3.3-V supply
 - JTAG interface to support post-assembly scan of device I/O – boundary scan



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DESCRIPTION

The iceLynx-Micro (consumer electronics link with integrated microcontroller and physical layer (PHY)) is a high performance 1394 link-layer device designed as a total solution for digitally interfacing advanced audio/video consumer electronics applications. The device is offered in both a DTCP encryption/decryption version (TSB43CA43A and TSB43CA42) and a non-DTCP encryption/decryption version (TSB43CB43).

In addition to supporting transmit and receive of MPEG2 and DSS formatted transport streams with encryption and decryption, the iceLynx-Micro supports the IEC 61883-6 and audio music protocol standards for audio format and packetizing and asynchronous and asynchronous stream (as defined by 1394).

The device also features an embedded ARM7TDMI microprocessor core with access to 256K bytes of internal program memory. The ARM7 is embedded to process 1394 specific transactions, thus significantly reducing the processing power required by the host CPU and the development time required by the user. The ARM7 is accessed from the 16/1-bit host CPU interface, from a UART communication port, or from a JTAG debug port.

The iceLynx-Micro integrated 3-port PHY allows the user enhanced flexibility as two additional devices can be utilized in a system application. The PHY's speeds are capable of running at 100 Mbps, 200 Mbps, or 400 Mbps. The PHY follows all requirements as stated in the IEEE 1394-1995 and IEEE 1394a-2000 standards.

The TSB43CA43A and TSB43CA42 version of iceLynx-Micro incorporates two M6 baseline ciphers (one per HSDI port) per the 5C specification to support transmit and receive of MPEG2 formatted transport streams with encryption and decryption. The TSB43CB43 version of iceLynx-Micro is identical to the TSB43CA43A without implementation of the encryption/decryption features. The TSB43CB43 device allows customers that do not require the encryption/decryption features to incorporate iceLynx-Micro without becoming DTLA licensees. Both devices support the IEC 61883-6 and audio music protocol standards for audio format and packetizing.

NOTE:

This product is for high-volume CE applications only. For a complete datasheet or more information contact support@ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSB43CA42ZGW	ACTIVE	BGA MICROSTAR	ZGW	176	126	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-20 to 70	TSB43CA42Z	Samples
TSB43CB43APGF	ACTIVE	LQFP	PGF	176	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 70	TSB43CB43A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

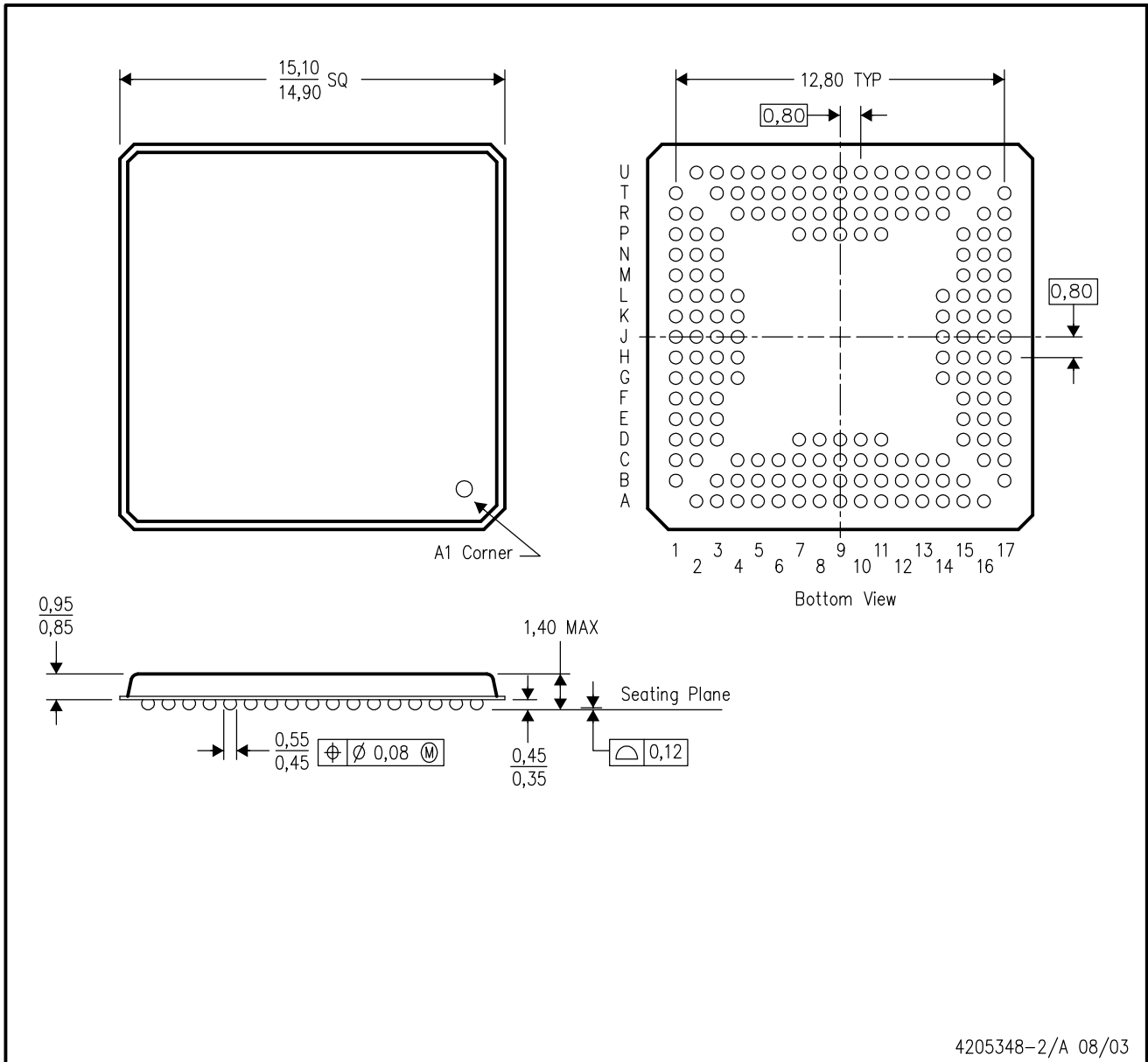
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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ZGW (S-PBGA-N176)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar BGA™ configuration
 - D. This package is lead-free.

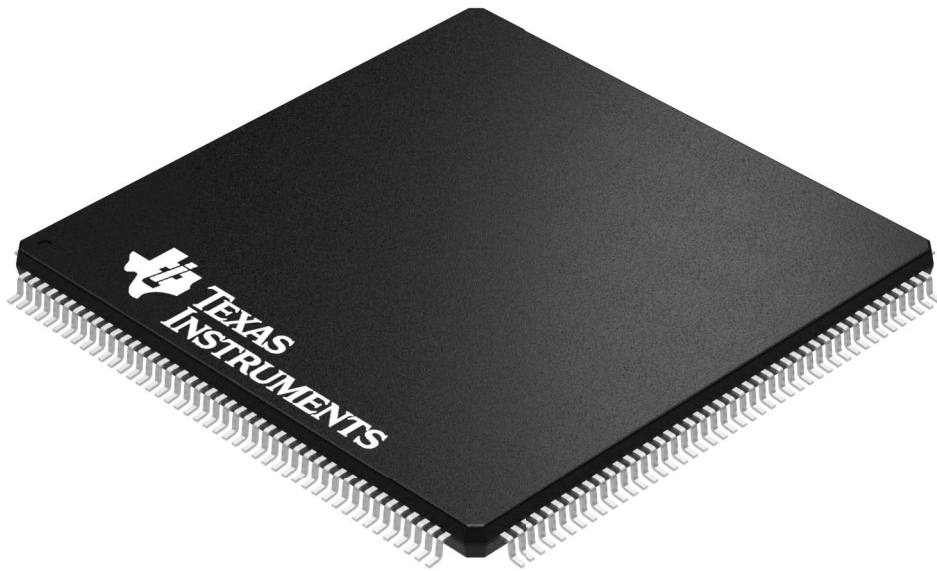
MicroStar BGA is a trademark of Texas Instruments.

GENERIC PACKAGE VIEW

PGF 176

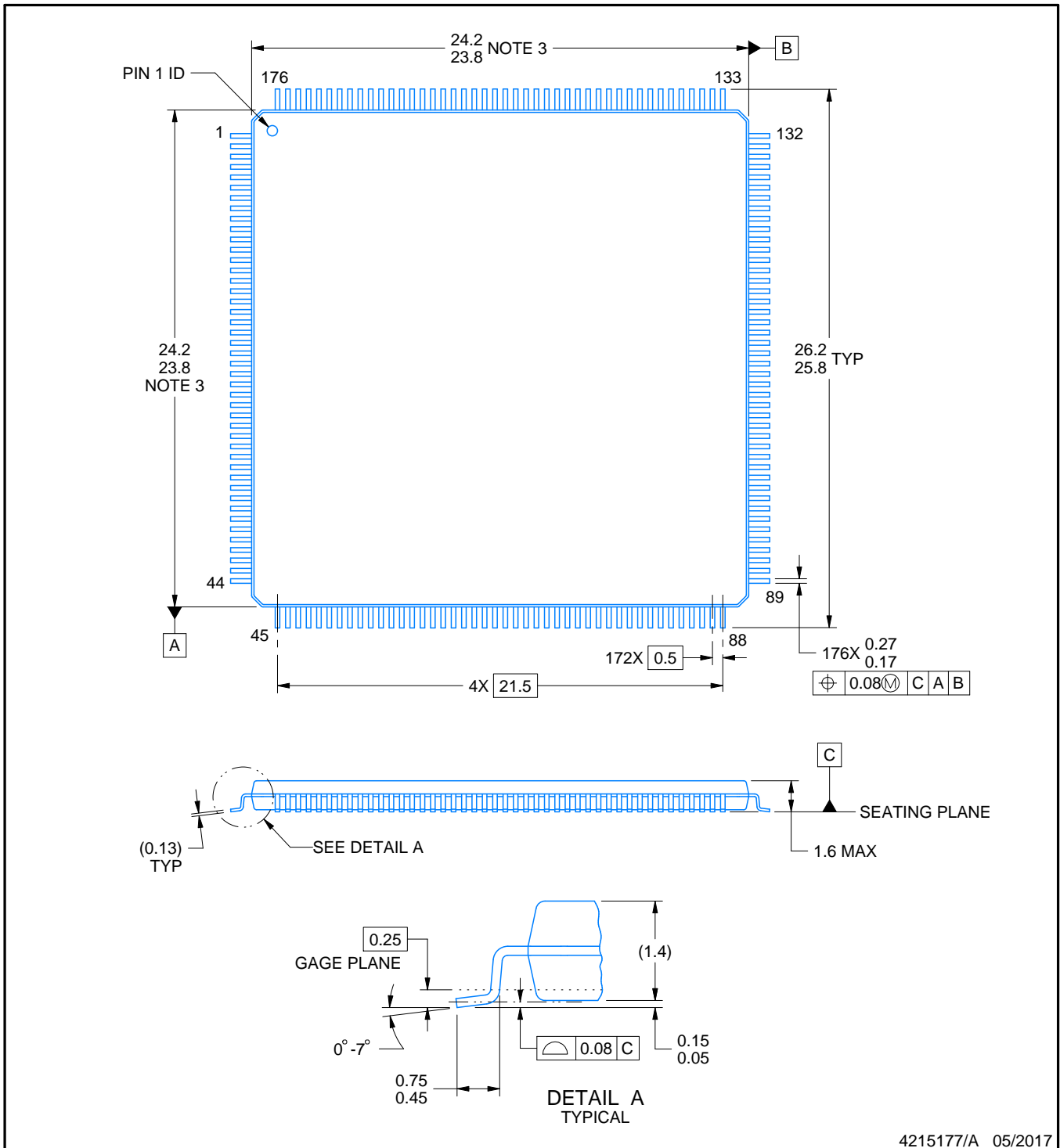
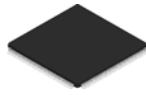
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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NOTES:

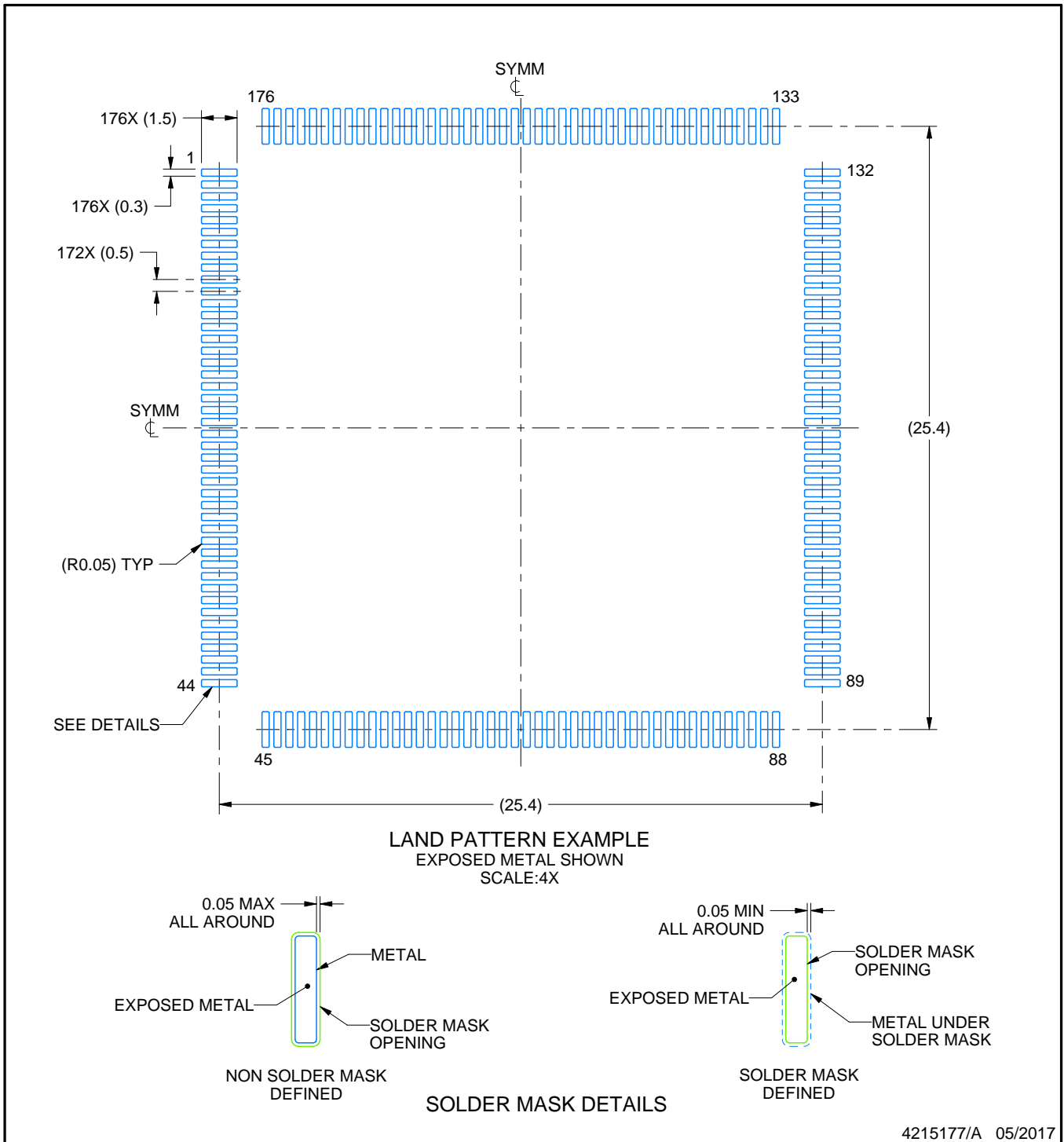
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

PGF0176A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

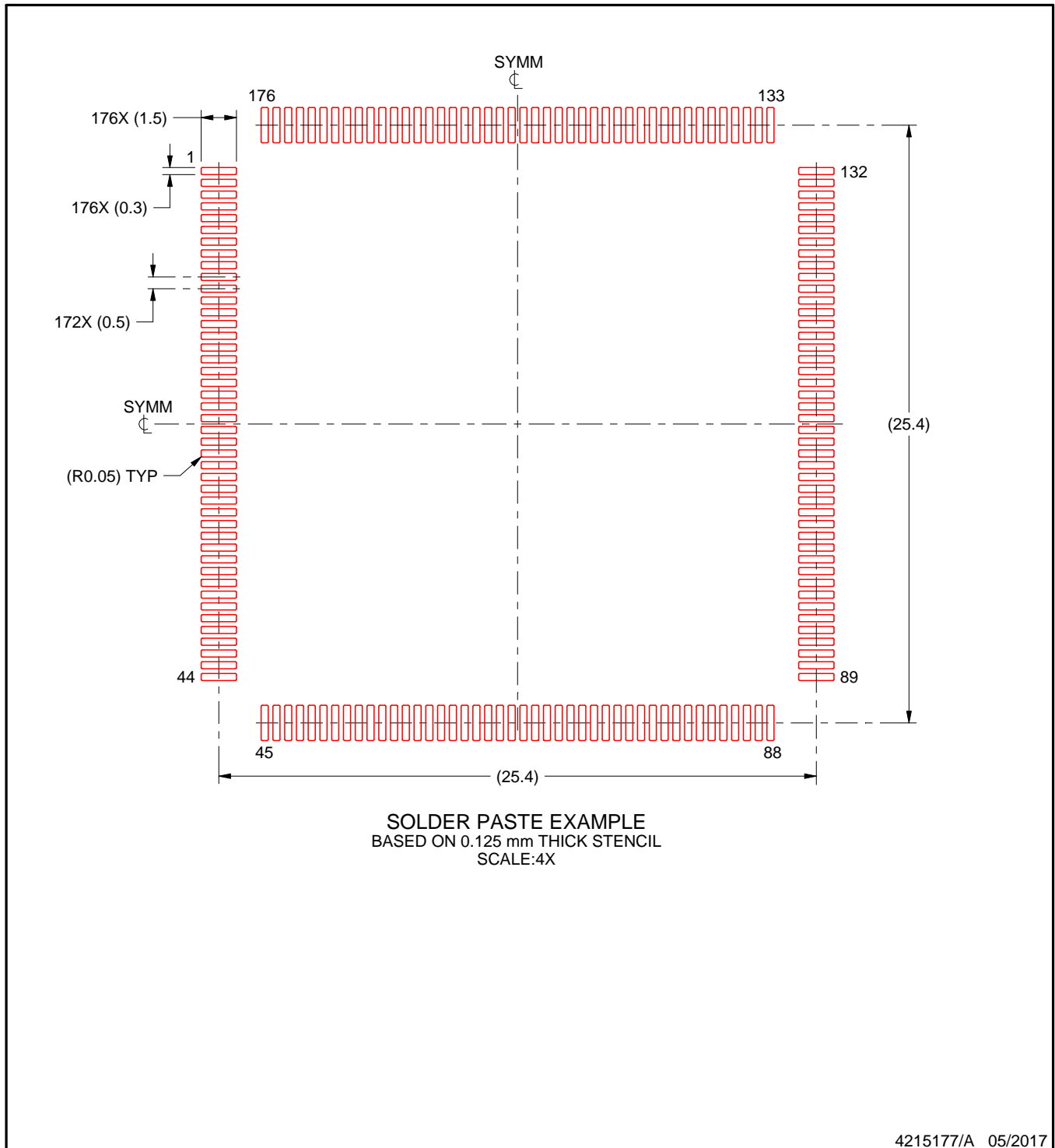
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PGF0176A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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