



**THE DATASHEET OF
TLC2254CDRG4**



TLC225x, TLC225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS176D – FEBRUARY 1997 – REVISED MARCH 2001

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Very Low Power . . . 35 μA Per Channel Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage**
850 μV Max at T_A = 25°C (TLC225xA)
- **Macromodel Included**
- **Performance Upgrades for the TS27L2/L4 and TLC27L2/L4**
- **Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards**

description

The TLC2252 and TLC2254 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC225x family consumes only 35 μA of supply current per channel. This micropower operation makes them good choices for battery-powered applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Looking at Figure 1, the TLC225x has a noise level of 19 nV/√Hz at 1kHz; four times lower than competitive micropower solutions.

The TLC225x amplifiers, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC225xA family is available and has a maximum input offset voltage of 850 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2252/4 also makes great upgrades to the TLC27L2/L4 or TS27L2/L4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage ranges, see the TLV2432 and TLV2442 devices. If the design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

**EQUIVALENT INPUT NOISE VOLTAGE
VS
FREQUENCY**

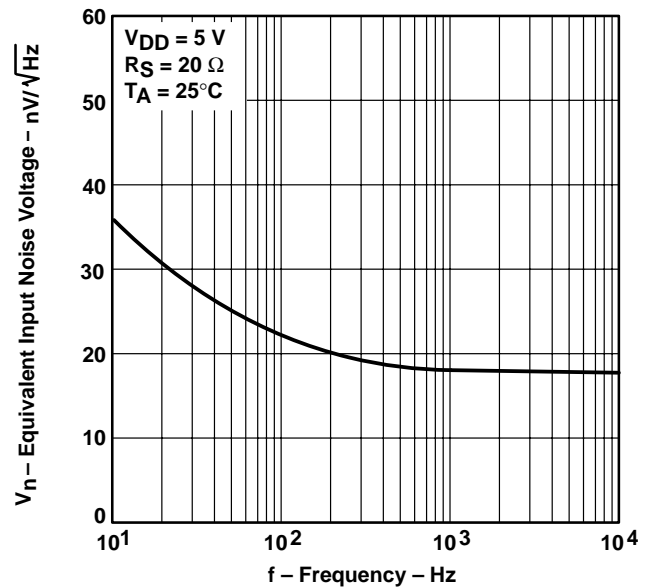


Figure 1



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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 On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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TLC2252 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP‡ (PW)	CERAMIC FLATPACK (U)
0°C to 70°C	1500 µV	TLC2252CD	—	—	TLC2252CP	TLC2252CPW	—
–40°C to 125°C	850 µV 1500 µV	TLC2252AID TLC2252ID	— —	— —	TLC2252AIP TLC2252IP	TLC2252AIPW —	— —
–40°C to 125°C	850 µV 1500 µV	TLC2252AQD TLC2252QD	— —	— —	— —	— —	— —
–55°C to 125°C	850 µV 1500 µV	— —	TLC2252AMFK TLC2252MFK	TLC2252AMJG TLC2252MJG	— —	— —	TLC2252AMU TLC2252MU

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2262CDR).

‡ The PW package is available only left-ended taped and reeled.

§ Chip forms are tested at 25°C only.

TLC2254 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP‡ (PW)	CERAMIC FLATPACK (W)
0°C to 70°C	1500 µV	TLC2254CD	—	—	TLC2254CN	TLC2254CPW	—
–40°C to 125°C	850 µV 1500 µV	TLC2254AID TLC2254ID	— —	— —	TLC2254AIN TLC2254IN	TLC2254AIPW —	— —
–40°C to 125°C	850 µV 1500 µV	TLC2254AQD TLC2254QD	— —	— —	— —	— —	— —
–55°C to 125°C	850 µV 1500 µV	— —	TLC2254AMFK TLC2254MFK	TLC2254AMJ TLC2254MJ	— —	— —	TLC2254AMW TLC2254MW

† The D packages are available taped and reeled. Add R suffix to the device type (e.g., TLC2254CDR).

‡ The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

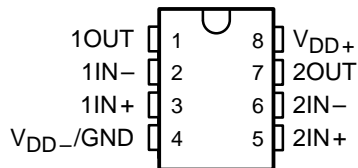
§ Chip forms are tested at 25°C only.



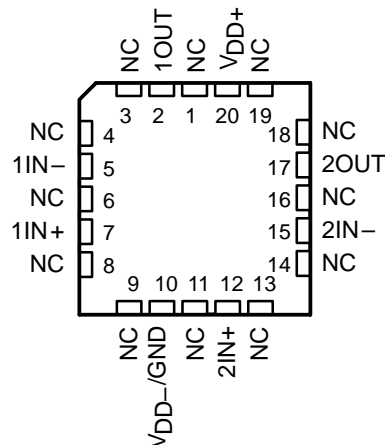
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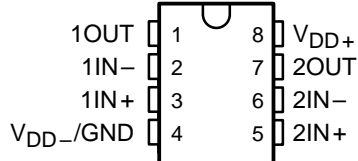
TLC2252C, TLC2252AC
TLC2252I, TLC2252AI
TLC2252Q, TLC2252AQ
D, P, OR PW PACKAGE
(TOP VIEW)



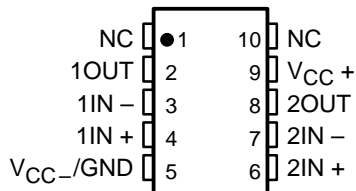
TLC2252M, TLC2252AM ... FK PACKAGE
(TOP VIEW)



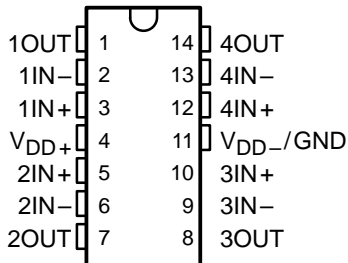
TLC2252M, TLC2252AM ... JG PACKAGE
(TOP VIEW)



TLC2262M, TLC2252AM ... U PACKAGE
(TOP VIEW)



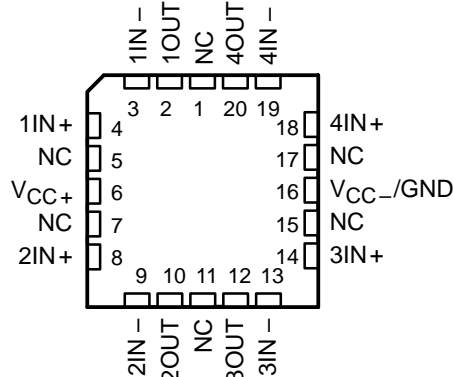
TLC2254C, TLC2254AC
TLC2254I, TLC2254AI
TLC2254Q, TLC2254AQ
D, N, OR PW PACKAGE
(TOP VIEW)



TLC2254M, TLC2254AM
J OR W PACKAGE
(TOP VIEW)



TLC2254M, TLC2254AM
FK PACKAGE
(TOP VIEW)

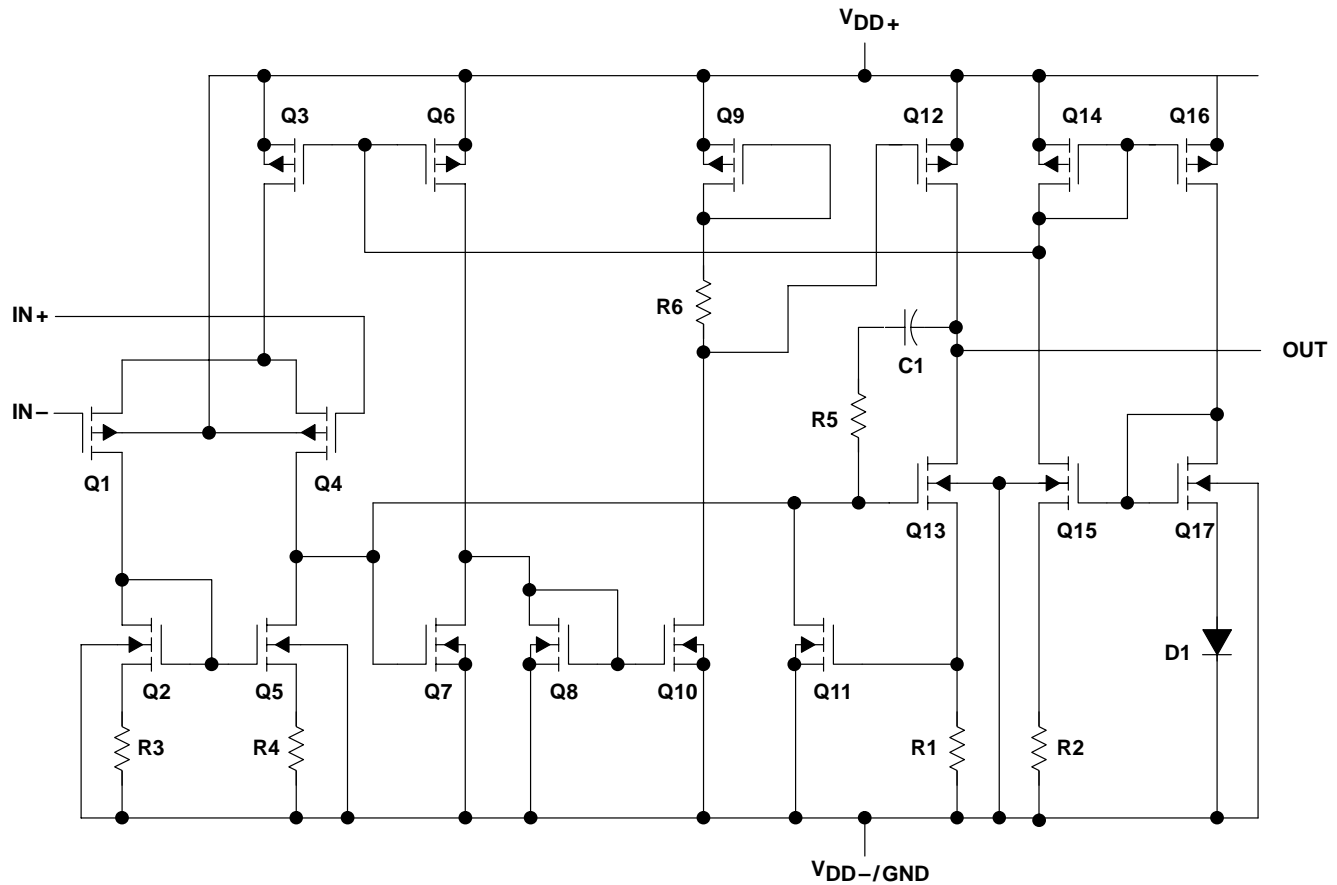


NC – No internal connection

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equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLC2252	TLC2254
Transistors	38	76
Resistors	30	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	–8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage, V_I (any input, see Note 1)	±8 V
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+}	±50 mA
Total current out of V_{DD-}	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	–40°C to 125°C
Q suffix	–40°C to 125°C
M suffix	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current flows when input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D–8	724 mW	5.8 mW/°C	464 mW	377 mW	144 mW
D–14	950 mW	7.6 mW/°C	608 mW	450 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	736 mW	—
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—
PW–8	525 mW	4.2 mW/°C	336 mW	273 mW	—
PW–14	700 mW	5.6 mW/°C	448 mW	448 mW	—
U	700 mW	5.5 mW/°C	246 mW	330 mW	150 mW
W	700 mW	5.5 mW/°C	246 mW	330 mW	150 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	±2.2	±8	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V
Operating free-air temperature, T_A	0	70	–40	125	–40	125	–55	125	°C



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2252C			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} \pm = \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	200	1500	μV	
		Full range	1750			
α_{VIO} Temperature coefficient of input offset voltage		25°C to 70°C	0.5		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	60	pA	
		Full range	100			
I_{IB} Input bias current		25°C	1	60	pA	
		Full range	100			
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega,$ $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.98		V	
	$I_{OH} = -75\ \mu\text{A}$	25°C	4.9	4.94		
	Full range	4.8				
	$I_{OH} = -150\ \mu\text{A}$	25°C	4.8	4.88		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 50\ \mu\text{A}$	25°C	0.01		V	
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 500\ \mu\text{A}$	25°C	0.09	0.15		
		Full range	0.15			
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 1\text{ mA}$	25°C	0.2	0.3		
		Full range	0.3			
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 4\text{ mA}$	25°C	0.7	1		
		Full range	1.2			
	A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C		100
$R_L = 1\text{ M}\Omega^\ddagger$			Full range	10		
			25°C	1700		
r_{id} Differential input resistance		25°C	10^{12}		Ω	
r_{ic} Common-mode input resistance		25°C	10^{12}		Ω	
c_{ic} Common-mode input capacitance	$f = 10\text{ kHz},$ P package	25°C	8		pF	
z_o Closed-loop output impedance	$f = 25\text{ kHz},$ $A_V = 10$	25°C	200		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	70	83	dB	
		Full range	70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C	80	95	dB	
		Full range	80			
I_{DD} Supply current	$V_O = 2.5\text{ V},$ No load	25°C	70	125	μA	
		Full range	150			

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T_A †	TLC2252C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V}, R_L = 100\text{ k}\Omega^\ddagger,$ $C_L = 100\text{ pF}^\ddagger$		25°C	0.07	0.12	$\text{V}/\mu\text{s}$	
				Full range	0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C	36		$\text{nV}/\sqrt{\text{Hz}}$	
		f = 1 kHz		25°C	19			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7		μV	
		f = 0.1 Hz to 10 Hz		25°C	1.1			
I_n	Equivalent input noise current			25°C	0.6		$\text{fA}/\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V},$ f = 10 kHz, $R_L = 50\text{ k}\Omega^\ddagger$		25°C	$A_V = 1$			
					$A_V = 10$			
	Gain-bandwidth product	f = 10 kHz, $C_L = 100\text{ pF}^\ddagger$		25°C	$R_L = 50\text{ k}\Omega^\ddagger$		MHz	
					0.2			
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V},$ $R_L = 50\text{ k}\Omega^\ddagger$		25°C	$A_V = 1,$ $C_L = 100\text{ pF}^\ddagger$		kHz	
					30			
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger,$ $C_L = 100\text{ pF}^\ddagger$		25°C	63°			
	Gain margin			25°C	15		dB	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise specified)

PARAMETER	TEST CONDITIONS	T _A †	TLC2252C			UNIT
			MIN	TYP	MAX	
V _{IO} Input offset voltage	V _{IC} = 0, V _O = 0, R _S = 50 Ω	25°C	200	1500	μV	
		Full range	1750			
αV _{IO} Temperature coefficient of input offset voltage		25°C to 70°C	0.5		μV/°C	
Input offset voltage long-term drift (see Note 4)		25°C	0.003		μV/mo	
I _{IO} Input offset current		25°C	0.5	60	pA	
		Full range	100			
I _{IB} Input bias current		25°C	1	60	pA	
		Full range	100			
V _{ICR} Common-mode input voltage range	V _{IO} ≤ 5 mV, R _S = 50 Ω	25°C	-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			
V _{OM+} Maximum positive peak output voltage	I _O = -20 μA	25°C	4.98		V	
	I _O = -100 μA	25°C	4.9	4.93		
		Full range	4.7			
	I _O = -200 μA	25°C	4.8	4.86		
V _{OM-} Maximum negative peak output voltage	V _{IC} = 0, I _O = 50 μA	25°C	-4.99		V	
		25°C	-4.85	-4.91		
	V _{IC} = 0, I _O = 500 μA	Full range	-4.85			
		25°C	-4.7	-4.8		
	V _{IC} = 0, I _O = 1 mA	Full range	-4.7			
		25°C	-4	-4.3		
	V _{IC} = 0, I _O = 4 mA	Full range	-3.8			
		25°C	45	650		V/mV
A _{VD} Large-signal differential voltage amplification	V _O = ±4 V	R _L = 100 kΩ	10			
		R _L = 1 MΩ	3000			
Full range		10				
r _{id} Differential input resistance		25°C	10 ¹²		Ω	
r _{ic} Common-mode input resistance		25°C	10 ¹²		Ω	
c _{ic} Common-mode input capacitance	f = 10 kHz, P package	25°C	8		pF	
z _o Closed-loop output impedance	f = 25 kHz, A _V = 10	25°C	190		Ω	
CMRR Common-mode rejection ratio	V _{IC} = -5 V to 2.7 V, V _O = 0, R _S = 50 Ω	25°C	75	88	dB	
		Full range	75			
k _{SVR} Supply-voltage rejection ratio (ΔV _{DD±} /ΔV _{IO})	V _{DD±} = 2.2 V to ±8 V, V _{IC} = 0, No load	25°C	80	95	dB	
		Full range	80			
I _{DD} Supply current	V _O = 0, No load	25°C	80	125	μA	
		Full range	150			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T_A †	TLC2252C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 1.9\text{ V}$, $C_L = 100\text{ pF}$	$R_L = 100\text{ k}\Omega$	25°C	0.07	0.12	V/ μs	
				Full range	0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C	38		nV/ $\sqrt{\text{Hz}}$	
		f = 1 kHz		25°C	19			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8		μV	
		f = 0.1 Hz to 10 Hz		25°C	1.1			
I_n	Equivalent input noise current			25°C	0.6		fA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion pulse duration	$V_O = \pm 2.3\text{ V}$, f = 10 kHz, $R_L = 50\text{ k}\Omega$	$A_V = 1$	25°C	0.2%			
			$A_V = 10$		1%			
Gain-bandwidth product		f = 10 kHz, $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.21		MHz	
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 50\text{ k}\Omega$	$A_V = 1$, $C_L = 100\text{ pF}$	25°C	14		kHz	
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$		25°C	63°			
	Gain margin			25°C	15		dB	

† Full range is 0°C to 70°C.

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2254C			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD\pm} = \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	200	1500		μV
		Full range		1750		
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage		25°C to 70°C	0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		pA
		Full range		100		
I_{IB} Input bias current		25°C	1	60		pA
		Full range		100		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega,$ $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		V
		Full range	0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C	4.9	4.94		
	Full range		4.8			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 50\ \mu\text{A}$	25°C		0.01		V
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 500\ \mu\text{A}$	25°C	0.09	0.15		
	Full range			0.15		
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 1\text{ mA}$	25°C	0.2	0.3		
	Full range			0.3		
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 4\text{ mA}$	25°C	0.7	1		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega$ ‡	25°C	100	350	V/mV
		Full range		10		
		$R_L = 1\text{ M}\Omega$ ‡	25°C		1700	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}	Ω	
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}	Ω	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz},$ N package	25°C		8	pF	
z_o Closed-loop output impedance	$f = 25\text{ kHz},$ $A_V = 10$	25°C		200	Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	70	83		dB
		Full range	70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C	80	95		dB
		Full range	80			
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V},$ No load	25°C	140	250		μA
		Full range		300		

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T_A †	TLC2254C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.4\text{ V to }2.6\text{ V}$ $R_L = 100\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡		25°C	0.07	0.12	$\text{V}/\mu\text{s}$	
				Full range	0.05			
V_n	Equivalent input noise voltage			25°C	36		$\text{nV}/\sqrt{\text{Hz}}$	
				25°C	19			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage			25°C	0.7		μV	
				25°C	1.1			
I_n	Equivalent input noise current			25°C	0.6		$\text{fA}/\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 10\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡		25°C	$A_V = 1$			
					$A_V = 10$			
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$ ‡	$R_L = 50\text{ k}\Omega$ ‡,	25°C	0.2		MHz	
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡,	$A_V = 1$, $C_L = 100\text{ pF}$ ‡	25°C	30		kHz	
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$ ‡,	$C_L = 100\text{ pF}$ ‡	25°C	63°			
	Gain margin			25°C	15		dB	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise specified)

PARAMETER	TEST CONDITIONS	T _A †	TLC2254C			UNIT
			MIN	TYP	MAX	
V _{IO} Input offset voltage	V _{IC} = 0, V _O = 0, R _S = 50 Ω	25°C	200	1500	μV	
		Full range	1750			
α _{VIO} Temperature coefficient of input offset voltage		25°C to 70°C	0.5		μV/°C	
Input offset voltage long-term drift (see Note 4)		25°C	0.003		μV/mo	
I _{IO} Input offset current		25°C	0.5	60	pA	
		Full range	100			
I _{IB} Input bias current		25°C	1	60	pA	
		Full range	100			
V _{ICR} Common-mode input voltage range	V _{IO} ≤ 5 mV, R _S = 50 Ω	25°C	-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			
V _{OM+} Maximum positive peak output voltage	I _O = -20 μA	25°C	4.98		V	
	I _O = -100 μA	25°C	4.9	4.93		
		Full range	4.7			
	I _O = -200 μA	25°C	4.8	4.86		
V _{OM-} Maximum negative peak output voltage	V _{IC} = 0, I _O = 50 μA	25°C	-4.99		V	
	V _{IC} = 0, I _O = 500 μA	25°C	-4.85	-4.91		
		Full range	-4.85			
	V _{IC} = 0, I _O = 1 mA	25°C	-4.7	-4.8		
		Full range	-4.7			
	V _{IC} = 0, I _O = 4 mA	25°C	-4	-4.3		
Full range		-3.8				
A _{VD} Large-signal differential voltage amplification	V _O = ±4 V	R _L = 100 kΩ	25°C	40	150	V/mV
		R _L = 1 MΩ	Full range	10		
			25°C	3000		
r _{i(d)} Differential input resistance		25°C	10 ¹²		Ω	
r _{i(c)} Common-mode input resistance		25°C	10 ¹²		Ω	
c _{i(c)} Common-mode input capacitance	f = 10 kHz, N package	25°C	8		pF	
z _O Closed-loop output impedance	f = 25 kHz, A _V = 10	25°C	190		Ω	
CMRR Common-mode rejection ratio	V _{IC} = -5 V to 2.7 V, V _O = 0, R _S = 50 Ω	25°C	75	88	dB	
		Full range	75			
k _{SVR} Supply-voltage rejection ratio (ΔV _{DD±} /ΔV _{IO})	V _{DD±} = ±2.2 V to ±8 V, V _{IC} = 0, No load	25°C	80	95	dB	
		Full range	80			
I _{DD} Supply current (four amplifiers)	V _O = 0, No load	25°C	160	250	μA	
		Full range	300			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T_A †	TLC2254C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 1.9\text{ V}$, $C_L = 100\text{ pF}$	$R_L = 100\text{ k}\Omega$	25°C	0.07	0.12	$\text{V}/\mu\text{s}$	
				Full range	0.05			
V_n	Equivalent input noise voltage			25°C	38		$\text{nV}/\sqrt{\text{Hz}}$	
				25°C	19			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage			25°C	0.8		μV	
				25°C	1.1			
I_n	Equivalent input noise current			25°C	0.6		$\text{fA}/\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$		25°C	$A_V = 1$			
					$A_V = 10$			
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.21		MHz	
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 50\text{ k}\Omega$	$A_V = 1$, $C_L = 100\text{ pF}$	25°C	14		kHz	
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$	$C_L = 100\text{ pF}$	25°C	63°			
	Gain margin			25°C	15		dB	

† Full range is 0°C to 70°C.

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PARAMETER	TEST CONDITIONS	T_A †	TLC2252I			TLC2252AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	200	1500		200	850	μV	
		Full range		1750		1000			
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA	
		Full range		1000		1000			
I_{IB} Input bias current	25°C	1	60		1	60	pA		
	Full range		1000		1000				
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V	
		Full range	3.5			3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.98		4.98		V		
	$I_{OH} = -75\ \mu\text{A}$	25°C	4.9	4.94	4.9	4.94			
	Full range	4.8		4.8					
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C	0.01		0.01		V		
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	0.09	0.15	0.09	0.15			
		Full range	0.15		0.15				
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 4\text{ mA}$	25°C	0.8	1	0.7	1			
		Full range	1.2		1.2				
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega$ ‡	25°C	100	350	100	350	V/mV	
		$R_L = 1\text{ M}\Omega$ ‡	Full range	10		10			
			25°C	1700		1700			
r_{id} Differential input resistance		25°C	10^{12}		10^{12}		Ω		
r_{ic} Common-mode input resistance		25°C	10^{12}		10^{12}		Ω		
C_{ic} Common-mode input capacitance	$f = 10\text{ kHz}$, P package	25°C	8		8		pF		
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C	200		200		Ω		
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83	70	83	dB		
		Full range	70		70				
kSVR Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95	80	95	dB		
		Full range	80		80				
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C	70	125	70	125	μA		
		Full range	150		150				

† Full range is -40°C to 125°C .

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2252I			TLC2252AI			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew rate at unity gain $V_O = 1.5\text{ V to }3.5\text{ V}$, $R_L = 100\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.07	0.12		0.07	0.12		V/ μs	
		Full range	0.05			0.05				
V_n	Equivalent input noise voltage	f = 10 Hz	36			36			nV/ $\sqrt{\text{Hz}}$	
		f = 1 kHz	19			19				
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	0.7			0.7			μV	
		f = 0.1 Hz to 10 Hz	1.1			1.1				
I_n	Equivalent input noise current	25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise $V_O = 0.5\text{ V to }2.5\text{ V}$, f = 10 kHz, $R_L = 50\text{ k}\Omega$ ‡	$A_V = 1$	0.2%			0.2%				
		$A_V = 10$	1%			1%				
	Gain-bandwidth product	f = 50 kHz, $C_L = 100\text{ pF}$ ‡	$R_L = 50\text{ k}\Omega$ ‡,	0.2			0.2			MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡,	$A_V = 1$, $R_L = 50\text{ k}\Omega$ ‡,	30			30			kHz
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$ ‡,	$C_L = 100\text{ pF}$ ‡	25°C			63°			
				25°C			15			
	Gain margin			25°C			15			dB

† Full range is –40°C to 125°C.

‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2252I			TLC2252AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50 \Omega$	25°C	200	1500		200	850	μV	
		Full range			1750		1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C	0.5			0.5		$\mu V/^\circ C$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu V/mo$	
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA	
		Full range			1000		1000		
I_{IB} Input bias current	25°C	1	60		1	60	pA		
	Full range			1000		1000			
V_{ICR} Common-mode input voltage range	$R_S = 50 \Omega, V_{IO} \leq 5 mV$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20 \mu A$	25°C		4.98		4.98	V		
	$I_O = -100 \mu A$	25°C	4.9	4.93		4.9		4.93	
		Full range		4.7				4.7	
	$I_O = -200 \mu A$	25°C	4.8	4.86		4.8		4.86	
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50 \mu A$	25°C		-4.99		-4.99	V		
	$V_{IC} = 0, I_O = 500 \mu A$	25°C	-4.85	-4.91		-4.85		-4.91	
		Full range		-4.85				-4.85	
	$V_{IC} = 0, I_O = 4 mA$	25°C	-4	-4.3		-4		-4.3	
AVD Large-signal differential voltage amplification	$V_O = \pm 4 V$	$R_L = 50 k\Omega$	25°C	40	150		40	150	V/mV
			Full range		10			10	
			$R_L = 1 M\Omega$	25°C		3000			
r_{id} Differential input resistance		25°C		10 ¹²			10 ¹²	Ω	
r_{ic} Common-mode input resistance		25°C		10 ¹²			10 ¹²	Ω	
C_{ic} Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8	pF	
Z_o Closed-loop output impedance	f = 25 kHz, $A_V = 10$	25°C		190			190	Ω	
CMRR Common-mode rejection ratio	$V_{IC} = -5 V$ to 2.7 V, $V_O = 0, R_S = 50 \Omega$	25°C	75	88		75	88	dB	
		Full range		75			75		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD} = 4.4 V$ to 16 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95	dB	
		Full range		80			80		
I_{DD} Supply current	$V_O = 2.5 V$, No load	25°C	80	125		80	125	μA	
		Full range			150				150

† Full range is -40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2252I			TLC2252AI			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew rate at unity gain	$V_O = \pm 1.9\text{ V}$, $R_L = 100\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C	0.07	0.12		0.07	0.12	V/ μs	
			Full range	0.05			0.05			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C	38			38			nV/ $\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$	19			19			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C	0.8			0.8			μV
			$f = 0.1\text{ Hz to }10\text{ Hz}$	1.1			1.1			
I_n	Equivalent input noise current		25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$, $R_L = 50\text{ k}\Omega$, $f = 10\text{ kHz}$	25°C	$A_V = 1$			0.2%			
				$A_V = 10$			1%			
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	25°C	0.21			0.21			MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $A_V = 1$, $R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C	14			14			kHz
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C	63°			63°			
	Gain margin		25°C	15			15			dB

† Full range is -40°C to 125°C .

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PARAMETER	TEST CONDITIONS	T_A †	TLC2254I			TLC2254AI			UNIT			
			MIN	TYP	MAX	MIN	TYP	MAX				
V_{IO} Input offset voltage		25°C	200		1500	200		850	μV			
		Full range	1750			1000						
α_{VIO} Temperature coefficient of input offset voltage	$V_{DD} \pm = \pm 2.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C to 125°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$			
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$			
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA			
		Full range	1000			1000						
I_{IB} Input bias current	25°C	1	60		1	60		pA				
	Full range	1000			1000							
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V				
		Full range	0 to 3.5		0 to 3.5							
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.98			4.98			V			
		25°C	4.9	4.94		4.9	4.94					
		Full range	4.8			4.8						
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C	0.01			0.01			V			
		25°C	0.09	0.15		0.09	0.15					
	Full range	0.15			0.15							
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	0.8			1	0.7			1		
		Full range	1.2			1.2						
$V_{IC} = 2.5\text{ V}$, $I_{OL} = 4\text{ mA}$	25°C	100			350	100		350				
	Full range	10			10							
	25°C	1700			1700							
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega$ ‡	100			350		100		350		V/mV
		Full range	10			10						
$R_L = 1\text{ M}\Omega$ ‡	25°C	1700			1700							
$r_{i(d)}$ Differential input resistance		25°C	10 ¹²			10 ¹²			Ω			
$r_{i(c)}$ Common-mode input resistance		25°C	10 ¹²			10 ¹²			Ω			
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, N package	25°C	8			8			pF			
Z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C	200			200			Ω			
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83		70	83		dB			
		Full range	70			70						
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB			
		Full range	80			80						
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	25°C	140	250		140	250		μA			
		Full range	300			300						

† Full range is -40°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2254I			TLC2254AI			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew rate at unity gain $V_O = 1.4\text{ V to }2.6\text{ V}$, $R_L = 100\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.07	0.12		0.07	0.12		V/ μs	
		Full range	0.05			0.05				
V_n	Equivalent input noise voltage $f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C	36			36			nV/ $\sqrt{\text{Hz}}$	
		25°C	19			19				
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage $f = 0.1\text{ Hz to }1\text{ Hz}$ $f = 0.1\text{ Hz to }10\text{ Hz}$	25°C	0.7			0.7			μV	
		25°C	1.1			1.1				
I_n	Equivalent input noise current	25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise $V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡	$A_V = 1$	0.2%			0.2%				
		$A_V = 10$	1%			1%				
	Gain-bandwidth product $f = 50\text{ kHz}$, $C_L = 100\text{ pF}$ ‡	$R_L = 50\text{ k}\Omega$ ‡, 25°C	0.2			0.2			MHz	
BOM	Maximum output-swing bandwidth $V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡,	$A_V = 1$, $C_L = 100\text{ pF}$ ‡	25°C	30			30			kHz
ϕ_m	Phase margin at unity gain $R_L = 50\text{ k}\Omega$ ‡,	$C_L = 100\text{ pF}$ ‡	25°C	63°			63°			
	Gain margin		25°C	15			15			dB

† Full range is –40°C to 125°C.

‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2254I			TLC2254AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C	200	1500		200	850	μV	
		Full range			1750		1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA	
		Full range			1000		1000		
I_{IB} Input bias current	25°C	1	60		1	60	pA		
	Full range			1000		1000			
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega, V_{IO} \leq 5\ \text{mV}$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C		4.98			4.98	V	
	$I_O = -100\ \mu\text{A}$	25°C	4.9	4.93		4.9	4.93		
		Full range		4.7			4.7		
	$I_O = -200\ \mu\text{A}$	25°C	4.8	4.86		4.8	4.86		
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50\ \mu\text{A}$	25°C		-4.99			-4.99	V	
	$V_{IC} = 0, I_O = 500\ \mu\text{A}$	25°C	-4.85	-4.91		-4.85	-4.91		
		Full range		-4.85			-4.85		
	$V_{IC} = 0, I_O = 4\ \text{mA}$	25°C	-4	-4.3		-4	-4.3		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\ \text{V}$	$R_L = 100\ \text{k}\Omega$	25°C	40	150		40	150	V/mV
			Full range		10			10	
		$R_L = 1\ \text{M}\Omega$	25°C		3000			3000	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}	Ω	
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}	Ω	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}, \text{ N package}$	25°C		8			8	pF	
z_o Closed-loop output impedance	$f = 25\ \text{kHz}, A_V = 10$	25°C		190			190	Ω	
CMRR Common-mode rejection ratio	$V_{IC} = -5\ \text{V to } 2.7\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	75	88		75	88	dB	
		Full range		75			75		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2\ \text{V to } \pm 8\ \text{V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	95	dB	
		Full range		80			80		
I_{DD} Supply current (four amplifiers)	$V_O = 0, \text{ No load}$	25°C	160	250		160	250	μA	
		Full range			300		300		

† Full range is -40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2254I			TLC2254AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = \pm 1.9\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 100\text{ k}\Omega$	25°C	0.07	0.12		0.07	0.12		V/ μ s
		Full range	0.05			0.05			
V_n	Equivalent input noise voltage	25°C	38			38			nV/ $\sqrt{\text{Hz}}$
		25°C	19			19			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	25°C	0.8			0.8			μ V
		25°C	1.1			1.1			
I_n	Equivalent input noise current	25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise $V_O = \pm 2.3\text{ V}$, $R_L = 50\text{ k}\Omega$, $f = 20\text{ kHz}$	25°C	0.2%			0.2%			
			1%			1%			
	Gain-bandwidth product $f = 10\text{ kHz}$, $C_L = 100\text{ pF}$, $R_L = 50\text{ k}\Omega$	25°C	0.21			0.21			MHz
BOM	Maximum output-swing bandwidth $V_{O(PP)} = 4.6\text{ V}$, $R_L = 50\text{ k}\Omega$, $A_V = 1$, $C_L = 100\text{ pF}$	25°C	14			14			kHz
ϕ_m	Phase margin at unity gain $R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C	63°			63°			
		25°C	15			15			
	Gain margin	25°C	15			15			dB

† Full range is -40°C to 125°C .

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2252Q TLC2252M			TLC2252AQ TLC2252AM			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	200	1500		200	850	μV		
		Full range			1750		1000			
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA		
		Full range			1000		1000			
I_{IB} Input bias current	25°C	1	60		1	60	pA			
	Full range			1000		1000				
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V		
		Full range	0 to 3.5		0 to 3.5					
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$ $I_{OH} = -75\ \mu\text{A}$ $I_{OH} = -150\ \mu\text{A}$	25°C	4.98			4.98			V	
		25°C	4.9	4.94		4.9	4.94			
		Full range	4.8			4.8				
		25°C	4.8	4.88		4.8	4.88			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ $I_{OL} = 500\ \mu\text{A}$ $I_{OL} = 4\text{ mA}$	25°C	0.01			0.01			V	
		25°C	0.09	0.15		0.09	0.15			
		Full range	0.15			0.15				
		25°C	0.8	1		0.7	1			
		Full range	1.2			1.2				
		25°C	100	350		100	350			
AVD Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega$ ‡	25°C	100			100			V/mV
			Full range	10			10			
		$R_L = 1\text{ M}\Omega$ ‡	25°C	1700			1700			
r_{id} Differential input resistance		25°C	10^{12}			10^{12}			Ω	
r_{ic} Common-mode input resistance		25°C	10^{12}			10^{12}			Ω	
c_{ic} Common-mode input capacitance	$f = 10\text{ kHz}$, $f = 10\text{ kHz}$	25°C	8			8			pF	
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C	200			200			Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $R_S = 50\ \Omega$, $V_O = 2.5\text{ V}$	25°C	70	83		70	83	dB		
		Full range	70			70				
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95	dB		
		Full range	80			80				
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C	70	125		70	125	μA		
		Full range	150			150				

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2252Q TLC2252M			TLC2252AQ TLC2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = 0.5\text{ V to }3.5\text{ V}$, $R_L = 100\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.07	0.12		0.07	0.12		V/ μs
		Full range	0.05			0.05			
V_n	Equivalent input noise voltage $f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C	36			36			nV/ $\sqrt{\text{Hz}}$
		25°C	19			19			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage $f = 0.1\text{ Hz to }1\text{ Hz}$ $f = 0.1\text{ Hz to }10\text{ Hz}$	25°C	0.7			0.7			μV
		25°C	1.1			1.1			
I_n	Equivalent input noise current	25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise $V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 10\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡	$A_V = 1$	0.2%			0.2%			
		$A_V = 10$	1%			1%			
	Gain-bandwidth product $f = 50\text{ kHz}$, $C_L = 100\text{ pF}$ ‡	$R_L = 50\text{ k}\Omega$ ‡, 25°C	0.2			0.2			MHz
B_{OM}	Maximum output-swing bandwidth $V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡, $A_V = 1$, $C_L = 100\text{ pF}$ ‡	25°C	30			30			kHz
ϕ_m	Phase margin at unity gain $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	63°			63°			
		25°C	15			15			dB

† Full range is – 40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2252Q TLC2252M			TLC2252AQ TLC2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50 \Omega$	25°C	200	1500		200	850	μV	
		Full range			1750		1000		
αV_{IO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5		$\mu V/^\circ C$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu V/mo$	
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA	
		Full range			1000		1000		
I_{IB} Input bias current	25°C	1	60		1	60	pA		
	Full range			1000		1000			
V_{ICR} Common-mode input voltage range	$R_S = 50 \Omega, V_{IO} \leq 5 mV$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20 \mu A$	25°C	4.98			4.98	V		
	$I_O = -100 \mu A$	25°C	4.9	4.93		4.9		4.93	
		Full range	4.7			4.7			
	$I_O = -200 \mu A$	25°C	4.8	4.86		4.8		4.86	
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50 \mu A$	25°C	-4.99			-4.99	V		
	$V_{IC} = 0, I_O = 500 \mu A$	25°C	-4.85	-4.91		-4.85		-4.91	
		Full range	-4.85			-4.85			
	$V_{IC} = 0, I_O = 4 mA$	25°C	-4	-4.3		-4		-4.3	
		Full range	-3.8			-3.8			
AVD Large-signal differential voltage amplification	$V_O = \pm 4 V$	$R_L = 100 k\Omega$	25°C	40	150		40	150	V/mV
			Full range	10			10		
		$R_L = 1 M\Omega$	25°C	3000			3000		
r_{id} Differential input resistance		25°C	10^{12}			10^{12}	Ω		
r_{ic} Common-mode input resistance		25°C	10^{12}			10^{12}	Ω		
c_{ic} Common-mode input capacitance	$f = 10 kHz, P$ package	25°C	8			8	pF		
z_o Closed-loop output impedance	$f = 25 kHz, A_V = 10$	25°C	190			190	Ω		
CMRR Common-mode rejection ratio	$V_{IC} = -5 V$ to 2.7 V, $V_O = 0, R_S = 50 \Omega$	25°C	75	88		75	88	dB	
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD} = \pm 2.2 V$ to $\pm 8 V, V_{IC} = 0, No load$	25°C	80	95		80	95	dB	
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5 V, No load$	25°C	80	125		80	125	μA	
		Full range			150		150		

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2252Q TLC2252M			TLC2252AQ TLC2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = \pm 2\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 100\text{ k}\Omega$	25°C	0.07	0.12		0.07	0.12		$\text{V}/\mu\text{s}$
		Full range	0.05			0.05			
V_n	Equivalent input noise voltage	25°C		38			38		$\text{nV}/\sqrt{\text{Hz}}$
		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	25°C		0.8			0.8		μV
		25°C		1.1			1.1		
I_n	Equivalent input noise current	25°C		0.6			0.6	$\text{fA}/\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise $V_O = \pm 2.3\text{ V}$, $R_L = 50\text{ k}\Omega$, $f = 10\text{ kHz}$	25°C		0.2%			0.2%		
		25°C		1%			1%		
	Gain-bandwidth product $f = 10\text{ kHz}$, $C_L = 100\text{ pF}$, $R_L = 50\text{ k}\Omega$	25°C		0.21			0.21	MHz	
BOM	Maximum output-swing bandwidth $V_{O(PP)} = 4.6\text{ V}$, $R_L = 50\text{ k}\Omega$, $A_V = 1$, $C_L = 100\text{ pF}$	25°C		14			14	kHz	
ϕ_m	Phase margin at unity gain $R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		63°			63°		
		25°C		15			15	dB	

† Full range is – 40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

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PARAMETER	TEST CONDITIONS	T_A †	TLC2254Q TLC2254M			TLC2254AQ TLC2254AM			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO} Input offset voltage		25°C	200	1500		200	850	μV		
		Full range		1750		1000				
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	0.003			0.003			$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA		
		125°C	1000			1000				
I_{IB} Input bias current		25°C	1	60		1	60	pA		
		125°C	1000			1000				
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V		
		Full range	0 to 3.5		0 to 3.5					
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.98			4.98			V	
	$I_{OH} = -75\ \mu\text{A}$	25°C	4.9	4.94		4.9	4.94			
	Full range	4.8			4.8					
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C	0.01			0.01			V	
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	0.09	0.15		0.09	0.15			
		Full range	0.15			0.15				
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 4\text{ mA}$	25°C	0.8	1		0.7	1			
		Full range	1.2			1.2				
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega$ ‡	25°C	100	350		100	350	V/mV	
		$R_L = 1\text{ M}\Omega$ ‡	Full range	10			10			
			25°C	1700			1700			
$r_{i(d)}$ Differential input resistance		25°C	1012			1012			Ω	
$r_{i(c)}$ Common-mode input resistance		25°C	1012			1012			Ω	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, N package	25°C	8			8			pF	
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C	200			200			Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83		70	83	dB		
		Full range	70			70				
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95	dB		
		Full range	80			80				
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	25°C	140	250		140	250	μA		
		Full range	300			300				

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2254Q TLC2254M			TLC2254AQ TLC2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = 0.5\text{ V to }3.5\text{ V}$, $R_L = 100\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.07	0.12		0.07	0.12		V/ μ s
		Full range	0.05			0.05			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$	36			36			nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	19			19			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	0.7			0.7			μ V
		$f = 0.1\text{ Hz to }10\text{ Hz}$	1.1			1.1			
I_n	Equivalent input noise current	25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise $V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡	$A_V = 1$	0.2%			0.2%			
		$A_V = 10$	1%			1%			
	Gain-bandwidth product $f = 50\text{ kHz}$, $C_L = 100\text{ pF}$ ‡	$R_L = 50\text{ k}\Omega$ ‡, 25°C	0.2			0.2			MHz
B_{OM}	Maximum output-swing bandwidth $V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡	$A_V = 1$, $C_L = 100\text{ pF}$ ‡, 25°C	30			30			kHz
ϕ_m	Phase margin at unity gain $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	63°			63°			
		25°C	15			15			dB

† Full range is – 40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2254Q TLC2254M			TLC2254AQ TLC2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50 \Omega$	25°C	200	1500		200	850	μV	
		Full range			1750		1000		
αV_{IO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5		$\mu V/^\circ C$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu V/mo$	
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA	
		125°C			1000		1000		
I_{IB} Input bias current	25°C	1	60		1	60	pA		
	125°C			1000		1000			
V_{ICR} Common-mode input voltage range	$R_S = 50 \Omega, V_{IO} \leq 5 mV$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20 \mu A$	25°C	4.98			4.98	V		
	$I_O = -100 \mu A$	25°C	4.9	4.93		4.9		4.93	
		Full range	4.7			4.7			
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50 \mu A$	25°C	-4.99			-4.99	V		
	$V_{IC} = 0, I_O = 500 \mu A$	25°C	-4.85	-4.91		-4.85		-4.91	
		Full range	-4.85			-4.85			
	$V_{IC} = 0, I_O = 4 mA$	25°C	-4	-4.3		-4		-4.3	
		Full range	-3.8			-3.8			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4 V$	$R_L = 100 k\Omega$	25°C	40	150		40	150	V/mV
			Full range	10			10		
		$R_L = 1 M\Omega$	25°C	3000			3000		
$r_{i(d)}$ Differential input resistance		25°C	10 ¹²			10 ¹²	Ω		
$r_{i(c)}$ Common-mode input resistance		25°C	10 ¹²			10 ¹²	Ω		
$C_{i(c)}$ Common-mode input capacitance	$f = 10 kHz, N$ package	25°C	8			8	pF		
Z_o Closed-loop output impedance	$f = 25 kHz, A_V = 10$	25°C	190			190	Ω		
CMRR Common-mode rejection ratio	$V_{IC} = -5 V$ to 2.7 V, $V_O = 0, R_S = 50 \Omega$	25°C	75	88		75	88	dB	
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2 V$ to $\pm 8 V, V_{IC} = V_{DD}/2, No load$	25°C	80	95		80	95	dB	
		Full range	80			80			
I_{DD} Supply current (four amplifiers)	$V_O = 0, No load$	25°C	160	250		160	250	μA	
		Full range			300		300		

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER	TEST CONDITIONS		T_A †	TLC2254Q TLC2254M			TLC2254AQ TLC2254AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = \pm 2\text{ V}$, $C_L = 100\text{ pF}$	$R_L = 100\text{ k}\Omega$	25°C	0.07	0.12		0.07	0.12		V/ μ s
			Full range	0.05			0.05			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C	38			38			nV/ $\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$		25°C	19			19			
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C	0.8			0.8			μ V
	$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C	1.1			1.1			
I_n Equivalent input noise current			25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$
THD + N Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$, $R_L = 50\text{ k}\Omega$, $f = 20\text{ kHz}$	$A_V = 1$	25°C	0.2%			0.2%			
		$A_V = 10$		1%			1%			
Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.21			0.21			MHz
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 50\text{ k}\Omega$	$A_V = 1$, $C_L = 100\text{ pF}$	25°C	14			14			kHz
ϕ_m Phase margin at unity gain	$R_L = 50\text{ k}\Omega$	$C_L = 100\text{ pF}$	25°C	63°			63°			
			Gain margin	25°C	15			15		

† Full range is – 40°C to 125°C for Q suffix, – 55°C to 125°C for M suffix.

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TYPICAL CHARACTERISTICS

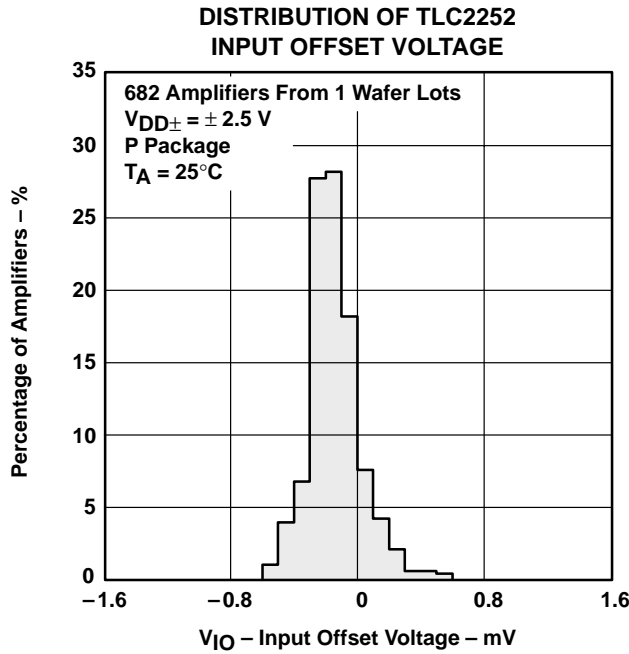


Figure 2

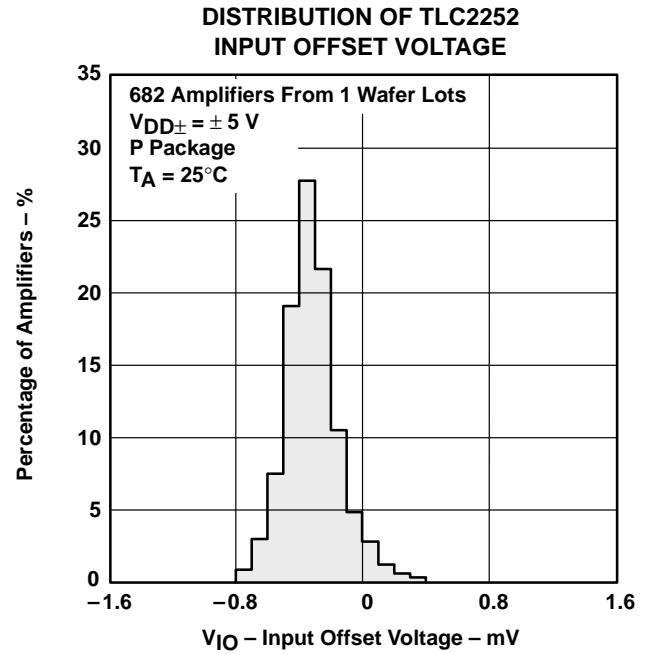


Figure 3

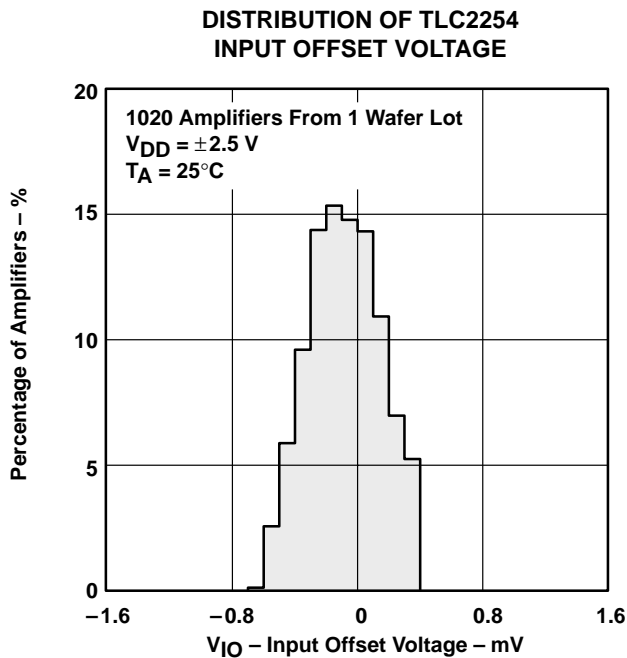


Figure 4

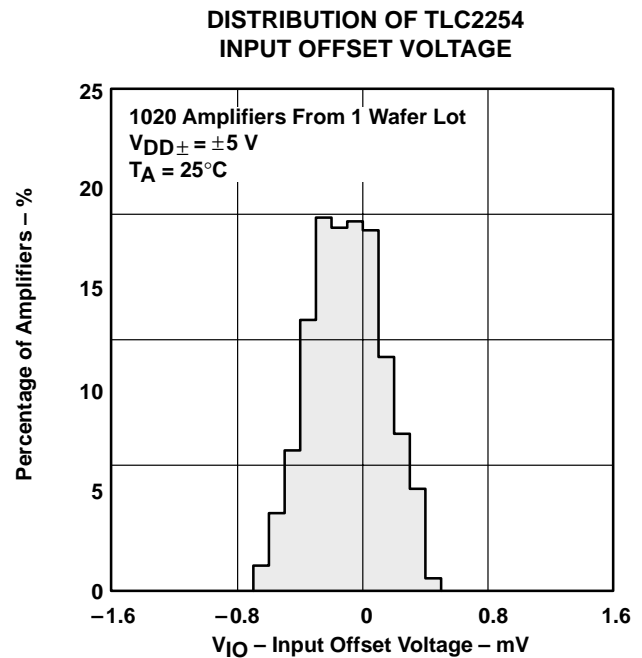


Figure 5

TYPICAL CHARACTERISTICS

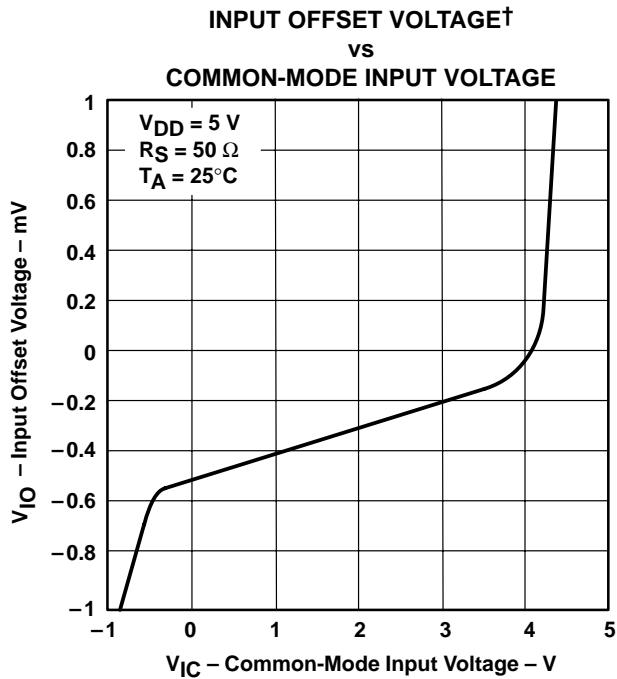


Figure 6

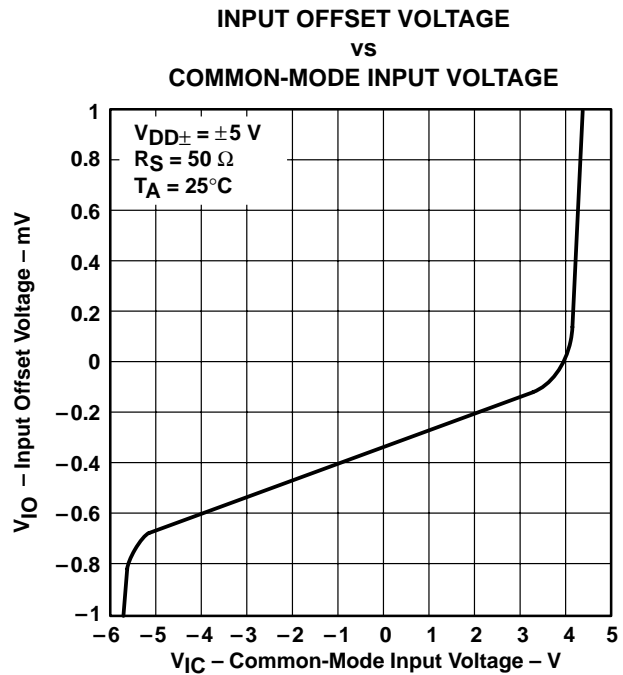


Figure 7

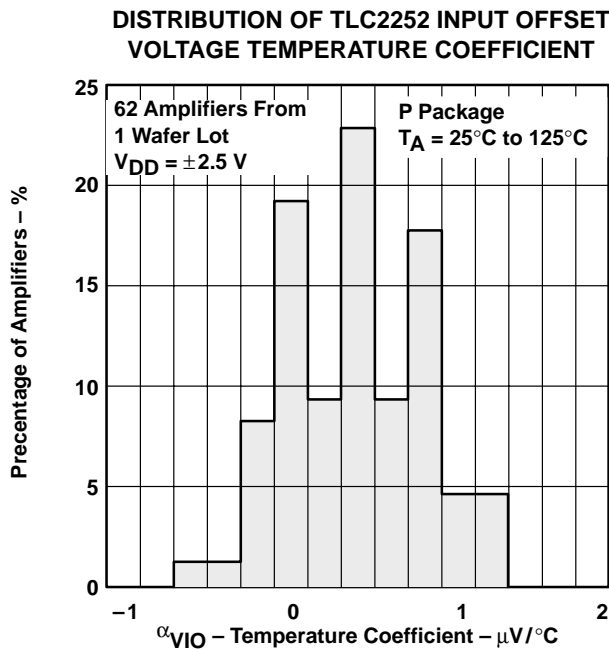


Figure 8

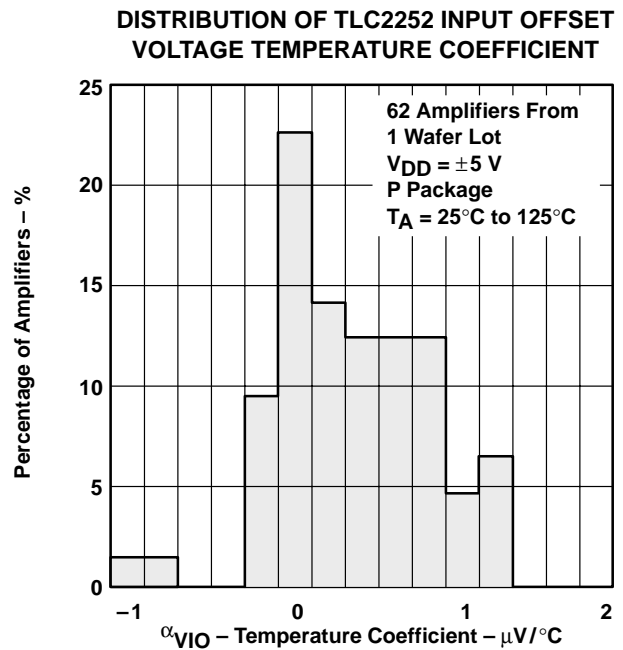


Figure 9

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



Figure 10



Figure 11



Figure 12



Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE RANGE†
vs
FREE-AIR TEMPERATURE

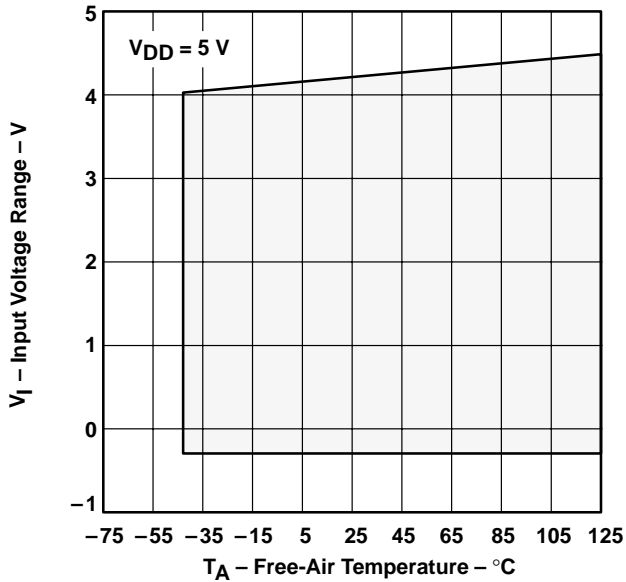


Figure 14

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

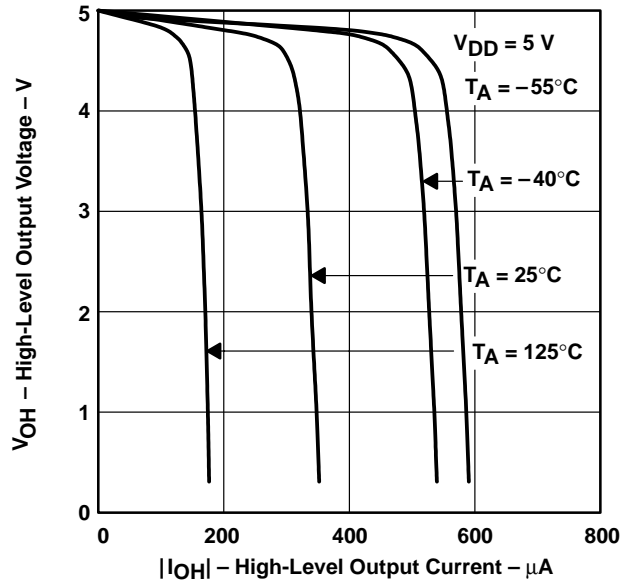


Figure 15

LOW-LEVEL OUTPUT VOLTAGE†
vs
LOW-LEVEL OUTPUT CURRENT

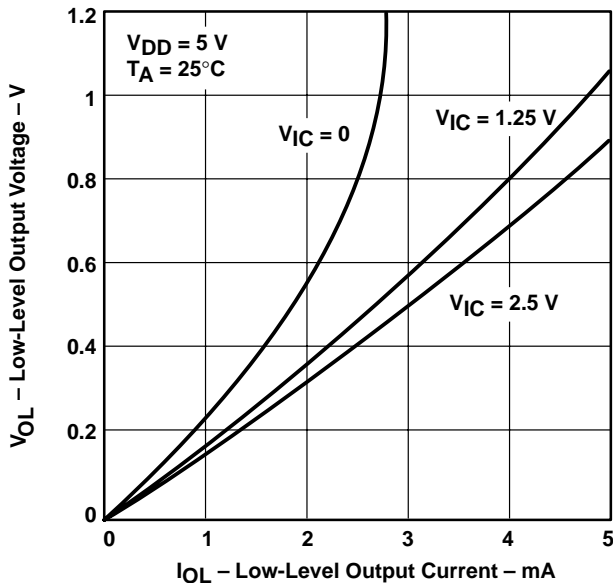


Figure 16

LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT

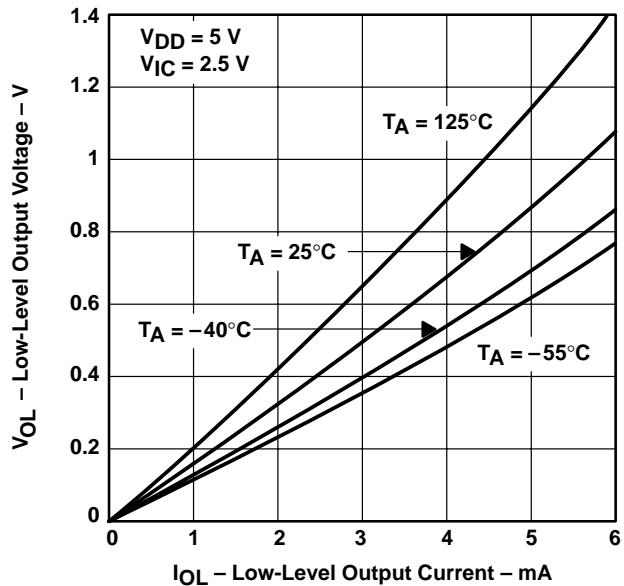


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE†
 vs
 OUTPUT CURRENT

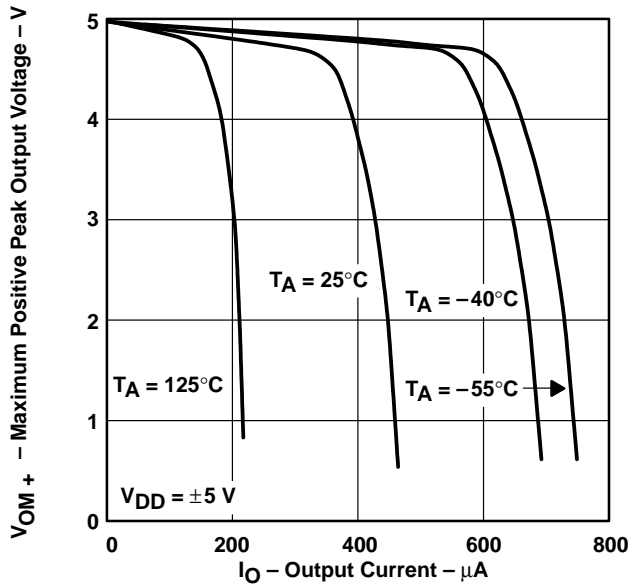


Figure 18

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE†
 vs
 OUTPUT CURRENT

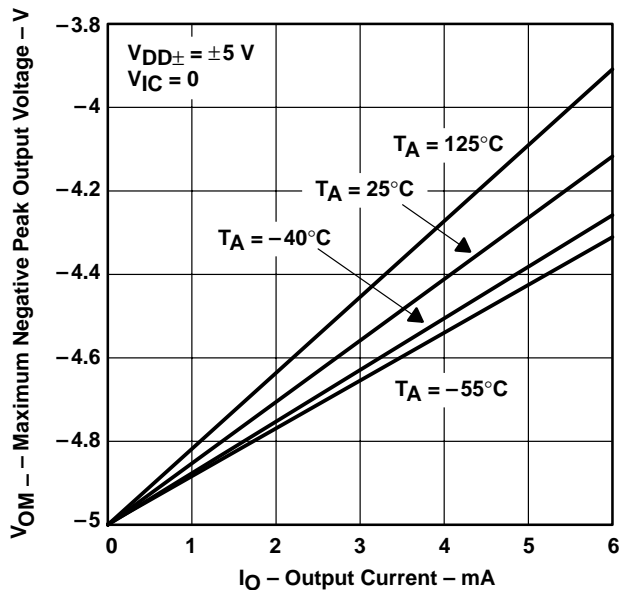


Figure 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE‡
 vs
 FREQUENCY

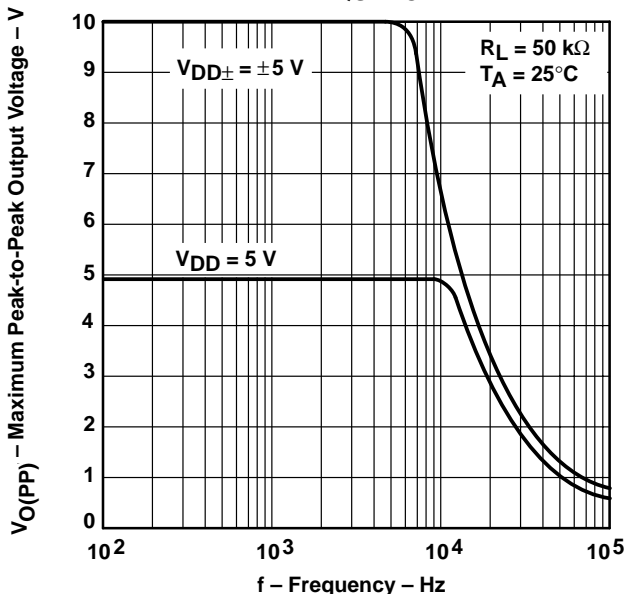


Figure 20

SHORT-CIRCUIT OUTPUT CURRENT
 vs
 SUPPLY VOLTAGE

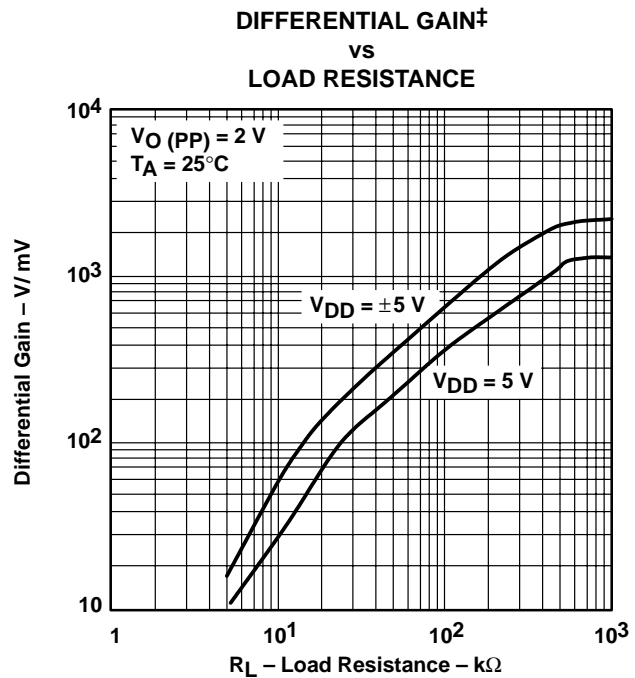
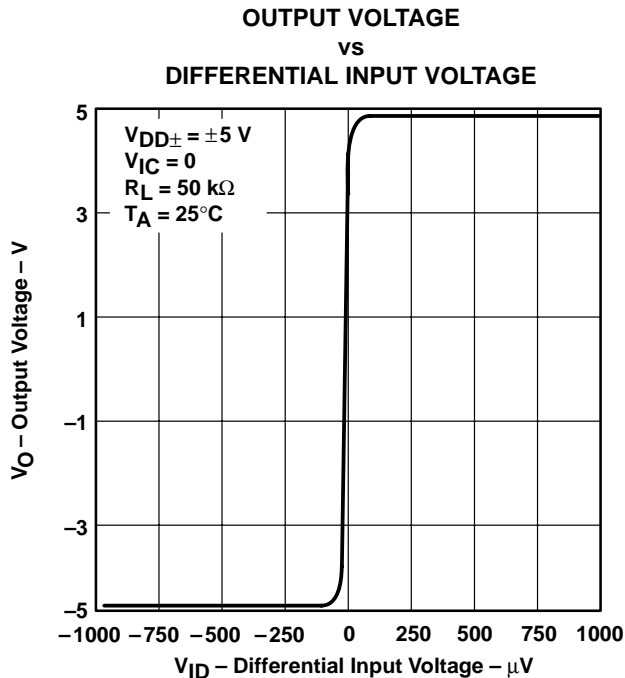
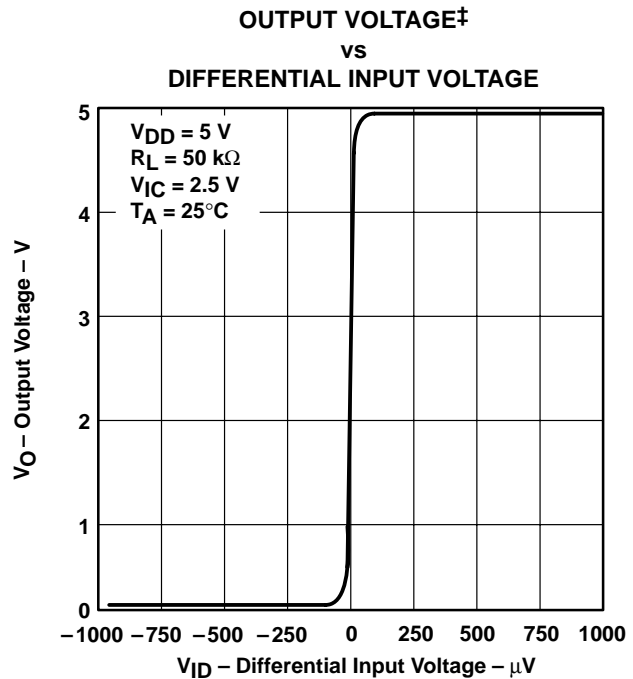
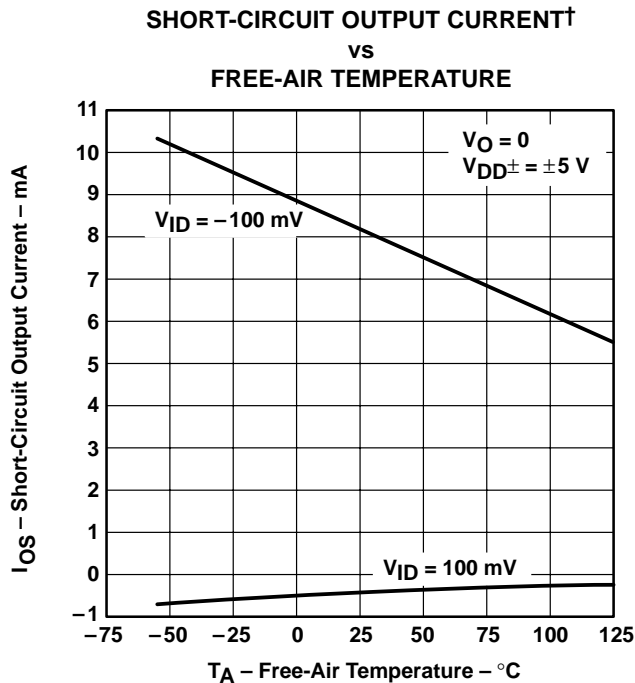


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE MARGIN†
 VS
 FREQUENCY



Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE MARGIN
 VS
 FREQUENCY

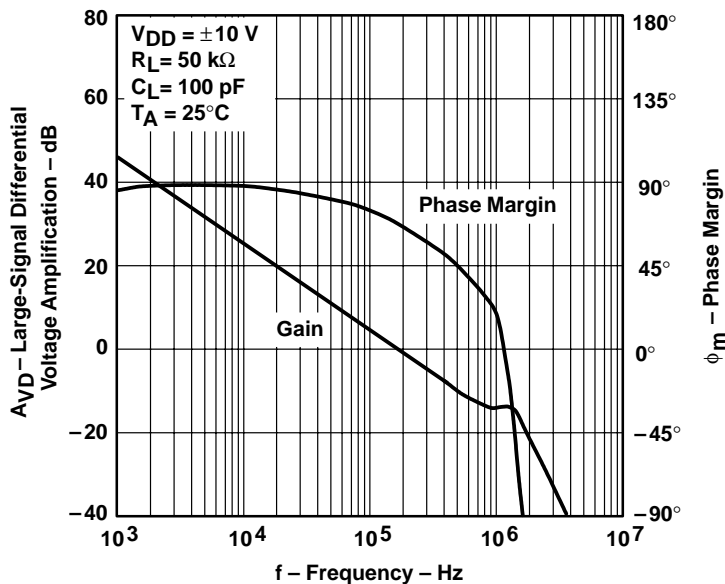


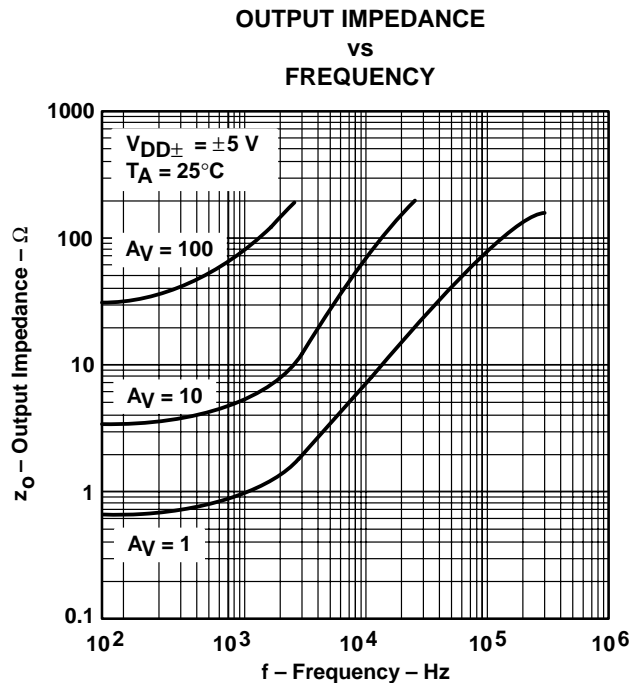
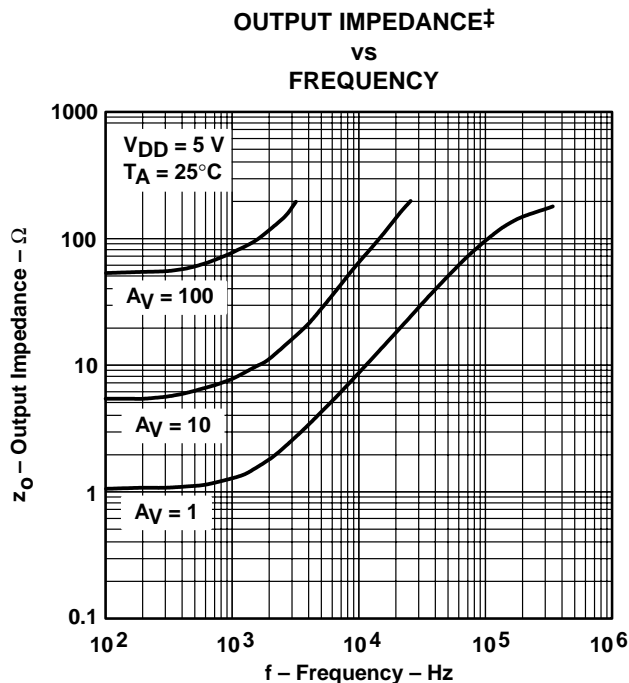
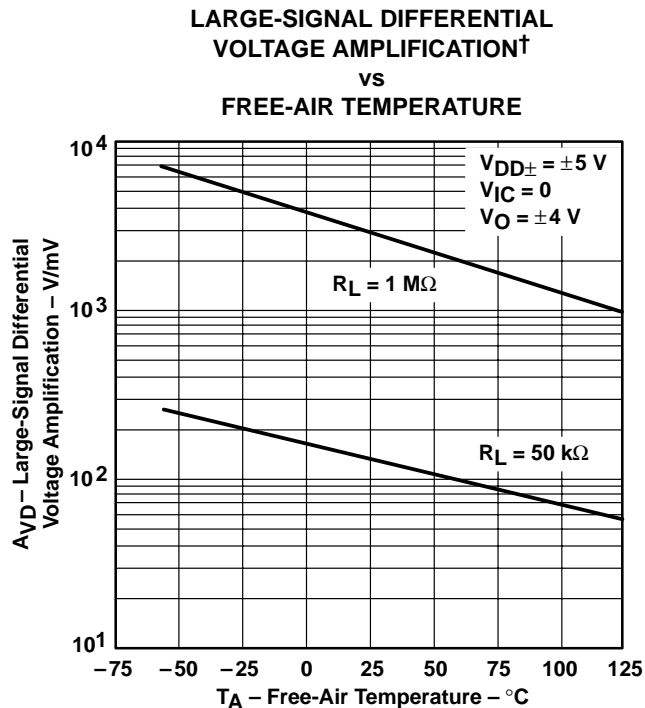
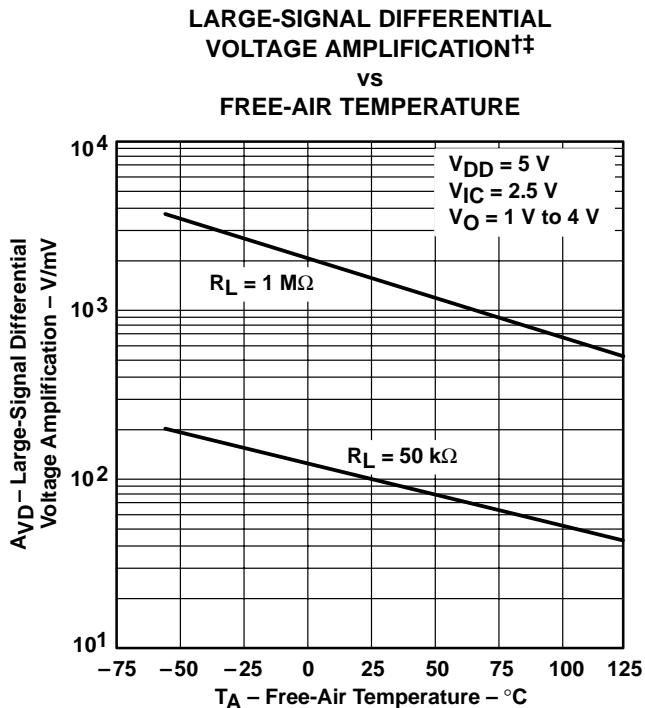
Figure 27

† For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.



TYPICAL CHARACTERISTICS



Figure 32

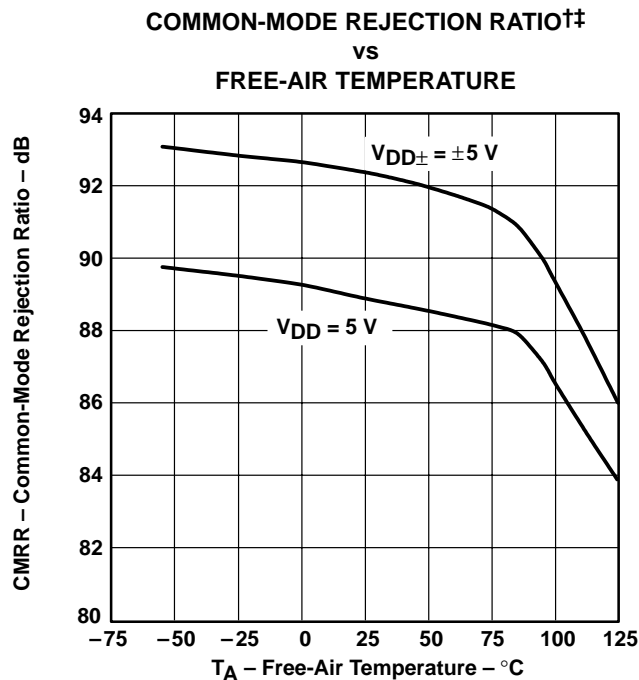


Figure 33



Figure 34

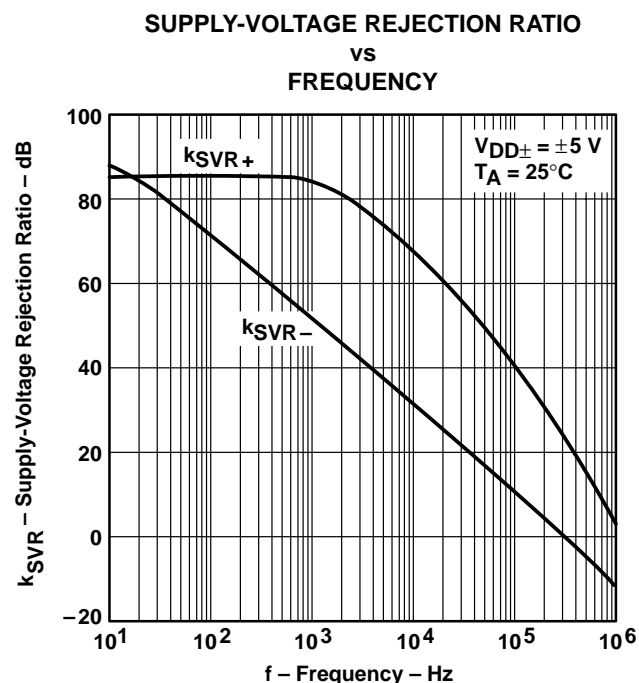


Figure 35

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

†† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO†
 vs
 FREE-AIR TEMPERATURE

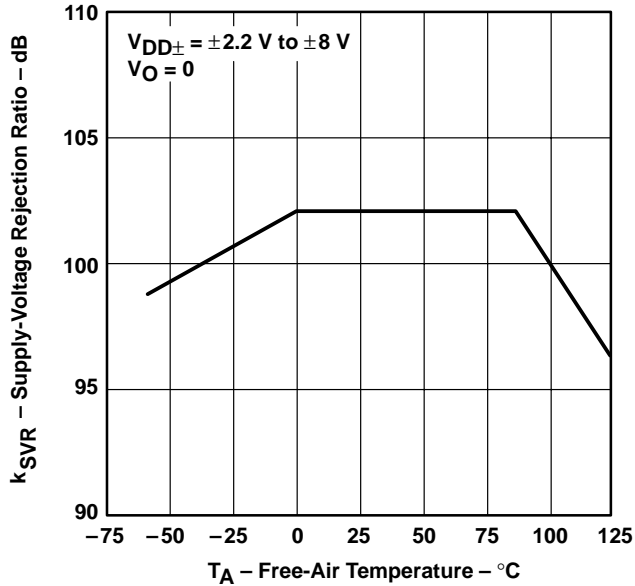


Figure 36

SUPPLY CURRENT†
 vs
 SUPPLY VOLTAGE

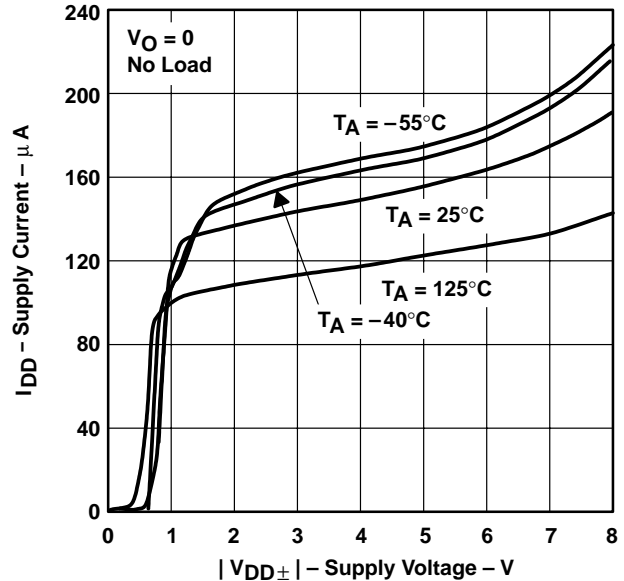


Figure 37

SUPPLY CURRENT‡
 vs
 FREE-AIR TEMPERATURE

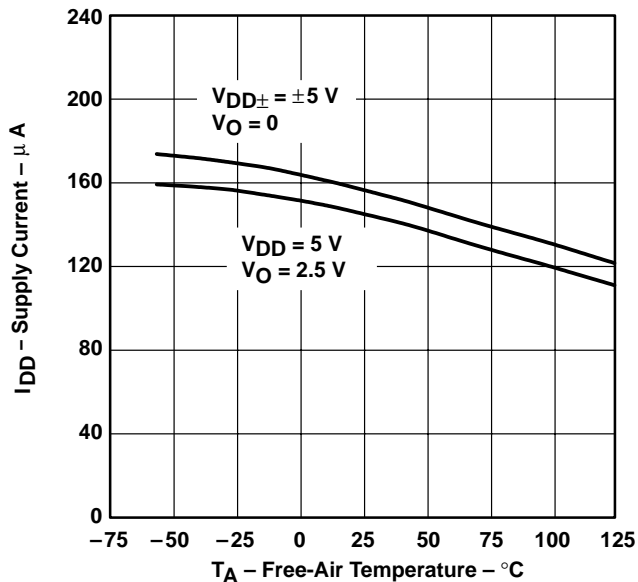


Figure 38

SLEW RATE‡
 vs
 LOAD CAPACITANCE

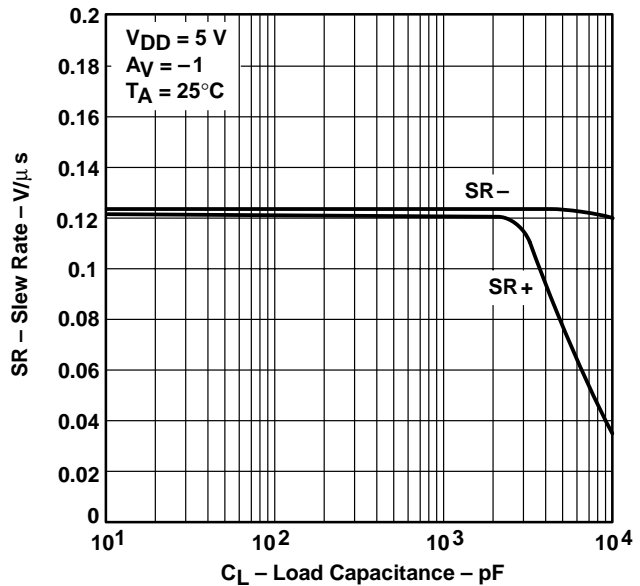
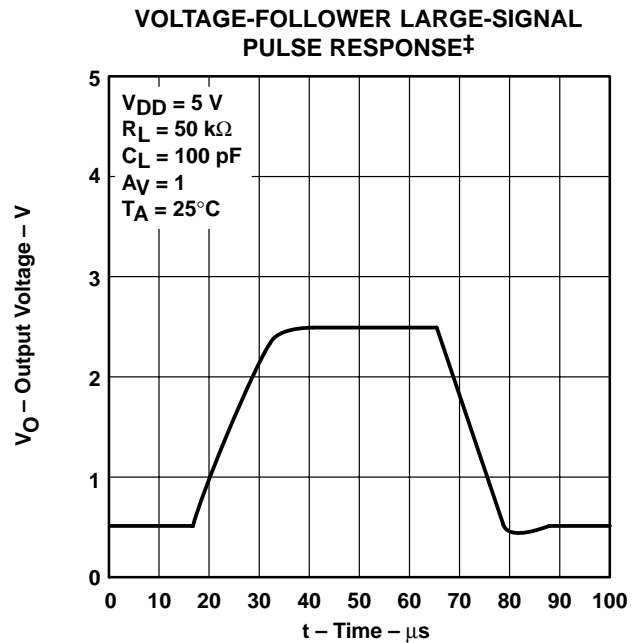
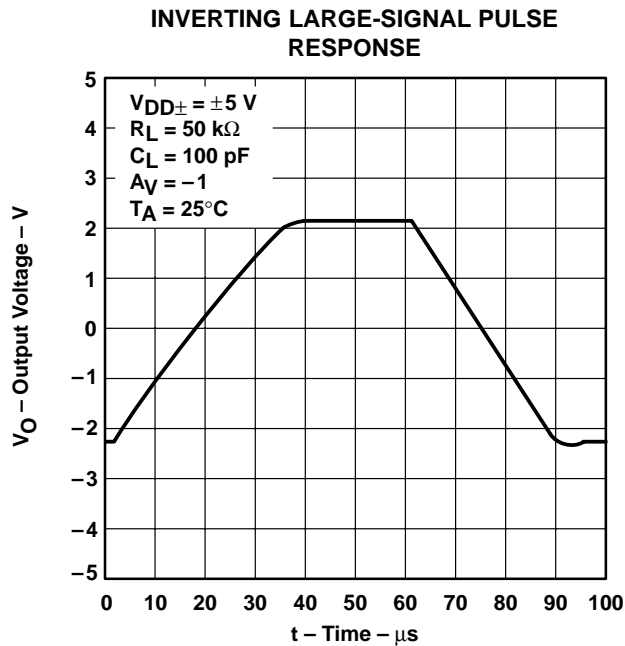
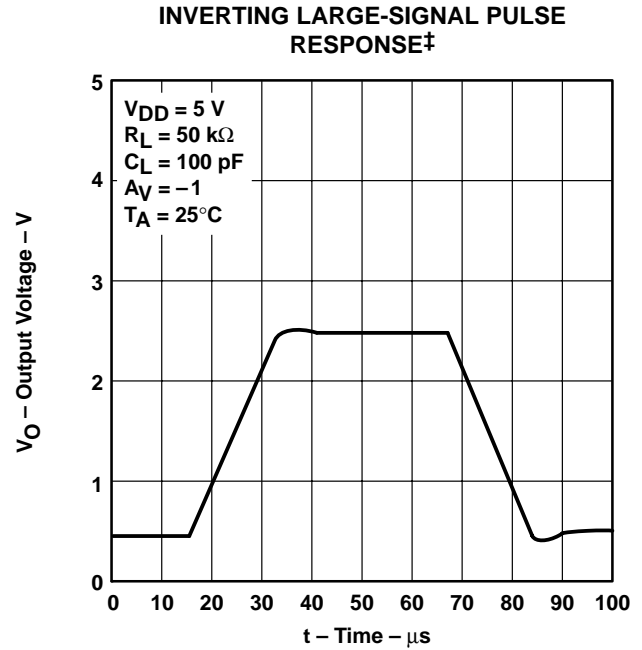


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

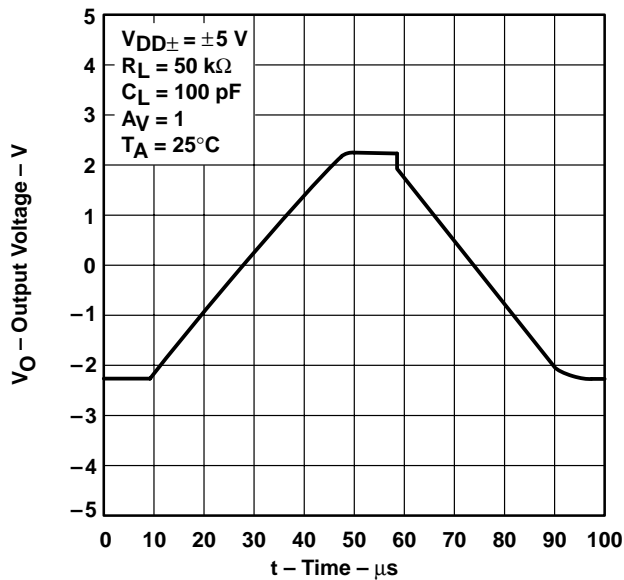


Figure 44

INVERTING SMALL-SIGNAL PULSE RESPONSE†

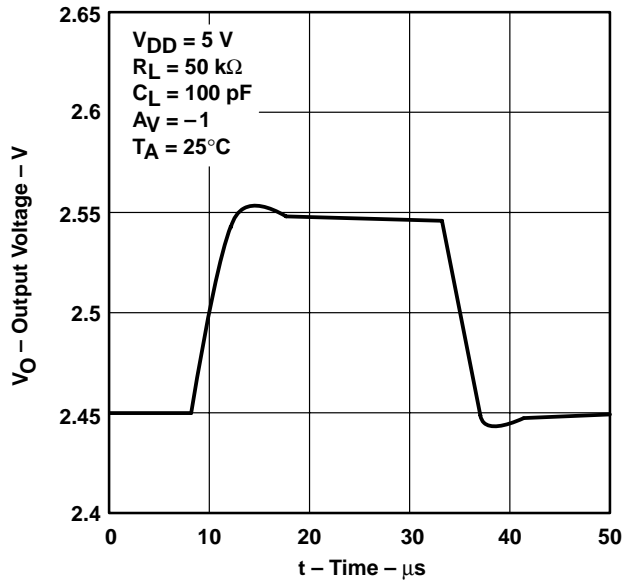


Figure 45

INVERTING SMALL-SIGNAL PULSE RESPONSE



Figure 46

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

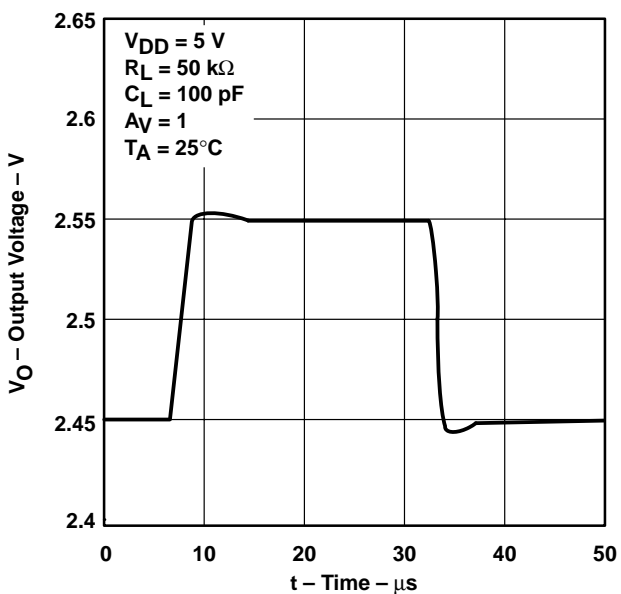


Figure 47

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



Figure 48

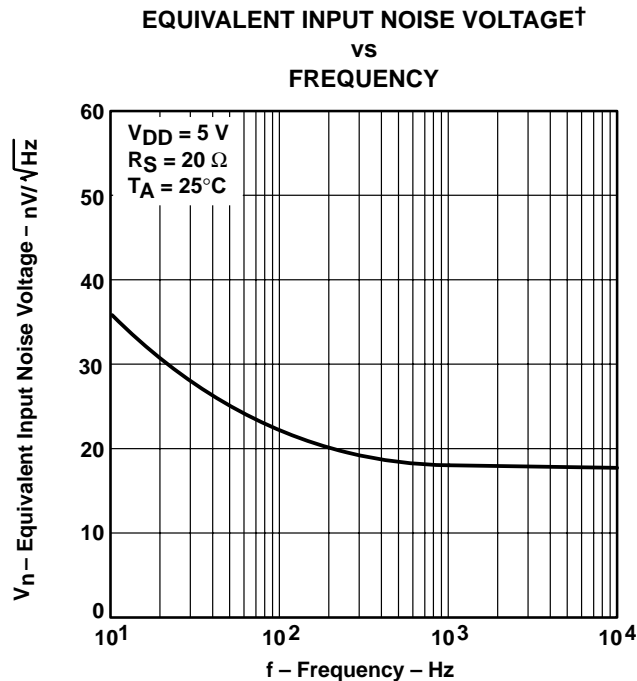


Figure 49



Figure 50

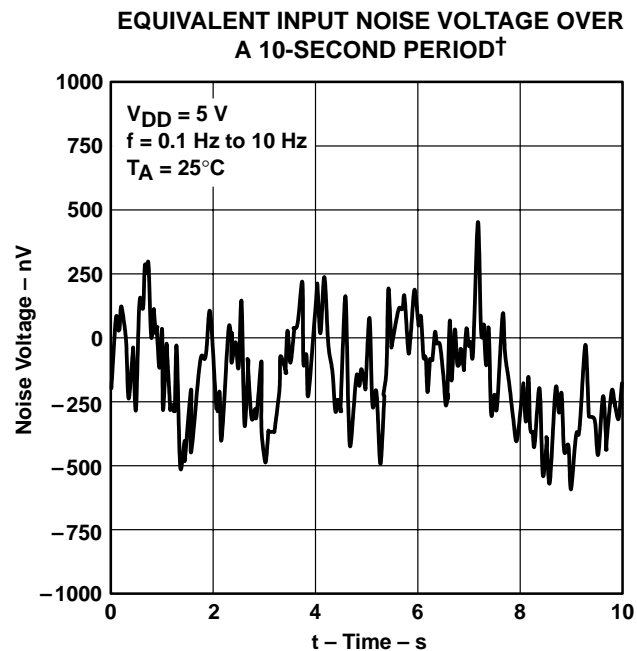


Figure 51

† For curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

**INTEGRATED NOISE VOLTAGE
 VS
 FREQUENCY**



Figure 52

**TOTAL HARMONIC DISTORTION PLUS NOISE†
 VS
 FREQUENCY**



Figure 53

**GAIN-BANDWIDTH PRODUCT‡
 VS
 FREE-AIR TEMPERATURE**



Figure 54

**GAIN-BANDWIDTH PRODUCT
 VS
 SUPPLY VOLTAGE**



Figure 55

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V .

‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



Figure 56

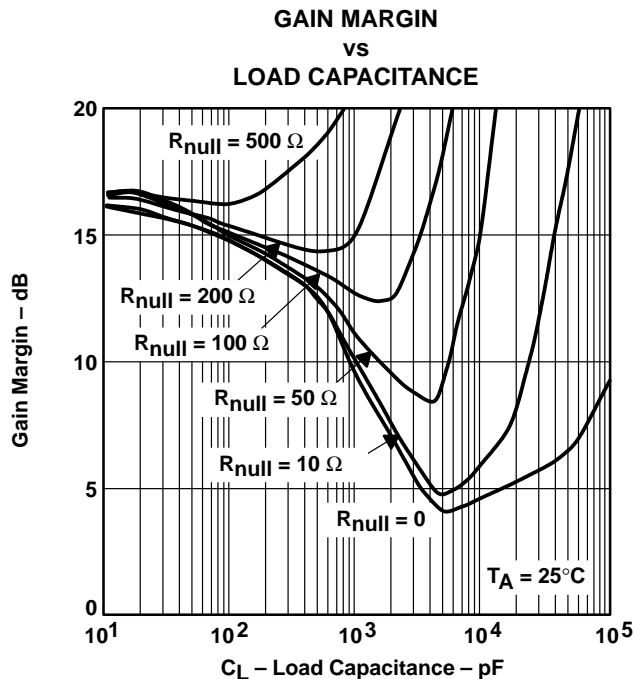


Figure 57

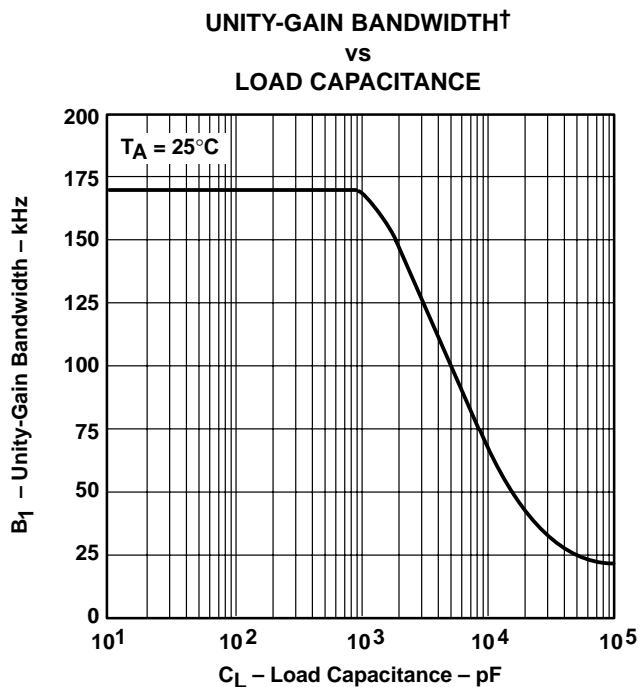


Figure 58

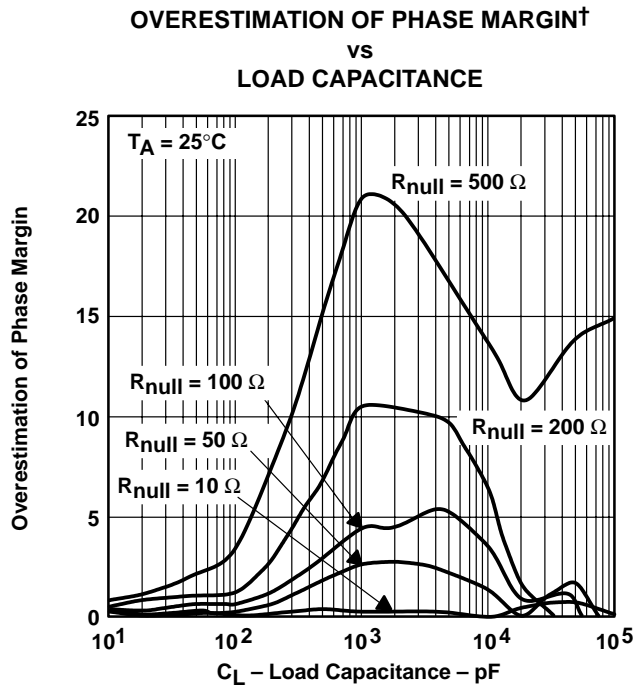


Figure 59

† See application information

APPLICATION INFORMATION

driving large capacitive loads

The TLC225x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 56 and Figure 57 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 60) improves the gain and phase margins when driving large capacitive loads. Figure 56 and Figure 57 show the effects of adding series resistances of 10 Ω , 50 Ω , 100 Ω , 200 Ω , and 500 Ω . The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \tag{1}$$

Where :

- $\Delta\phi_{m1}$ = Improvement in phase margin
- UGBW = Unity-gain bandwidth frequency
- R_{null} = Output series resistance
- C_L = Load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 58). To use equation 1, UGBW must be approximated from Figure 58.

Using equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 59. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 60, with equation 1 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

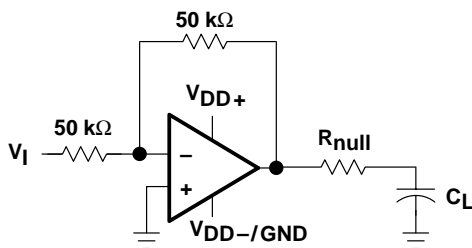


Figure 60. Series-Resistance Circuit

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using MicroSim *Parts*™, the model generation software used with MicroSim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 61 are generated using the TLC225x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



Figure 61. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9564001Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9564001Q2A TLC2252 MFKB	Samples
5962-9564001QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9564001QHA TLC2252M	Samples
5962-9564001QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9564001QPA TLC2252M	Samples
5962-9564002Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9564002Q2A TLC2254 MFKB	Samples
5962-9564002QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9564002QD A TLC2254MWB	Samples
5962-9564003NXD	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	Q2252A	Samples
5962-9564003NXDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	Q2252A	Samples
5962-9564003Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9564003Q2A TLC2252 AMFKB	Samples
5962-9564003QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9564003QHA TLC2252AM	Samples
5962-9564003QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9564003QPA TLC2252AM	Samples
5962-9564004Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9564004Q2A TLC2254 AMFKB	Samples
5962-9564004QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9564004QD A TLC2254AMWB	Samples
TLC2252AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2252AI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2252AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2252AI	Samples
TLC2252AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2252AI	Samples
TLC2252AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2252AI	Samples
TLC2252AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLC2252AI	Samples
TLC2252AIPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2252A	Samples
TLC2252AIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2252A	Samples
TLC2252AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9564003Q2A TLC2252 AMFKB	Samples
TLC2252AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9564003QPA TLC2252AM	Samples
TLC2252AMUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9564003QHA TLC2252AM	Samples
TLC2252AQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2252A	Samples
TLC2252AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C2252A	Samples
TLC2252CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2252C	Samples
TLC2252CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2252C	Samples
TLC2252CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2252C	Samples
TLC2252CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2252CP	Samples
TLC2252CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2252	Samples
TLC2252CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2252	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2252ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252I	Samples
TLC2252IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252I	Samples
TLC2252IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252I	Samples
TLC2252IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLC2252IP	Samples
TLC2252MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9564001Q2A TLC2252 MFKB	Samples
TLC2252MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9564001QPA TLC2252M	Samples
TLC2252MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9564001QHA TLC2252M	Samples
TLC2254AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2254AI	Samples
TLC2254AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2254AI	Samples
TLC2254AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2254AI	Samples
TLC2254AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2254AI	Samples
TLC2254AIN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLC2254AIN	Samples
TLC2254AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2254A	Samples
TLC2254AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2254A	Samples
TLC2254AIPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2254A	Samples
TLC2254AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9564004Q2A TLC2254 AMFKB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2254AMWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9564004QD A TLC2254AMWB	Samples
TLC2254AQD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC2254A	Samples
TLC2254AQDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC2254A	Samples
TLC2254AQDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PJ2254A	Samples
TLC2254CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU Call TI	Level-1-260C-UNLIM	0 to 70	TLC2254C	Samples
TLC2254CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	0 to 70	TLC2254C	Samples
TLC2254CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2254C	Samples
TLC2254CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2254C	Samples
TLC2254CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2254CN	Samples
TLC2254CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2254	Samples
TLC2254CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2254	Samples
TLC2254ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2254I	Samples
TLC2254IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2254I	Samples
TLC2254IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2254I	Samples
TLC2254IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2254I	Samples
TLC2254IN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLC2254IN	Samples
TLC2254MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9564002Q2A TLC2254 MFKB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2254MWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9564002QD A TLC2254MWB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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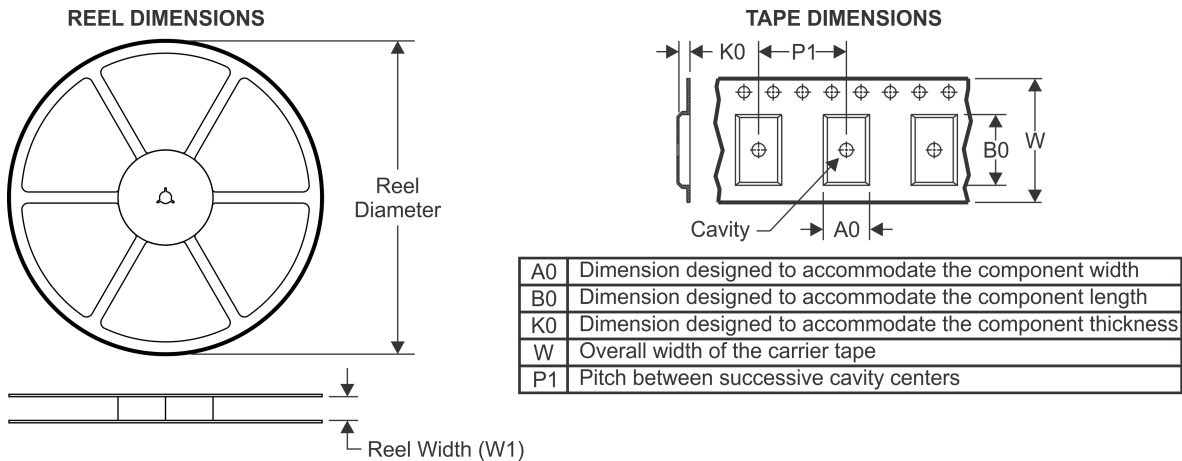
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OTHER QUALIFIED VERSIONS OF TLC2252, TLC2252A, TLC2252AM, TLC2252M, TLC2254, TLC2254A, TLC2254AM, TLC2254M :

- Catalog: [TLC2252A](#), [TLC2252](#), [TLC2254A](#), [TLC2254](#)
- Automotive: [TLC2252-Q1](#), [TLC2252A-Q1](#), [TLC2252A-Q1](#), [TLC2252-Q1](#), [TLC2254-Q1](#), [TLC2254A-Q1](#), [TLC2254A-Q1](#), [TLC2254-Q1](#)
- Enhanced Product: [TLC2252A-EP](#), [TLC2252A-EP](#), [TLC2254A-EP](#), [TLC2254A-EP](#)
- Military: [TLC2252M](#), [TLC2252AM](#), [TLC2254M](#), [TLC2254AM](#)

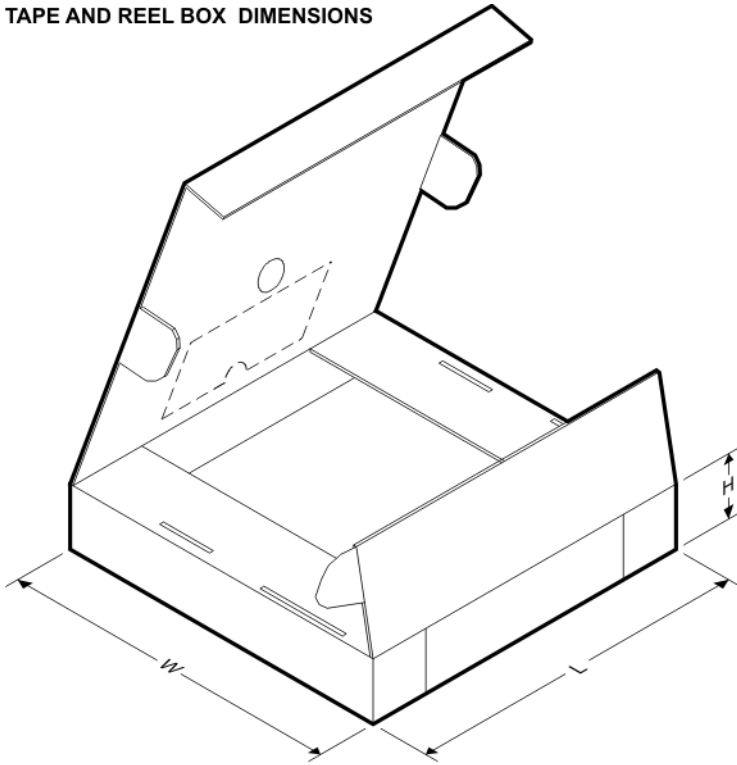
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
5962-9564003NXDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2252AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2252AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2252AQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TLC2252CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2252CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2252IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2254AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2254AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2254AQDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2254CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2254CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2254IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


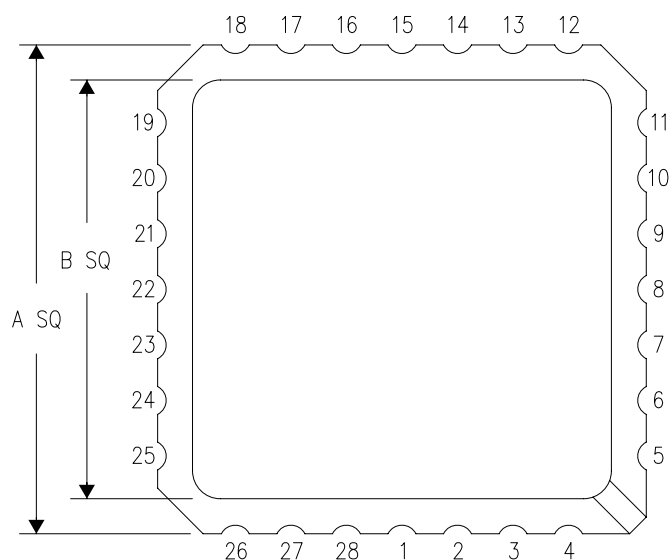
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
5962-9564003NXDR	SOIC	D	8	2500	350.0	350.0	43.0
TLC2252AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2252AIPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC2252AQDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2252CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2252CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC2252IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2254AIDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC2254AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2254AQDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC2254CDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC2254CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2254IDR	SOIC	D	14	2500	350.0	350.0	43.0

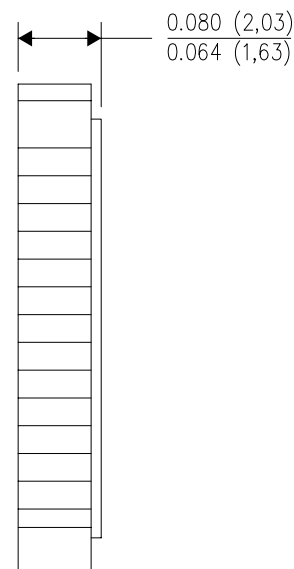
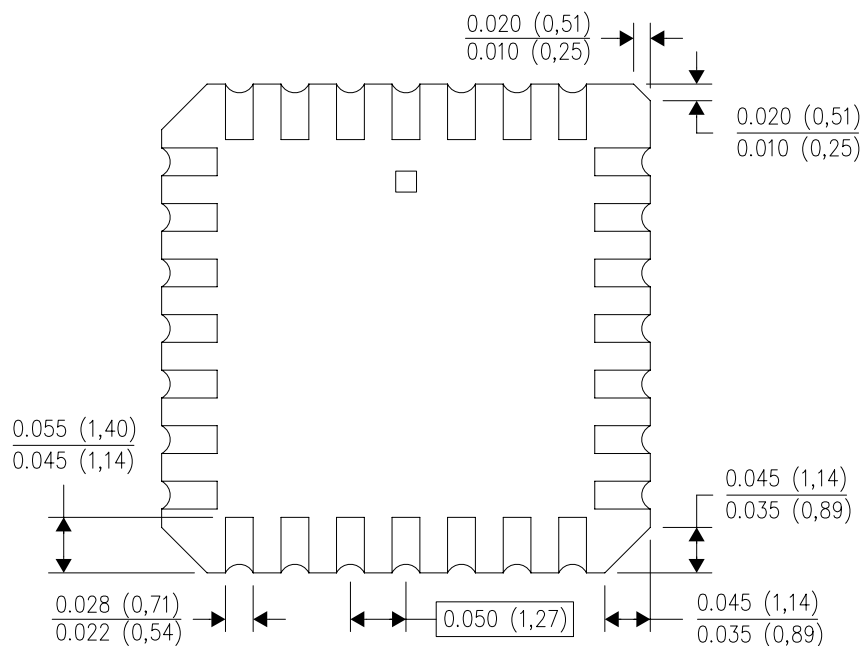
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

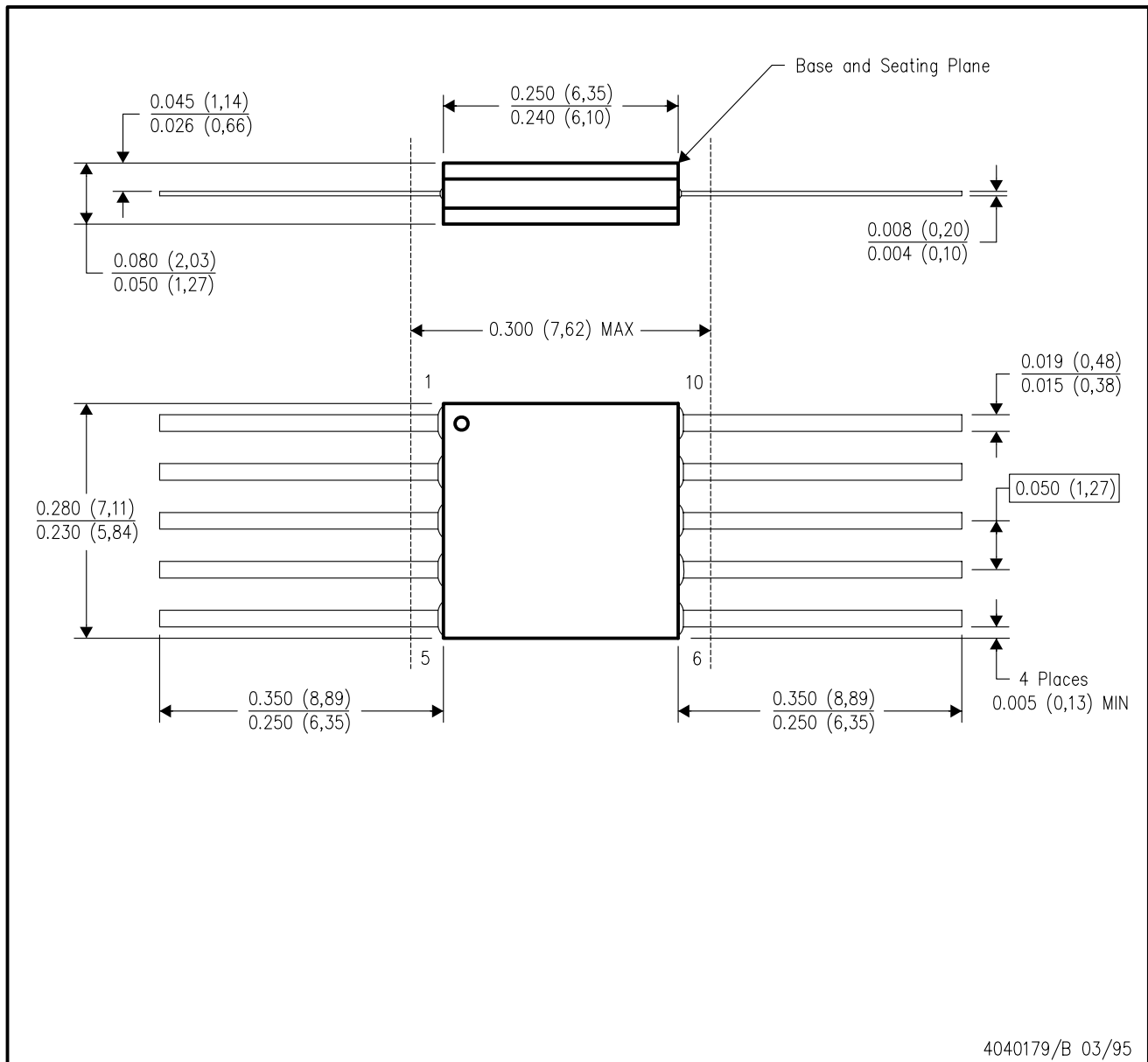


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

U (S-GDFP-F10)

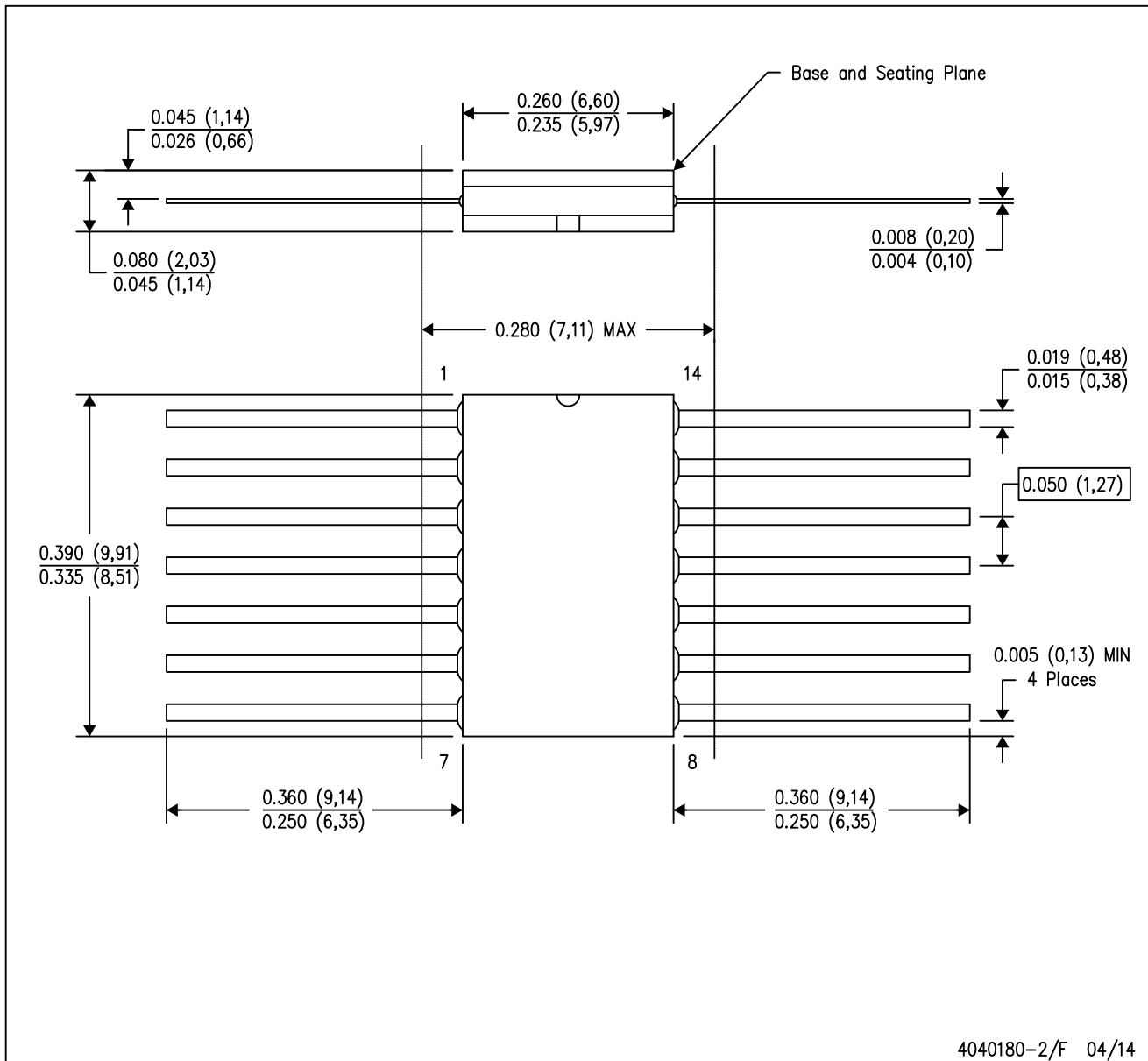
CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

W (R-GDFP-F14)

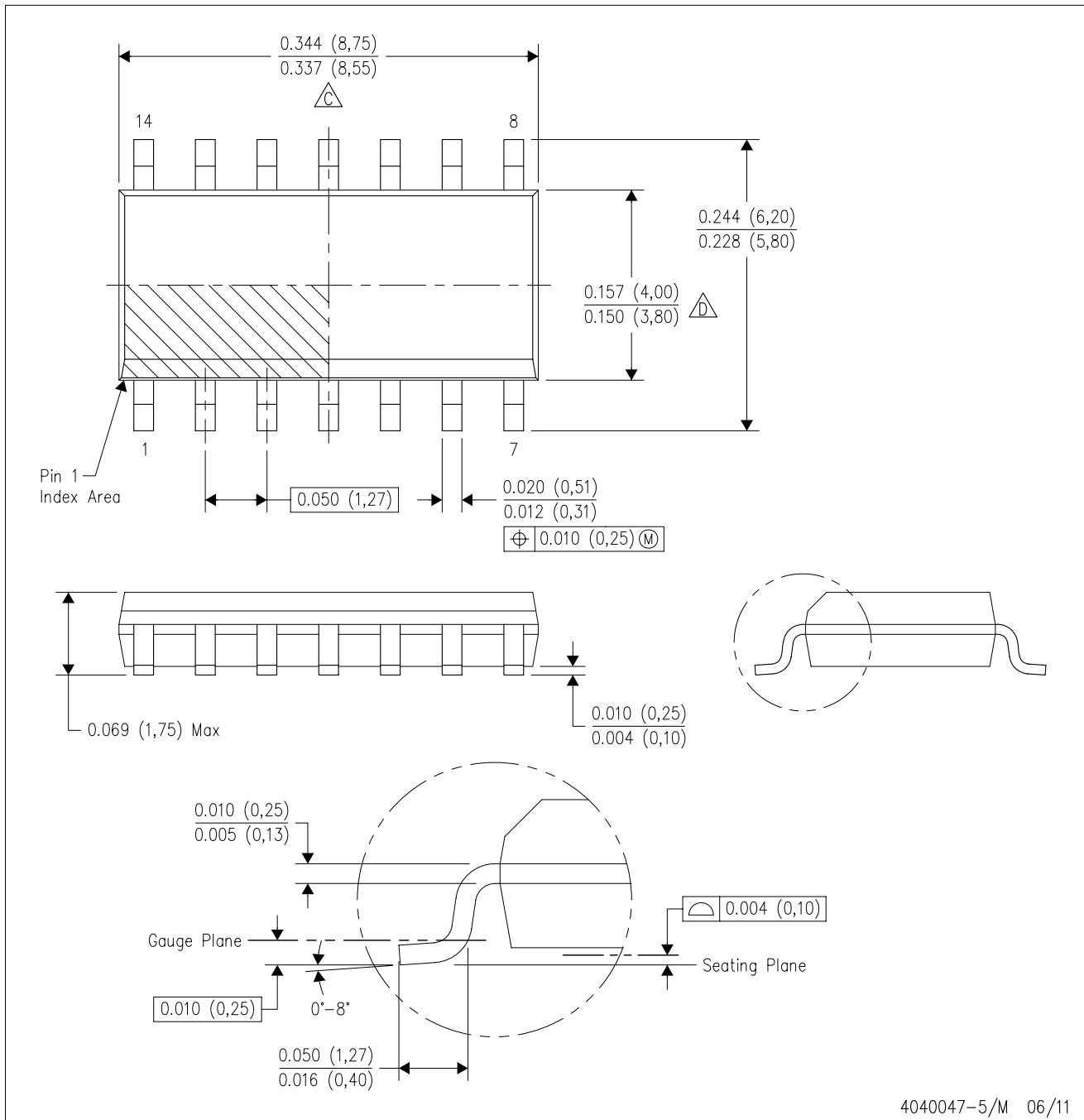
CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

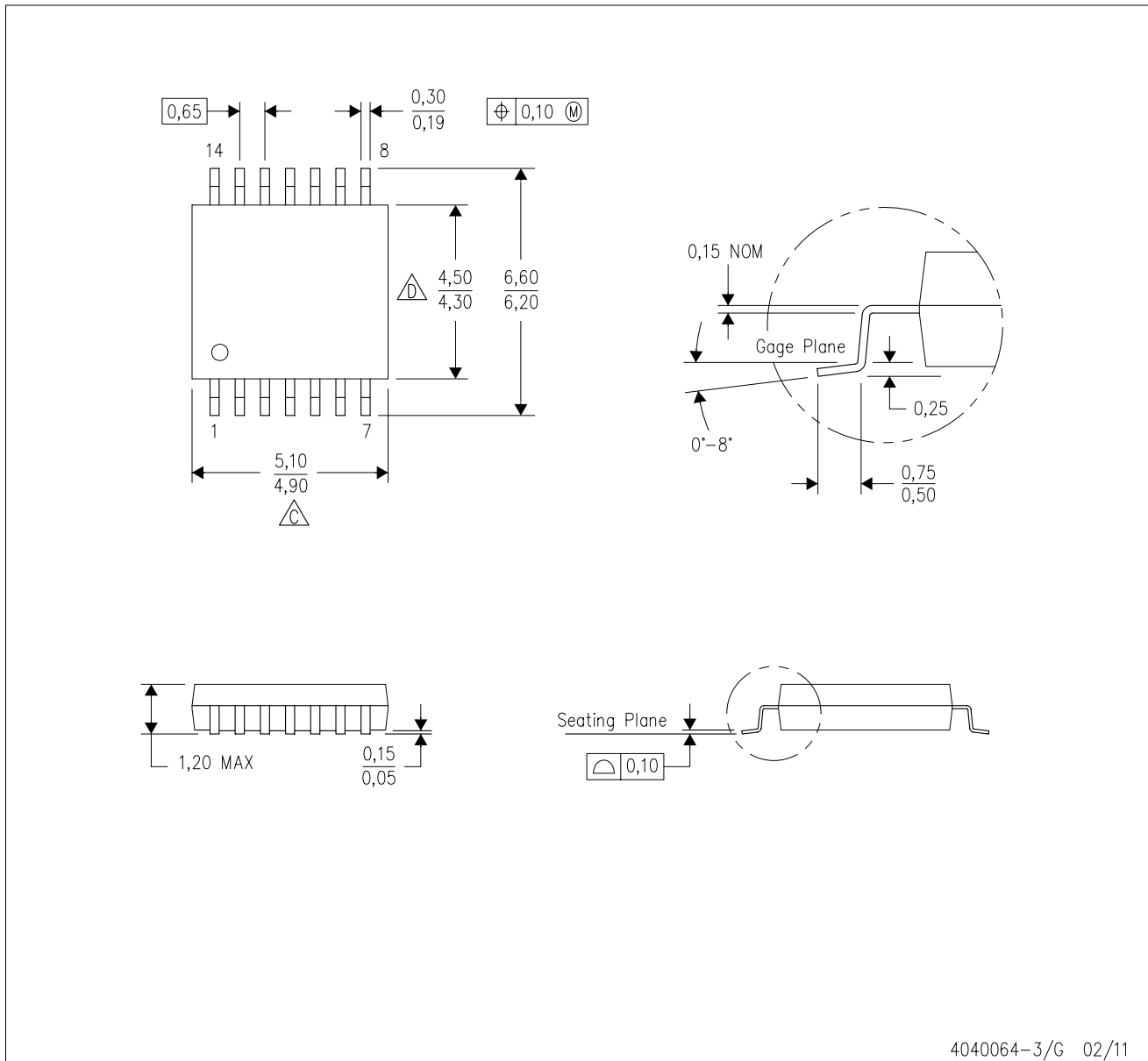


4211283-3/E 08/12



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

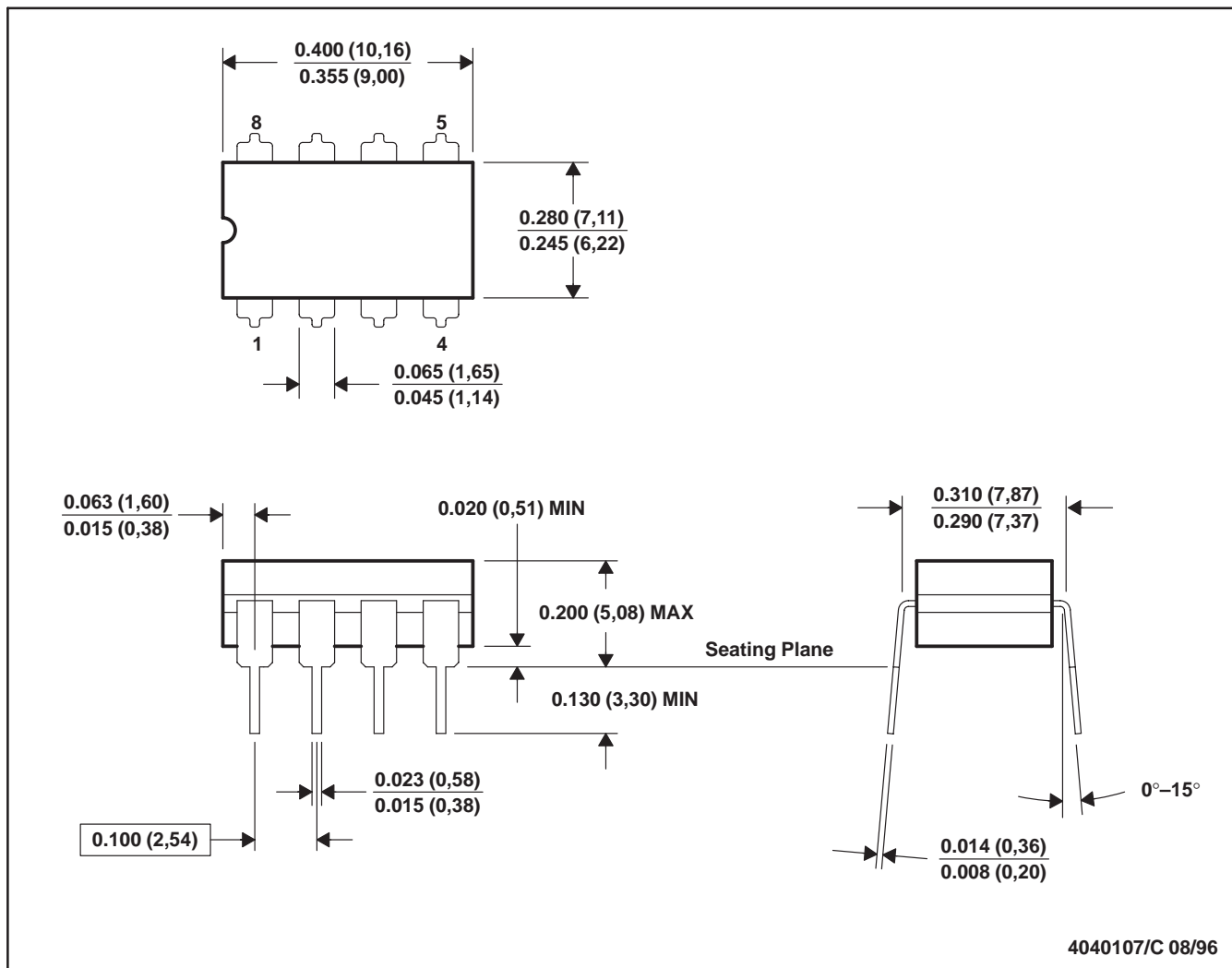
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

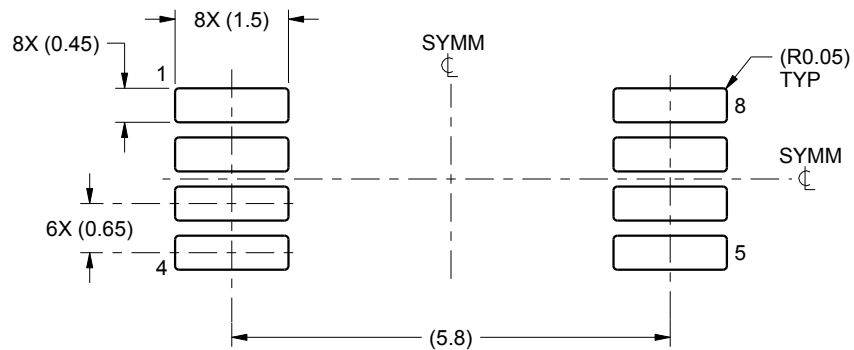
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

EXAMPLE BOARD LAYOUT

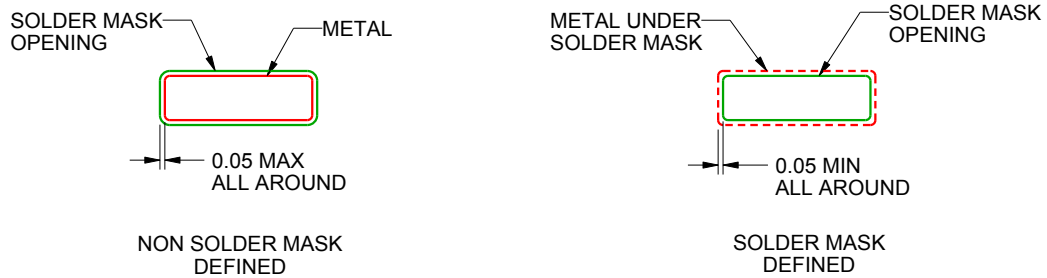
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

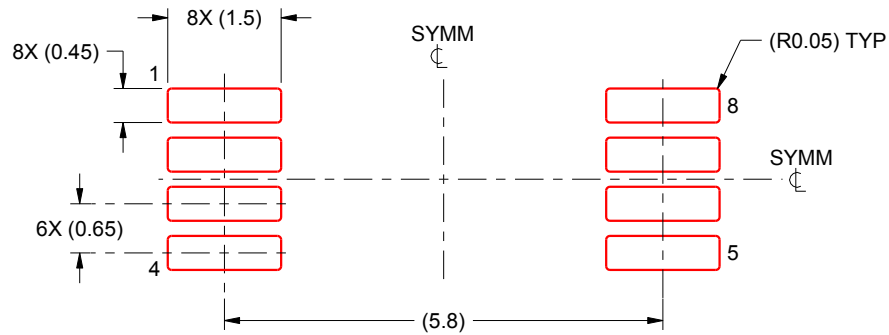
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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