THE DATASHEET OF

IR3575MTRPBF

FEATURES

- Peak efficiency up to 95% at 1.2V
- Integrated driver, control MOSFET, synchronous MOSFET and Schottky diode
- Input voltage (VIN) operating range up to 15V
- Output voltage range from 0.25V to Vcc-2.5V, or to 5.5V if internal current sense amplifier is not used
- Output current capability of 60A DC
- Operation up to 1.0MHz
- Integrated current sense amplifier
- VCC under voltage lockout
- Thermal flag
- Body-Braking® load transient support
- Diode-emulation high efficiency mode
- Compatible with 3.3V PWM logic and VCC tolerant
- Compliant with Intel DrMOS V4.0
- PCB footprint compatible with IR3550 and IR3551
- Enhanced top side cooling through exposed pad
- Small 6mm x 6mm x 0.9mm PQFN package
- Lead free RoHS compliant package

APPLICATIONS

- Voltage Regulators for CPUs, GPUs, and DDR memory arrays
- High current, low profile DC-DC converters

DESCRIPTION

The IR3575 exposed-top integrated PowIRstage® is a synchronous buck gate driver co-packed with a control MOSFET and a synchronous MOSFET with integrated Schottky diode. It is optimized internally for PCB layout, heat transfer and driver/MOSFET timing. Custom designed gate driver and MOSFET combination enables higher efficiency at lower output voltages required by cutting edge CPU, GPU and DDR memory designs.

Up to 1.0MHz switching frequency enables high performance transient response, allowing miniaturization of output inductors, as well as input and output capacitors while maintaining industry leading efficiency. The IR3575's superior efficiency enables smallest size and lower solution cost. The IR3575 PCB footprint is compatible with the IR3550 (60A), IR3551 (50A) and IR3553 (40A).

Integrated current sense amplifier achieves superior current sense accuracy and signal to noise ratio vs. best-in-class controller based Inductor DCR sense methods.

The IR3575 incorporates the Body-Braking® feature which enables reduction of output capacitors. Synchronous diode emulation mode in the IR3575 removes the zero-current detection burden from the PWM controller and increases system light-load efficiency.

The IR3575 is optimized specifically for CPU core power delivery in server applications. The ability to meet the stringent requirements of the server market also makes the IR3575 ideally suited to powering GPU and DDR memory designs and other high current applications.

BASIC APPLICATION

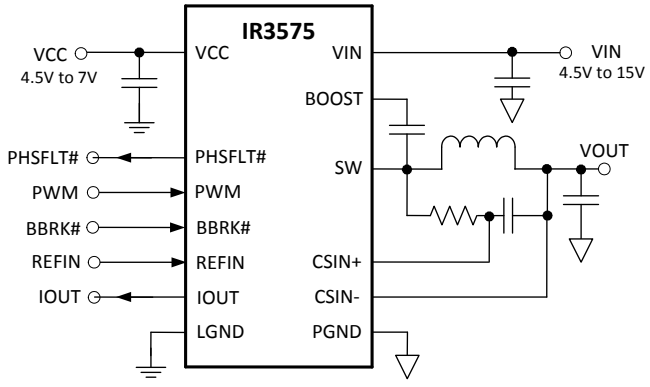


Figure 1: IR3575 Basic Application Circuit

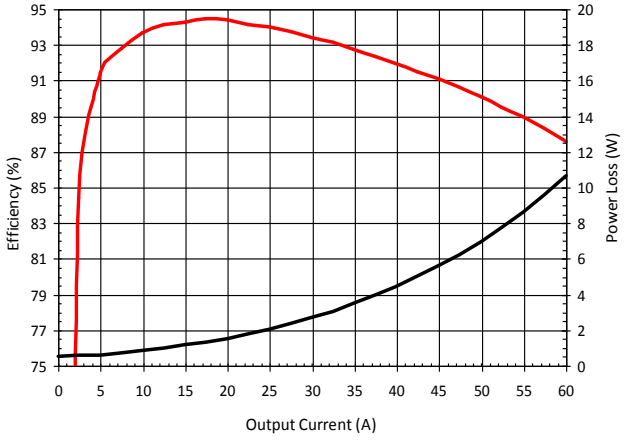


Figure 2: Typical IR3575 Efficiency & Power Loss (See Note 2 on Page 8)

PINOUT DIAGRAM

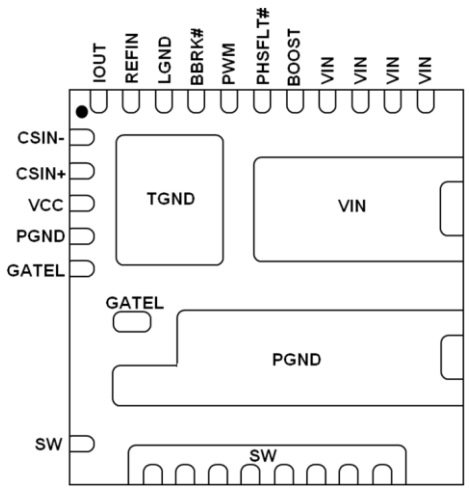


Figure 3: IR3575 Pin Diagram, Top View

ORDERING INFORMATION

Package	Tape & Reel Qty	Part Number
PQFN, 32 Lead 6mm x 6mm	3000	**IR3575MTRPBF**
Package	**Qty**	**Part Number**
PQFN, 32 Lead 6mm x 6mm	100	**IR3575MPBF**

TYPICAL APPLICATION DIAGRAM

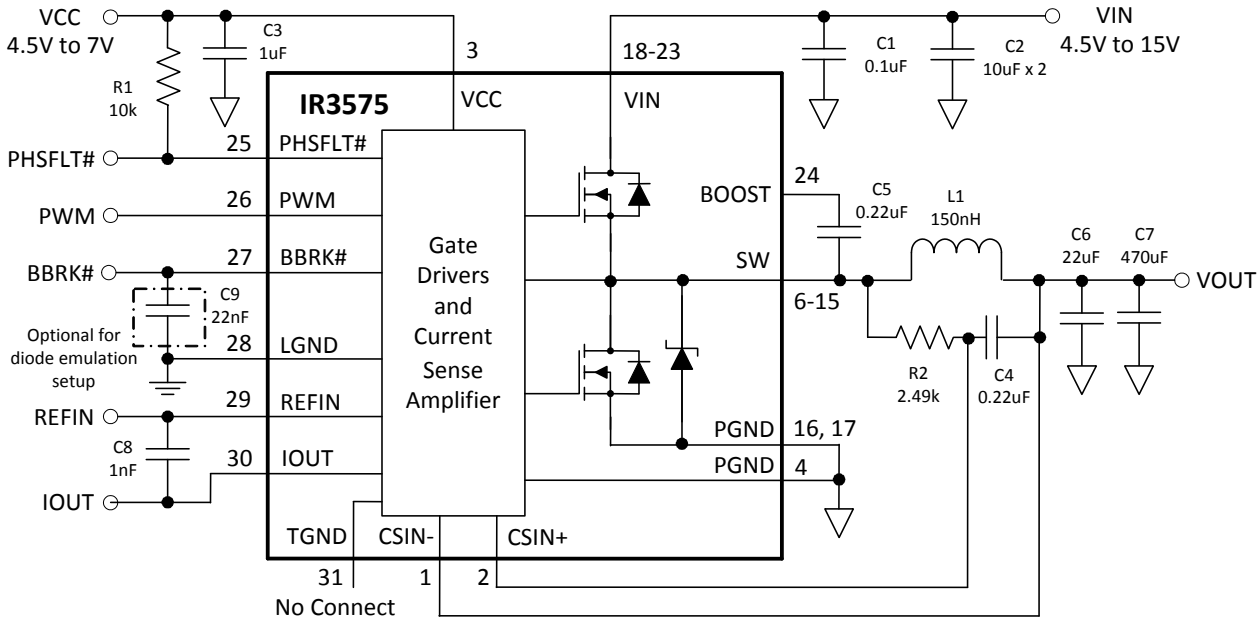


Figure 4: Application Circuit with Current Sense Amplifier

TYPICAL APPLICATION DIAGRAM (CONTINUED)

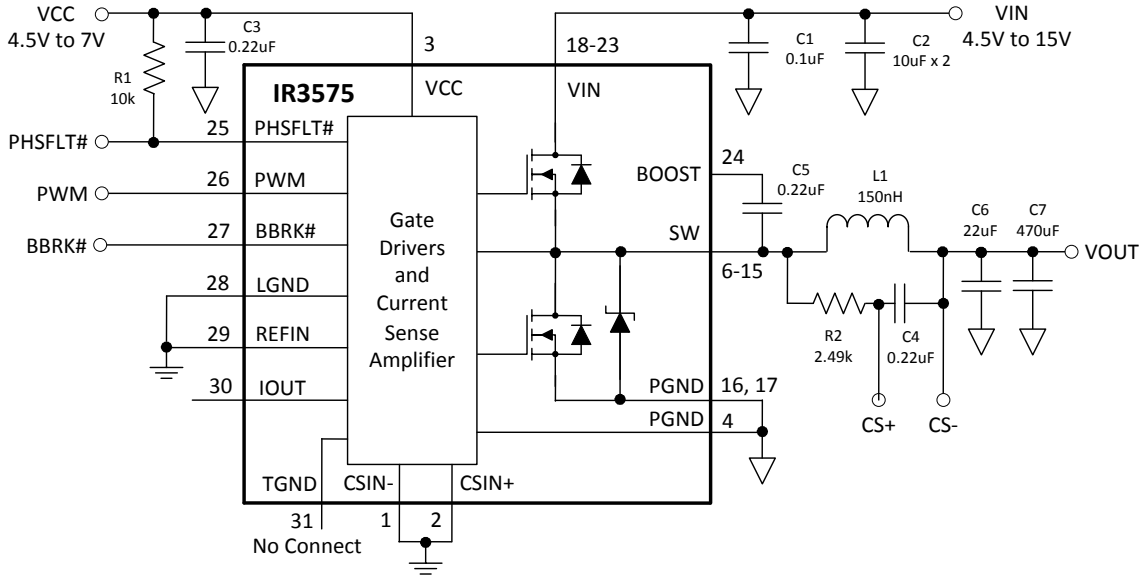


Figure 5: Application Circuit without Current Sense Amplifier

FUNCTIONAL BLOCK DIAGRAM

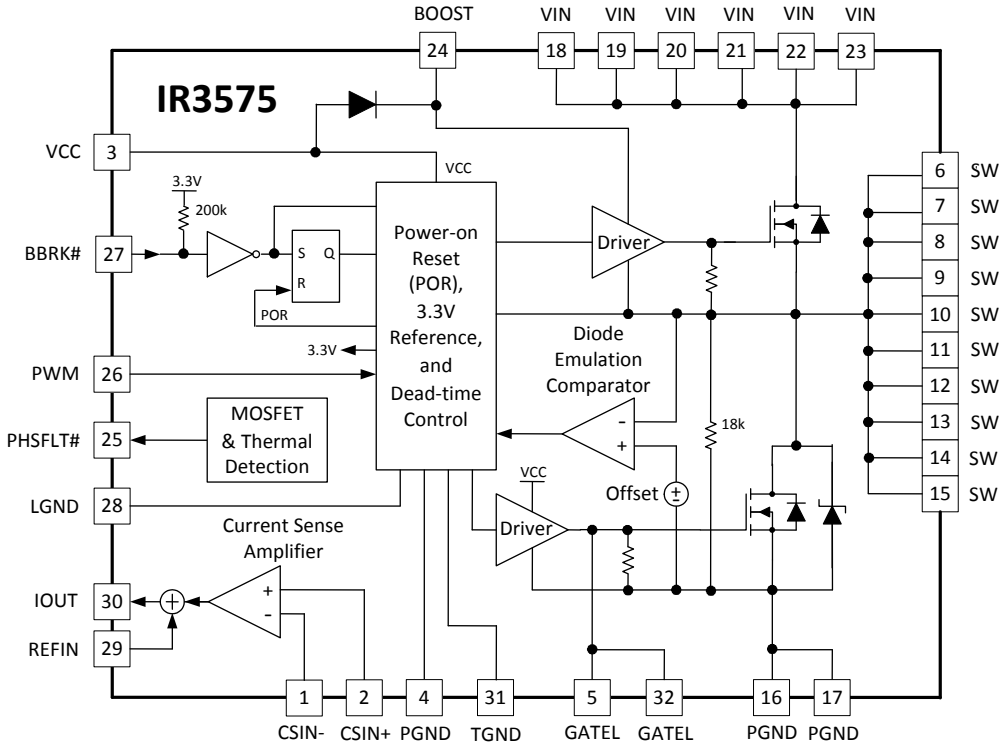


Figure 6: IR3575 Functional Block Diagram

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	CSIN-	Inverting input to the current sense amplifier. Connect to LGND if the current sense amplifier is not used.
2	CSIN+	Non-Inverting input to the current sense amplifier. Connect to LGND if the current sense amplifier is not used.
3	VCC	Bias voltage for control logic. Connect a minimum 1uF cap between VCC and PGND (pin 4) if current sense amplifier is used. Connect a minimum 0.22uF cap between VCC and PGND (pin 4) if current sense amplifier is not used.
4, 16, 17	PGND	Power ground of MOSFET driver and the synchronous MOSFET. MOSFET driver signal is referenced to this pin.
5, 32	GATEL	Low-side MOSFET driver pins that can be connected to a test point in order to observe the waveform.
6 – 15	SW	Switch node of synchronous buck converter.
18 – 23	VIN	High current input voltage connection. Recommended operating range is 4.5V to 15V. Connect at least two 10uF 1206 ceramic capacitors and a 0.22uF 0402 ceramic capacitor. Place the capacitors as close as possible to VIN pins and PGND pins (16-17). The 0.22uF 0402 capacitor should be on the same side of the PCB as the IR3575.
24	BOOST	Bootstrap capacitor connection. The bootstrap capacitor provides the charge to turn on the control MOSFET. Connect a minimum 0.22µF capacitor from BOOST to SW pin. Place the capacitor as close to BOOST pin as possible and minimize parasitic inductance of PCB routing from the capacitor to SW pin.
25	PHSFLT#	Open drain output of the phase fault circuits. Connect to an external pull-up resistor. Output is low when a MOSFET fault or over temperature condition is detected.
26	PWM	3.3V logic level tri-state PWM input and 7V tolerant. “High” turns the control MOSFET on, and “Low” turns the synchronous MOSFET on. “Tri-state” turns both MOSFETs off in Body-Braking® mode. In diode emulation mode, “Tri-state” activates internal diode emulation control. See “PWM Tri-state Input” Section for further details about the PWM Tri-State functions.
27	BBRK#	3.3V logic level input and 7V tolerant with internal weak pull-up to 3.3V. Logic low disables both MOSFETs. Pull up to VCC directly or by a 4.7kΩ resistor if Body-Braking® is not used. The second function of the BBRK# pin is to select diode emulatiom mode. Pulling BBRK# low at least 20ns after VCC passes its UVLO threshold selects internal diode emulation control. See “Body-Braking® Mode” Section for further details.
28	LGND	Signal ground. Driver control logic, analog circuits and IC substrate are referenced to this pin.
29	REFIN	Reference voltage input from the PWM controller. IOUT signal is referenced to the voltage on this pin. Connect to LGND if the current sense amplifier is not used.
30	IOUT	Current output signal. Voltage on this pin is equal to V(REFIN) + 32.5 * [V(CSIN+) – V(CSIN-)]. Float this pin if the current sense amplifier is not used.
31	TGND	This pin is connected to internal power and signal ground of the driver. For best performance of the current sense amplifier, TGND must be electrically isolated from Power Ground (PGND) and Signal Ground (LGND) in the PCB layout. Connect to PGND if the current sense amplifier is not used.
Exposed Pad	SW	Exposed pad on top side of the package. Connect to a heat sink through insulated thermal material to improve the thermal performance of the package.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PIN Number	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	CSIN-	VCC + 0.3V	-0.3V	1mA	1mA
2	CSIN+	VCC + 0.3V	-0.3V	1mA	1mA
3	VCC	8V	-0.3V	NA	5A for 100ns, 200mA DC
4	PGND	0.3V	-0.3V	15mA	15mA
5, 32	GATEL	VCC + 0.3V	-3V for 20ns, -0.3V DC	1A for 100ns, 200mA DC	1A for 100ns, 200mA DC
6-15	SW [2]	25V	-5V for 20ns, -0.3V DC	65A RMS, 90A Peak	30A RMS, 35A Peak
16, 17	PGND	NA	NA	30A RMS, 35A Peak	65A RMS, 90A Peak
18-23	VIN [2]	25V	-0.3V	5A RMS	25A RMS, 30A Peak
24	BOOST [1]	33V	-0.3V	1A for 100ns, 100mA DC	5A for 100ns, 100mA DC
25	PHSFLT#	VCC + 0.3V	-0.3V	1mA	20mA
26	PWM	VCC + 0.3V	-0.3V	1mA	1mA
27	BBRK#	VCC + 0.3V	-0.3V	1mA	1mA
28	LGND	0.3V	-0.3V	15mA	15mA
29	REFIN	3.5V	-0.3V	1mA	1mA
30	IOUT	VCC + 0.3V	-0.3V	5mA	5mA
31	TGND	0.3V	-0.3V	NA	NA

Note:
1. Maximum BOOST – SW = 8V.
2. Maximum VIN – SW = 25V.
3. All the maximum voltage ratings are referenced to PGND (Pins 16 and 17).

THERMAL INFORMATION	
Thermal Resistance, Junction to Top (θ_{JC_TOP})	0.5 °C/W
Thermal Resistance, Junction to PCB (pin 17) (θ_{JB})	1.7 °C/W
Thermal Resistance (θ_{JA})[1]	19.1 °C/W
Maximum Operating Junction Temperature	-40 to 150°C
Maximum Storage Temperature Range	-65°C to 150°C
ESD rating	HBM Class 1B JEDEC Standard
MSL Rating	3
Reflow Temperature	260°C

Note:
1. Thermal Resistance (θ_{JA}) is measured with the component mounted on a high effective thermal conductivity test board in free air. Refer to International Rectifier Application Note AN-994 for details.

ELECTRICAL SPECIFICATIONS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

PARAMETER	SYMBOL	MIN	MAX	UNIT
Recommended VIN Range	VIN	4.5	15	V
Recommended VCC Range	VCC	4.5	7	V
Recommended REFIN Range	REFIN	0.25	VCC - 2.5	V
Recommended Switching Frequency	f_{SW}	200	1000	kHz
Recommended Operating Junction Temperature	T_J	-40	125	°C

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Efficiency and Maximum Current						
IR3575 Peak Efficiency Note 1	η	Note 2. See Figure 2.		94.5		%
		Note 3. See Figure 7.		93.5		%
IR3575 Maximum DC Current Note 1	I_{DC_MAX}	Note 2.		60		A
IR3575 Maximum Peak Current Note 1	I_{PK_MAX}	Note 4. 5ms load pulse width, 10% load duty cycle.		90		A
PWM Comparator						
PWM Input High Threshold	V_{PWM_HIGH}	PWM Tri-state to High	2.5			V
PWM Input Low Threshold	V_{PWM_LOW}	PWM Tri-state to Low			0.8	V
PWM Tri-state Float Voltage	V_{PWM_TRI}	PWM Floating	1.2	1.65	2.1	V
Hysteresis	V_{PWM_HYS}	Active to Tri-state or Tri-state to Active, Note 1	65	76	100	mV
Tri-state Propagation Delay	t_{PWM_DELAY}	PWM Tri-state to Low transition to GATEL >1V		38		ns
		PWM Tri-state to High transition to GATEH >1V		18		ns
PWM Sink Impedance	R_{PWM_SINK}		3.67	5.1	8.70	kΩ
PWM Source Impedance	R_{PWM_SOURCE}		3.67	5.1	8.70	kΩ
Internal Pull up Voltage	V_{PWM_PULLUP}	VCC > UVLO		3.3		V
Minimum Pulse Width	t_{PWM_MIN}	Note 1		41	58	ns
Current Sense Amplifier						
CSIN+/- Bias Current	I_{CSIN_BIAS}		-100	0	100	nA
CSIN+/- Bias Current Mismatch	I_{CSIN_BIASMM}		-50	0	50	nA
Calibrated Input Offset Voltage	V_{CSIN_OFFSET}	Self-calibrated offset, 0.5V ≤ V(REFIN) ≤ 2.25V		±450		µV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Gain	G_{CS}	0.5V ≤ V(REFIN) ≤ 2.25V, -5mV ≤ [V(CSIN+) –V(CSIN-)] ≤ 25mV, 0°C ≤ T_J ≤ 125°C	30.0	32.5	35.0	V/V
		0.5V ≤ V(REFIN) ≤ 2.25V, -5mV ≤ [V(CSIN+) – V(CSIN-)] ≤ 25mV	30.0	33.0	36.0	V/V
		0.8V ≤ V(REFIN) ≤ 2.25V, -10mV ≤[V(CSIN+)–V(CSIN-)] ≤ 25mV	28.0	31.5	35.0	V/V
Unity Gain Bandwidth	f_{BW}	C(IOUT) = 10pF. Measure at IOUT. Note 1	4.8	6.8	8.8	MHz
Slew Rate	S_R			6		V/µs
Differential Input Range	V_{D_IN}	0.8V ≤ V(REFIN) ≤ 2.25V,	-10		25	mV
Common Mode Input Range	V_{C_IN}		0		VCC-2.5	V
Output Impedance (IOUT)	R_{CS_OUT}			62	200	Ω
IOUT Sink Current	I_{CS_SINK}	Driving external 3 kΩ	0.5	0.8	1.1	mA
Diode Emulation Mode Comparator						
Input Offset Voltage	V_{IN_OFFSET}	Note 1	-12	-3	3	mV
Leading Edge Blanking Time	t_{BLANK}	V(GATEL)>1V Starts Timer	50	150	200	ns
Negative Current Time-Out	t_{NC_TOUT}	PWM = Tri-State, V(SW) ≤ -10mV	12	28	46	µs
Digital Input – BBRK#						
Input voltage high	$V_{BBRK\#\_IH}$		2.0			V
Input voltage low	$V_{BBRK\#\_IL}$				0.8	V
Internal Pull Up Resistance	$R_{BBRK\#\_PULLUP}$	VCC > UVLO	69	200	338	kΩ
Internal Pull Up Voltage	$V_{BBRK\#\_PULLUP}$	VCC > UVLO		3.3		V
Digital Output – PHSFLT#						
Output voltage high	$V_{PHASFLT\#\_OH}$				VCC	V
Output voltage low	$V_{PHASFLT\#\_OL}$	4mA		150	300	mV
Input current	$I_{PHASFLT\#\_IN}$	V(PHSFLT#) = 5.5V		0	1	µA
Phase Fault Detection						
Control MOSFET Short Threshold	V_{CM_SHORT}	Measure from SW to PGND		3.3		V
Synchronous MOSFET Short Threshold	V_{SM_SHORT}	Measure from SW to PGND	150	200	250	mV
Synchronous MOSFET Open Threshold	V_{SM_OPEN}	Measure from SW to PGND	-250	-200	-150	mV
Propagation Delay	t_{PROP}	PWM High to Low Cycles		15		Cycle
Thermal Flag						
Rising Threshold	T_{RISE}	PHSFLT# Drives Low, Note 1		160		°C
Falling Threshold	T_{FALL}	Note 1		135		°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Bootstrap Diode						
Forward Voltage	V_{FWD}	I(BOOST) = 30mA, VCC=6.8V	360	520	920	mV
VCC Under Voltage Lockout						
Start Threshold	V_{VCC_START}		3.3	3.7	4.1	V
Stop Threshold	V_{VCC_STOP}		3.0	3.4	3.8	V
Hysteresis	V_{VCC_HYS}		0.2	0.3	0.4	V
General						
VCC Supply Current	I_{VCC}	VCC = 4.5V to 7V	4	8	12	mA
VIN Supply Leakage Current	I_{VIN}	VIN = 20V, 125C, V(PWM) = Tri-State			1	µA
BOOST Supply Current	I_{BOOST}	4.75V < V(BOOST)-V(SW) < 8V	0.5	1.5	3.0	mA
REFIN Bias Current	I_{REFIN}		-1.5	0	1	µA
SW Floating Voltage	V_{SW_FLOAT}	V(PWM) = Tri-State		0.2	0.4	V
SW Pull Down Resistance	$R_{SW\_PULLDOWN}$	BBRK# is Low or VCC = 0V		18		kΩ

Notes

1. Guaranteed by design but not tested in production
2. V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 300kHz, L=210nH (0.2mΩ), VCC=6.8V, C_{IN}=47uF x 4, C_{OUT} =470uF x3, 400LFM airflow, no heat sink, 25°C ambient temperature, and 8-layer PCB of 3.7" (L) x 2.6" (W). PWM controller loss and inductor loss are not included.
3. V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), VCC=7V, C_{IN}=47uF x 4, C_{OUT} =470uF x3, no airflow, no heat sink, 25°C ambient temperature, and 8-layer PCB of 3.7" (L) x 2.6" (W). PWM controller loss and inductor loss are not included.
4. V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=210nH (0.2mΩ, 13mm x 13mm x 8mm), VCC=6.8V, C_{IN}=47uF x 4, C_{OUT} =470uF x3, no heat sink, 25°C ambient temperature, 8-layer PCB of 3.7" (L) x 2.6" (W), 5ms load pulse width, 10% load duty cycle, and IR3575 junction temerature below 125°C.

TYPICAL OPERATING CHARACTERISTICS

Circuit of Figure 32, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), VCC=7V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

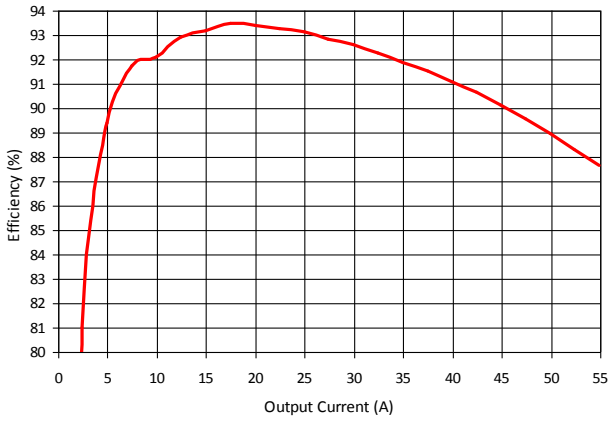


Figure 7: Typical IR3575 Efficiency

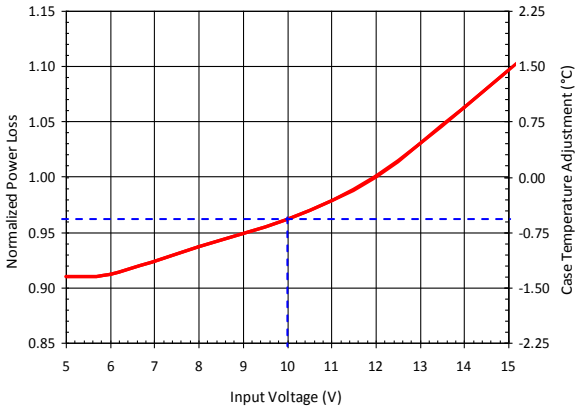


Figure 10: Normalized Power Loss vs. Input Voltage

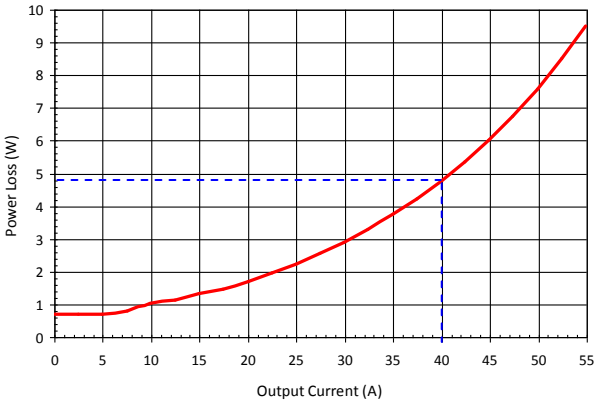


Figure 8: Typical IR3575 Power Loss

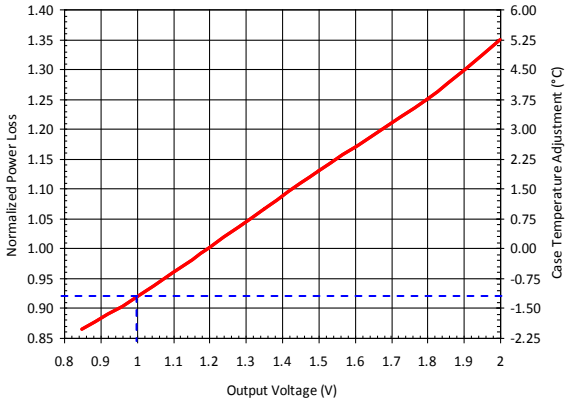


Figure 11: Normalized Power Loss vs. Output Voltage

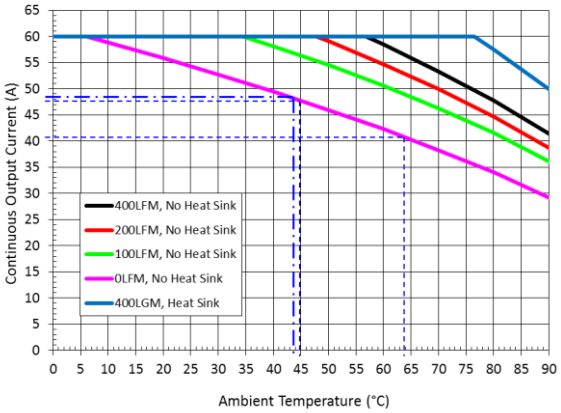


Figure 9: Thermal Derating Curve, T_{CASE} <= 125°C

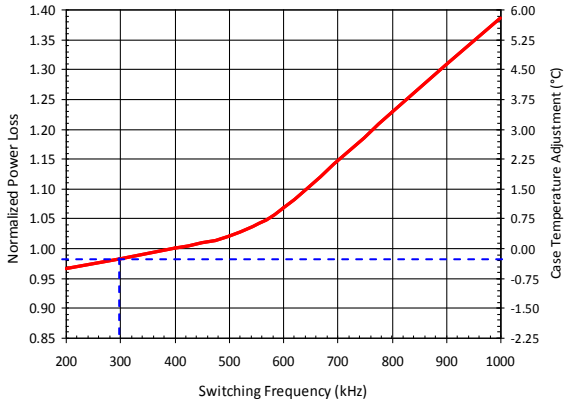


Figure 12: Normalized Power Loss vs. Switching Frequency

TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

Circuit of Figure 32, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), VCC=7V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

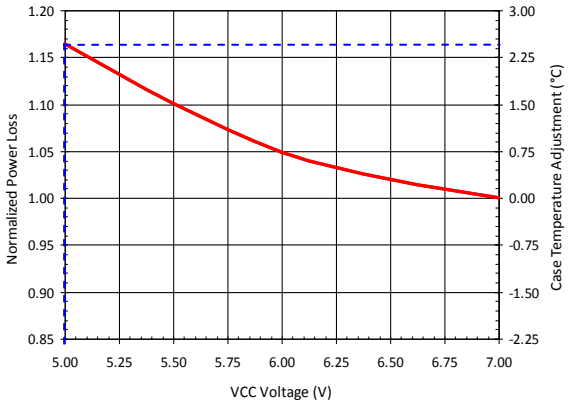


Figure 13: Normalized Power Loss vs. VCC Voltage

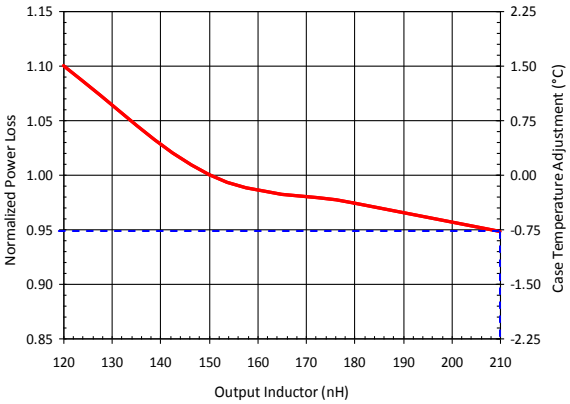


Figure 14: Power Loss vs. Output Inductor

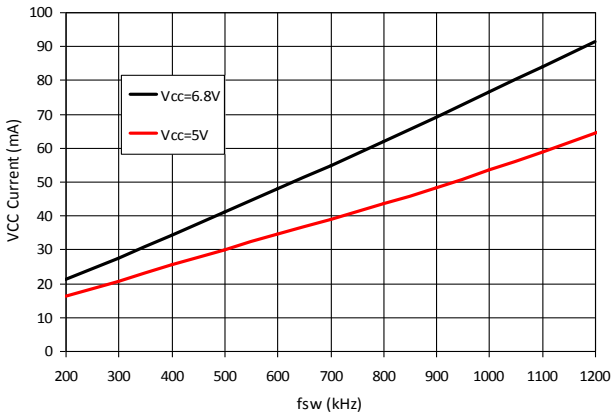


Figure 15: VCC Current vs. Switching Frequency

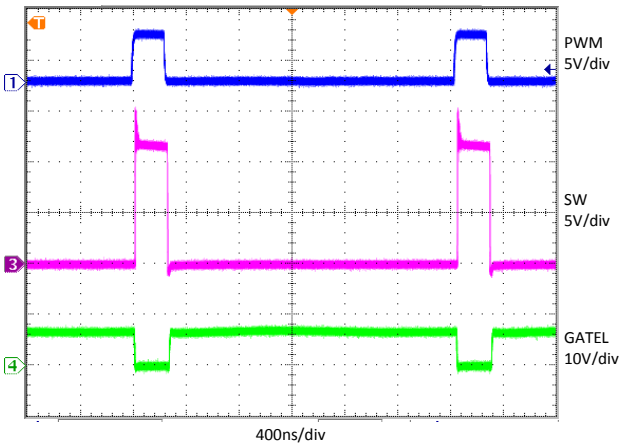


Figure 16: Switching Waveform, I_{OUT} = 0A

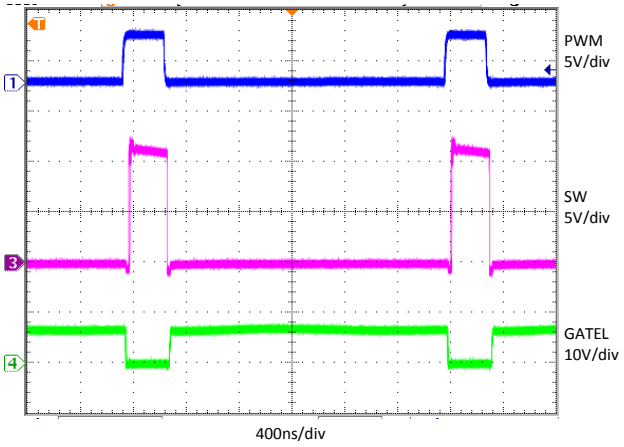


Figure 17: Switching Waveform, I_{OUT} = 50A

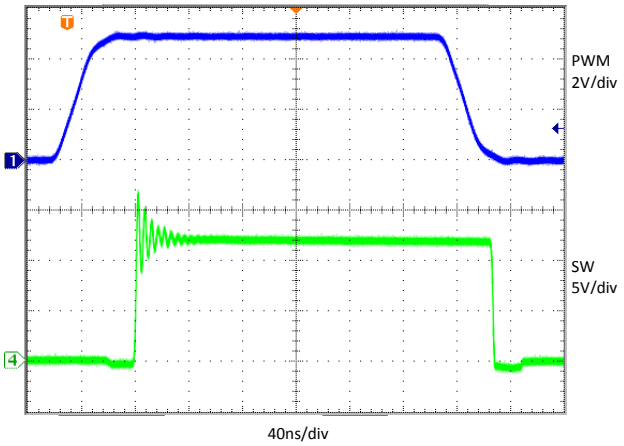


Figure 18: PWM to SW Delays, I_{OUT} = 10A

TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

Circuit of Figure 32, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), VCC=7V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

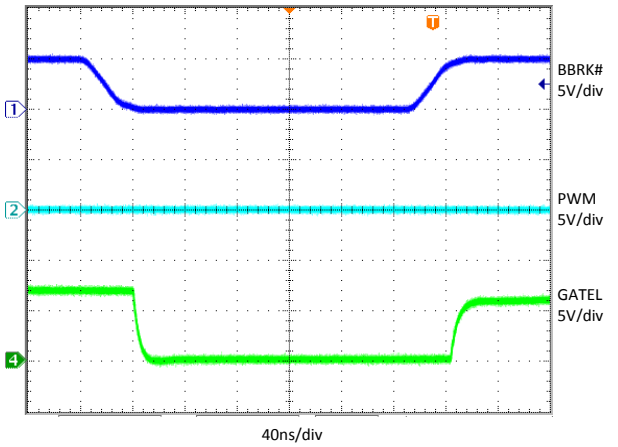


Figure 19: Body-Braking® Delays

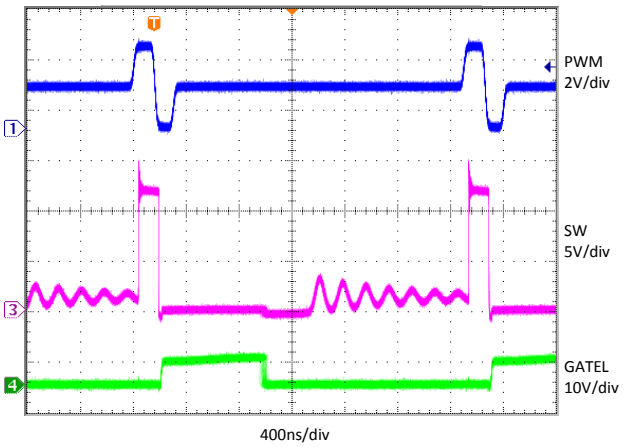


Figure 22: Diode Emulation Mode, I_{OUT} = 3A

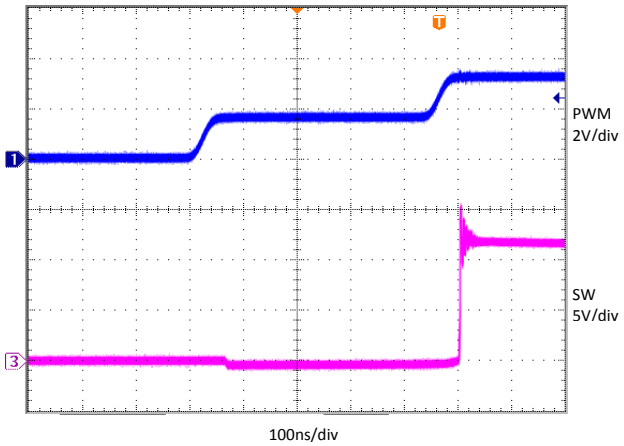


Figure 20: PWM Tri-state Delays, I_{OUT} = 10A

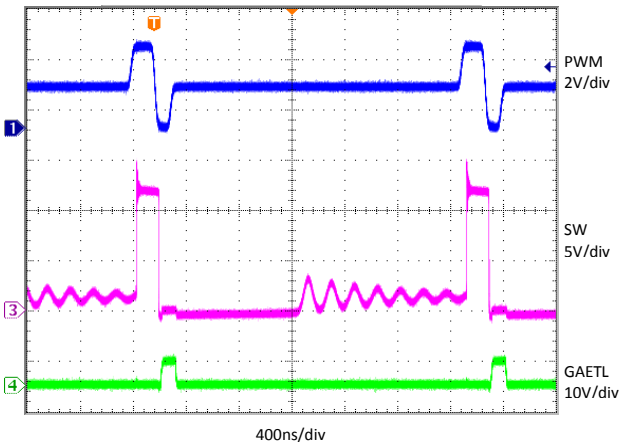


Figure 23: Body-Braking® Mode, I_{OUT} = 3A

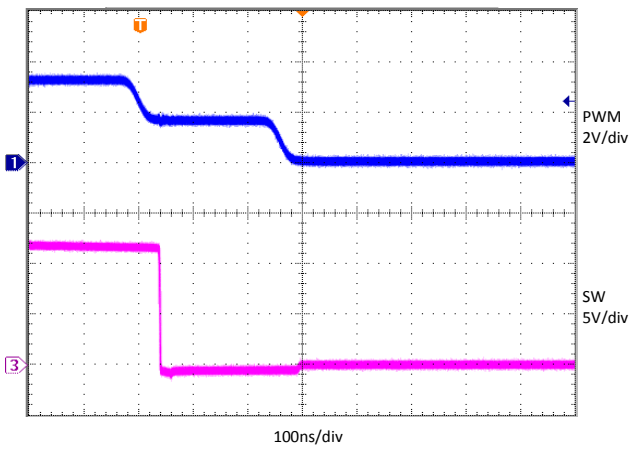


Figure 21: PWM Tri-state Delays, I_{OUT} = 10A

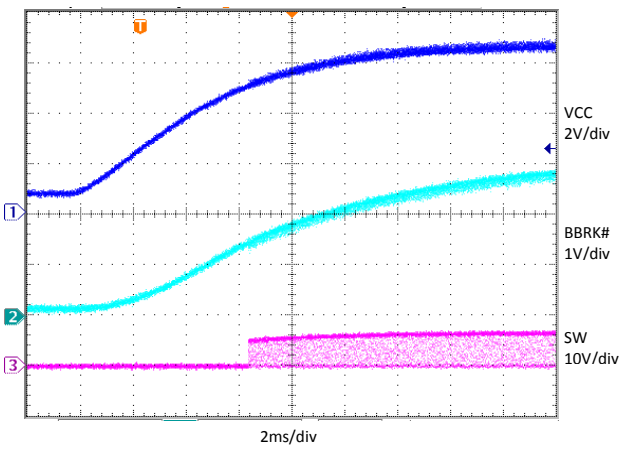


Figure 24: Diode Emulation Setup through BBRK# Capacitor

TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

Circuit of Figure 32, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), VCC=7V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

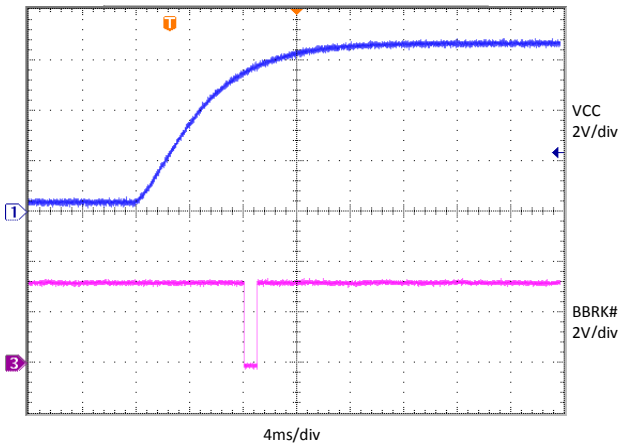


Figure 25: Diode Emulation Setup through BBRK# Input

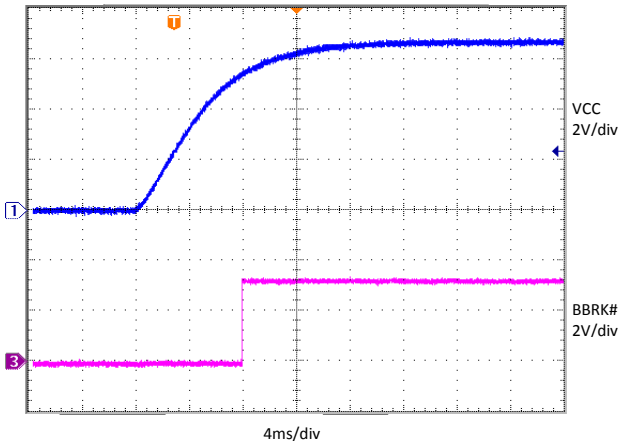


Figure 26: Diode Emulation Setup through BBRK# Input

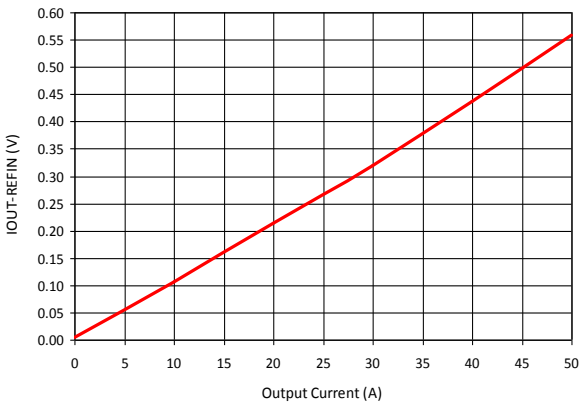


Figure 27: Current Sense Amplifier Output vs. Current

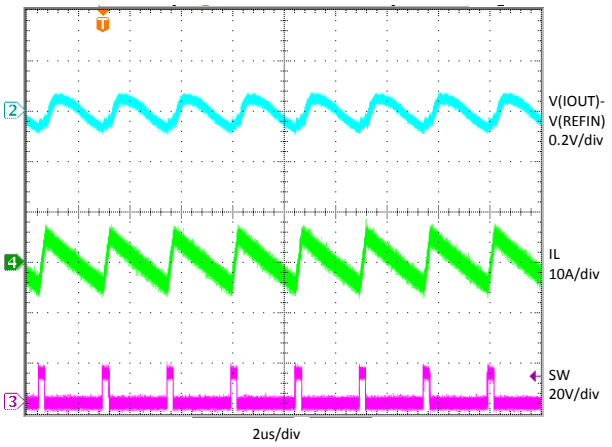


Figure 28: Current Sense Amplifier Output, I_{OUT} = 0A

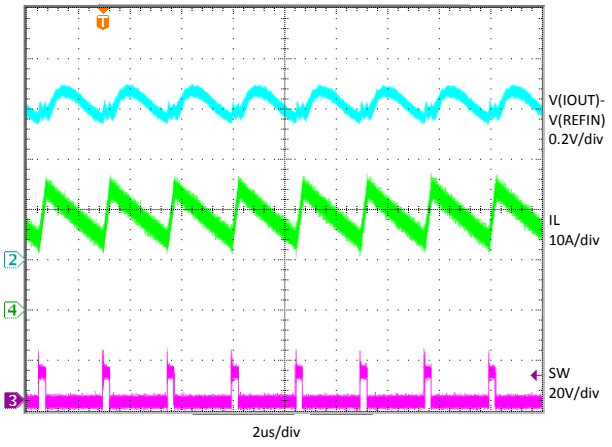


Figure 29: Current Sense Amplifier Output, I_{OUT} = 20A

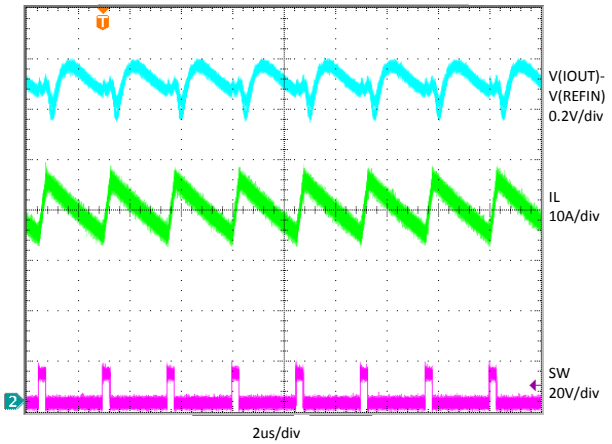


Figure 30: Current Sense Amplifier Output, I_{OUT} = 40A

THEORY OF OPERATION

DESCRIPTION

The IR3575 Exposed-top PowIRstage® is a synchronous buck driver with co-packed MOSFETs with integrated Schottky diode, which provides system designers with ease of use and flexibility required in cutting edge CPU, GPU and DDR memory power delivery designs and other high-current low-profile applications.

The IR3575 is designed to work with a PWM controller. It incorporates a continuously self-calibrated current sense amplifier, optimized for use with inductor DCR sensing. The current sense amplifier provides signal gain and noise immunity, supplying multiphase systems with a superior design toolbox for programmed impedance designs.

The IR3575 provides a phase fault signal capable of detecting open or shorted MOSFETs, or an over-temperature condition in the vicinity of the power stage.

The IR3575 accepts an active low Body-Braking® input which disables both MOSFETs to enhance transient performance or provide a high impedance output.

The IR3575 provides diode emulation feature which avoids negative current in the synchronous MOSFET and improves light load efficiency.

The IR3575 PWM input is compatible with 3.3V logic signal and 7V tolerant. It accepts 3-level PWM input signals with tri-state.

BBRK# PIN FUNCTIONS

The BBRK# pin has two functions. During normal operation, it accepts direct control signal from the PWM controller to enable Body-Braking®, which turns off both control and synchronous MOSFETs to improve the load transient response.

The second function of BBRK# pin is to select Body-Braking® (tri-state) or diode emulation mode when PWM pin receives a tri-state signal. The seletion is recongnized right after VCC passes its UVLO threshold during the VCC power up. If the BBRK# input is always high, the default operation mode is Body- Braking®, in which both MOSFETs will be turned off when the PWM input is in tri-state. If the BBRK# input has been pulled low for at least 20ns after the VCC passes its UVLO threshold during power up, the diode emulation mode is set. PWM input in tri-state will activate a synchronous diode emulation feature allowing designers to maximize system efficiency at light loads without compromising transient performance. Once the diode emulation mode is set, it cannot be reset until the VCC power is recycled.

PWM TRI-STATE INPUT

The IR3575 PWM accepts 3-level input signals. When PWM input is high, the synchronous MOSFET is turned off and the control MOSFET is turned on. When PWM input is low, control MOSFET is turned off and synchronous MOSFET is turned on. Figures 16-18 show the PWM input and the corresponding SW and GATEL output. If PWM pin is floated , the built-in resistors pull the PWM pin into a tri-state region centered around 1.65V.

When PWM input voltage is in tri-state region, the IR3575 will go into either Body-Braking® mode or diode emulation mode depending on BBRK# selection during VCC power up.

BODY-BRAKING® MODE

International Rectifier's Body-Braking® is an operation mode in which two MOSFETs are turned off. When the synchronous MOSFET is off, the higher voltage across the Shottky diode in parallel helps discharging the inductor current faster, which reduces the output voltage overshoot. The Body-Braking® can be used either to enhance transient response of the converter after load release or to provide a high impedance output.

There are two ways to place the IR3575 in Body-Braking® mode, either controlling the BBRK# pin directly or through a PWM tri-state signal. Both control signals are usually from the PWM controller.

Pulling BBRK# low forces the IR3575 into Body-Braking® mode rapidly, which is usually used to enhance converter transient response after load release, as shown in Figure 19. Releasing BBRK# forces the IR3575 out of Body-Braking® mode quickly.

The BBRK# low turns off both MOSFETs and therefore can also be used to disable a converter. Please note that soft start may not be available when BBRK# is pulled high to enable the converter.

If the BBRK# input is always high, the Body-Braking® is activated when the PWM input enters the tri-state region, as shown in Figures 20 and 21. Comparing to pulling down the BBRK# pin directly, the Body-Braking® response to PWM tri-state signal is slower due to the hold-off time

created by the PWM pin parasitic capacitor with the pull-up and pull-down resistors of PWM pin. For better performance, no more than 100pF parasitic capacitive load should be present on the PWM line of IR3575.

SYNCHRONOUS DIODE EMULATION MODE

An additional feature of the IR3575 is the synchronous diode emulation mode. This function enables increased efficiency by preventing negative inductor current from flowing in the synchronous MOSFET.

As shown in Figure 22, when the PWM input enters the tri-state region the control MOSFET is turned off first, and the synchronous MOSFET is initially turned on and then is turned off when the output current reaches zero. If the sensed output current does not reach zero within a set amount of time the gate driver will assume that the output is de-biased and turn off the synchronous MOSFET, allowing the switch node to float.

This is in contrast to the Body-Braking® mode shown in Figure 23, where GATEL follows PWM input. The Schottky diode in parallel with the synchronous MOSFET conducts for a longer period of time and therefore lowers the light load efficiency.

The zero current detection circuit in the IR3575 is independent of the current sense amplifier and therefore still functions even if the current sense amplifier is not used. As shown in Figure 6, an offset is added to the diode emulation comparator so that a slightly positive output current in the inductor and synchronous MOSFET is treated as zero current to accommodate propagation delays, preventing any negative current flowing in the synchronous MOSFET. This causes the Schottky diode in parallel with the synchronous MOSFET to conduct before the inductor current actually reaches zero, and the conduction time increases with inductance of the output inductor.

To set the IR3575 in diode emulation mode, the BBRK# pin must be toggled low at least once after the VCC passes its UVLO threshold during power up. One simple way is to use the internal BBRK# pull-up resistor (200kΩ typical) with an external capacitor from BBRK# pin to LGND, as shown in Figure 4. To ensure the diode emulation mode is properly set, the BBRK# voltage should be lower than 0.8V when the VCC voltage passes its UVLO threshold (3.3V minimum and 3.7V typical), as shown in Figure 24. A digital signal from the PWM controller can also be used to set the diode emulation mode. The BBRK# signal can either be pulled low for at least 20ns after the VCC passes its UVLO threshold, as shown in Figure 25, or be pulled low before VCC power up and then released after the VCC passes its UVLO threshold, as shown in Figure 26.

Once the diode emulation mode is set, it cannot be reset until the VCC power is recycled.

PHASE FAULT AND THERMAL FLAG OUTPUT

The phase fault circuit looks at the switch node with respect to ground to determine whether there is a defective MOSFET in the phase. The output of the phase fault signal is high during normal operation and is pulled low when there is a fault. Each driver monitors the MOSFET it drives. If the switch node is less than a certain voltage above ground when the PWM signal goes low or if the switch node is a certain voltage above ground when the PWM signal rises, this gives a fault signal. If there are a number of consecutive faults the phase fault signal is asserted.

Thermal flag circuit monitors the temperature of the IR3575. If the temperature goes above a threshold (160°C typical) the PHSFLT# pin is pulled low after a maximum delay of 100us.

The PHSFLT# pin can be pulled low by either the phase fault circuit or the thermal flag circuit, but the IR3575 relies on the system to take protective actions. The phase fault signal could be used by the system to turn off the AC/DC converter or blow a fuse to disconnect the DC/DC converter input from the supply.

If PHSFLT# is not used it can be floated or connected to LGND.

LOSSLESS AVERAGE INDUCTOR CURRENT SENSING

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 31.

The equation of the current sensing network is as follows.

$$v_{CS}(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)R_L\frac{1+s\frac{L}{R_L}}{1+sR_{CS}C_{CS}}$$

$$= i_L(s)R_L \quad when\ L/R_L = R_{CS}C_{CS}$$

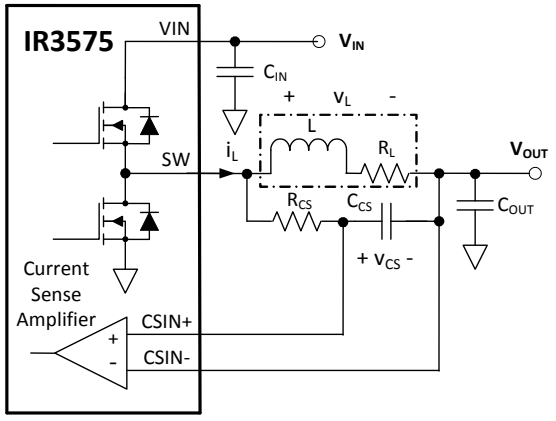


Figure 31: Inductor current sensing

Usually the resistor R_{CS} and capacitor C_{CS} are chosen so that the time constant of R_{CS} and C_{CS} equals the inductor time constant, which is the inductance L over the inductor DCR (R_L). If the two time constants match, the voltage across C_{CS} is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. This is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

CURRENT SENSE AMPLIFIER

A high speed differential current sense amplifier is located in the IR3575, as shown in Figure 6. Its gain is nominally 32.5, and the inductor DCR increase with temperature is not compensated inside the IR3575. The current sense amplifier output IOUT is referenced to REFIN, which is usually connected to a reference voltage from the PWM controller. Figure 27 shows the differential voltage of V(IOUT) – V(REFIN) versus the inductor current and reflects the inductor DCR increase with temperature at higher current.

The current sense amplifier can accept positive differential input up to 25mV and negative input up to -10mV before clipping. The output of the current sense amplifier is summed with the reference voltage REFIN and sent to the IOUT pin. The REFIN voltage is to ensure at light loads there is enough output range to accommodate the negative current ripple shown in Figure 28. In a multiphase converter, the IOUT pins of all the phases can be tied together through resistors, and the IOUT voltage represents the average current through all the inductors and is used by the controller for adaptive voltage positioning.

The input offset voltage is the primary source of error for the current signal. In order to obtain very accurate current signal, the current sense amplifier continuously calibrates itself, and the input offset of this amplifier is within +/- 450uV. This calibration algorithm can create a small ripple on IOUT with a frequency of fsw/128.

If the IR3575 current sense amplifier is required, connect its output IOUT and the reference voltage REFIN to the PWM controller and connect the inductor sense circuit as shown in Figure 4. If the current sense amplifier is not needed, tie CSIN+, CSIN- and REFIN pins to LGND and float IOUT pin, as shown in Figure 5.

MAXIMUM OUTPUT VOLTAGE

When the IR3575 current sense amplifier is used, the maximum output voltage is limited by the VCC voltage used and should be lower than VCC – 2.5V to ensure enough headroom for the current sense amplifier. The maximum voltage is 4.3V when 6.8V VCC is used, but is only 2.5V when 5V VCC is used.

When the IR3575 current sense amplifier is not used, the maximum voltage is not limited by the VCC voltage. The IR3575 can support up to 5.5V output voltage but the output current must be derated since the MOSFET ratio was optimized for duty cycles of 10% to 20%.

DESIGN PROCEDURES

POWER LOSS CALCULATION

The single-phase IR3575 efficiency and power loss measurement circuit is shown in Figure 32.

The IR3575 power loss is determined by,

$$P_{LOSS} = V_{IN} \times I_{IN} + V_{CC} \times I_{VCC} - V_{SW} \times I_{OUT}$$

Where both MOSFET loss and the driver loss are included, but the PWM controller and the inductor losses are not included.

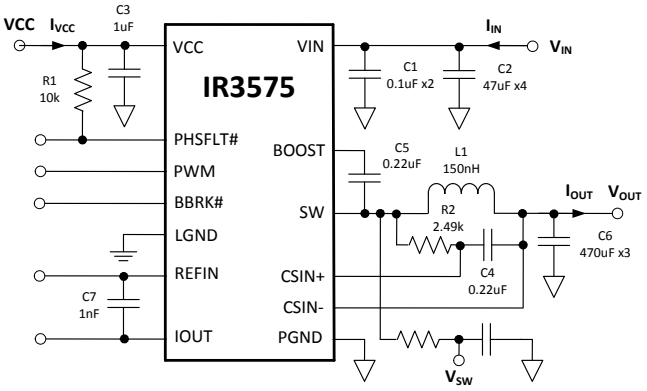


Figure 32: IR3575 Power Loss Measurement

Figure 7 shows the measured single-phase IR3575 efficiency under the default test conditions, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), VCC=7V, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow.

The efficiency of an interleaved multiphase IR3575 converter is always higher than that of a single-phase under the same conditions due to the reduced input RMS current and more input/output capacitors.

The measured single-phase IR3575 power loss under the same conditions is provided in Figure 8.

If any of the application condition, i.e. input voltage, output voltage, switching frequency, VCC MOSFET driver voltage or inductance, is different from those of Figure 8, a set of normalized power loss curves should be used. Obtain the normalizing factors from Figure 10 to Figure 14 for the new application conditions; multiply these factors by the power loss obtained from Figure 8 for the required load current.

As an example, the power loss calculation procedures under different conditions, V_{IN}=10V, V_{OUT}=1V, f_{SW} = 300kHz, VCC=5V, L=210nH, VCC=5V, I_{OUT}=40A, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow, are as follows.

1) Determine the power loss at 40A under the default test conditions of V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH, VCC=7V, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow. It is 4.8W from Figure 8.

2) Determine the input voltage normalizing factor with V_{IN}=10V, which is 0.96 based on the dashed lines in Figure 10.

3) Determine the output voltage normalizing factor with V_{OUT}=1V, which is 0.92 based on the dashed lines in Figure 11.

4) Determine the switching frequency normalizing factor with f_{SW} = 300kHz, which is 0.98 based on the dashed lines in Figure 12.

5) Determine the VCC MOSFET drive voltage normalizing factor with VCC=5V, which is 1.16 based on the dashed lines in Figure 13.

6) Determine the inductance normalizing factor with L=210nH, which is 0.95 based on the dashed lines in Figure 14.

7) Multiply the power loss under the default conditions by the five normalizing factors to obtain the power loss under the new conditions, which is 4.8W x 0.96 x 0.92 x 0.98 x 1.16 x 0.95 = 4.58W.

THERMAL DERATING

Figure 9 shows the IR3575 thermal derating curve with the case temperature controlled at or below 125°C. The test conditions are V_{IN}=12V, V_{OUT}=1.2V, f_{SW}=400kHz, L=150nH (0.29mΩ), VCC=7V, $T_{AMBIENT}$ = 0°C to 90°C, with and without heat sink, and Airflow = 0LFM /100LFM /200LFM /400LFM.

If any of the application condition, i.e. input voltage, output voltage, switching frequency, VCC MOSFET driver voltage, or inductance is different from those of Figure 9, a set of IR3575 case temperature adjustment curves should be used. Obtain the temperature deltas from Figure 10 to Figure 14 for the new application conditions; sum these deltas and then subtract from the IR3575 case temperature obtained from Figure 9 for the required load current.

8) From Figure 9, determine the maximum current at the required ambient temperature under the default conditions, which is 48A at 45°C with 0LFM airflow and the IR3550 case temperature of 125°C.

9) Determine the case temperature with V_{IN}=10V, which is -0.6° based on the dashed lines in Figure 10.

10) Determine the case temperature with V_{OUT}=1V, which is -1.2° based on the dashed lines in Figure 11.

11) Determine the case temperature with f_{SW} = 300kHz, which is -0.3° based on the dashed lines in Figure 12.

12) Determine the case temperature with VCC = 5V, which is +2.4° based on the dashed lines in Figure 13.

13) Determine the case temperature with L=210nH, which is -0.8° based on the dashed lines in Figure 14.

14) Sum the case temperature adjustment from 9) to 13), -0.6° -1.2° -0.3° +2.4° -0.8° = -0.5°. Add the delta to the required ambient temperature in step 8), 45°C + (-0.5°C) = 44.5°C, at which the maximum current is reduced to 49A when the allowed junction temperature is 125°C, as shown in Figure 9. If only 105°C junction temperature is allowed, the required ambient temperature is equivalent to 44.5°C + (125°C - 105°C) = 64.5°C, which indicates 41A maximum current at the 45°C required ambient temperature.

INDUCTOR CURRENT SENSING CAPACITOR C_{CS} AND RESISTOR R_{CS}

If the IR3575 is used with inductor DCR sensing, care must be taken in the printed circuit board layout to make a Kelvin connection across the inductor DCR. The DC resistance of the inductor is utilized to sense the inductor current. Usually the resistor R_{CS} and capacitor C_{CS} in parallel with the inductor are chosen to match the time constant of the inductor, and therefore the voltage across the capacitor C_{CS} represents the inductor current.

Measure the inductance L and the inductor DC resistance R_L. Pre-select the capacitor C_{CS} and calculate R_{CS} as follows.

$$R_{CS} = \frac{L/R_L}{C_{CS}}$$

INPUT CAPACITORS C_{VIN}

At least two 10uF 1206 ceramic capacitors and one 0.22uF 0402 ceramic capacitor are recommended for decoupling the VIN to PGND connection. The 0.22uF 0402 capacitor should be on the same side of the PCB as the IR3575 and next to the VIN and PGND pins. Adding additional capacitance and use of capacitors with lower ESR and mounted with low inductance routing will improve efficiency and reduce overall system noise, especially in single-phase designs or during high current operation.

BOOTSTRAP CAPACITOR C_{BOOST}

A minimum of 0.22uF 0402 capacitor is required for the bootstrap circuit. A high temperature 0.22uF or greater value 0402 capacitor is recommended. It should be mounted on the same side of the PCB as the IR3575 and as close as possible to the BOOST pin. A low-inductance PCB routing of the SW pin connection to the other terminal of the bootstrap capacitor is required to minimize the ringing between the BOOST and SW pins.

VCC DECOUPLING CAPACITOR C_{VCC}

A 0.22uF to 1uF ceramic decoupling capacitor is required at the VCC pin. It should be mounted on the same side of the PCB as the IR3575 and as close as possible to the VCC and PGND (pin 4). Low inductance routing between the VCC capacitor and the IR3575 pins is strongly recommended.

BODY-BRAKING® PIN FUNCTION

The BBRK# pin should be pulled up to VCC if the feature is not used by the PWM controller. Use of a 4.7kΩ resistor or a direct connection to VCC is recommended.

MOUNTING OF HEAT SINKS

Care should be taken in the mounting of heat sinks so as not to short-circuit nearby components. The VCC and Bootstrap capacitors are typically mounted on the same side of the PCB as the IR3575. The mounting height of these capacitors must be considered when selecting their package sizes.

HIGH OUTPUT VOLTAGE DESIGN CONSIDERATIONS

The IR3575 is capable of creating output voltages above the 3.3V recommended maximum output voltage as there are no restrictions inside the IR3575 on the duty cycle applied to the PWM pin. However if the current sense feature is required, the common mode range of the current sense amplifier inputs must be considered. A violation of the current sense input common mode range may cause unexpected IR3575 behavior. Also the output current rating of the device will be reduced as the duty cycle increases. In very high duty cycle applications sufficient time must be provided for replenishment of the Bootstrap capacitor for the control MOSFET drive.

LAYOUT EXAMPLE

Contact International Rectifier for a layout example suitable for your specific application.

METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to prevent shorting.
- Lead land length should be equal to maximum part lead length +0.15 - 0.3 mm outboard extension and 0 to + 0.05mm inboard extension. The outboard extension ensures a large and visible toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width.
- Only 0.30mm diameter via shall be placed in the area of the power pad lands and connected to power planes to minimize the noise effect on the IC and to improve thermal performance.

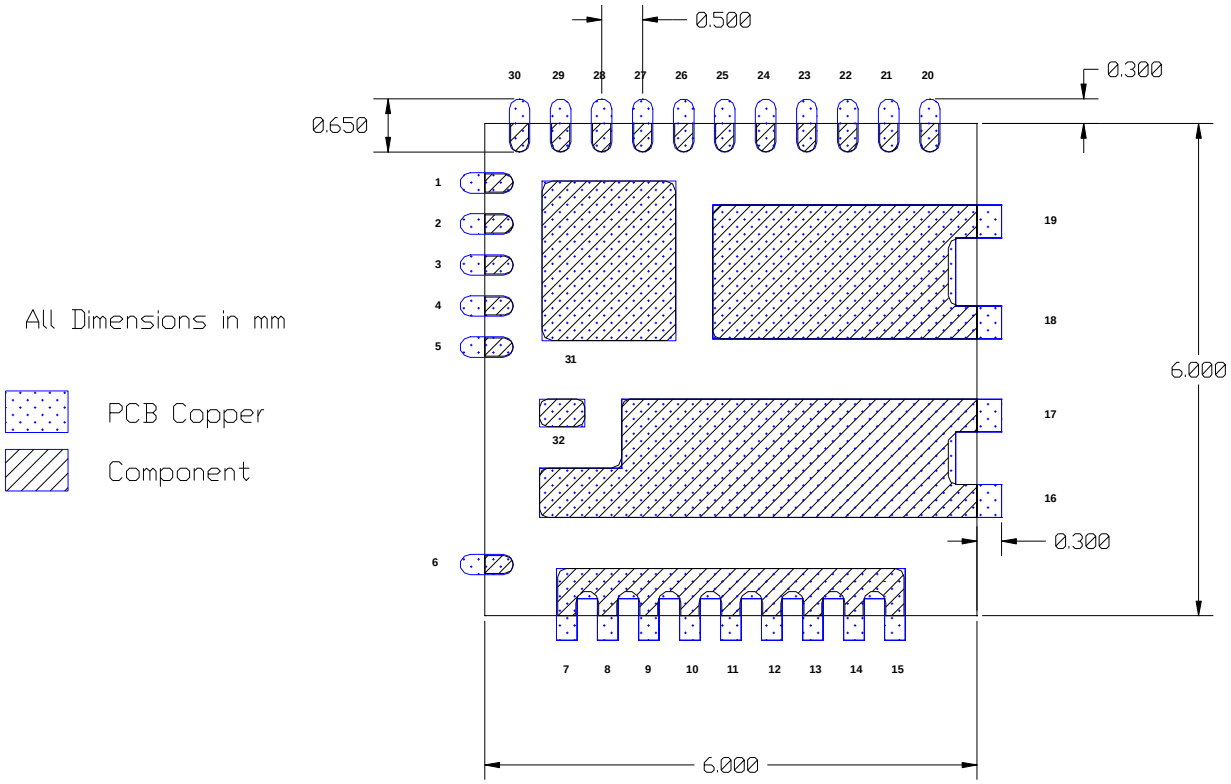


Figure 33: Metal and component placement

* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist miss-alignment is a maximum of 0.05mm and it is recommended that the low power signal lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm typical.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The dimensions of power land pads, VIN, PGND, TGND and SW, are Non Solder Mask Defined (NSMD). The equivalent PCB layout becomes Solder Mask Defined (SMD) after power shape routing.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

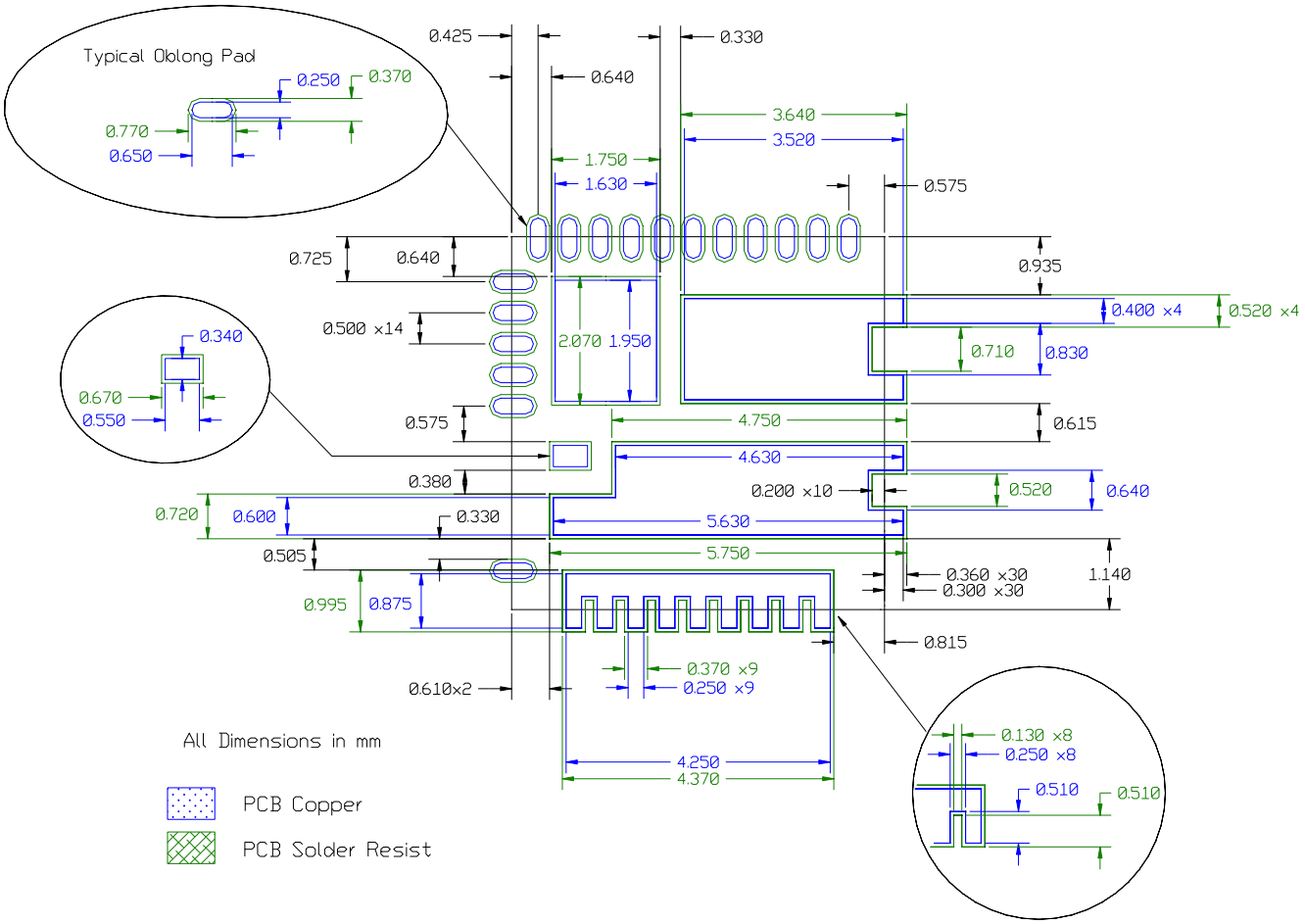


Figure 34: Solder resist

* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

STENCIL DESIGN

- The stencil apertures for the lead lands should be approximately 65% to 75% of the area of the lead lands depending on stencil thickness. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The low power signal stencil lead land apertures should therefore be shortened in length to keep area ratio of 65% to 75% while centered on lead land.
- The power pads VIN, PGND, TGND and SW, land pad apertures should be approximately 65% to 75% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open. Solder paste on large pads is broken down into small sections with a minimum gap of 0.2mm between allowing for out-gassing during solder reflow.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.

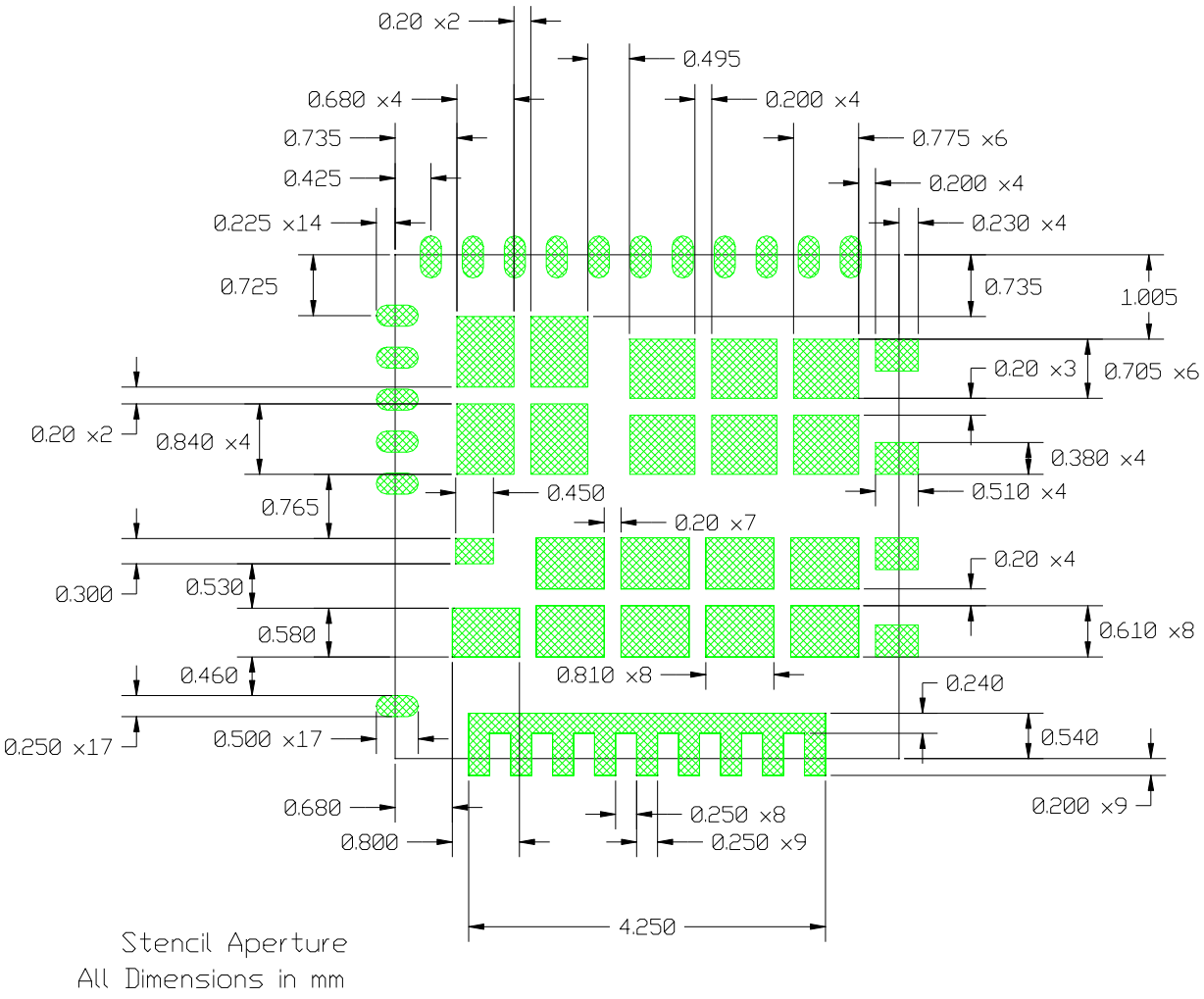


Figure 35: Stencil design

* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

MARKING INFORMATION

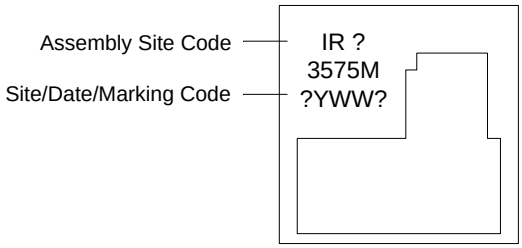
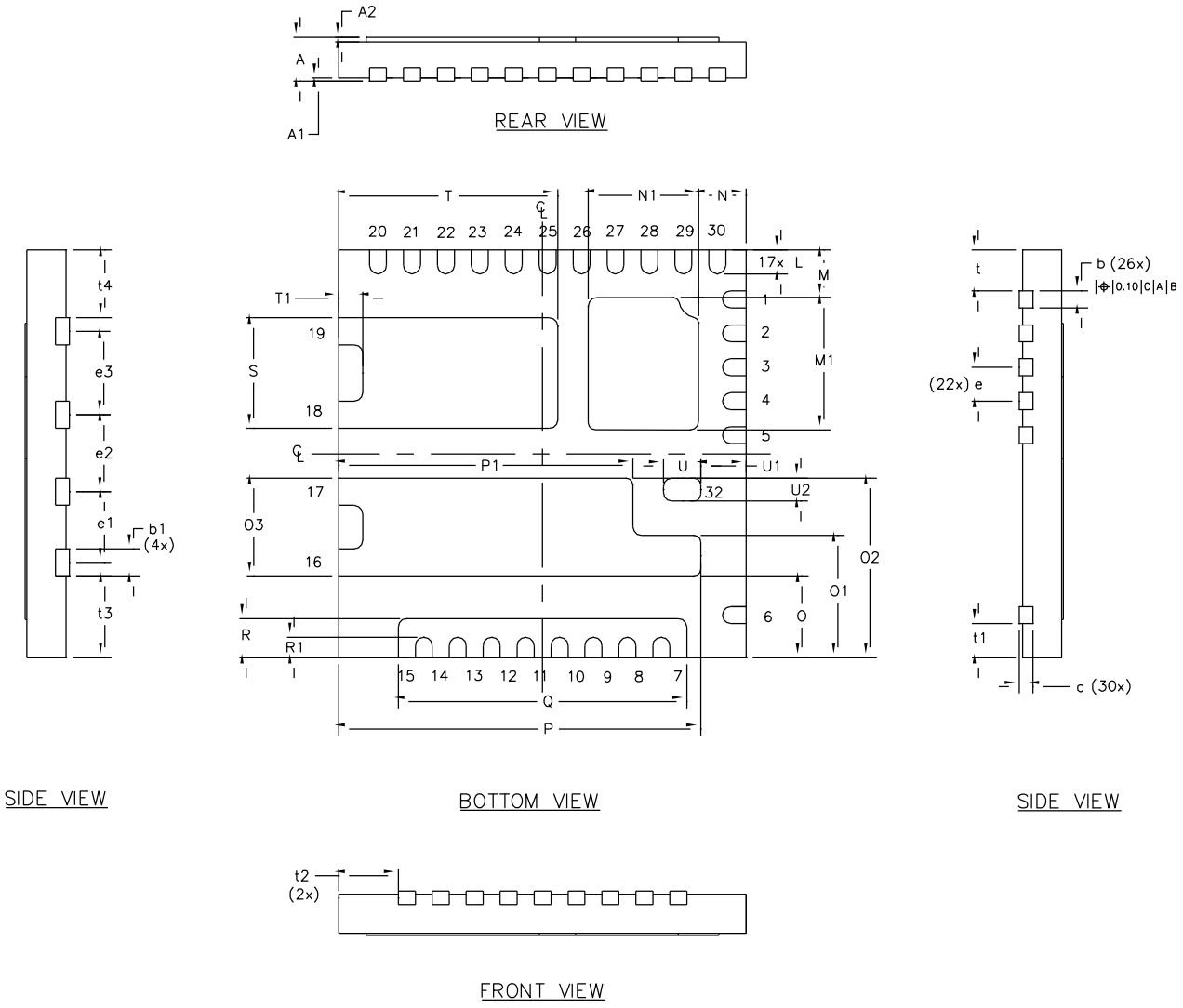
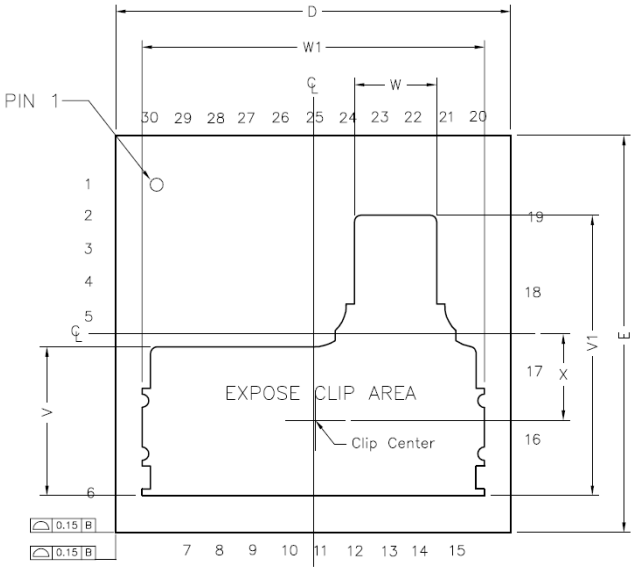


Figure 36: PQFN 6mm x 6mm

PACKAGE INFORMATION





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.55	0.75	.0217	.0295
A1	0.000	0.050	.0000	.0020
A2	0.000	0.070	.0000	.0028
b	0.20	0.30	.0079	.0118
b1	0.350	0.450	.0138	.0177
c	0.203 REF.		.0080 REF.	
D	6.000 BASIC		.2362 BASIC	
E	6.000 BASIC		.2362 BASIC	
e	0.500 BASIC		.0197 BASIC	
e1	1.041 BASIC		.0410 BASIC	
e2	1.134 BASIC		.0446 BASIC	
e3	1.230 BASIC		.0484 BASIC	
t	0.600 BASIC		.0236 BASIC	
t1	0.500 BASIC		.0197 BASIC	
t2	0.875 BASIC		.0344 BASIC	
t3	1.200 BASIC		.0472 BASIC	
t4	0.996 BASIC		.0392 BASIC	
t5	0.450 BASIC		.0177 BASIC	
t6	0.300 BASIC		.0118 BASIC	
L	0.300	0.400	.0118	.0157
M	0.650	0.750	.0256	.0295
M1	1.896	1.996	.0747	.0786
N	0.650	0.750	.0256	.0296
N1	1.577	1.677	.0621	.0660

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
O	1.150	1.250	.0453	.0492
O1	1.750	1.850	.0689	.0728
O2	2.591	2.691	.1020	.1060
O3	1.391	1.491	.0548	.0587
P	5.281	5.381	.2079	.2119
P1	4.281	4.381	.1685	.1725
Q	4.200	4.300	.1654	.1693
R	0.525	0.625	.0207	.0246
R1	0.250	0.350	.0098	.0138
S	1.580	1.680	.0622	.0661
T	3.173	3.273	.1249	.1289
T1	0.300	0.400	.0118	.0157
U	0.500	0.600	.0197	.0236
U1	0.619	0.719	.0244	.0283
U2	0.287	0.387	.0130	.0152
V	2.147	2.347	.0845	.0924
V1	4.140	4.340	.1630	.1709
W	1.148	1.348	.0452	.0531
W1	5.100	5.300	.0200	.0208
X	1.207	1.407	.0475	.0554

Figure 37: PQFN 6mm x 6mm

Data and specifications subject to change without notice.
This product will be designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International IOR Rectifier

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