THE DATASHEET OF

LMH6704MA/NOPB

LMH6704 650 MHz Selectable Gain Buffer with Disable

Check for Samples: LMH6704

FEATURES

- **Wideband operation**
  - **A_V = +1, V_O = 0.5 V_{PP} 650 MHz**
  - **A_V = +2, V_O = 0.5 V_{PP} 450 MHz**
  - **A_V = +2, V_O = 2 V_{PP} 400 MHz**
- **High output current ±90 mA**
- **Very low distortion**
  - **$2^{nd}/3^{rd}$ harmonics (10 MHz, R_L = 100Ω): −62/−78dBc**
  - **Differential gain/Differential phase: 0.02%/0.02°**
- **Low noise 2.3nV/√Hz**
- **High slew rate 3000 V/μs**
- **Supply current 11.5 mA**

APPLICATIONS

- **HDTV, NTSC and PAL video systems**
- **Video switching and distribution**
- **ADC driver**
- **DAC buffer**
- **RGB driver**
- **High speed multiplexer**

DESCRIPTION

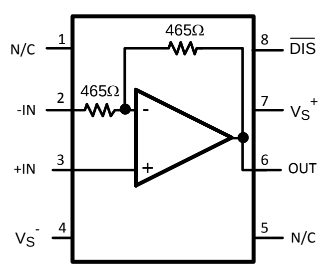
The LMH™6704 is a very wideband, DC coupled selectable gain buffer designed specifically for wide dynamic range systems requiring exceptional signal fidelity. The LMH6704 includes on chip feedback and gain set resistors, simplifying PCB layout while providing user selectable gains of +1, +2 and −1 V/V. The LMH6704 provides a disable pin, which places the amplifier in a high output impedance, low power mode. The Disable pin may be allowed to float high.

With a 650 MHz Small Signal Bandwidth (A_V = +1), full power gain flatness to 200 MHz, and excellent Differential Gain and Phase, the LMH6704 is optimized for video applications. High resolution video systems will benefit from the LMH6704 ability to drive multiple video loads at low levels of differential gain or differential phase distortion.

The LMH6704 is constructed with proprietary high speed complementary bipolar process using proven current feedback circuit architectures. It is available in 8 Pin SOIC and 6 Pin SOT-23 packages.

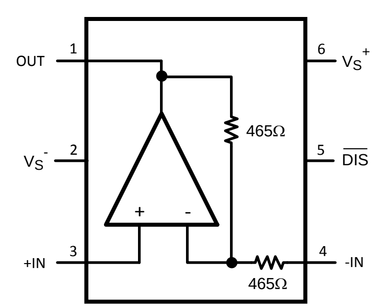
CONNECTION DIAGRAM

8 Pin SOIC
Top View



See Package Number D0008A

6 Pin SOT-23
Top View



See Package Number DBV0006A

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance (2)	Human Body Model	2000V
	Machine Model	200V
Supply Voltage		13.5V
I_{OUT}		(3)
Common-Mode Input Voltage		V_S^- to V_S^+
Maximum Junction Temperature		150°C
Storage Temperature Range		−65°C to 150°C
Soldering Information	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C
	Lead Temp. (soldering 10 sec.)	300°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications, see the Electrical Characteristics tables.
(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(3) The maximum output current (I_{OUT}) is determined by device power dissipation limitations.

Operating Ratings (1)

Nominal Supply Voltage		±4V to ±6V
Temperature Range (2)		−40°C to 85°C
Thermal Resistance		
Package	**(θ_{JC})**	**(θ_{JA})**
8-Pin SOIC	75°C/W	160°C/W
6-Pin SOT23	120°C/W	187°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications, see the Electrical Characteristics tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Electrical Characteristics [1]

T_A = +25°C , A_V = +2, V_S = ±5V, R_L = 100Ω; unless specified.

Symbol	Parameter	Conditions	Min [2]	Typ [2]	Max [2]	Units
Dynamic Performance						
SSBW	-3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}, A_V = +1		650		MHz
SSBW		V_{OUT} = 0.5 V_{PP}		450		
LSBW		V_{OUT} = 2 V_{PP}		400		
$GF_{0.1dB}$	0.1 dB Gain Bandwidth	V_{OUT} = 2 V_{PP}		200		MHz
SR	Slew Rate	V_{OUT} = 4 V_{PP}, 40% to 60% [3]		3000		V/µs
TRS/TRL	Rise and Fall Time (10% to 90%)	2V Step		0.9		ns
t_s	Settling Time to 0.1%	2V Step		10		ns
Distortion and Noise Response						
HD2L	2nd Harmonic Distortion	V_{OUT} = 2.0 V_{PP}, f = 10 MHz		−62		dBc
HD2H		V_{OUT} = 2.0 V_{PP}, f = 40 MHz		−52		
HD3L	3rd Harmonic Distortion	V_{OUT} = 2.0 V_{PP}, f = 10 MHz		−78		dBc
HD3H		V_{OUT} = 2.0 V_{PP}, f = 40 MHz		−65		
IMD	Two-Tone Intermodulation	f = 10 MHz, P_{OUT} = 10 dBm/tone		−65		dBc
V_N	Output Noise Voltage	f = 100 kHz, A_V = +2		10.5		nV/√Hz
		f = 100 kHz, A_V = +1		9.3		
		f = 100 kHz, A_V = −1		10.5		
I_{NN}	Non-Inverting Input Noise Current			3		pA/√Hz
DG	Differential Gain	R_L = 150Ω, f = 4.43 MHz		.02		%
DP	Differential Phase	R_L = 150Ω, f = 4.43 MHz		0.02		deg
Static, DC Performance						
A_V	Gain		1.98 **1.96**	2.00	2.02 **2.04**	V/V
	Gain Error		−1 **−2**		+1 **+2**	%
V_{IO}	Input Offset Voltage			2	±7 **±8.3**	mV
DV_{IO}	Input Offset Voltage Average Drift			35		µV/°C
I_{BN}	Input Bias Current	Non-Inverting [4]		−5	±15 **±18**	µA
I_{BI}	Input Bias Current	Inverting		5	±22 **±31**	
CMIR	Common Mode Input Range	V_{IO} ≤ 15 mV	±1.9	±2		V
PSRR	Power Supply Rejection Ratio	DC	48 **47**	52		dB
V_O	Output Voltage Swing	R_L = ∞	±3.3 **±3.18**	±3.5		V
		R_L = 100Ω	±3.2 **±3.12**	±3.5		
I_O	Linear Output Current	V_{OUT} ≤ 80 mV	±55	±90		mA
I_S	Supply Current (Enabled)	$\overline{DIS}$ = 2V, R_L = ∞		11.5	12.5 **13.7**	mA
	Supply Current (Disabled)	$\overline{DIS}$ = 0.8V, R_L = ∞		0.25	0.9 **0.925**	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. Parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Min/Max ratings are based on production testing unless otherwise specified.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested on shipped production material.
(3) Slew Rate is the average of the rising and falling edges.
(4) Negative current implies current flowing out of the device.

Electrical Characteristics [1] (continued)

T_A = +25°C , A_V = +2, V_S = ±5V, R_L = 100Ω; unless specified.

Symbol	Parameter	Conditions	Min [2]	Typ [2]	Max [2]	Units
R_F & R_G	Internal R_F and R_G		375	465	563	Ω
R_{OUT}	Closed Loop Output Resistance	DC		0.05		Ω
R_{IN+}	Input Resistance			1		MΩ
C_{IN+}	Input Capacitance			1		pF
Enable/Disable Performance (Disabled Low)						
T_{ON}	Enable Time			10		ns
T_{OFF}	Disable Time			10		ns
	Output Glitch			50		mV_{PP}
V_{IH}	Enable Voltage	$\overline{DIS} \geq V_{IH}$	2.0			V
V_{IL}	Disable Voltage	$\overline{DIS} \leq V_{IL}$			0.8	
I_{IH}	Disable Input Bias Current, High	$\overline{DIS} = V^+$, [4]		−1	**±50**	µA
I_{IL}	Disable Input Bias Current, Low	$\overline{DIS}$ = 0V [4]	**0**	−100	**−350**	µA
I_{OZ}	Disabled Output Leakage Current	A_V = +1, V_{OUT} = ±1.8V		0.2	±25 **±50**	µA

Typical Performance Characteristics

(T_A = 25°C, V_S = ±5V, R_L = 100Ω, A_V = +2, V_{OUT} = 0.5 V_{PP}; Unless Specified).

Small Signal Frequency Response vs. Gain

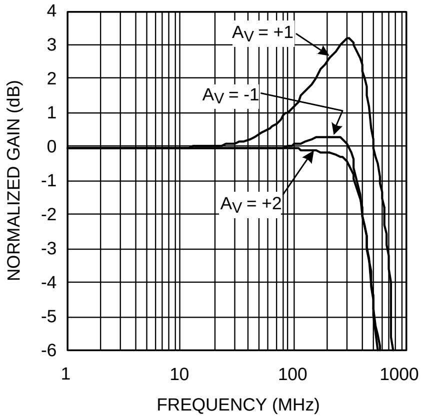

Figure 1.

Frequency Response vs. V_{OUT}

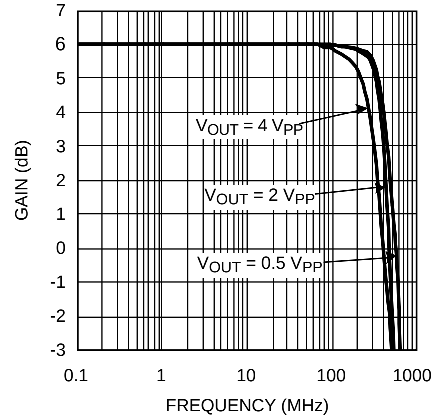

Figure 2.

Small Signal Frequency Response vs. R_{LOAD}

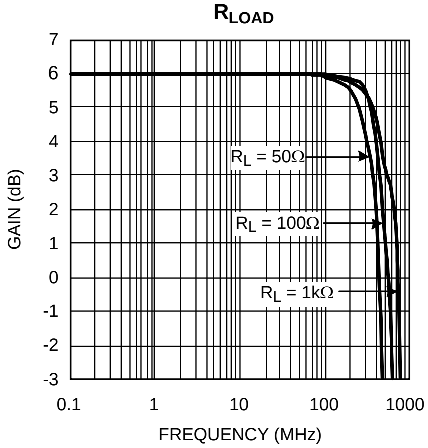

Figure 3.

Large Signal Gain Flatness

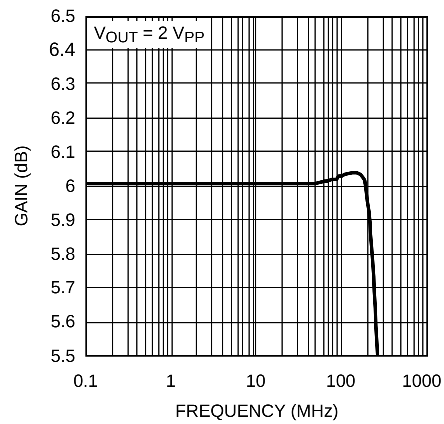

Figure 4.

Small Signal Frequency Response vs. Capacitive Load

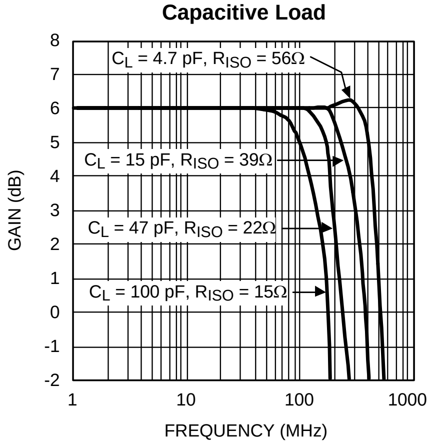

Figure 5.

Series Output Isolation Resistance vs. Capacitive Load

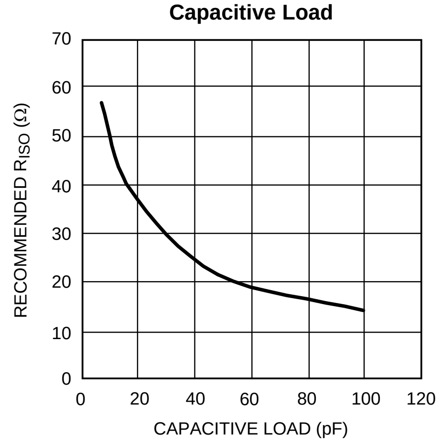

Figure 6.

Typical Performance Characteristics (continued)

(T_A = 25°C, V_S = ±5V, R_L = 100Ω, A_V = +2, V_{OUT} = 0.5 V_{PP}; Unless Specified).

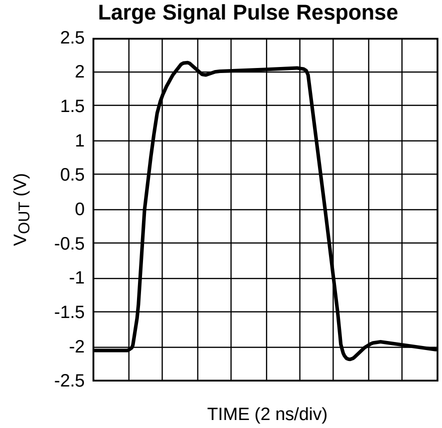

Figure 7.

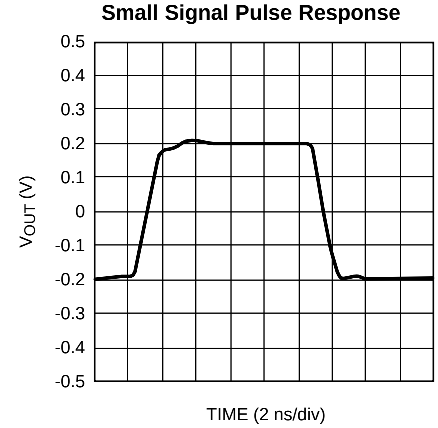

Figure 8.

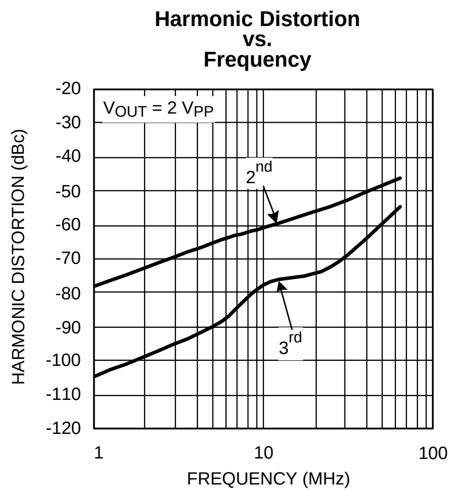

Figure 9.

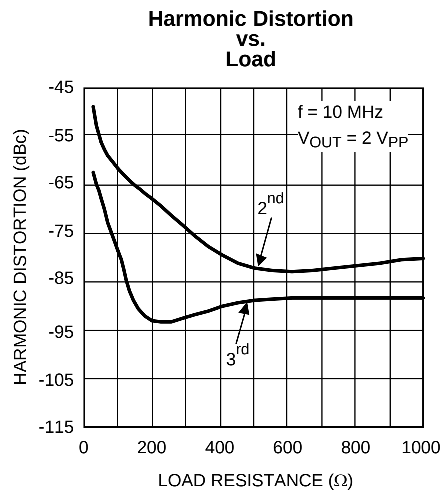

Figure 10.

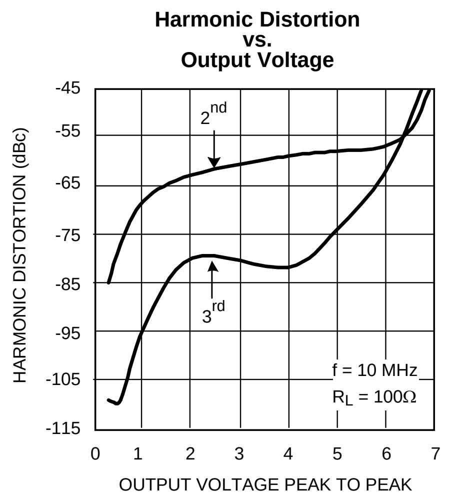

Figure 11.

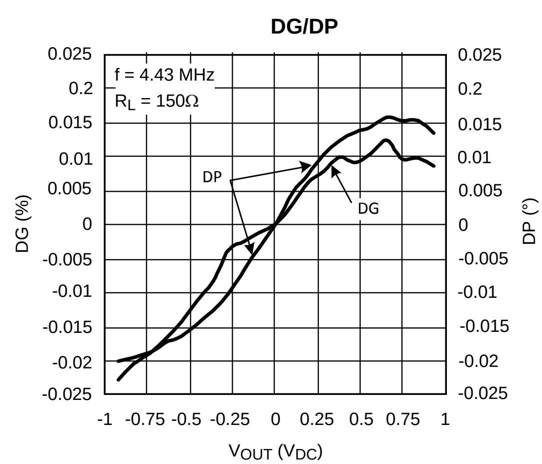

Figure 12.

Typical Performance Characteristics (continued)

(T_A = 25°C, V_S = ±5V, R_L = 100Ω, A_V = +2, V_{OUT} = 0.5 V_{PP}; Unless Specified).

PSRR vs. Frequency

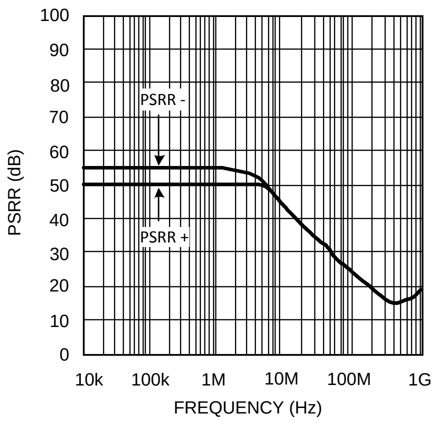

Figure 13.

DC Errors vs. Temperature (A Typical Unit, (1))

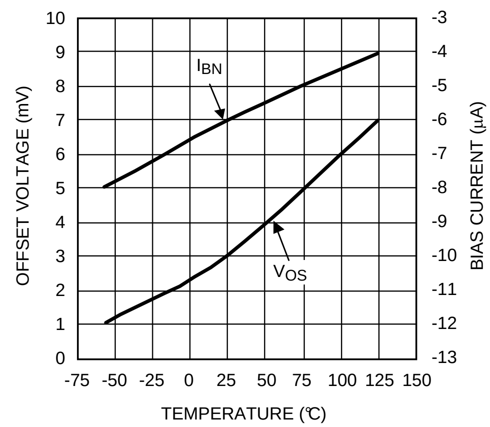

Figure 14.

Disable Timing

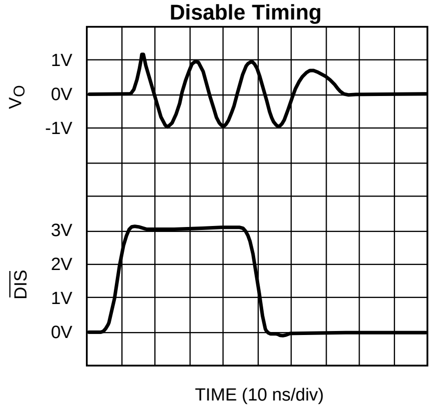

Figure 15.

Disable Output Glitch

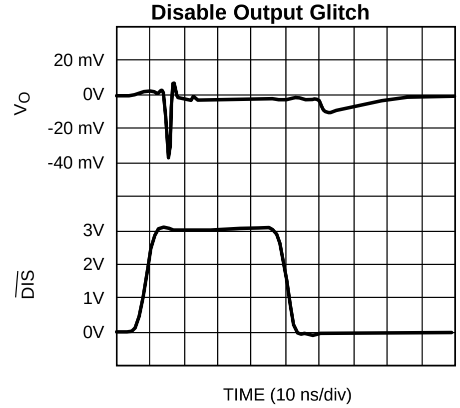

Figure 16.

(1) Negative current implies current flowing out of the device.

APPLICATION INFORMATION

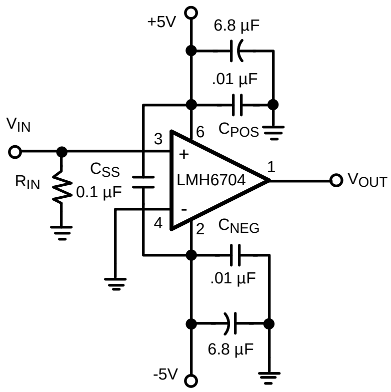

Figure 17. Recommended Gain of +2 Circuit

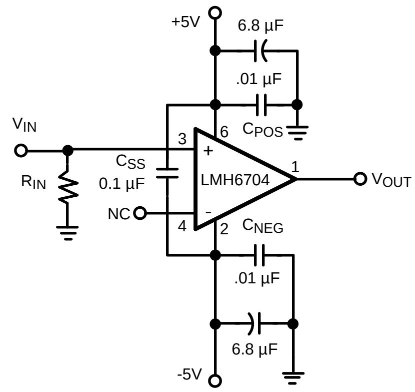

Figure 18. Recommended Gain of +1 Circuit

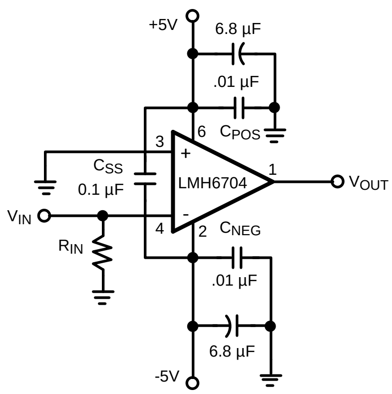

Figure 19. Recommended Gain of −1 Circuit

GENERAL INFORMATION

The LMH6704 is a high speed current feedback Selectable Gain Buffer (SGB), optimized for very high speed and low distortion. With its internal feedback and gain-setting resistors the LMH6704 offers excellent AC performance while simplifying board layout and minimizing the affects of layout related parasitic components. The LMH6704 has no internal ground reference so single or split supply configurations are both equally useful.

SETTING THE CLOSED LOOP GAIN

The LMH6704 is a current feedback amplifier with on-chip $R_F = R_G = 465\Omega$. As such it can be configured with an $A_V = +2$, $A_V = +1$, or an $A_V = -1$ by connecting pins 3 and 4 as described in Table 1.

Table 1.

GAIN A_V	Input Connections	
	Non-Inverting (Pin 3, SOT-23)	Inverting (Pin 4, SOT-23)
−1 V/V	Ground	Input Signal
+1 V/V	Input Signal	NC (Open)
+2 V/V	Input Signal	Ground

The gain accuracy of the LMH6704 is accurate over temperature to within ±1%. The internal gain setting resistors, $R_F$and R_G, match very well. The LMH6704 architecture takes advantage of the fact that the internal gain setting resistors track each other well over a wide range of temperature and process variation to keep the overall gain constant, despite the fact that the individual resistors have nominal temperature drifts. Therefore, using external resistors in series with R_G to change the gain will result in poor gain accuracy over temperature.

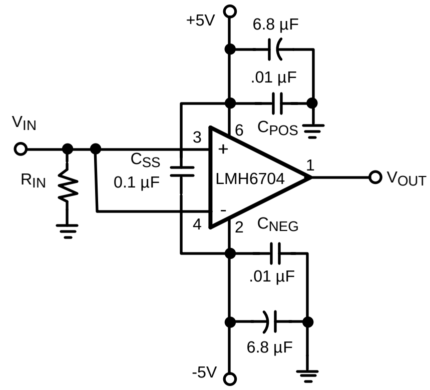

Figure 20. Alternate Unity Gain Configuration

UNITY GAIN COMPENSATION

With a current feedback Selectable Gain Buffer like the LMH6704, the feedback resistor is a compromise between the value needed for stability at unity gain and the optimized value needed at a gain of two. In standard open-loop current feedback operational amplifiers the feedback resistor, R_F, is external and its value can be adjusted to match the required gain. Since the feedback resistor is integrated in the LMH6704, it is not possible to adjust it's value. However, we can employ the circuit shown in Figure 20. This circuit modifies the noise gain of the amplifier to eliminate the peaking associated with using the circuit shown in Figure 18. The frequency response is shown in Figure 21. The decreased peaking does come at a price as the output referred voltage noise density increases by a factor of 1.1.

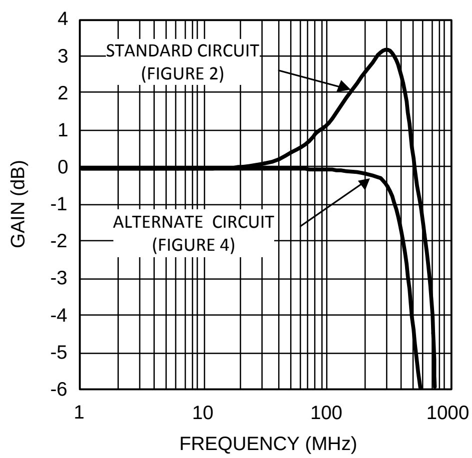

Figure 21. Unity Gain Frequency Response

OUTPUT VOLTAGE NOISE

Open-loop operational amplifiers specify three input referred noise parameters: input voltage noise, non-inverting input current noise, and inverting input current noise. These specifications are used to calculate the total voltage noise produced at the output of the amplifier. The LMH6704 is a closed loop amplifier with internal resistors, thus only the non-inverting input current noise flows through external components. All other noise sources are internal to the part. There are four possible values for the noise at the output depending on the gain configuration as shown in Table 2. For more information on calculating noise in current feedback amplifiers see Application Notes OA-12 and AN104 available at www.ti.com.

The total noise voltage at the output can be calculated using Equation 1:

$$E_O = \sqrt{(4kTR_{SOURCE} + (I_{BN} * R_{SOURCE})^2) * G_N^2 + (\text{OUTPUT REFERRED NOISE VOLTAGE})^2}, \text{ Where}$$

G_N = Noise Gain and 4kT = 16E-21 Joules @ Room Temperature (1)

For example, if an A_V = +2 configuration is used with a source impedance of 37.5Ω (parallel combination of 75Ω source and 75Ω termination impedances), where "I_{BN}" is 18.5pA/$\sqrt{Hz}$ and the output referred voltage noise (excluding non-inverting input noise current) can be found in Table 2. The total noise (E_O) at the output can be calculated as:

$$E_O = \sqrt{(16E\text{-}21 * 37.5 + (18.5\text{ pA} * 37.5)^2) * 2^2 + (10.5\text{ nV})^2} = 10.6\text{ nV}/\sqrt{Hz} \quad (2)$$

Table 2. Measured Output Noise Voltage(1)

Gain (A_V)	Output Referred Voltage Noise (nV/$\sqrt{Hz}$), excluding non-inverting noise current
+2	10.5
+1	9.3
+1, alternate method shown in Figure 20	10.5
-1	10.5

(1) Note: f ≥ 100 kHz

ENABLE/DISABLE

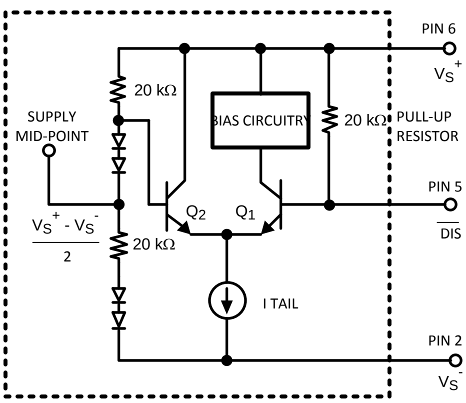

Figure 22. $\overline{\text{DIS}}$ Pin Simplified Schematic

The LMH6704 has a TTL logic compatible disable function. Apply a logic low (<.8V) to the DS pin and the LMH6704 is disabled. Apply a logic high (>2.0V), or let the pin float and the LMH6704 is enabled. Voltage, not current, at the Disable pin (DS) determines the enable/disable state. Care must be exercised to prevent the disable pin voltage from going more than .8V below the midpoint of the supply voltages (0V with split supplies, $V^+/2$ with single supply biasing). Doing so could cause transistor Q1 to Zener resulting in damage to the disable circuit (See Figure 22 or the simplified internal schematic diagram using SOT-23 package pin numbers). The core amplifier is unaffected by this, but the disable operation could become permanently slower as a result.

Disabled, the LMH6704 inputs and output become high impedances. While disabled the LMH6704 quiescent current is approximately 250 µA. Because of the pull up resistor on the disable circuit, the I_{CC} and I_{EE} currents (positive and negative supply currents respectively) are not balanced in the disabled state. The positive supply current (I_{CC}) is approximately 350 µA while the negative supply current (I_{EE}) is only 250 µA. The remaining I_{EE} current of 100 µA flows through the disable pin.

The disable function can be used to create analog switches or multiplexers. Implement a single analog switch with one LMH6704 positioned between an input and output. Create an analog multiplexer with several LMH6704's. Use the circuit shown in for multiplexer applications because there is no RG to shunt signals to ground.

EVALUATION BOARDS

Texas Instruments provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the data sheet plots were measured with these boards.

Device	Package	Evaluation Board Part Number
LMH6704MA	SOIC-8	CLC730227
LMH6704MF	SOT23-6	CLC730216

DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor R_{ISO}. Figure 23 shows the use of a series output resistor, R_{ISO}, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The chart "Suggested R_{ISO} vs. Cap Load" gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{ISO} can be reduced slightly from the recommended values.

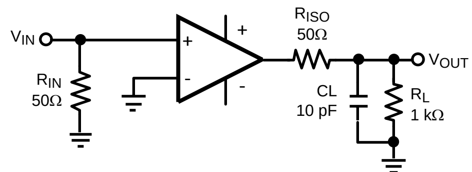

Figure 23. Decoupling Capacitive Loads

LAYOUT CONSIDERATIONS

Whenever questions about layout arise, use the evaluation board as a guide. To reduce parasitic capacitances ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. In Figure 17, Figure 18, and Figure 19 C_{SS} is optional, but is recommended for best second order harmonic distortion. Another option to using C_{SS} is to use pairs of 0.01 µF and 0.1 µF ceramic capacitors for each supply bypass.

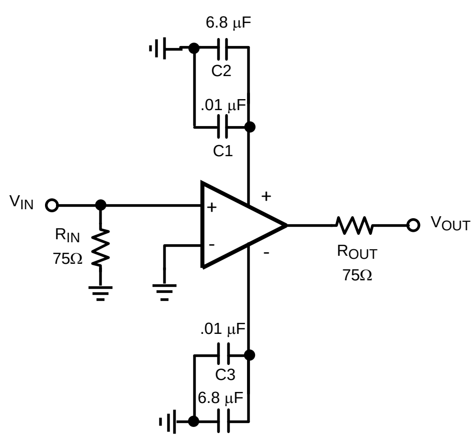

Figure 24. Typical Video Application

VIDEO PERFORMANCE

The LMH6704 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. NTSC and PAL performance is nearly flawless with DG of 0.02% and DP of 0.02°. Best performance will be obtained with back terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. Figure 24 shows a typical configuration for driving a 75Ω Cable. The amplifier is configured for a gain of two to make up for the 6 dB of loss in R_{OUT}.

POWER DISSIPATION

Follow these steps to determine the Maximum power dissipation for the LMH6704:

1. Calculate the quiescent (no-load) power:

   $$P_{AMP} = I_{CC^*} (V_S) \tag{3}$$

   where $V_S = V^+ - V^-$
2. Calculate the RMS power dissipated in the output stage:

   $$P_D \text{ (rms)} = \text{rms} ((V_S - V_{OUT}) \times I_{OUT}) \tag{4}$$

   where V_{OUT} and I_{OUT} are the voltage and current across the external load and V_S is the total supply current
3. Calculate the total RMS power:

   $$P_T = P_{AMP} + P_D \tag{5}$$

The maximum power that the LMH6704, package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150° – T_{AMB})/ θ_{JA}$, where T_{AMB} = Ambient temperature (°C) and $θ_{JA}$ = Thermal resistance, from junction to ambient, for a given package (°C/W). For the SOT-23 package $θ_{JA}$ is 187°C/W.

ESD PROTECTION

The LMH6704 is protected against electrostatic discharge (ESD) on all pins. The LMH6704 will survive 2000V Human Body model and 200V Machine model events. Input and Output pins have ESD diodes to either supply pin (V^+ and $V^−$) which are reverse biased and essentially have no effect under most normal operating conditions. There are occasions, however, when the ESD diodes will be evident. If the LMH6704 is driven by a large signal while the device is powered down, the ESD diodes might enter forward operating region and conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to inadvertently power up the LMH6704 with a large signal applied to the input pins. Shorting the power pins to each other will prevent the chip from being powered up through the input.

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6704MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH67 04MA	Samples
LMH6704MF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	B07A	Samples
LMH6704MFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	B07A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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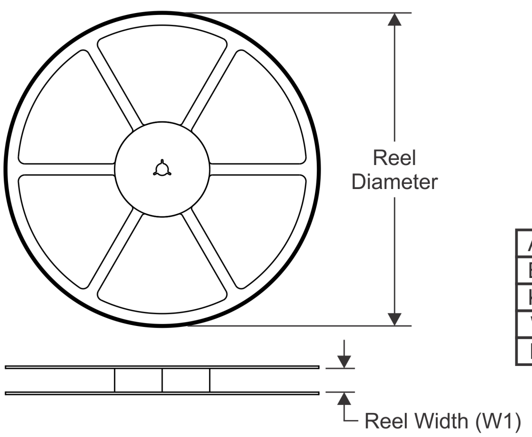
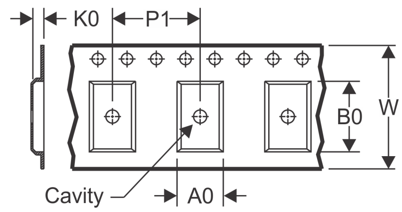
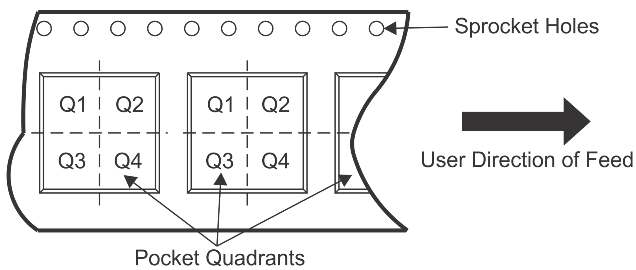
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

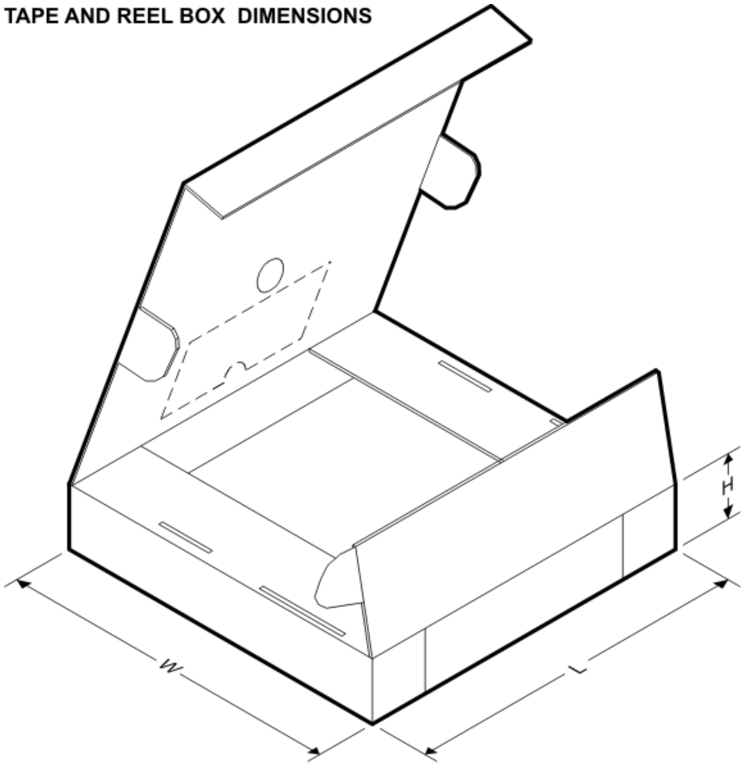
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

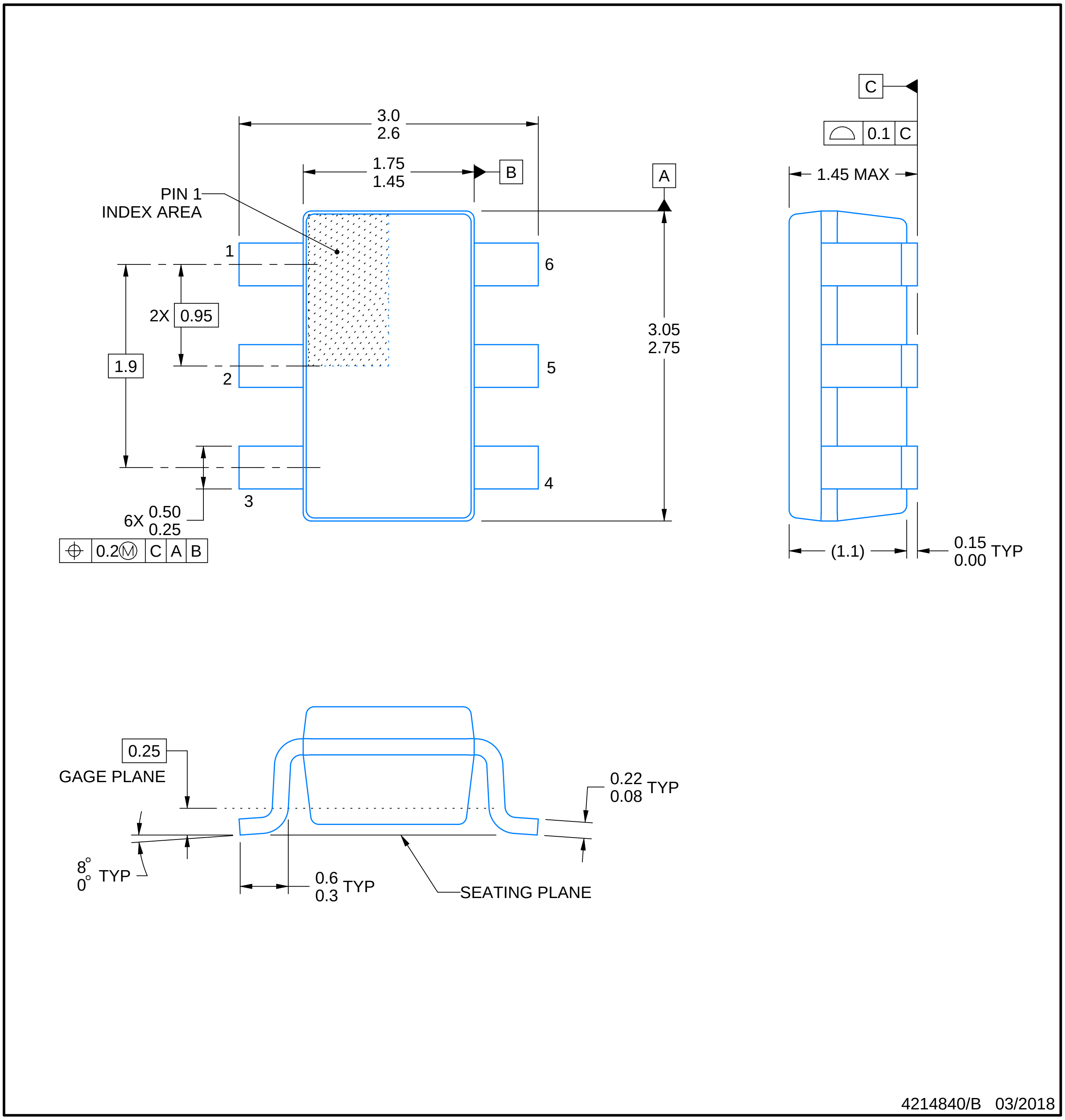
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6704MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6704MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

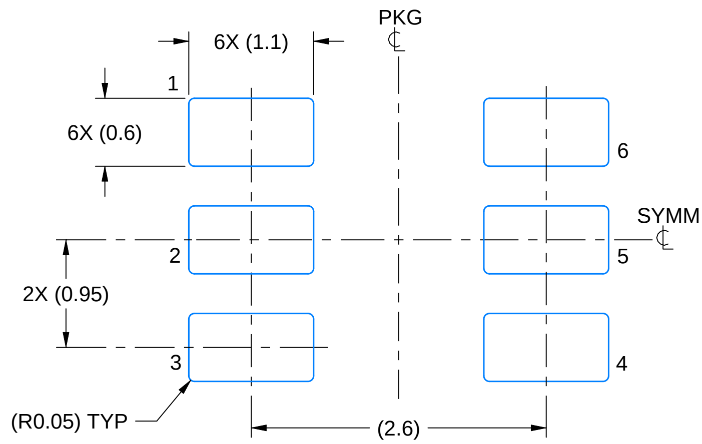
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6704MF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LMH6704MFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0



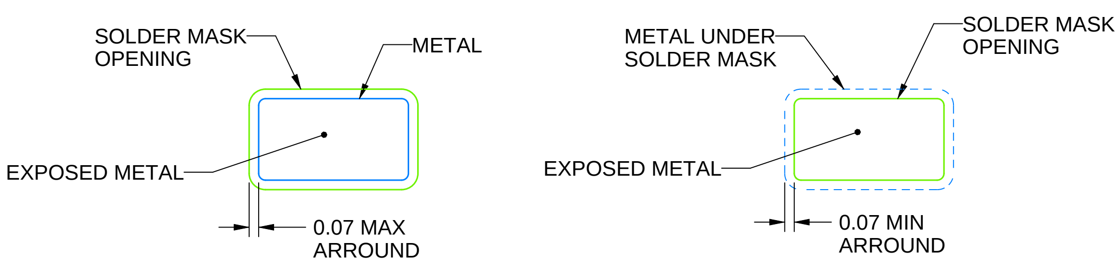
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

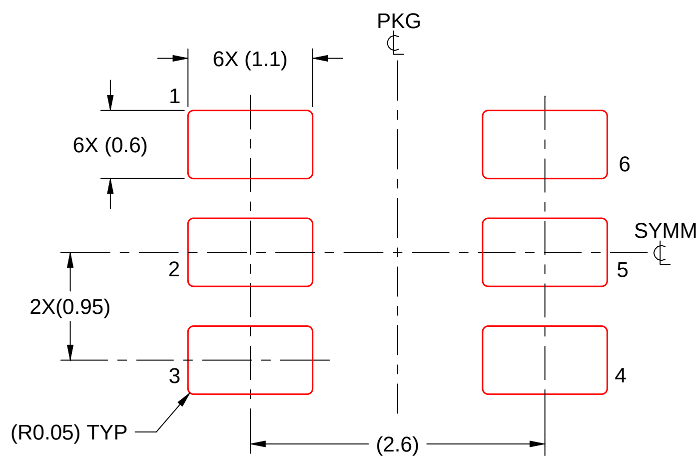
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

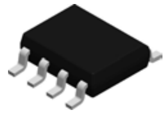


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

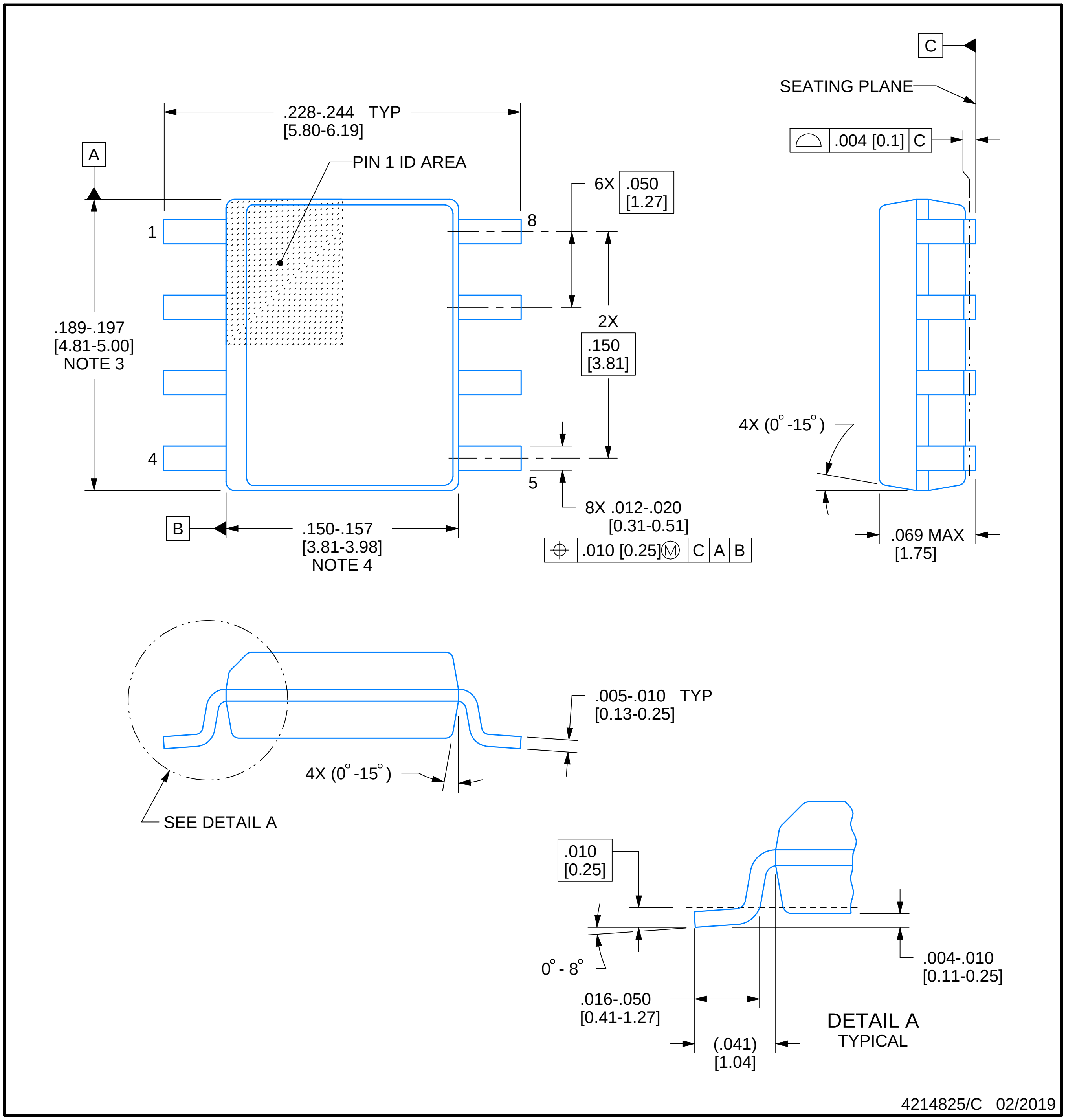
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

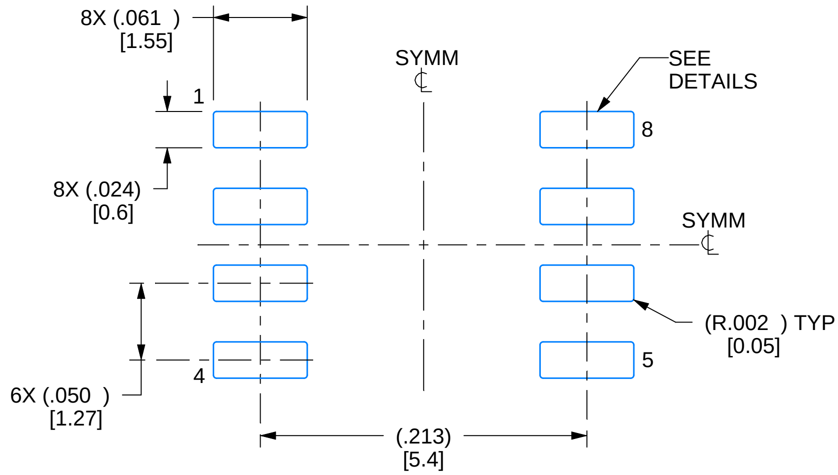
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

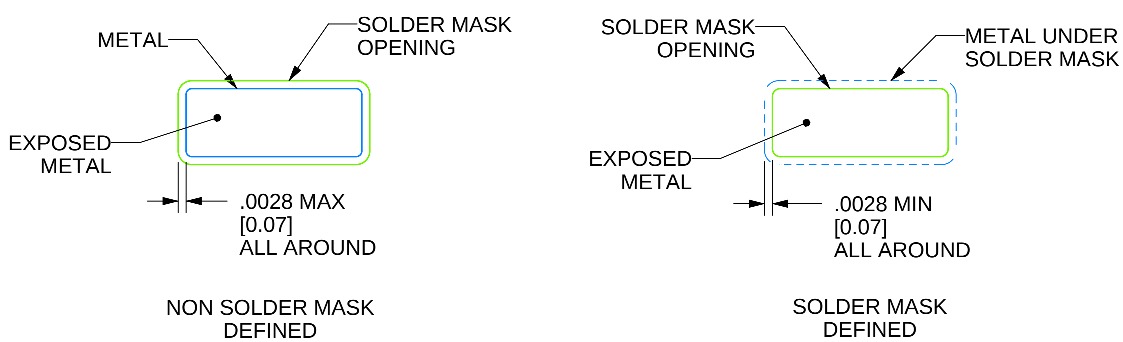


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

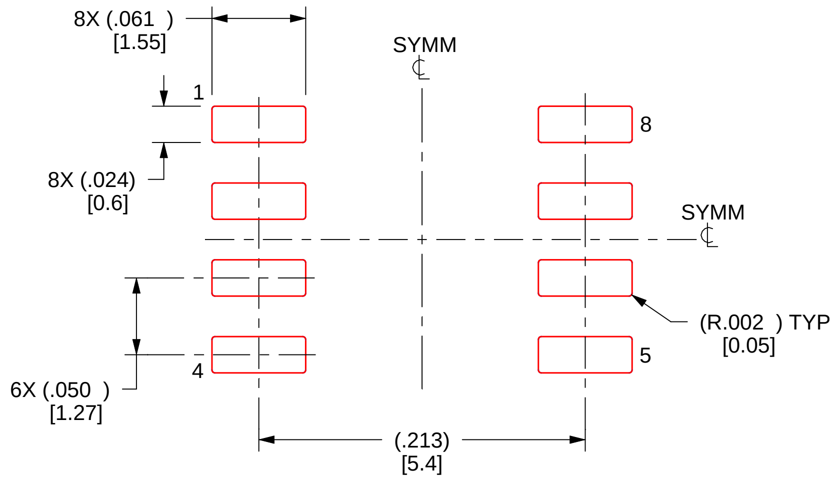


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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