



**THE DATASHEET OF
74LVTH16245BDGG,11**



74LVT16245B; 74LVTH16245B

3.3 V 16-bit transceiver; 3-state

Rev. 11 — 31 October 2018

Product data sheet

1. General description

The 74LVT16245B; 74LVTH16245B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an output enable input ($n\overline{OE}$) for easy cascading and a direction input ($n\overline{DIR}$) for direction control.

2. Features and benefits

- 16-bit bidirectional bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
 - JESD78B Class II exceeds 500 mA
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-----------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | Version |
| 74LVT16245BDL | -40 °C to +85 °C | SSOP48 | plastic shrink small outline package; 48 leads; body width 7.5 mm | SOT370-1 |
| 74LVTH16245BDL | | | | |
| 74LVT16245BDGG | -40 °C to +85 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |
| 74LVTH16245BDGG | | | | |

4. Functional diagram

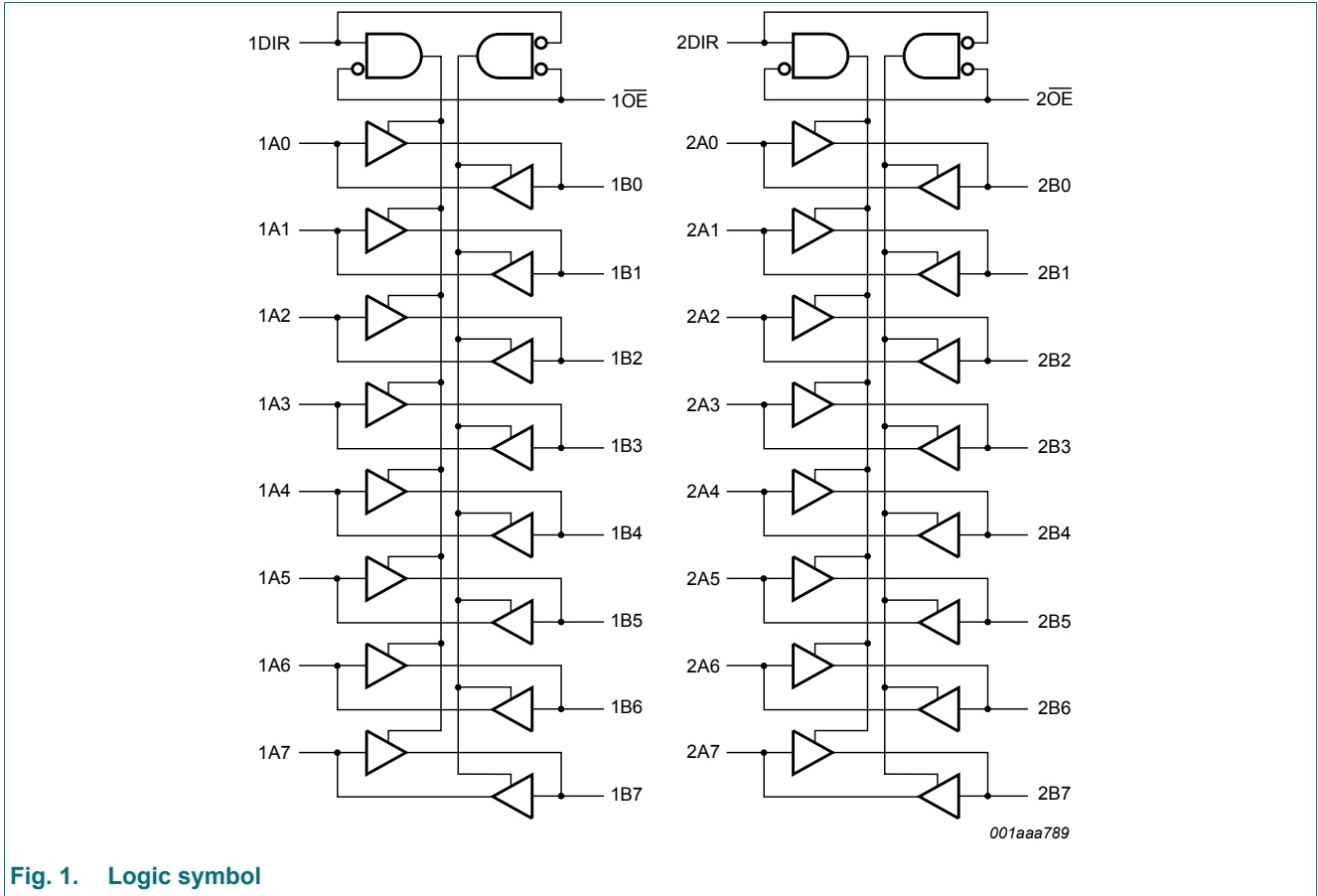


Fig. 1. Logic symbol

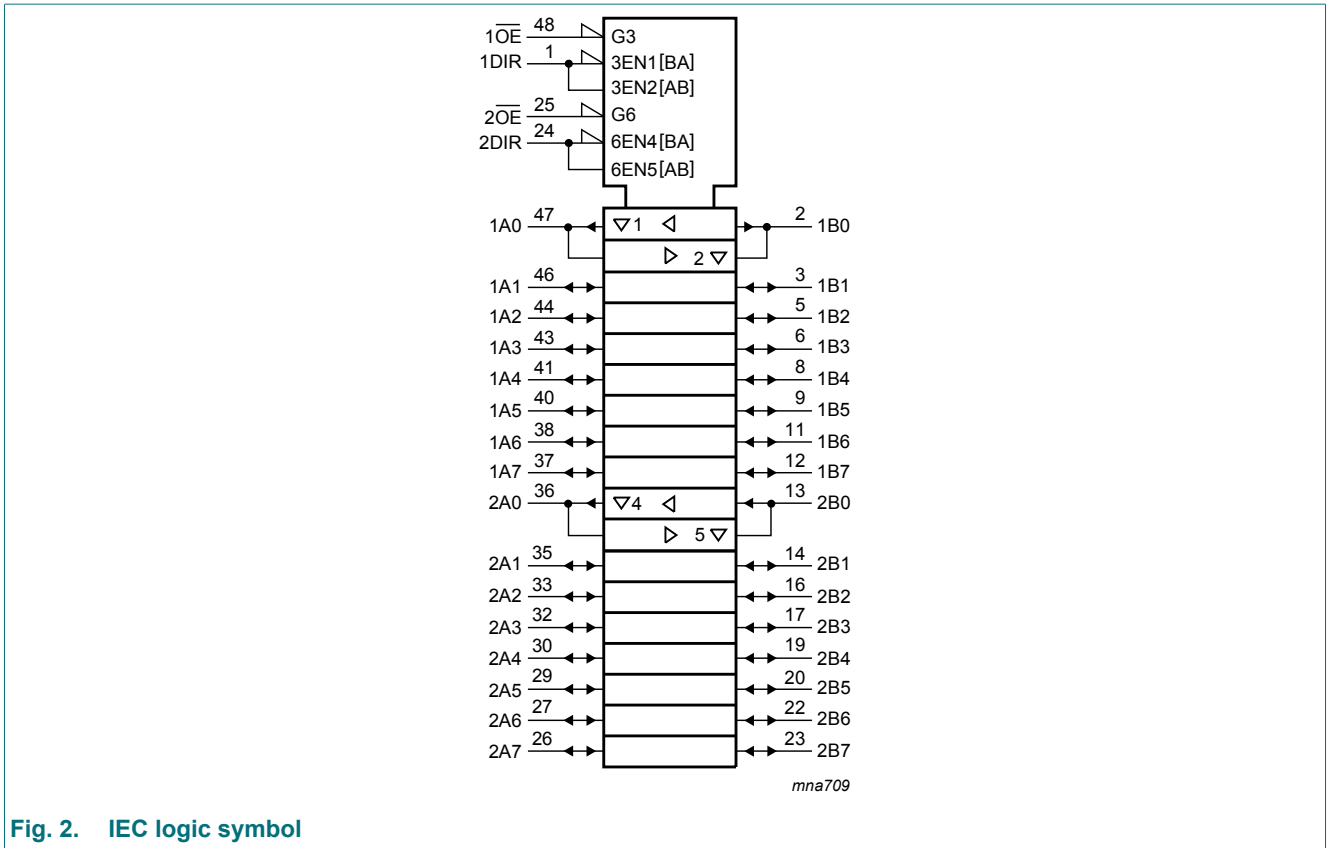


Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning

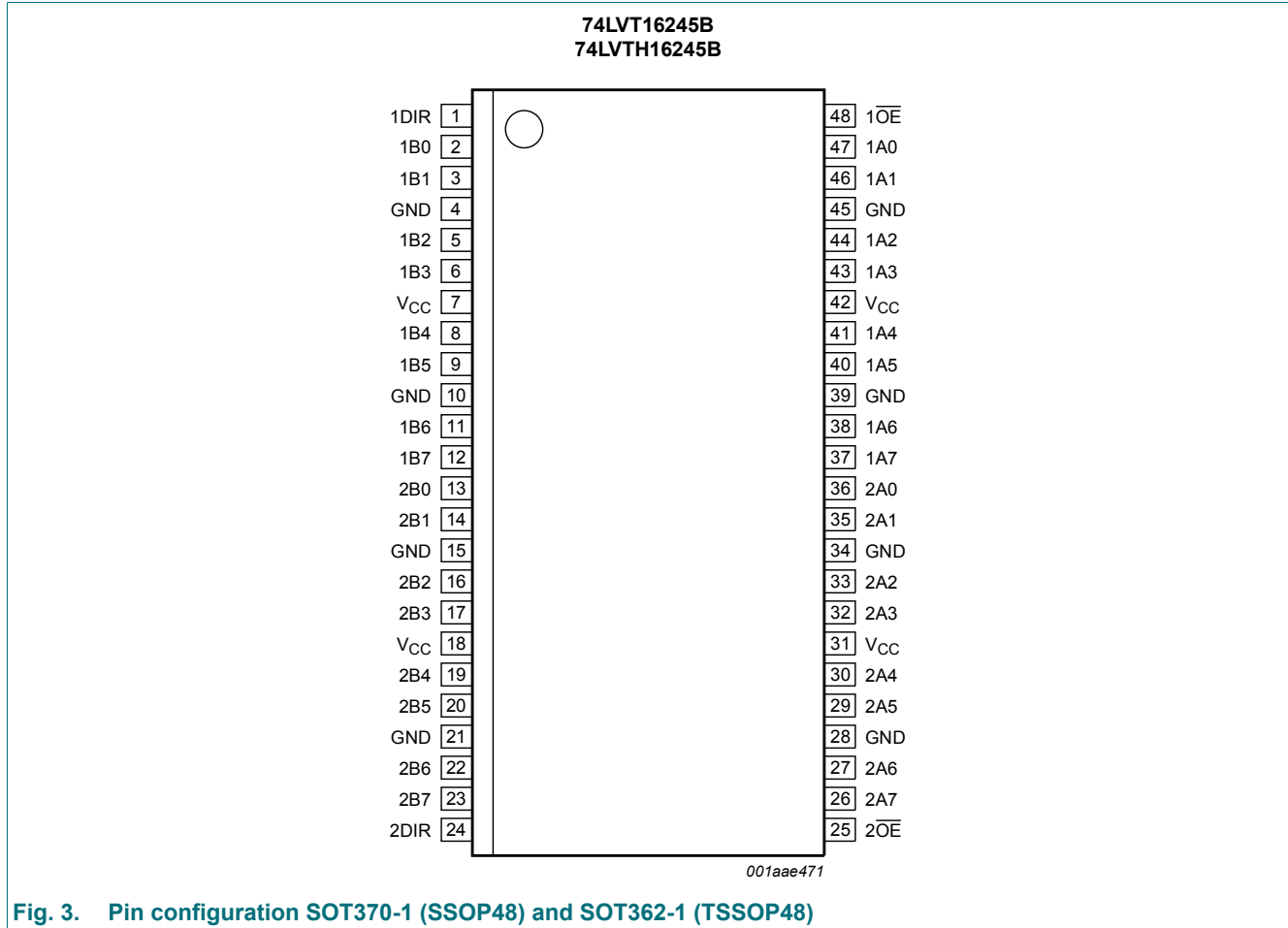


Fig. 3. Pin configuration SOT370-1 (SSOP48) and SOT362-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--|--------------------------------|----------------------------------|
| 1DIR, 2DIR | 1, 24 | direction control input |
| 1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7 | 2, 3, 5, 6, 8, 9, 11, 12 | data input/output |
| 2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7 | 13, 14, 16, 17, 19, 20, 22, 23 | data input/output |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | ground (0 V) |
| V _{CC} | 7, 18, 31, 42 | supply voltage |
| 1OE, 2OE | 48, 25 | output enable input (active LOW) |
| 2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7 | 36, 35, 33, 32, 30, 29, 27, 26 | data input/output |
| 1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7 | 47, 46, 44, 43, 41, 40, 38, 37 | data input/output |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

| Control | | Input/output | |
|---------|------|------------------|------------------|
| nOE | nDIR | nAn | nBn |
| L | L | output nAn = nBn | input |
| L | H | input | output nBn = nAn |
| H | X | Z | Z |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|--------------------------------------|------|------|------|
| V _{CC} | supply voltage | | -0.5 | +4.6 | V |
| V _I | input voltage | | [1] | +7.0 | V |
| V _O | output voltage | output in OFF-state or HIGH-state | [1] | +7.0 | V |
| I _{IK} | input clamping current | V _I < 0 V | -50 | - | mA |
| I _{OK} | output clamping current | V _O < 0 V | -50 | - | mA |
| I _O | output current | output in LOW-state | - | 128 | mA |
| | | output in HIGH-state | -64 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| T _j | junction temperature | | [2] | 150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +85 °C; | [3] | 500 | mW |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|-------------------------------------|---|-----|-----|-----|------|
| V _{CC} | supply voltage | | 2.7 | - | 3.6 | V |
| V _I | input voltage | | 0 | - | 5.5 | V |
| V _{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V _{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| I _{OH} | HIGH-level output current | | -32 | - | - | mA |
| I _{OL} | LOW-level output current | none | - | - | 32 | mA |
| | | current duty cycle ≤ 50 %; f _i ≥ 1 kHz | - | - | 64 | mA |
| T _{amb} | ambient temperature | in free-air | -40 | - | +85 | °C |
| Δt/ΔV | input transition rise and fall rate | outputs enabled | - | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit |
|----------------|------------------------------------|--|----------------|----------|---------------|---------------|
| V_{IK} | input clamping voltage | $V_{CC} = 2.7\text{ V}$; $I_{IK} = -18\text{ mA}$ | -1.2 | -0.85 | - | V |
| V_{OH} | HIGH-level output voltage | $I_{OH} = -100\text{ }\mu\text{A}$; $V_{CC} = 2.7\text{ V}$ to 3.6 V | $V_{CC} - 0.2$ | V_{CC} | - | V |
| | | $I_{OH} = -8\text{ mA}$; $V_{CC} = 2.7\text{ V}$ | 2.4 | 2.5 | - | V |
| | | $I_{OH} = -32\text{ mA}$; $V_{CC} = 3.0\text{ V}$ | 2.0 | 2.3 | - | V |
| V_{OL} | LOW-level output voltage | $V_{CC} = 2.7\text{ V}$ | | | | |
| | | $I_{OL} = 100\text{ }\mu\text{A}$ | - | 0.07 | 0.2 | V |
| | | $I_{OL} = 24\text{ mA}$ | - | 0.3 | 0.5 | V |
| | | $V_{CC} = 3.0\text{ V}$ | | | | |
| | | $I_{OL} = 16\text{ mA}$ | - | 0.25 | 0.4 | V |
| | | $I_{OL} = 32\text{ mA}$ | - | 0.3 | 0.5 | V |
| I_I | input leakage current | control pins | | | | |
| | | $V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND | - | 0.1 | ± 1 | μA |
| | | $V_{CC} = 0\text{ V}$ or 3.6 V ; $V_I = 5.5\text{ V}$ | - | 0.1 | 10 | μA |
| | | input/output data pins; $V_{CC} = 3.6\text{ V}$ [2] | | | | |
| | | $V_I = 5.5\text{ V}$ | - | 0.1 | 20 | μA |
| | | $V_I = V_{CC}$ | - | 0.5 | 10 | μA |
| | $V_I = 0\text{ V}$ | -5 | -0.1 | - | μA | |
| I_{OFF} | power-off leakage current | $V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V}$ to 4.5 V | - | 0.1 | ± 100 | μA |
| I_{BHL} | bus hold LOW current | $V_{CC} = 3\text{ V}$; $V_I = 0.8\text{ V}$ | 75 | 135 | - | μA |
| I_{BHH} | bus hold HIGH current | $V_{CC} = 3\text{ V}$; $V_I = 2.0\text{ V}$ | - | -135 | -75 | μA |
| I_{BHLO} | bus hold LOW overdrive current | nAn input; $V_I = 0\text{ V}$ to 3.6 V ; $V_{CC} = 3.6\text{ V}$ [3] | 500 | - | - | μA |
| I_{BHHO} | bus hold HIGH overdrive current | nAn input; $V_I = 0\text{ V}$ to 3.6 V ; $V_{CC} = 3.6\text{ V}$ [3] | - | - | -500 | μA |
| I_{LO} | output leakage current | output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5\text{ V}$; $V_{CC} = 3.0\text{ V}$ | - | 75 | 125 | μA |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; nOE = don't care [4] | - | 40 | ± 100 | μA |

| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit |
|-----------------|------------------------------------|---|-----|---------|------|------|
| I_{CC} | supply current | $V_{CC} = 3.6\text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$ | | | | |
| | | outputs HIGH | - | 0.07 | 0.12 | mA |
| | | outputs LOW | - | 4.7 | 6.0 | mA |
| | | outputs disabled [5] | - | 0.07 | 0.12 | mA |
| ΔI_{CC} | additional supply current | per input pin; $V_{CC} = 3.0\text{ V}$ to 3.6 V ; one input at $V_{CC} - 0.6\text{ V}$, other inputs at V_{CC} or GND [6] | - | 0.1 | 0.2 | mA |
| C_I | input capacitance | pins nDIR and n \overline{OE} , $V_O = 0\text{ V}$ or 3.0 V | - | 3 | - | pF |
| $C_{iO(off)}$ | off-state input/output capacitance | pins nAn and nBn, outputs disabled; $V_O = \text{GND}$ or V_{CC} | - | 9 | - | pF |

[1] Typical values are measured at $V_{CC} = 3.3\text{ V}$ and at $T_{amb} = 25\text{ }^\circ\text{C}$.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms .

From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ a transition time of $100\text{ }\mu\text{s}$ is permitted. This parameter is valid for $T_{amb} = 25\text{ }^\circ\text{C}$ only.

[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

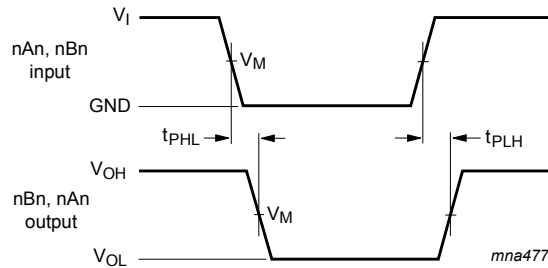
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$; For test circuit see Fig. 6.

| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit |
|-----------|-------------------------------------|---|-----|---------|-----|------|
| t_{PLH} | LOW to HIGH propagation delay | nAn to nBn or nBn to nAn; see Fig. 4 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 3.5 | ns |
| | | $V_{CC} = 3.0\text{ V}$ to 3.6 V | 1.0 | 1.9 | 3.3 | ns |
| t_{PHL} | HIGH to LOW propagation delay | nAn to nBn or nBn to nAn; see Fig. 4 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 3.5 | ns |
| | | $V_{CC} = 3.0\text{ V}$ to 3.6 V | 1.0 | 1.7 | 3.3 | ns |
| t_{PZH} | OFF-state to HIGH propagation delay | n \overline{OE} to nAn or nBn; see Fig. 5 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 5.3 | ns |
| | | $V_{CC} = 3.0\text{ V}$ to 3.6 V | 1.0 | 2.8 | 4.5 | ns |
| t_{PZL} | OFF-state to LOW propagation delay | n \overline{OE} to nAn or nBn; see Fig. 5 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 5.1 | ns |
| | | $V_{CC} = 3.0\text{ V}$ to 3.6 V | 1.0 | 2.8 | 4.1 | ns |
| t_{PHZ} | HIGH to OFF-state propagation delay | n \overline{OE} to nAn or nBn; see Fig. 5 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 5.7 | ns |
| | | $V_{CC} = 3.0\text{ V}$ to 3.6 V | 1.5 | 3.2 | 5.1 | ns |
| t_{PLZ} | LOW to OFF-state propagation delay | n \overline{OE} to nAn or nBn; see Fig. 5 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 4.6 | ns |
| | | $V_{CC} = 3.0\text{ V}$ to 3.6 V | 1.5 | 3.0 | 4.6 | ns |

[1] All typical values are at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^\circ\text{C}$.

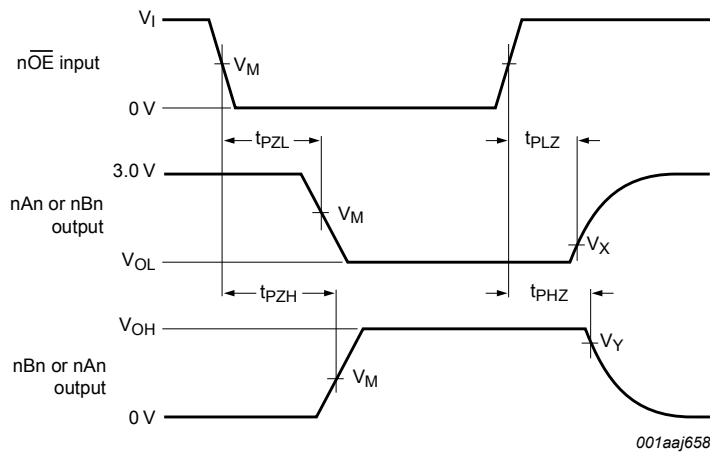
10.1. Waveforms and test circuit



Measurements points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Propagation delay input (nAn, nBn) to output (nBn, nAn)



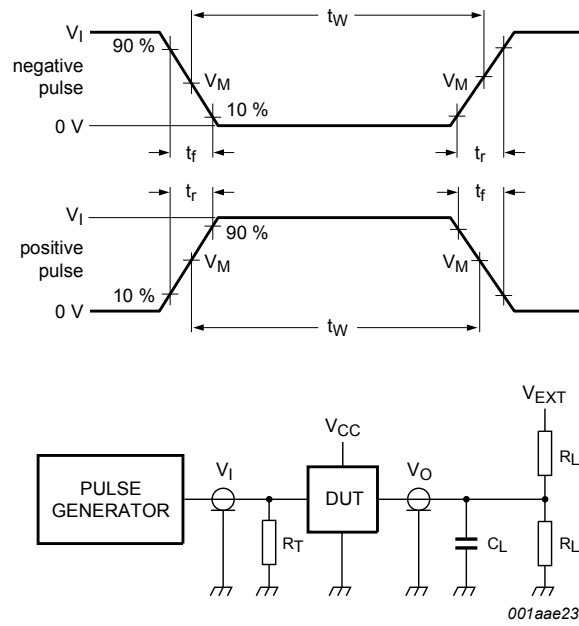
Measurements points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. 3-state output enable and disable times

Table 8. Measurement points

| Input | Output | | |
|-------|--------|------------------|------------------|
| V_M | V_M | V_X | V_Y |
| 1.5 V | 1.5 V | $V_{OL} + 0.3 V$ | $V_{OH} - 0.3 V$ |



Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 6. Test circuit for measuring switching times

Table 9. Test data

| Input | | | | Load | | V_{EXT} | | |
|-------|---------------|--------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| V_I | f_i | t_w | t_r, t_f | C_L | R_L | t_{PHZ}, t_{PZH} | t_{PLZ}, t_{PZL} | t_{PLH}, t_{PHL} |
| 2.7 V | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V | open |

11. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

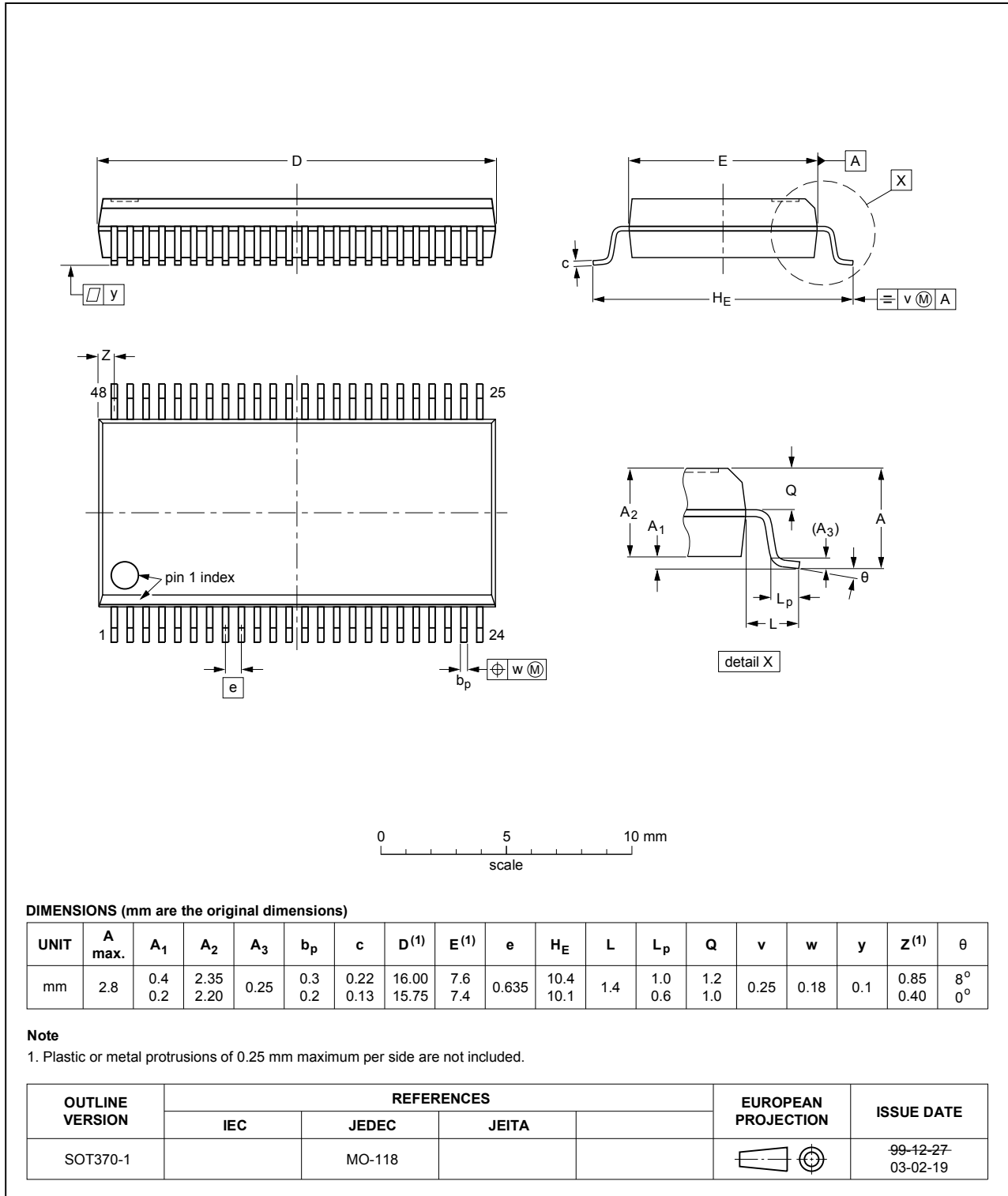


Fig. 7. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

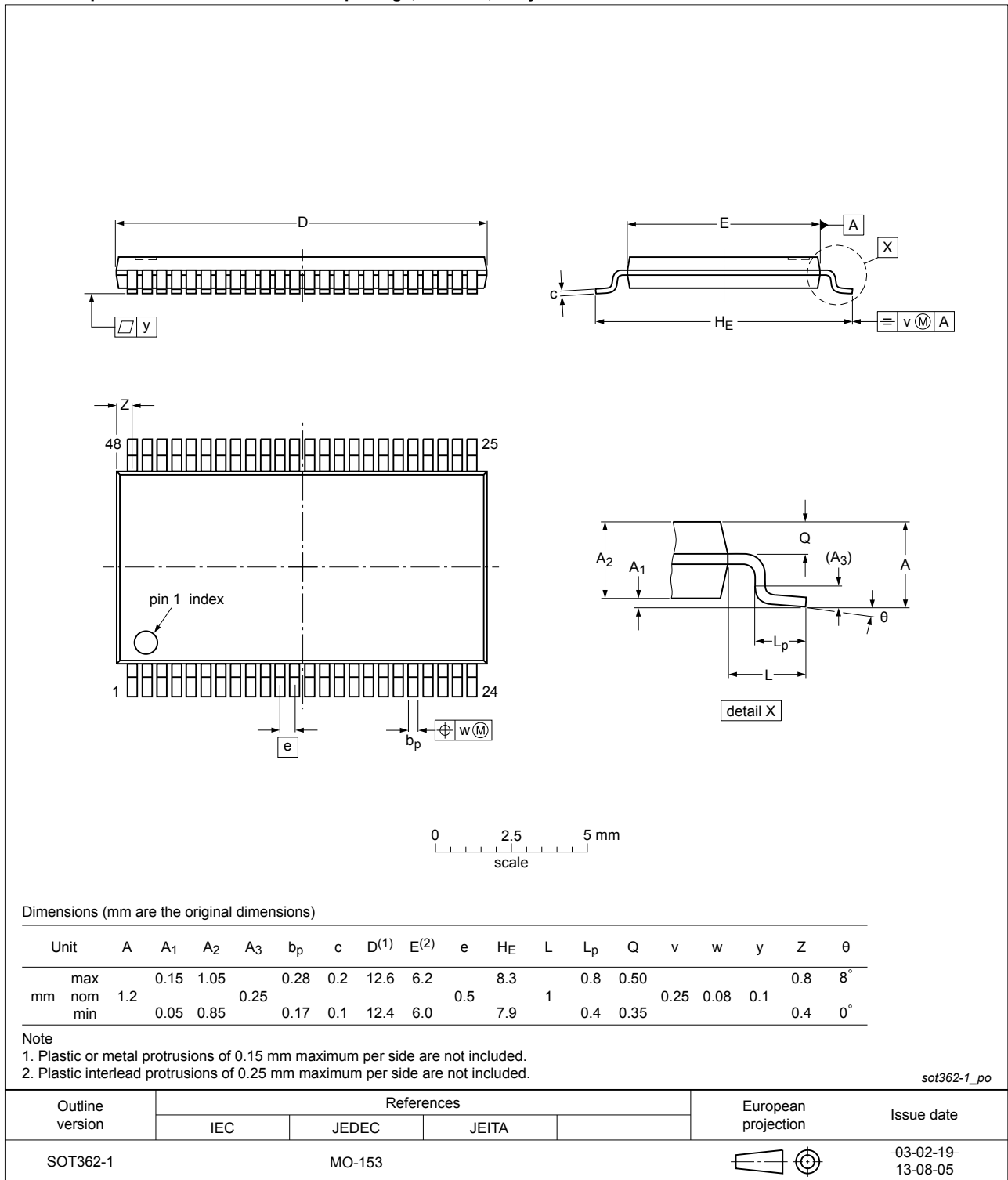


Fig. 8. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------------|--|-----------------------|---------------|-----------------------|
| 74LVT_LVTH16245B v.11 | 20181031 | Product data sheet | - | 74LVT_LVTH16245B v.10 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74LVT16245BEV (SOT702-1), 74LVT16245BBX and 74LVTH16245BBX (SOT1134-2) removed. Package outline drawing SOT362-1 updated. | | | |
| 74LVT_LVTH16245B v.10 | 20120301 | Product data sheet | - | 74LVT_LVTH16245B v.9 |
| Modifications: | <ul style="list-style-type: none"> For type number 74LVT16245BBX and 74LVTH16245BBX the sot code has changed to SOT1134-2. | | | |
| 74LVT_LVTH16245B v.9 | 20111122 | Product data sheet | - | 74LVT_LVTH16245B v.8 |
| Modifications: | <ul style="list-style-type: none"> Legal pages updated. | | | |
| 74LVT_LVTH16245B v.8 | 20110617 | Product data sheet | - | 74LVT_LVTH16245B v.7 |
| 74LVT_LVTH16245B v.7 | 20100329 | Product data sheet | - | 74LVT_LVTH16245B v.6 |
| 74LVT_LVTH16245B v.6 | 20090409 | Product data sheet | - | 74LVT_LVTH16245B v.5 |
| 74LVT_LVTH16245B v.5 | 20090312 | Product data sheet | - | 74LVT_LVTH16245B v.4 |
| 74LVT_LVTH16245B v.4 | 20060323 | Product data sheet | - | 74LVT16245B v.3 |
| 74LVT16245B v.3 | 20021031 | Product data sheet | - | 74LVT16245B v.2 |
| 74LVT16245B v.2 | 19980219 | Product specification | - | 74LVT16245B v.1 |
| 74LVT16245B v.1 | 19940523 | Product specification | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

| | |
|--|-----------|
| 1. General description | 1 |
| 2. Features and benefits | 1 |
| 3. Ordering information | 1 |
| 4. Functional diagram | 2 |
| 5. Pinning information | 4 |
| 5.1. Pinning..... | 4 |
| 5.2. Pin description..... | 4 |
| 6. Functional description | 5 |
| 7. Limiting values | 5 |
| 8. Recommended operating conditions | 5 |
| 9. Static characteristics | 6 |
| 10. Dynamic characteristics | 7 |
| 10.1. Waveforms and test circuit..... | 8 |
| 11. Package outline | 10 |
| 12. Abbreviations | 12 |
| 13. Revision history | 12 |
| 14. Legal information | 13 |

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