THE DATASHEET OF

LTC4215CUFD-3#PBF

Hot Swap Controller with I²C Compatible Monitoring

FEATURES

- **Allows Safe Insertion into Live Backplane**
- **8-Bit ADC Monitors Current and Voltage**
- **I²C/SMBus Interface**
- **Wide Operating Voltage Range: 2.9V to 15V**
- **dI/dt Controlled Soft-Start**
- **Circuit Breaker Timeout: 20µs (LTC4215-1) or 420µs (LTC4215-3)**
- **Three General Purpose Outputs**
- High Side Drive for External N-channel MOSFET
- No External Gate Capacitor Required
- Input Overvoltage/Undervoltage Protection
- Optional Latchoff or Auto-Retry After Faults
- Alerts Host After Faults
- Inrush Current Limit with Foldback
- Available in 24-Pin (4mm × 5mm) QFN

APPLICATIONS

- Live Board Insertion
- Electronic Circuit Breakers
- Computers, Servers
- Platform Management

DESCRIPTION

The LTC®4215-1/LTC4215-3 Hot Swap™ controllers allow a board to be safely inserted and removed from a live backplane. Using an external N-channel pass transistor, board supply voltage and inrush current are ramped up at an adjustable rate. An I²C interface and onboard ADC allow for monitoring of load current, voltage and fault status.

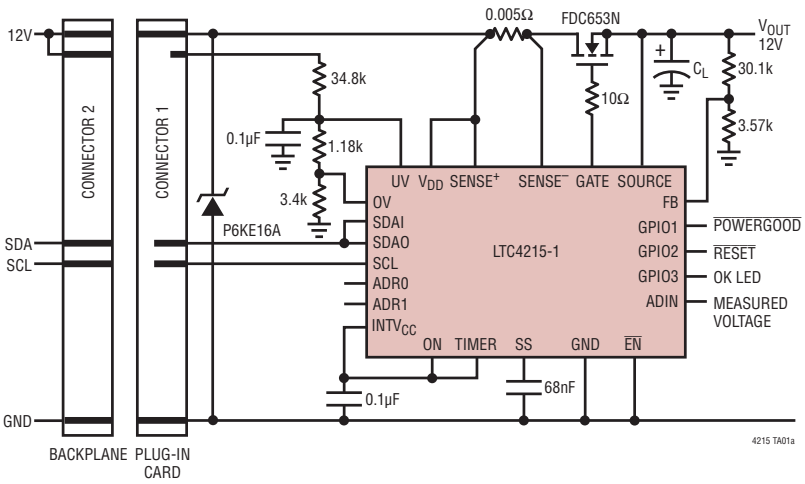
The device features adjustable foldback current limit and a soft-start pin that sets the dI/dt of the inrush current. An I²C interface may configure the part to latch off or automatically restart after the LTC4215-1/LTC4215-3 detect a current limit fault.

The controller has additional features to interrupt the host when a fault has occurred, provide three general purpose outputs, notify when output power is good, detect insertion of a load card, and power-up either automatically upon insertion or wait for an I²C command to turn on.

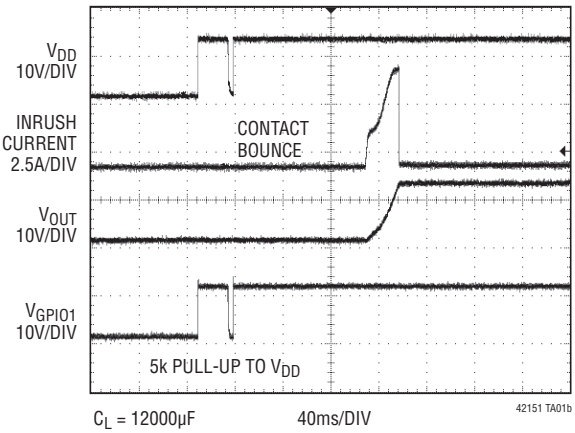
The LTC4215-1 has a 20µs circuit breaker filter for applications that require a fast fault response time. The LTC4215-3 has an extended 420µs circuit breaker filter for applications where supply transients may exceed 20µs.

TYPICAL APPLICATION

12V Application With 5A Circuit Breaker



Start-Up Waveform

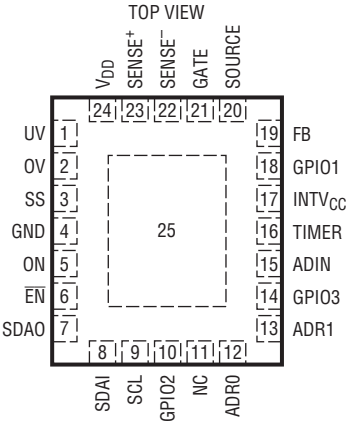


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) ..... –0.3V to 24V
Supply Voltage ($INTV_{CC}$) ..... –0.3V to 6.5V
Input Voltages
  GATE-SOURCE (Note 3) ..... –0.3V to 5V
  $SENSE^+$, $SENSE^-$ ..... V_{DD} – 0.3V to V_{DD} + 0.3V
  SOURCE ..... –5V to 24V
  $\overline{EN}$, FB, ON, OV, UV ..... –0.3V to 12V
  ADR0, ADR1, TIMER,
  ADIN, SS ..... –0.3V to $INTV_{CC}$ + 0.3V
  GPIO2, GPIO3, SCL, SDA, SDAI, SDAO –0.3V to 6.5V
Output Voltages
  GATE, GPIO1 ..... –0.3V to 24V
  GPIO2, GPIO3 ..... –0.3V to 6.5V
Operating Temperature Range
  LTC4215C-1 ..... 0°C to 70°C
  LTC4215I-1 ..... –40°C to 85°C
Storage Temperature Range
  QFN ..... –65°C to 125°C

PIN CONFIGURATION



UFD PACKAGE
24-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W (EXPOSED PAD IS SOLDERED)
EXPOSED PAD (PIN 25) PCB GND CONNECTION OPTIONAL

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4215CUFD-1#PBF	LTC4215CUFD-1#TRPBF	42151	24-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4215IUFD-1#PBF	LTC4215IUFD-1#TRPBF	42151	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC4215CUFD-3#PBF	LTC4215CUFD-3#TRPBF	42153	24-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4215IUFD-3#PBF	LTC4215IUFD-3#TRPBF	42153	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC4215CUFD-1	LTC4215CUFD-1#TR	42151	24-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4215IUFD-1	LTC4215IUFD-1#TR	42151	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC4215CUFD-3	LTC4215CUFD-3#TR	42153	24-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4215IUFD-3	LTC4215IUFD-3#TR	42153	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{DD}	Input Supply Range		●	2.9		15	V
$V_{OV(VDD)}$	Input Supply Overvoltage Threshold		●	15	15.6	16.5	V
I_{DD}	Input Supply Current		●		3	5	mA
$V_{DD(UVL)}$	Input Supply Undervoltage Lockout	V_{DD} Rising	●	2.75	2.84	2.89	V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{DD(HYST)}$	Input Supply Undervoltage Lockout Hysteresis		●	75	100	125	mV
$INTV_{CC}$	Internal Regulator Voltage	$V_{DD} \geq 3.3V$	●	2.9	3.1	3.4	V
$INTV_{CC(UVL)}$	$INTV_C$ Undervoltage Lockout	$INTV_{CC}$ Rising	●	2.55	2.64	2.79	V
$INTV_{CC(HYST)}$	$INTV_C$ Undervoltage Lockout Hysteresis		●	20	55	75	mV
Current Limit and Circuit Breaker							
$\Delta V_{SENSE(TH)}$	Circuit Breaker Threshold ($V_{DD} - V_{SENSE}$)		●	22.5	25	27.5	mV
ΔV_{SENSE}	Current Limit Voltage ($V_{DD} - V_{SENSE}$)	V_{FB} = 1.3V V_{FB} = 0V Start-Up Timer Expired	● ● ●	22 6.5 65	25 10 75	29 13 90	mV mV mV
$t_{D(OC)}$	OC Fault Filter	ΔV_{SENSE} = 50mV (LTC4215-1) ΔV_{SENSE} = 50mV (LTC4215-3)	● ●	15 300	20 420	30 600	µs µs
$I_{SENSE(IN)}$	SENSE± Pin Input Current	V_{SENSE} = 12V	●	10	20	35	µA
Gate Drive							
ΔV_{GATE}	External N-channel Gate Drive ($V_{GATE} - V_{SOURCE}$) (Note 3)	V_{DD} = 2.9V to 15V	●	4.7	5.9	6.5	V
$I_{GATE(UP)}$	External N-channel Gate Pull-Up Current	Gate On, V_{GATE} = 0V	●	–15	–20	–30	µA
$I_{GATE(DN)}$	External N-channel Gate Pull-Down Current	Gate Off, V_{GATE} = 15V	●	0.8	1	1.6	mA
$I_{GATE(DN)}$ Fast	Pull-Down Current from GATE to SOURCE During OC/UVLO	V_{DD} – SENSE = 100mV, V_{GS} = 4V		300	450	700	mA
$t_{PHL(SENSE)}$	(V_{DD} – SENSE) High to GATE Low	V_{DD} – SENSE = 100mV, C_{GS} = 10nF	●		0.5	1	µs
$V_{GS(POWERBAD)}$	Gate-Source Voltage for Power Bad Fault	V_{SOURCE} = 2.9V – 15V	●	3.8	4.3	4.7	V
Comparator Inputs							
$V_{ON(TH)}$	ON Pin Threshold Voltage	V_{ON} Rising	●	1.210	1.235	1.26	V
$\Delta V_{ON(HYST)}$	ON Pin Hysteresis		●	60	128	180	mV
$I_{ON(IN)}$	ON Pin Input Current	V_{ON} = 1.2V	●		0	±1	µA
$V_{\overline{EN}(TH)}$	$\overline{EN}$ Input Threshold	$V_{\overline{EN}}$ = Rising	●	1.215	1.235	1.255	V
$\Delta V_{\overline{EN}(HYST)}$	$\overline{EN}$ Hysteresis		●	50	128	200	mV
$I_{\overline{EN}}$	$\overline{EN}$ Pin Input Current	$\overline{EN}$ = 3.5V	●		0	±1	µA
$V_{OV(TH)}$	OV Pin Threshold Voltage	V_{OV} Rising	●	1.215	1.235	1.255	V
$\Delta V_{OV(HYST)}$	OV Pin Hysteresis		●	10	30	40	mV
$I_{OV(IN)}$	OV Pin Input Current	V_{OV} = 1.8V	●		0.2	±1	µA
$V_{UV(TH)}$	UV Pin Threshold Voltage	V_{UV} Rising	●	1.215	1.235	1.255	V
$\Delta V_{UV(HYST)}$	UV Pin Hysteresis		●	60	80	100	mV
$I_{UV(IN)}$	UV Pin Input Current	V_{UV} = 1.8V	●		0.2	±1	µA
$V_{UV(RTH)}$	UV Pin Reset Threshold Voltage	V_{UV} Falling	●	0.33	0.4	0.47	V
$\Delta V_{UV(RHYST)}$	UV Pin Reset Threshold Hysteresis		●	60	125	210	mV
V_{FB}	Foldback Pin Power Good Threshold	FB Rising	●	1.215	1.235	1.255	V
$\Delta V_{FB(HYST)}$	FB Pin Power Good Hysteresis		●	3	8	15	mV
I_{FB}	Foldback Pin Input Current	FB = 1.8V	●		0.2	±1	µA
$V_{GPIO1(TH)}$	GPIO1 Pin Input Threshold	V_{GPIO1} Rising	●	0.8	1	1.2	V
$V_{GPIO2(TH)}$	GPIO2 Pin Input Threshold	V_{GPIO2} Rising	●	1	1.6	2	V
$V_{GPIO3(TH)}$	GPIO3 Pin Input Threshold	V_{GPIO3} Rising	●	1	1.6	2	V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Other Pin Functions							
$V_{GPIO1(OL)}$	GPIO1 Pin Output Low Voltage	I_{GPIO1} = 5mA	●		0.25	0.4	V
$V_{GPIO2(OL)}$	GPIO2 Output Low Voltage	I_{GPIO2} = 3mA	●		0.2	0.4	V
$V_{GPIO3(OL)}$	GPIO3 Output Low Voltage	I_{GPIO3} = 1mA	●		0.2	0.4	V
$I_{GPIO1-3(OH)}$	GPIO1-3 Pin Input Leakage Current	V_{GPIO1} = 15V, $V_{GPIO2-3}$ = 5V	●		0	±1	µA
I_{SOURCE}	SOURCE Pin Input Current	SOURCE = 15V	●	40	80	120	µA
$t_{P(GATE)}$	Input (ON, OV, UV, $\overline{EN}$) to GATE Off Propagation Delay		●		3	5	µs
$t_{D(GATE)}$	Turn-On Delay	ON UV, OV, $\overline{EN}$ Overcurrent Auto-Retry	● ● ●	 50 2.5	1 100 5	2 150 7.5	µs ms s
$V_{TIMERL(TH)}$	Timer Low Threshold		●	0.17	0.2	0.23	V
$V_{TIMERH(TH)}$	Timer High Threshold		●	1.2	1.235	1.26	V
$I_{TIMER(UP)}$	TIMER Pin Pull-Up Current		●	–80	–100	–120	µA
$I_{TIMER(DOWN)}$	TIMER Pin Pull-Down Current for OC Auto-Retry		●	1.4	2	2.6	µA
$I_{TIMER(UP/DOWN)}$	TIMER Current Up/Down Ratio		●	40	50	60	
I_{SS}	Soft-Start Ramp Pull-Up Current	Ramping Waiting for GATE to Slew	● ●	–7.5 –0.4	–10 –0.7	–12.5 –1.0	µA µA
ADC							
RES	Resolution (No Missing Codes)		●	8			Bits
INL	Integral Nonlinearity	V_{DD} – SENSE (Note 5) SOURCE ADIN	● ● ●	–2 –1.25 –1.25	0.5 0.2 0.2	2 1.25 1.25	LSB LSB LSB
V_{OS}	Offset Error (Note 4)	V_{DD} – SENSE SOURCE ADIN	● ● ●			±2.0 ±1.0 ±1.0	LSB LSB LSB
TUE	Total Unadjusted Error	V_{DD} – SENSE SOURCE ADIN	● ● ●			±5.5 ±5.0 ±5.0	LSB LSB LSB
FSE	Full-Scale Error	V_{DD} – SENSE SOURCE ADIN	● ● ●			±5.5 ±5.0 ±5.0	LSB LSB LSB
V_{FS}	Full-Scale Voltage (255 • V_{LSB})	V_{DD} – SENSE SOURCE ADIN	● ● ●	37.625 15.14 1.205	38.45 15.44 1.23	39.275 15.74 1.255	mV V V
R_{ADIN}	ADIN Pin Sampling Resistance	V_{ADIN} = 1.28V	●	1	2		MΩ
I_{ADIN}	ADIN Pin Input Current	V_{ADIN} = 1.28V	●		0	±0.1	µA
	Conversion Rate				10		Hz
I^2C Interface							
$V_{ADR(H)}$	ADR0, ADR1, Input High Voltage		●	$INTV_{CC}$ –0.8	$INTV_{CC}$ –0.4	$INTV_{CC}$ –0.2	V
$I_{ADR(IN,Z)}$	ADR0, ADR1, Hi-Z Input Current	ADR0, ADR1= 0.8V ADR0, ADR1= $INTV_{CC}$ – 0.8V	● ●	 3		–3	µA µA
$V_{ADR(L)}$	ADR0, ADR1, Input Low Voltage		●	0.2	0.4	0.8	V
$I_{ADR(IN)}$	ADR0, ADR1, Input Current	ADR0, ADR1 = 0V, $INTV_{CC}$	●	–80		80	µA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{SDA,SCL(TH)}$	SDA, SCL Input Threshold		●	1.3	1.7	1.9	V
$I_{SDA,SCL(OH)}$	SDA, SCL Input Current	SCL, SDA = 5V	●			±1	µA
$V_{SDA(OL)}$	SDA Output Low Voltage	I_{SDA} = 3mA	●		0.2	0.4	V
I²C Interface Timing							
$f_{SCL(MAX)}$	SCL Clock Frequency	Operates with $f_{SCL} \le f_{SCL(MAX)}$	●	400	1000		kHz
$t_{BUF(MIN)}$	Bus Free Time Between Stop/Start Condition		●		0.12	1.3	µs
$t_{HD,STA(MIN)}$	Hold Time After (Repeated) Start Condition		●		30	600	ns
$t_{SU,STA(MIN)}$	Repeated Start Condition Set-Up Time		●		30	600	ns
$t_{SU,STO(MIN)}$	Stop Condition Set-Up Time		●		140	600	ns
$t_{HD,DAT(MIN)}$	Data Hold Time (Input)		●		30	100	ns
$t_{HD,DATO}$	Data Hold Time (Output)		●	300	500	900	ns
$t_{SU,DAT(MIN)}$	Data Set-Up Time		●		30	600	ns
t_{SP}	Suppressed Spike Pulse Width		●	50	110	250	ns
C_X	SCL, SDA Input Capacitance	SDAI Tied to SDAO (Note 6)	●			10	pF

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the GATE pin to a minimum of 5V above SOURCE. Driving this pin to voltages beyond the clamp may damage the device.

Note 4: Offset error is the offset voltage measured from 1LSB when the output code flickers between 0000 0000 and 0000 0001.

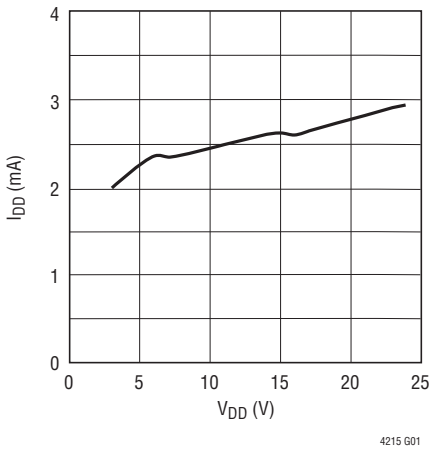
Note 5: Integral nonlinearity is defined as the deviation of a code from a precise analog input voltage. Maximum specifications are limited by the LSB step size and the single shot measurement. Typical specifications are measured from the 1/4, 1/2 and 3/4 areas of the quantization band.

Note 6: Guaranteed by design and not subject to test.

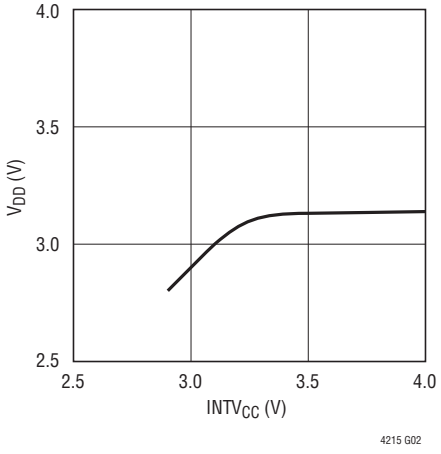
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 12V unless otherwise noted.

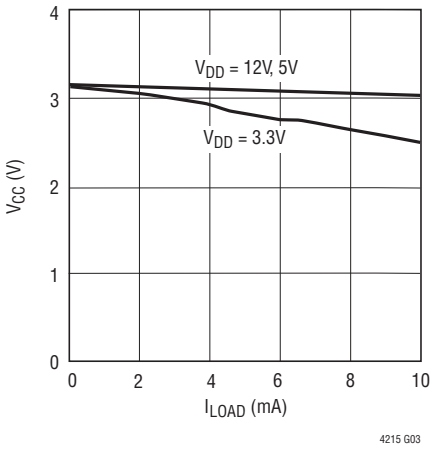
I_{DD} vs V_{DD}



$INTV_{CC}$ vs V_{DD}

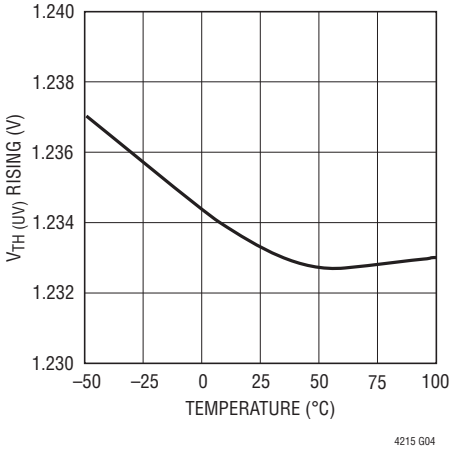


$INTV_{CC}$ vs I_{LOAD}

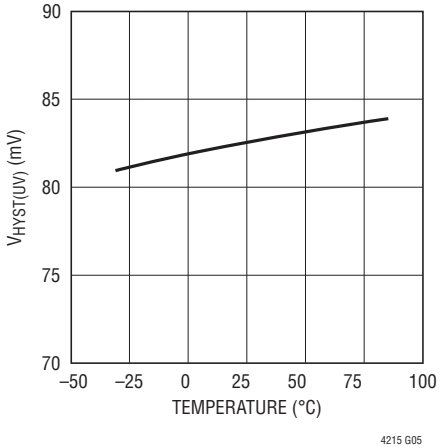


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{DD} = 12V unless otherwise noted.

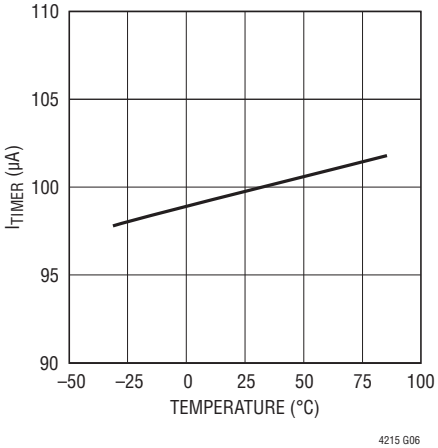
$V_{TH(UV)}$ vs Temperature



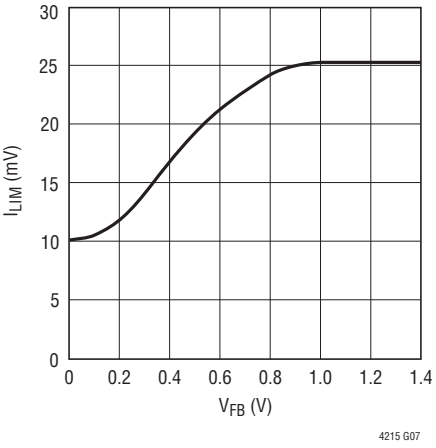
$V_{HYST(UV)}$ vs Temperature



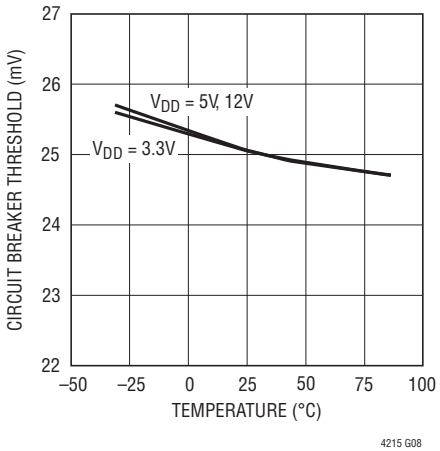
I_{TIMER} vs Temperature



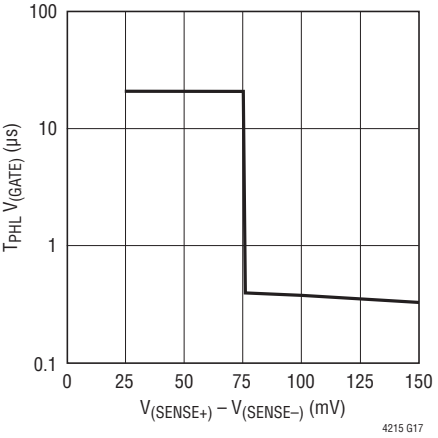
Current Limit vs V_{FB}



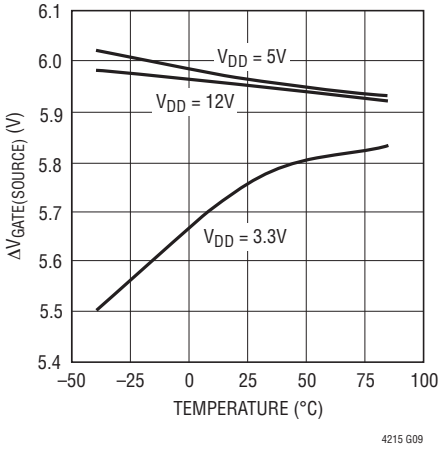
V_{TH} Circuit Breaker vs Temperature



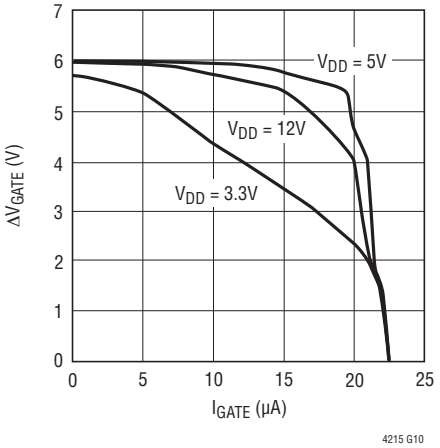
$T_{PHL(GATE)}$ vs Sense Voltage



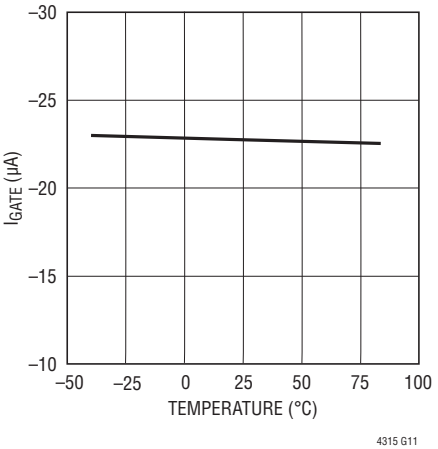
ΔV_{GATE} vs Temperature



ΔV_{GATE} vs I_{GATE}

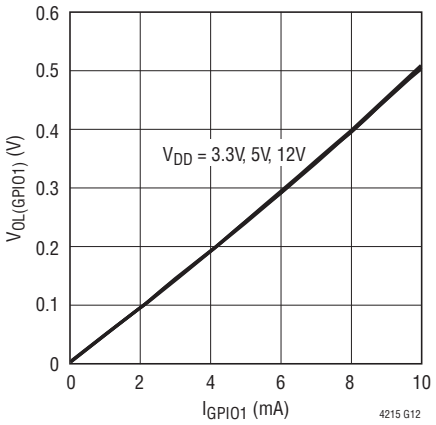


I_{GATE} Pull-Up vs Temperature

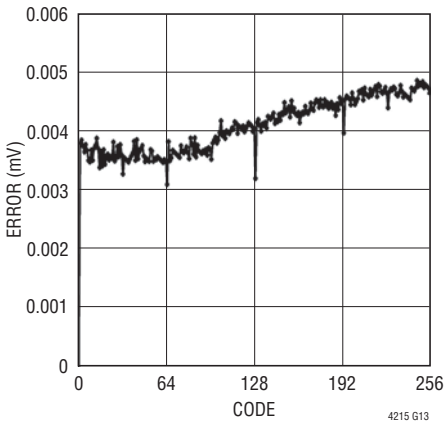


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{DD} = 12V unless otherwise noted.

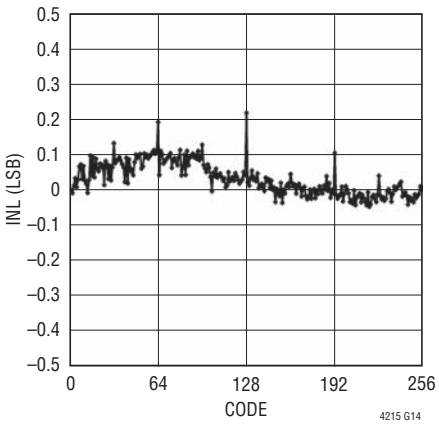
$V_{OL(GPIO1)}$ vs I_{GPIO1}



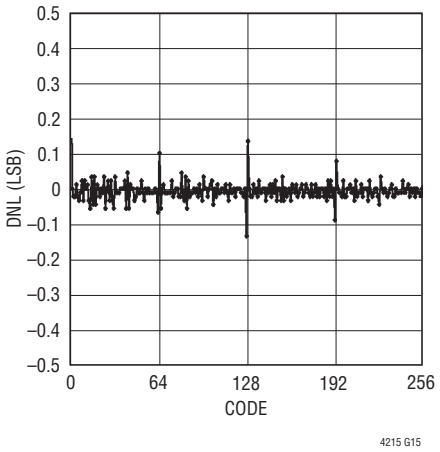
Total Unadjusted Error vs Code (ADIN)



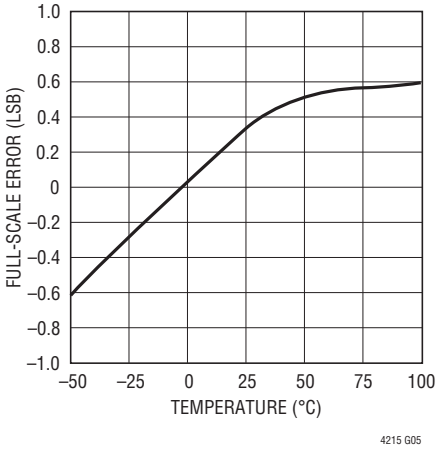
ADC INL vs Code (ADIN)



ADC DNL vs Code (ADIN)



ADC Full-Scale Error vs Temperature



PIN FUNCTIONS

ADIN: ADC Input. A voltage between 0V and 1.235V applied to this pin is measured by the onboard ADC. Tie to ground if unused.

ADR0, ADR1: Serial Bus Address Inputs. Tying these pins to ground, to the $INTV_{CC}$ pin or leaving open configures one of 9 possible addresses. See Table 1 in Applications Information.

$\overline{EN}$: Enable Input. Ground this pin to indicate a board is present and enable the N-channel MOSFET to turn on. When this pin is high, the MOSFET is not allowed to turn on. An internal 10µA current source pulls up this pin. Transitions on this pin are recorded in the Fault register. A high-to-low transition activates the logic to read the state of the ON pin and clear Faults. See Applications Information.

Exposed Pad (Pin 25): Exposed Pad may be left open or connected to device ground.

FB: Foldback Current Limit and Power Good Input. A resistive divider from the output is tied to this pin. When the voltage at this pin drops below 1.235V, power is not considered good. The power bad condition may result in the GPIO1 pin pulling low or going high impedance depending on the configuration of control register bits A6 and A7. Also a power bad fault is logged in this condition if the LTC4215-1/LTC4215-3 have finished the start-up cycle and the GATE pin is high (See Applications Information). The start-up current limit folds back from a 25mV sense voltage to 10mV as the FB pin voltage drops from 1.3V to 0V. Foldback is not active once the part leaves start-up and the current limit is increased to 75mV.

GATE: Gate Drive for External N-channel MOSFET. An internal 20µA current source charges the gate of the MOSFET. No compensation capacitor is required on the GATE pin, but a resistor and capacitor network from this pin to ground may be used to set the turn-on output voltage slew rate (See Applications Information). During turn-off there is a 1mA pull-down current. During a short circuit or undervoltage lockout (V_{DD} or $INTV_{CC}$), a 450mA pull-down current source between GATE and SOURCE is activated.

GND: Device Ground.

GPIO1: General Purpose Input/Output and Signals Power Good/Bad. Open drain logic output that is pulled to ground if bit B6 is reset. Status register bit C6 indicates if GPIO1 is high or low. High impedance output (high) by default. GPIO1 may also be configured to indicate power-good or power-bad as detected by the FB pin in status bit C3. See applications information. Tie to ground if unused. Configure according to Table 2 and 3.

GPIO2: General Purpose Input/Output and Fault Alert Output. Open drain logic output that is pulled to ground when bit D6 is set. Status register bit C5 indicates if GPIO2 is high or low. GPIO2 may be configured as an output that is pulled to ground when a fault occurs to alert the host controller. A fault alert is enabled by the ALERT register. GPIO2 is configured as a general purpose output (high) with all alerts disabled by default. See Applications Information. Tie to ground if unused. Configure according to Tables 3 and 5.

GPIO3: General Purpose Input/Output. Open drain logic output that is pulled to ground when bit D7 is set. Status register bit C2 indicates if GPIO3 is high or low. GPIO3 is configured as output low by default. See Applications Information. Tie to ground if unused. Configure according to Table 5.

$INTV_{CC}$: Low Voltage Supply Decoupling Output. Connect a 0.1µF capacitor from this pin to ground.

ON: On Control Input. A rising edge turns on the external N-channel MOSFET and a falling edge turns it off. This pin also configures the state of the FET On bit in the control register (and hence the external MOSFET) at power up. For example, if the ON pin is tied high, then the FET On bit (A3 in Table 2) goes high 100ms after power-up. Likewise if the ON pin is tied low then the part remains off after power-up until the FET On bit is set high using the I^2C bus. A high-to-low transition on this pin clears the fault register.

PIN FUNCTIONS

OV: Overvoltage Comparator Input. Connect this pin to an external resistive divider from V_{DD}. If the voltage at this pin rises above 1.235V, an overvoltage fault is detected and the GATE turns off. Tie to GND if unused.

SCL: Serial Bus Clock Input. Data at the SDA pin is shifted in or out on rising edges of SCL. This is a high impedance pin that is generally driven by an open-collector output from a master controller. An external pull-up resistor or current source is required.

SDAO: Serial Bus Data Output. Open-drain output for sending data back to the master controller or acknowledging a write operation. Normally tied to SDAI to form the SDA line. An external pull-up resistor or current source is required.

SDAI: Serial Bus Data Input. A high impedance input for shifting in address, command or data bits. Normally tied to SDAO to form the SDA line.

SENSE$^+$: Positive Current Sense Input. Connect this pin to the input of the current sense resistor. Must be connected to the same trace as V_{DD}.

SENSE$^-$: Negative Current Sense Input. Connect this pin to the output of the current sense resistor. This pin provides sense voltage feedback and monitoring for the current limit, circuit breaker and ADC.

SOURCE: N-channel MOSFET Source and ADC Input. Connect this pin to the source of the external N-channel MOSFET switch for gate drive return. This pin also serves as the ADC input to monitor output voltage. The pin provides a return for the gate pull-down circuit.

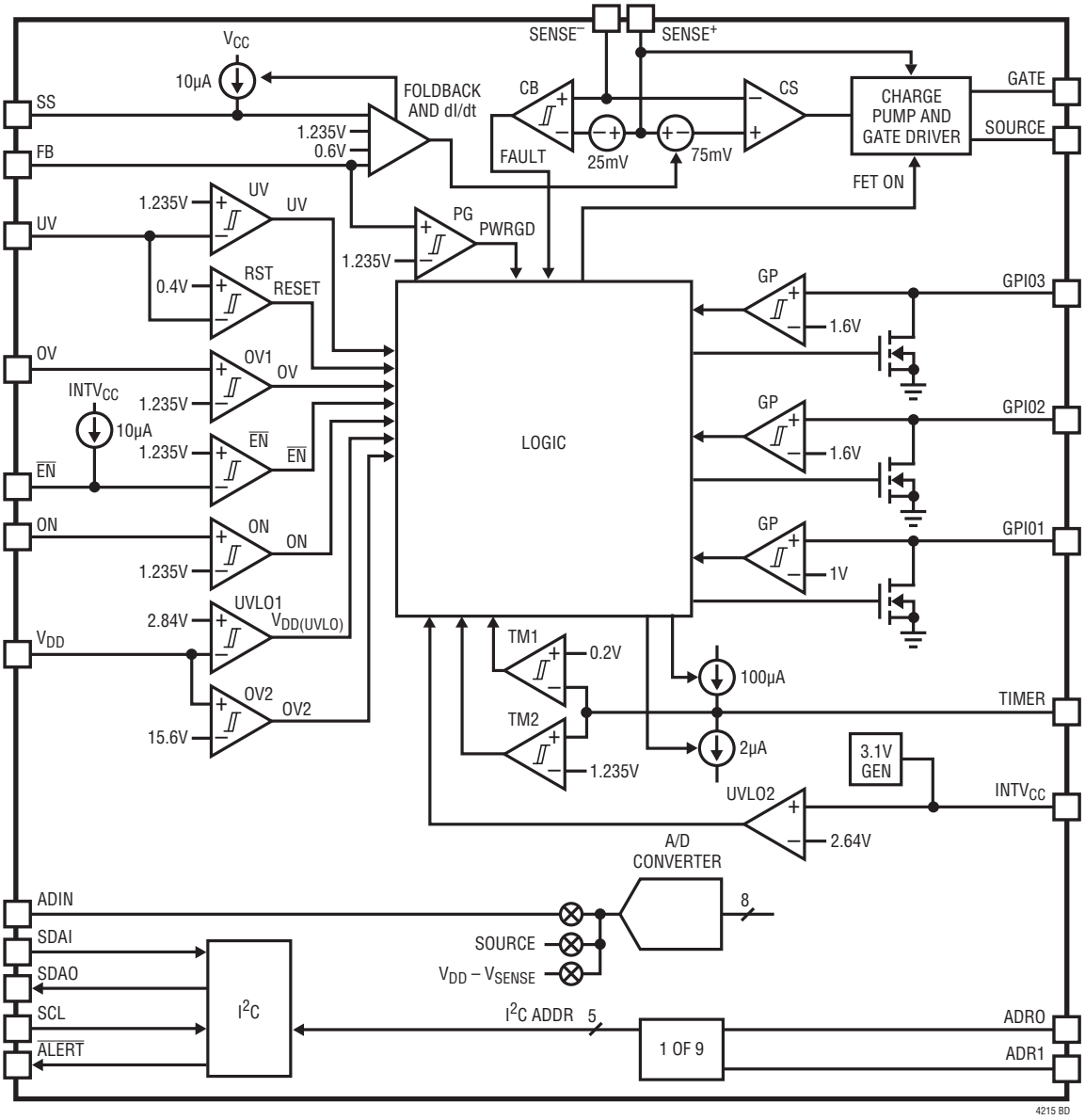
SS: Soft Start Input. Sets the inrush current slew rate at start-up. Connect a 68nF capacitor to provide 5mV/ms as the slew rate for the sense voltage in start-up. This corresponds to 1A/ms with a 5mΩ sense resistor. Note that a large soft-start capacitor and a small TIMER capacitor may result in a condition where the timer expires before the inrush current has started. Allow an additional 10nF of timer capacitance per 1nF of soft-start capacitor to ensure proper start-up. Use 1nF minimum to ensure an accurate inrush current.

TIMER: Start-Up Timer Input. Connect a capacitor between this pin and ground to set a 12.3ms/µF duration for start-up, after which an overcurrent fault is logged if the inrush is still current limited. The duration of the off time is 600ms/µF when overcurrent auto retry is enabled, resulting in a 1:50 duty cycle. An internal timer provides a 100ms start-up time and 5 seconds auto-retry time if this pin is tied to $INTV_{CC}$. Allow an additional 10nF of timer capacitance per 1nF of soft-start (SS) capacitor to ensure proper start-up. The minimum value for the TIMER capacitor is 10nF.

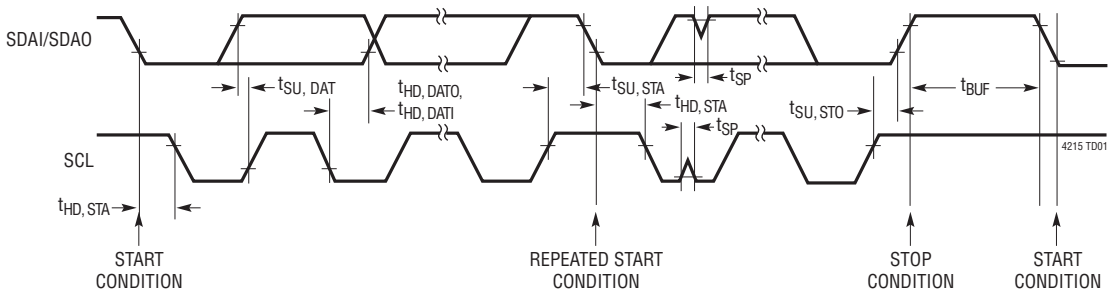
UV: Undervoltage Comparator Input. Connect this pin to an external resistive divider from V_{DD}. If the voltage at this pin falls below 1.155V, an undervoltage fault is detected and the GATE turns off. Pulling this pin below 0.4V resets all faults and allows the GATE to turn back on. Tie to $INTV_{CC}$ if unused.

V_{DD}: Supply Voltage Input. This pin has an undervoltage lockout threshold of 2.84V and overvoltage lockout threshold of 15.6V

FUNCTIONAL DIAGRAM



TIMING DIAGRAM



OPERATION

The LTC4215-1/LTC4215-3 are designed to turn a board's supply voltage on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. During normal operation, the charge pump and gate driver turn on an external N-channel MOSFET's gate to pass power to the load. The gate driver uses a charge pump that derives its power from the V_{DD} pin. Also included in the gate driver is an internal 6.5V GATE-to-SOURCE clamp. During start-up the inrush current is tightly controlled by using current limit foldback, soft start dI/dt limiting and output dV/dt limiting.

The current sense (CS) amplifier monitors the load current using the difference between the $SENSE^+$ and $SENSE^-$ pin voltages. The CS amplifier limits the current in the load by pulling back on the GATE-to-SOURCE voltage in an active control loop when the sense voltage exceeds the commanded value. The CS amplifier requires 20µA input bias current from both the $SENSE^+$ and the $SENSE^-$ pins.

A short circuit on the output to ground results in excessive power dissipation during active current limiting. To limit this power, the CS amplifier regulates the voltage between the $SENSE^+$ and $SENSE^-$ pins at 75mV.

If an overcurrent condition persists, the internal circuit breaker (CB) registers a fault when the sense voltage exceeds 25mV for more than 20µs in the case of the LTC4215-1 or 420µs in the case of the LTC4215-3. This indicates to the logic that it is time to turn off the GATE to prevent overheating. At this point the start-up TIMER capacitor voltage ramps down using the 2µA current source until the voltage drops below 0.2V (comparator TM1) which tells the logic that the pass transistor has cooled and it is safe to turn it on again if overcurrent auto-retry is enabled. If the TIMER pin is tied to $INTV_{CC}$, the cool-down time defaults to 5 seconds on an internal system timer in the logic.

The output voltage is monitored using the FB pin and the Power Good (PG) comparator to determine if the power is available for the load. The power good condition can be signaled by the GPIO1 pin using an open-drain pull-down transistor. The GPIO1 pin may also be configured to signal power bad, or as a general purpose input (GP comparator), or a general purpose open drain output.

GPIO2 and GPIO3 may also be configured as a general purpose inputs or general purpose open drain outputs. GPIO2 may also be configured to generate interrupts when faults occur.

The Functional Diagram shows the monitoring blocks of the LTC4215-1/LTC4215-3. The group of comparators on the left side includes the undervoltage (UV), overvoltage (OV), reset (RST), enable ($\overline{EN}$) and (ON) comparators. These comparators determine if the external conditions are valid prior to turning on the GATE. But first the two undervoltage lockout circuits, UVLO1 and UVLO2, validate the input supply and the internally generated 3.1V supply, $INTV_{CC}$. UVLO2 also generates the power-up initialization to the logic circuits as $INTV_{CC}$ crosses this rising threshold. If the fixed internal overvoltage comparator, OV2, detects that V_{DD} is greater than 15.6V, the part immediately generates an overvoltage fault and turns the GATE off.

Included in the LTC4215-1/LTC4215-3 is an 8-bit A/D converter. The converter has a 3-input multiplexer to select between the ADIN pin, the SOURCE pin and the V_{DD} – SENSE voltage.

An I^2C interface is provided to read the A/D registers. It also allows the host to poll the device and determine if faults have occurred. If the GPIO2 line is configured as an $\overline{ALERT}$ interrupt, the host is enabled to respond to faults in real time. The typical SDA line is divided into an SDAI (input) and SDAO (output). This simplifies applications using an optoisolator driven directly from the SDAO output. An application which uses optoisolation is shown in the Typical Applications section. The I^2C device address is decoded using the ADR0 and ADR1 pins. These inputs have three states each that decode into a total of 9 device addresses.

APPLICATIONS INFORMATION

A typical LTC4215-1/LTC4215-3 application is in a high availability system in which a positive voltage supply is distributed to power individual cards. The device measures card voltages and currents and records past and present fault conditions. The system queries each LTC4215-1/LTC4215-3 over the I^2C periodically and reads status and measurement information.

A basic LTC4215-1/LTC4215-3 application circuit is shown in Figure 1. The following sections cover turn-on, turn-off and various faults that the LTC4215-1/LTC4215-3 detect and act upon. External component selection is discussed in detail in the Design Example section.

Turn-On Sequence

The power supply on a board is controlled by using an external N-channel pass transistor (Q1) placed in the power path. Note that resistor R_S provides current detection. Resistors R1, R2 and R3 define undervoltage and overvoltage levels. R5 prevents high frequency oscillations in Q1, and R6 and C1 form an optional network that may be used to provide an output dV/dt limited start-up.

Several conditions must be present before the external MOSFET turns on. First the external supply, V_{DD}, must exceed its 2.84V undervoltage lockout levels. Next the internally generated supply, $INTV_{CC}$, must cross its 2.64V undervoltage threshold. This generates a 60µs to 120µs power-on-reset pulse. During reset the fault registers are cleared and the control registers are set or cleared as described in the register section.

After a power-on-reset pulse, the LTC4215-1/LTC4215-3 go through the following turn-on sequence. First the UV and OV comparators indicate that input power is within the acceptable range, which is indicated by bits C0-C1 in Table 4. Second, the $\overline{EN}$ pin is externally pulled low. Finally, all of these conditions must be satisfied for the duration of 100ms to ensure that any contact bounce during insertion has ended.

When these initial conditions are satisfied, the ON pin is checked and its state written to bit A3 in Table 2. If it is high, the external MOSFET is turned on. If the ON pin is low, the external MOSFET is turned on when the ON pin is brought high or if a serial bus turn-on command is sent by setting bit A3.

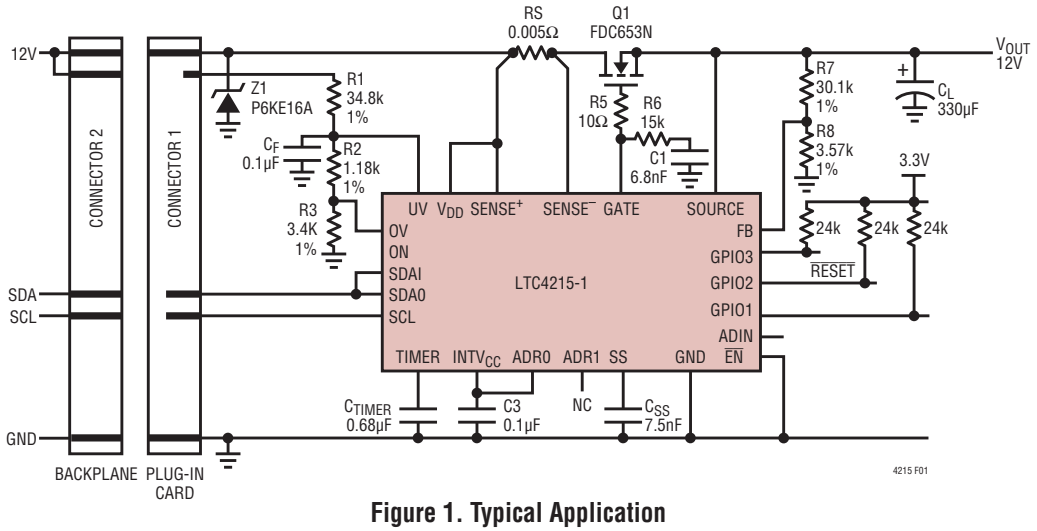


Figure 1. Typical Application

APPLICATIONS INFORMATION

The MOSFET is turned on by charging up the GATE with a 20µA current source. When the GATE voltage reaches the MOSFET threshold voltage, the MOSFET begins to turn on and the SOURCE voltage then follows the GATE voltage as it increases.

When the MOSFET is turning on, it ramps inrush current up linearly at a dI/dt rate selected by capacitor C_{SS}. Once the inrush current reaches the limit set by the FB pin, the dI/dt ramp stops and the inrush current follows the fold-back profile as shown in Figure 2. The TIMER capacitor integrates at 100µA during start-up and once it reaches its threshold of 1.235V, the part checks to see if it is in current limit, which indicates that it has started up into a short-circuit condition. If this is the case, the overcurrent fault bit, D2 in Table 5, is set and the part turns off. If the part is not in current limit, the 25mV circuit breaker is armed and the current limit is switched to 75mV. Alternately an internal 100ms start-up timer may be selected by tying the TIMER pin to $INTV_{CC}$.

As the SOURCE voltage rises, the FB pin follows as set by R7 and R8. Once FB crosses its 1.235V threshold, and the start-up timer has expired, the GPIO1 pin, if configured to indicate power-good, ceases to pull low and indicates that power is now good. Alternately bit C3 can be read to check power-good status, where a zero indicates that power is good.

If R6 and C1 are employed for a constant current during start-up, which produces a constant dV/dt at the output, a 20µA pull-up current from the gate pin slews the gate upwards and the part is not in current limit. The start-up TIMER may expire in this condition and an overcurrent (OC) fault is not generated even though start-up has not completed. Either the sense voltage increases to the 25mV CB threshold and generates an OC fault, or the FB pin voltage crosses its 1.235V power good threshold and is indicated in bit C3 as well as the GPIO1 pin if GPIO1 is configured to do so.

GATE Pin Voltage

A curve of GATE-to-SOURCE drive vs V_{DD} is shown in the Typical Performance Characteristics. At minimum input supply voltage of 2.9V, the minimum GATE-to-SOURCE drive voltage is 4.7V. The GATE-to-SOURCE voltage is clamped below 6.5V to protect the gates of logic level N-channel MOSFETs.

Turn-Off Sequence

The GATE is turned off by a variety of conditions. A normal turn-off is initiated by the ON pin going low or a serial bus turn-off command. Additionally, several fault conditions turn off the GATE. These include an input overvoltage

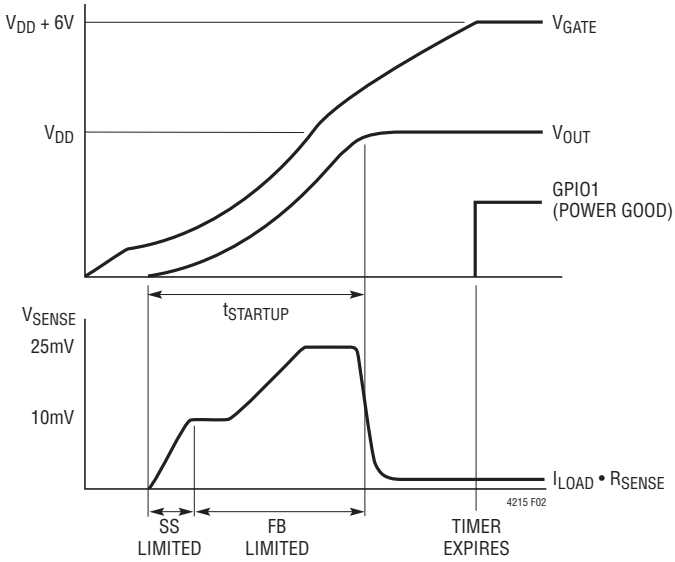


Figure 2. Power-Up Waveforms

APPLICATIONS INFORMATION

(OV pin), input undervoltage (UV pin), overcurrent circuit breaker (SENSE$^-$ pin), or $\overline{EN}$ transitioning high. Writing a logic one into the UV, OV or OC fault bits (D0-D2 in Table 5) also latches off the GATE if their auto-retry bits are set to false.

Normally the MOSFET is turned off with a 1mA current pulling down the GATE pin to ground. With the MOSFET turned off, the SOURCE and FB voltages drop as CL discharges. When the FB voltage crosses below its threshold, GPIO1 may be configured to pull low to indicate that the output power is no longer good.

If the V_{DD} pin falls below 2.74V for greater than 2µs or $INTV_{CC}$ drops below 2.60V for greater than 1µs, a fast shut down of the MOSFET is initiated. The GATE pin is pulled down with a 450mA current to the SOURCE pin.

Overcurrent Fault

The LTC4215-1/LTC4215-3 feature an adjustable current limit that protects against short circuits or excessive load current. An overcurrent fault occurs when the circuit breaker 25mV threshold has been exceeded for longer than the 20µs (LTC4215-1) or 420µs (LTC4215-3) time-out delay. Current limiting begins immediately when the current sense voltage between the V_{DD} and SENSE pins reaches 75mV.

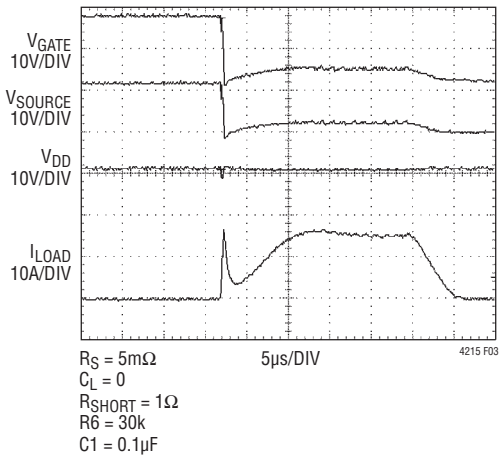


Figure 3. Short-Circuit Waveforms

The GATE pin is then brought down and regulated in order to limit the current sense voltage to 75mV. When the 20µs (LTC4215-1) or 420µs (LTC4215-3) circuit breaker time out has expired, the external MOSFET is turned off and the overcurrent fault bit D2 is set.

After the MOSFET is turned off, the TIMER capacitor begins discharging with a 2µA pull-down current. When the TIMER pin reaches its 0.2V threshold the MOSFET is allowed to turn on again if the overcurrent fault has been cleared. However, if the overcurrent auto-retry bit, A2 has been set then the MOSFET turns on again automatically without resetting the overcurrent fault. Use a minimum value of 10nF for C_T. If the TIMER pin is bypassed by tying it to $INTV_{CC}$, the part is allowed to turn on again after an internal 5 second timer has expired, in the same manner as the TIMER pin passing its 0.2V threshold.

Overvoltage Fault

An overvoltage fault occurs when either the OV pin rises above its 1.235V threshold, or the V_{DD} pin rises above its 15.6V threshold, for more than 2µs. This shuts off the GATE with a 1mA current to ground and sets the overvoltage present bit C0 and the overvoltage fault bit D0. If the pin subsequently falls back below the threshold for 100ms, the GATE is allowed to turn on again unless overvoltage auto-retry has been disabled by clearing bit A0.

Undervoltage Fault

An undervoltage fault occurs when the UV pin falls below its 1.235V threshold for more than 2µs. This turns off the GATE with a 1mA current to ground and sets undervoltage present bit C1 and undervoltage fault bit D1. If the UV pin subsequently rises above the threshold for 100ms, the GATE is turned on again unless undervoltage auto-retry has been disabled by clearing bit A1. When power is applied to the device, if UV is below its 1.235V threshold after $INTV_{CC}$ crosses its 2.64V undervoltage lockout threshold, an undervoltage fault is logged in the fault register.

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Board Present Change of State

Whenever the $\overline{EN}$ pin toggles, bit D4 is set to indicate a change of state. When the $\overline{EN}$ pin goes high, indicating board removal, the GATE turns off immediately (with a 1mA current to ground) and clears the board present bit, C4. If the $\overline{EN}$ pin is pulled low, indicating a board insertion, all fault bits except D4 are cleared and enable bit, C4, is set. If the $\overline{EN}$ pin remains low for 100ms the state of the ON pin is captured in 'FET On' control bit A3. This turns the switch on if the ON pin is tied high. There is an internal 10µA pull-up current source on the $\overline{EN}$ pin.

If the system shuts down due to a fault, it may be desirable to restart the system simply by removing and reinserting a load card. In cases where the LTC4215-1/LTC4215-3 and the switch reside on a backplane or midplane and the load resides on a plug-in card, the $\overline{EN}$ pin detects when the plug-in card is removed. Figure 4 shows an example where the $\overline{EN}$ pin is used to detect insertion. Once the plug-in card is reinserted the fault register is cleared (except for D4). After 100ms the state of the ON pin is latched into bit A3 of the control register. At this point the system starts up again.

If a connection sense on the plug-in card is driving the $\overline{EN}$ pin, insertion or removal of the card may cause the pin voltage to bounce. This results in clearing the fault register when the card is removed. The pin may be debounced using a filter capacitor, $C_{\overline{EN}}$, on the $\overline{EN}$ pin as shown in Figure 4. The filter time is given by:

$$t_{FILTER} = C_{\overline{EN}} \bullet 123\ [ms/\mu F]$$

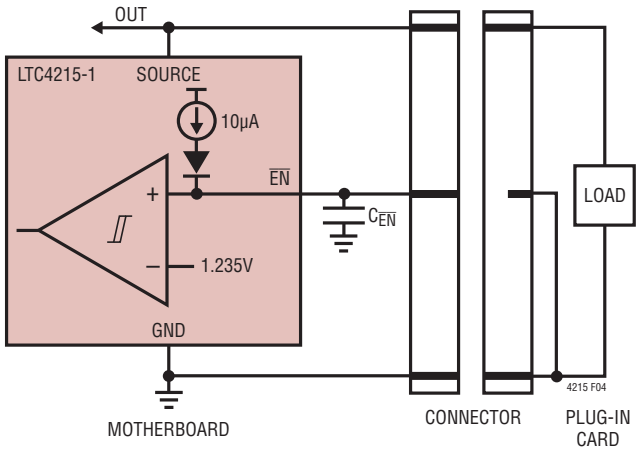

Figure 4. Plug-In Card Insertion/Removal

FET Short Fault

A FET short fault is reported if the data converter measures a current sense voltage greater than or equal to 1.6mV while the GATE is turned off. This condition sets FET short fault bit D5.

Power Bad Fault

A power bad fault is reported if the FB pin voltage drops below its 1.235V threshold for more than 2µs when the GATE is high. This pulls the GPIO1 pin low immediately when configured as power-good, and sets power-bad present bit, C3, and power bad fault bit D3. A circuit prevents power-bad faults if the GATE-to-SOURCE voltage is low, eliminating false power-bad faults during power-up or power-down. If the FB pin voltage subsequently rises back above the threshold, a power-good configured GPIO1 pin returns to a high impedance state and bit C3 is reset.

Fault Alerts

When any of the fault bits in FAULT register D are set, an optional bus alert is generated if the appropriate bit in the ALERT register B has been set. This allows only selected faults to generate alerts. At power-up the default state is to not alert on faults and the GPIO2 pin is high. If an alert is enabled, the corresponding fault causes the GPIO2 pin to pull low. After the bus master controller broadcasts the Alert Response Address, the LTC4215-1/LTC4215-3 respond with their addresses on the SDA line and releases GPIO2 as shown in Table 6. If there is a collision between two LTC4215-1/LTC4215-3s responding with their addresses simultaneously, then the device with the lower address wins arbitration and responds first. The GPIO2 line is also released if the device is addressed by the bus master if GPIO2 is pulled low due to an alert.

APPLICATIONS INFORMATION

Once the GPIO2 signal has been released for one fault, it is not pulled low again until the FAULT register indicates a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults do not generate alerts until the associated FAULT register bit has been cleared.

The GPIO2 pin may also be used as a general purpose output by setting or resetting bit D6. When D6 is set, GPIO2 will pull low, and when D6 is reset (default) GPIO2 will be high or pulled low due to an alert. The LTC4215-1/LTC4215-3 will not respond to the alert response address if the GPIO2 pin is being pulled low due to bit D6 being set. See Figure 12 for a schematic detailing the behavior of the GPIO2 pin.

Resetting Faults

Faults are reset with any of the following conditions. First, a serial bus command writing zeros to the FAULT register D bits 0-5 clears the associated faults. Second, FAULT register bits 0-5 are cleared when the switch is turned off by the ON pin or bit A3 going from high to low, if the UV pin is brought below its 0.4V reset threshold for 2µs, or if $INTV_{CC}$ falls below its 2.64V undervoltage lockout threshold. Finally, when EN is brought from high to low, only FAULT bits D0-D3 and D5 are cleared, and bit D4, which indicates a EN change of state, is set. Note that faults that are still present, as indicated in STATUS Register C, cannot be cleared.

The FAULT register is not cleared when auto-retrying. When auto-retry is disabled the existence of a D0, D1 or D2 fault keeps the switch off. As soon as the fault is cleared, the switch turns on. If auto-retry is enabled, then a high value in C0 or C1 holds the switch off and the fault register is ignored. Subsequently, when bits C0 and C1 are cleared by removal of the fault condition, the switch is allowed to turn on again. The LTC4215-1/LTC4215-3 will set bit D2 and turn off in the event of an overcurrent fault, preventing it from remaining in an overcurrent condition. If configured to auto-retry, the LTC4215-1/LTC4215-3 will continually attempt to restart after cool-down cycles until it succeeds in starting up without generating an overcurrent fault.

Data Converter

The LTC4215-1/LTC4215-3 incorporate an 8-bit ΔΣ A/D converter that continuously monitors three different voltages. The ΔΣ architecture inherently averages signal noise during the measurement period. The SOURCE pin has a 1/12.5 resistive divider to monitor a full scale voltage of 15.4V with 60mV resolution. The ADIN pin is monitored with a 1.235V full scale and 4.82mV resolution, and the voltage between the V_{DD} and SENSE pins is monitored with a 38.6mV full scale and 151µV resolution.

Results from each conversion are stored in registers E (Sense), F (Source) and G (ADIN), as seen in Tables 6-8, and are updated 10 times per second. Setting CONTROL register bit A5 invokes a test mode that halts the data converter so that registers E, F, and G may be written to and read from for software testing.

Configuring the GPIO Pins

Table 2 describes the possible states of the GPIO1 pin using the control register bits A6 and A7. At power-up, the default state is for the GPIO1 pin to be a general purpose output with output value set by bit B6 (default 1 = GPIO1 Hi-Z). Other applications for the GPIO1 pin are to go high impedance when power is good (FB pin greater than 1.235V), pull down when power is good, and a general purpose input. Digital input information can be read from bit C6 (Table 4).

Table 3 is used to configure the GPIO2 pin as a fault alert output (See Fault Alerts) and also can be used as a general purpose output and a general purpose input. By default the GPIO2 pin is a general purpose output in the high-impedance state as set by bit D6 (default 0 = GPIO2 Hi-Z, Table 5). Digital input information can be read from bit C5 (Table 4).

The GPIO3 pin is a general purpose output/input that defaults to output-low as set by bit D7 (default 1 = GPIO3 pulled low, Table 5). Digital input information can be read from bit C2 (Table 4).

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Current Limit Stability

For many applications the LTC4215-1/LTC4215-3 current limits will be stable without additional components. However there are certain conditions where additional components may be needed to improve stability. The dominant pole of the current limit circuit is set by the capacitance and resistance at the gate of the external MOSFET, and larger gate capacitance makes the current limit loop more stable. Usually a total of 8nF gate to source capacitance is sufficient for stability and is typically provided by inherent MOSFET C_{GS}, however the stability of the loop is degraded by increasing R_{SENSE} or by reducing the size of the resistor on a gate RC network if one is used, which may require additional gate to source capacitance. Board level short-circuit testing is highly recommended as board layout can also affect transient performance, for stability testing the worst case condition for current limit stability occurs when the output is shorted to ground after a normal start-up.

There are two possible parasitic oscillations when the MOSFET operates as a source follower when ramping at power-up or during current limiting. The first type of oscillation occurs at high frequencies, typically above 1MHz. This high frequency oscillation is easily damped with R5 as shown in Figure 1. In some applications, one may find that R5 helps in short-circuit transient recovery as well. However, too large of an R5 value will slow down the turn-off time. The recommended R5 range is between 5Ω and 500Ω.

The second type of source follower oscillation occurs at frequencies between 200kHz and 800kHz due to load capacitance being between 0.2µF and 9µF, the presence of R5 resistance, the absence of a drain bypass capacitor, a combination of bus wiring inductance and bus supply output impedance. To prevent the second type of oscillation avoid load capacitance below 10µF, alternately connect an external capacitor from the MOSFET gate to ground with a value greater than 1.5nF.

Supply Transients

The LTC4215-1/LTC4215-3 are designed to ride through supply transients caused by load steps. If there is a shorted load and the parasitic inductance back to the supply is greater than 0.5µH, there is a chance that the supply collapses before the active current limit circuit brings down the GATE pin. If this occurs, the undervoltage monitors pull the GATE pin low. The undervoltage lockout circuit has a 2µs filter time after V_{DD} drops below 2.74V. The UV pin reacts in 2µs to shut the GATE off, but it is recommended to add a filter capacitor C_F to prevent unwanted shutdown caused by a transient. Eventually either the UV pin or undervoltage lockout responds to bring the current under control before the supply completely collapses.

Supply Transient Protection

The LTC4215-1/LTC4215-3 are safe from damage with supply voltages up to 24V. However, spikes above 24V may damage the part. During a short-circuit condition,

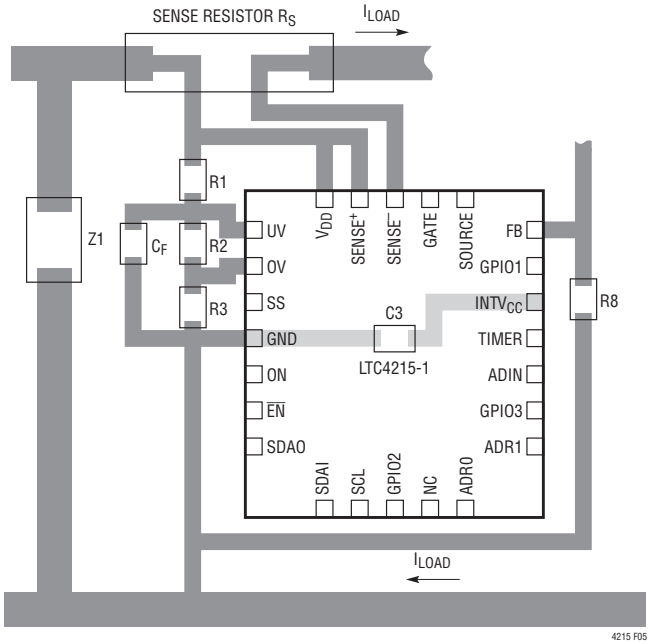

Figure 5. Recommended Layout

APPLICATIONS INFORMATION

large changes in current flowing through power supply traces may cause inductive voltage spikes which exceed 24V. To minimize such spikes, the power trace inductance should be minimized by using wider traces or heavier trace plating. Also, a snubber circuit dampens inductive voltage spikes. Build a snubber by using a 100Ω resistor in series with a 0.1µF capacitor between V_{DD} and GND. A surge suppressor, Z1 in Figure 1, at the input can also prevent damage from voltage surges.

Design Example

As a design example, take the following specifications: V_{IN} = 12V, I_{MAX} = 5A, I_{INRUSH} = 1A, dI/dt_{INRUSH} = 10A/ms, C_L = 330µF, $V_{UV(ON)}$ = 10.75V, $V_{OV(OFF)}$ = 14.0V, $V_{PWRGD(UP)}$ = 11.6V, and I^2C ADDRESS = 1001011. This completed design is shown in Figure 1.

Selection of the sense resistor, R_S, is set by the overcurrent threshold of 25mV:

$$R_S = \frac{25mV}{I_{MAX}} = 0.005\Omega$$

The MOSFET is sized to handle the power dissipation during inrush when output capacitor C_L is being charged. A method to determine power dissipation during inrush is based on the principle that:

Energy in C_L = Energy in Q1

This uses:

$$\text{Energy in } C_L = \frac{1}{2}CV^2 = \frac{1}{2}(0.33mF)(12)^2$$

or 0.024 Joules. Calculate the time it takes to charge up C_{OUT}:

$$t_{STARTUP} = C_L \bullet \frac{V_{DD}}{I_{INRUSH}} = 0.33mF \bullet \frac{12V}{1A} = 4ms$$

The power dissipated in the MOSFET:

$$P_{DISS} = \frac{\text{Energy in } C_L}{t_{STARTUP}} = 6W$$

The SOA (safe operating area) curves of candidate MOSFETs must be evaluated to ensure that the heat capacity of the package tolerates 6W for 4ms. The SOA curves of the Fairchild FDC653N provide for 2A at 12V (24W) for 10ms, satisfying this requirement. Since the FDC653N has less than 8nF of gate capacitance and we are using a GATE RC network, the short circuit stability of the current limit should be checked and improved by adding a capacitor from GATE to SOURCE if needed.

The inrush current is set to 1A using C1:

$$C1 = C_L \bullet \frac{I_{GATE}}{I_{INRUSH}}$$

$$C1 = 0.33mF \bullet \frac{20\mu A}{1A} \text{ or } C1 = 6.8nF$$

The inrush dI/dt is set to 10A/ms using C_{SS}:

$$C_{SS} = \frac{I_{SS}}{dI/dt\left(\frac{A}{s}\right)} \bullet 0.0375 \bullet \frac{1}{R_{SENSE}}$$

$$= \frac{10\mu A}{10000} \bullet 0.0375 \bullet \frac{1}{5m\Omega} = 7.5nF$$

For a start-up time of 4ms with a 2x safety margin we choose:

$$C_{TIMER} = 2 \bullet \frac{t_{STARTUP}}{12.3ms/\mu F} + C_{SS} \bullet 10$$

$$C_{TIMER} = \frac{8ms}{12.3ms/\mu F} + 7.5nF \bullet 10 \cong 0.68\mu F$$

Note the minimum value of C_{TIMER} is 10nF, and each 1nF of soft-start capacitance needs 10nF of TIMER capacitance/time during start-up.

The UV and OV resistor string values can be solved in the following method. First pick R3 based on I_{STRING} being

APPLICATIONS INFORMATION

1.235V/R3 at the edge of the OV rising threshold, where I_{STRING} > 40µA. Then solve the following equations:

$$R2 = \frac{V_{OV(OFF)}}{V_{UV(ON)}} \bullet R3 \bullet \frac{UV_{TH(RISING)}}{OV_{TH(FALLING)}} - R3$$

$$R1 = \frac{V_{UV(ON)} \bullet (R3+R2)}{UV_{TH(RISING)}} - R3 - R2$$

In our case we choose R3 to be 3.4k to give a resistor string currrent below 100µA. Then solving the equations results in R2 = 1.16k and R1 = 34.6k.

The FB divider is solved by picking R8 and solving for R7, choosing 3.57k for R8 we get:

$$R7 = \frac{V_{PWRGD(UP)} \bullet R8}{FB_{TH(RISING)}} - R8$$

Resulting in R7 = 30k.

A 0.1µF capacitor, C_F, is placed on the UV pin to prevent supply glitches from turning off the GATE via UV or OV.

The address is set with the help of Table 1, which indicates binary address 1001011 corresponds to address 4. Address 4 is set by setting ADR1 open and ADR0 high.

Next the value of R5 and R6 are chosen to be the default values 10Ω and 15k as discussed previously.

In addition a 0.1µF ceramic bypass capacitor is placed on the $INTV_{CC}$ pin.

Layout Considerations

To achieve accurate current sensing, a Kelvin connection is required. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530µΩ. Small resistances add up quickly in high current applications. To improve noise immunity, put the resistive dividers to the UV, OV and FB pins close to the device and keep traces to V_{DD} and GND short. It is also important to put the bypass capacitor for the $INTV_{CC}$ pin, C3, as close as possible between $INTV_{CC}$ and GND. A 0.1µF capacitor from the UV pin (and OV pin through resistor R2) to GND also helps reject supply noise. Figure 4 shows a layout that addresses these issues. Note that a surge suppressor, Z1, is placed between supply and ground using wide traces.

Digital Interface

The LTC4215-1/LTC4215-3 communicate with a bus master using a 2-wire interface compatible with I²C Bus and SMBus, an I²C extension for low power devices.

The LTC4215-1/LTC4215-3 are read-write slave devices and support SMBus bus Read Byte, Write Byte, Read Word and Write Word commands. The second word in a Read Word command is identical to the first word. The second word in a Write Word command is ignored. Data formats for these commands are shown in Figures 6 to 11.

START and STOP Conditions

When the bus is idle, both SCL and SDA are high. A bus master signals the beginning of a transmission with a start condition by transitioning SDA from high to low while SCL is high, as shown in Figure 6. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

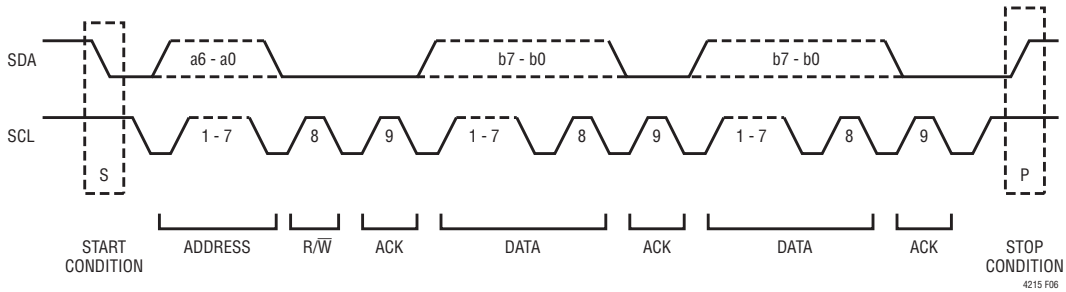

Figure 6. Data Transfer Over I²C or SMBus

APPLICATIONS INFORMATION

I²C Device Addressing

Nine distinct bus addresses are available using two 3-state address pins, ADR0 and ADR1. Table 1 shows the correspondence between pin states and addresses. Note that address bits B7 and B6 are internally configured to "10". In addition, the LTC4215-1/LTC4215-3 respond to two special addresses. Address (1011 111) is a mass write address that writes to all LTC4215-1/LTC4215-3s, regardless of their individual address settings. Mass write can be disabled by setting register bit A4 to zero. Address (0001 100) is the SMBus Alert Response Address. If the LTC4215-1/LTC4215-3 are pulling low on the GPIO2 pin due to an alert, it acknowledges this address by broadcasting its address and releasing the GPIO2 pin.

S	ADDRESS	$\overline{W}$	A	COMMAND	A	DATA	A	P
	1 0 a4:a0	0	0	X X X X X b2:b0	0	b7:b0	0	

FROM MASTER TO SLAVE
FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
$\overline{A}$: NOT ACKNOWLEDGE (HIGH)
R: READ BIT (HIGH)
$\overline{W}$: WRITE BIT (LOW)
S: START CONDITION
P: STOP CONDITION

4215 F07

Figure 7. LTC4215-1/LTC4215-3 Serial Bus SDA Write Byte Protocol

S	ADDRESS	$\overline{W}$	A	COMMAND	A	DATA	A	DATA	A	P
	1 0 a4:a0	0	0	X X X X X b2:b0	0	b7:b0	0	X X X X X X X X	0	

4215 F08

Figure 8. LTC4215-1/LTC4215-3 Serial Bus SDA Write Word Protocol

S	ADDRESS	$\overline{W}$	A	COMMAND	A	S	ADDRESS	R	A	DATA	$\overline{A}$	P
	1 0 a4:a0	0	0	X X X X X b2:b0	0		1 0 a4:a0	1	0	b7:b0	1	

4215 F10

Figure 9. LTC4215-1/LTC4215-3 Serial Bus SDA Read Byte Protocol

S	ADDRESS	$\overline{W}$	A	COMMAND	A	S	ADDRESS	R	A	DATA	A	DATA	$\overline{A}$	P
	1 0 a4:a0	0	0	X X X X X b2:b0	0		1 0 a4:a0	1	0	b7:b0	0	b7:b0	1	

4215 F11

Figure 10. LTC4215-1/LTC4215-3 Serial Bus SDA Read Word Protocol

S	ALERT RESPONSE ADDRESS	R	A	DEVICE ADDRESS	$\overline{A}$	P
	0 0 0 1 1 0 0	1	0	1 0 a4:a0 0	1	

4215 F11

Figure 11. LTC4215-1/LTC4215-3 Serial Bus SDA Alert Response Protocol

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Acknowledge

The acknowledge signal is used in handshaking between transmitter and receiver to indicate that the last byte of data was received. The transmitter always releases the SDA line during the acknowledge clock pulse. When the slave is the receiver, it pulls down the SDA line so that it remains LOW during this pulse to acknowledge receipt of the data. If the slave fails to acknowledge by leaving SDA high, then the master may abort the transmission by generating a STOP condition. When the master is receiving data from the slave, the master pulls down the SDA line during the clock pulse to indicate receipt of the data. After the last byte has been received the master leaves the SDA line HIGH (not acknowledge) and issues a stop condition to terminate the transmission.

Write Protocol

The master begins communication with a START condition followed by the seven bit slave address and the R/$\overline{W}$ bit set to zero, as shown in Figure 7. The addressed LTC4215-1/LTC4215-3 acknowledge this and then the master sends a command byte which indicates which internal register the master wishes to write. The LTC4215-1/LTC4215-3 acknowledge this and then latch the lower three bits of the command byte into its internal Register Address pointer. The master then delivers the data byte and the LTC4215-1/LTC4215-3 acknowledge once more and latch the data into its control register. The transmission is ended when the master sends a STOP condition. If the master continues sending a second data byte, as in a Write Word command, the second data byte is acknowledged by the LTC4215-1/LTC4215-3 but ignored, as shown in Figure 8.

Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave address and the R/$\overline{W}$ bit set to zero, as shown in Figure 9. The addressed LTC4215-1/LTC4215-3 acknowledge this and then the master sends a command byte which indicates which internal register the master wishes to read. The LTC4215-1/LTC4215-3 acknowledge this and then latch the lower three bits of the command byte into its internal Register Address pointer. The master then sends a repeated START condition followed by the same seven bit address with the R/$\overline{W}$ bit now set to one. The LTC4215-1/LTC4215-3 acknowledge and send the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the

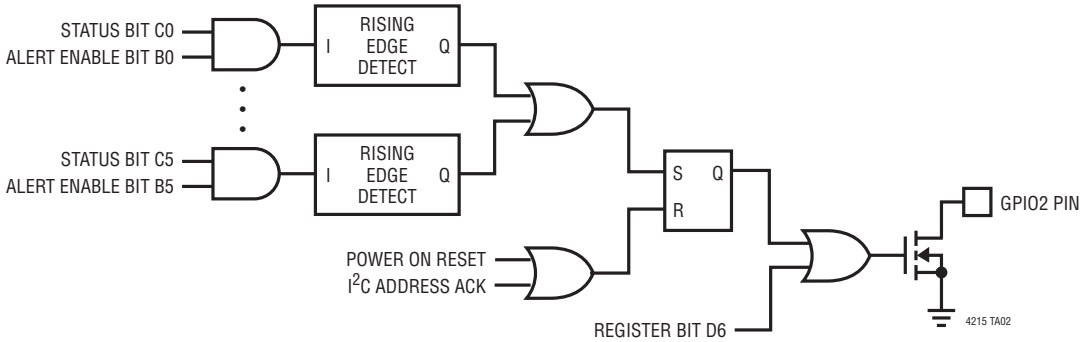

Figure 12. Control Logic for GPIO2 Pin

APPLICATIONS INFORMATION

master acknowledges the transmitted data byte, as in a Read Word command, Figure 10, the LTC4215-1/LTC4215-3 repeat the requested register as the second data byte.

Alert Response Protocol

When any of the fault bits in FAULT register D are set, an optional bus alert is generated if the appropriate bit in the ALERT register B is also set. If an alert is enabled, the corresponding fault causes the GPIO2 pin to pull low. After the bus master controller broadcasts the Alert Response Address, the LTC4215-1/LTC4215-3 respond with their address on the SDA line and then release GPIO2 as shown in Figure 11. The GPIO2 line is also released if the device is addressed by the bus master. The GPIO2 signal is not pulled low again until the FAULT register indicates a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults do not generate alerts until the associated FAULT register bit has been cleared.

Table 1. LTC4215-1/LTC4215-3 Device Addressing

DESCRIPTION*	DEVICE ADDRESS	DEVICE ADDRESS								LTC4215-1/LTC4215-3 ADDRESS PINS	
	h	7	6	5	4	3	2	1	0	ADR1	ADR0
Mass Write	BE	1	0	1	1	1	1	1	0	X	X
Alert Response	19	0	0	0	1	1	0	0	1	X	X
8	90	1	0	0	1	0	0	0	X	NC	L
9	92	1	0	0	1	0	0	1	X	H	NC
10	94	1	0	0	1	0	1	0	X	NC	NC
11	96	1	0	0	1	0	1	1	X	NC	H
12	98	1	0	0	1	1	0	0	X	L	L
13	9A	1	0	0	1	1	0	1	X	H	H
14	9C	1	0	0	1	1	1	0	X	L	NC
15	9E	1	0	0	1	1	1	1	X	L	H
25	B2	1	0	1	1	0	0	1	X	H	L

*Subset of LTC4215 addresses

APPLICATIONS INFORMATION

Table 2. CONTROL Register A (00h)—Read/Write

BIT	NAME	OPERATION
A7:6	GPIO1 Configure	<table><tr><th>FUNCTION</th><th>A6</th><th>A7</th><th>GPIO PIN</th></tr><tr><td>Power Good</td><td>0</td><td>0</td><td>GPIO = $\overline{C3}$</td></tr><tr><td>$\overline{\text{Power Good}}$</td><td>0</td><td>1</td><td>GPIO = C3</td></tr><tr><td>General Purpose Output (Default)</td><td>1</td><td>0</td><td>GPIO = B6</td></tr><tr><td>General Purpose Input</td><td>1</td><td>1</td><td>C6 = GPIO1</td></tr></table>
A5	Test Mode Enable	Enables Test Mode to Disable the ADC; 1 = ADC Disable, 0 = ADC Enable (Default)
A4	Mass Write Enable	Allows Mass Write Addressing; 1 = Mass Write Enabled (Default), 0 = Mass Write Disabled
A3	FET On Control	On Control Bit Latches the State of the ON Pin at the End of the Debounce Delay; 1 = FET On, 0 = FET Off
A2	Overcurrent Auto-Retry	Overcurrent Auto-Retry Bit; 1 = Auto-Retry After Overcurrent, 0 = Latch Off After Overcurrent (Default)
A1	Undervoltage Auto-Retry	Undervoltage Auto-Retry; 1 = Auto-Retry After Undervoltage (Default), 0 = Latch Off After Undervoltage
A0	Overvoltage Auto-Retry	Overvoltage Auto-Retry; 1 = Auto-Retry After Overvoltage (Default), 0 = Latch Off After Overvoltage

Table 3. ALERT Register B (01h)—Read/Write

BIT	NAME	OPERATION
B7	Reserved	Not Used
B6	GPIO1 Output	Output Data Bit to GPIO1 Pin when Configured as Output. Defaults to 1
B5	FET Short Alert	Enables Alert for FET Short Condition; 1 = Enable Alert, 0 = Disable Alert (Default)
B4	$\overline{EN}$ State Change Alert	Enables Alert when $\overline{EN}$ Changes State; 1 = Enable Alert, 0 Disable Alert (Default)
B3	Power Bad Alert	Enables Alert when Output Power is Bad; 1 = Enable Alert, 0 Disable Alert (Default)
B2	Overcurrent Alert	Enables Alert for Overcurrent Condition; 1 = Enable Alert, 0 Disable Alert (Default)
B1	Undervoltage Alert	Enables Alert for Undervoltage Condition; 1 = Enable Alert, 0 Disable Alert (Default)
B0	Overvoltage Alert	Enables Alert for Overvoltage Condition; 1 = Enable Alert, 0 Disable Alert (Default)

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Table 4. STATUS Register C (02h)—Read

BIT	NAME	OPERATION
C7	FET On	1 = FET On, 0 = FET Off
C6	GPIO1 Input	Reports the State of the GPIO1 Pin; 1 = GPIO1 High, 0 = GPIO1 Low
C5	GPIO2 Input	Reports the State of the GPIO2 Pin; 1 = GPIO2 High, 0 = GPIO2 Low
C4	$\overline{EN}$	Indicates if the LTC4215 is Enabled when $\overline{EN}$ is Low; 1 = $\overline{EN}$ Pin Low, 0 = $\overline{EN}$ Pin High
C3	Power Bad	Indicates Power is Bad when FB is Low; 1 = FB Low, 0 = FB High
C2	GPIO3 Input	Reports the State of the GPIO3 Pin; 1 = GPIO3 High, 0 = GPIO3 Low
C1	Undervoltage	Indicates Input Undervoltage when UV is Low; 1 = UV Low, 0 = UV High
C0	Overvoltage	Indicates V_{DD} or OV Input Overvoltage when OV is High; 1 = OV High, 0 = OV Low

Table 5. FAULT Register D (03h)—Read/Write

BIT	NAME	OPERATION
D7	GPIO3 Output	Sets the State of the GPIO3 Pin; 1 = GPIO3 Pulled Low (Default), 0 = GPIO3 High Impedance
D6	GPIO2 Output	Sets the State of the GPIO2 Pin; 1 = GPIO2 Pulled Low, 0 = GPIO2 High Impedance (Default)
D5	FET Short Fault Occurred	Indicates Potential FET Short was Detected when Measured Current Sense Volage Exceeded 1mV While FET was Off; 1 = FET is Shorted, 0 = FET is Good
D4	$\overline{EN}$ Changed State	Indicates That the LTC4215 was Enabled or Disabled when $\overline{EN}$ Changed State; 1 = $\overline{EN}$ Changed State, 0 = $\overline{EN}$ Unchanged
D3	Power Bad Fault Occurred	Indicates Power was Bad when FB when Low; 1 = FB was Low, 0 = FB was High
D2	Overcurrent Fault Occurred	Indicates Overcurrent Fault Occured; 1 = Overcurrent Fault Occured, 0 = Not Overcurrent Faults
D1	Undervoltage Fault Occurred	Indicates Input Undervoltage Fault Occured when UV went Low; 1 = UV was Low, 0 = UV was High
D0	Overvoltage Fault Occurred	Indicates Input Overvoltage Fault Occured when OV went High; 1 = OV was High, 0 = OV was Low

Table 6. SENSE Register E (04h)—Read/Write

BIT	NAME	OPERATION
E7:0	SENSE Voltage Measurement	Sense Voltage Data, 8-Bit Data with 151µV LSB and 38.45mV Full Scale

Table 7. SOURCE Register F (05h)—Read/Write

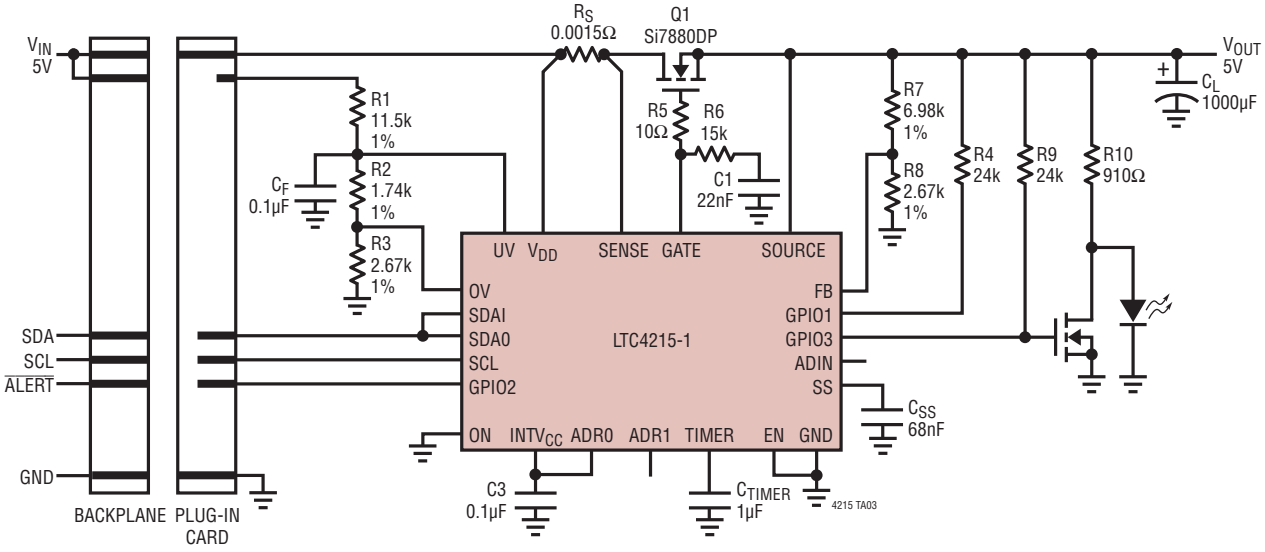
BIT	NAME	OPERATION
F7:0	SOURCE Voltage Measurement	SOURCE Voltage Data, 8-Bit Data with 60.5mV LSB and 15.44V Full Scale

Table 8. ADIN Register G (06h)—Read/Write

BIT	NAME	OPERATION
G7:0	ADIN Voltage Measurement	ADIN Voltage Data, 8-Bit Data with 4.82mV LSB and 1.23V Full Scale

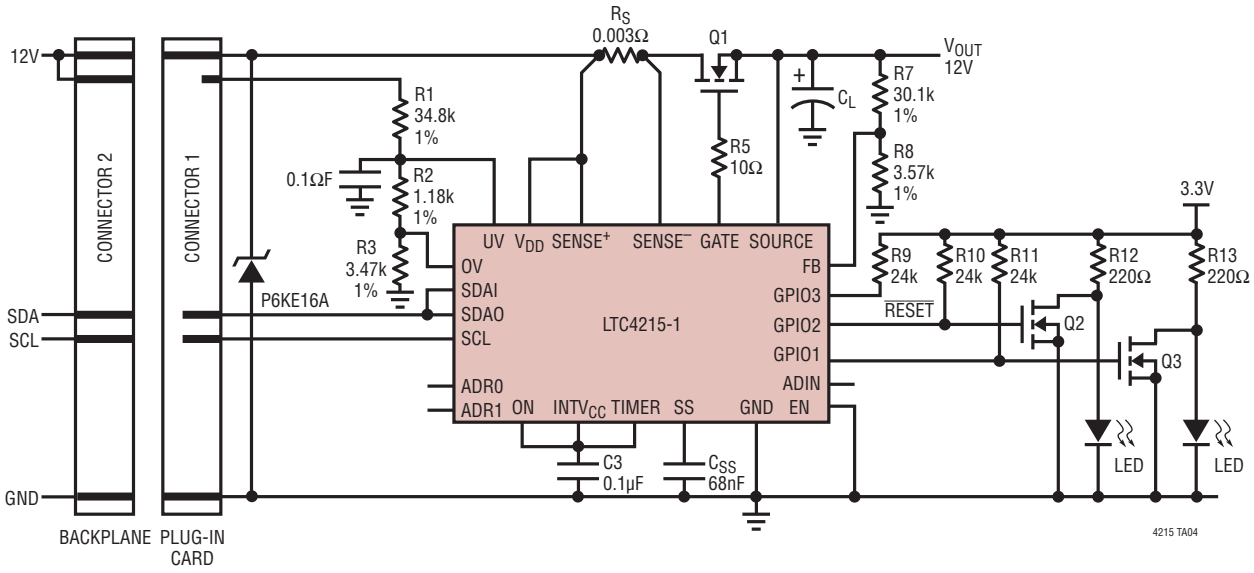
TYPICAL APPLICATIONS

5V Card Resident Application with Inverting LED Driver and 16.6A Circuit Breaker



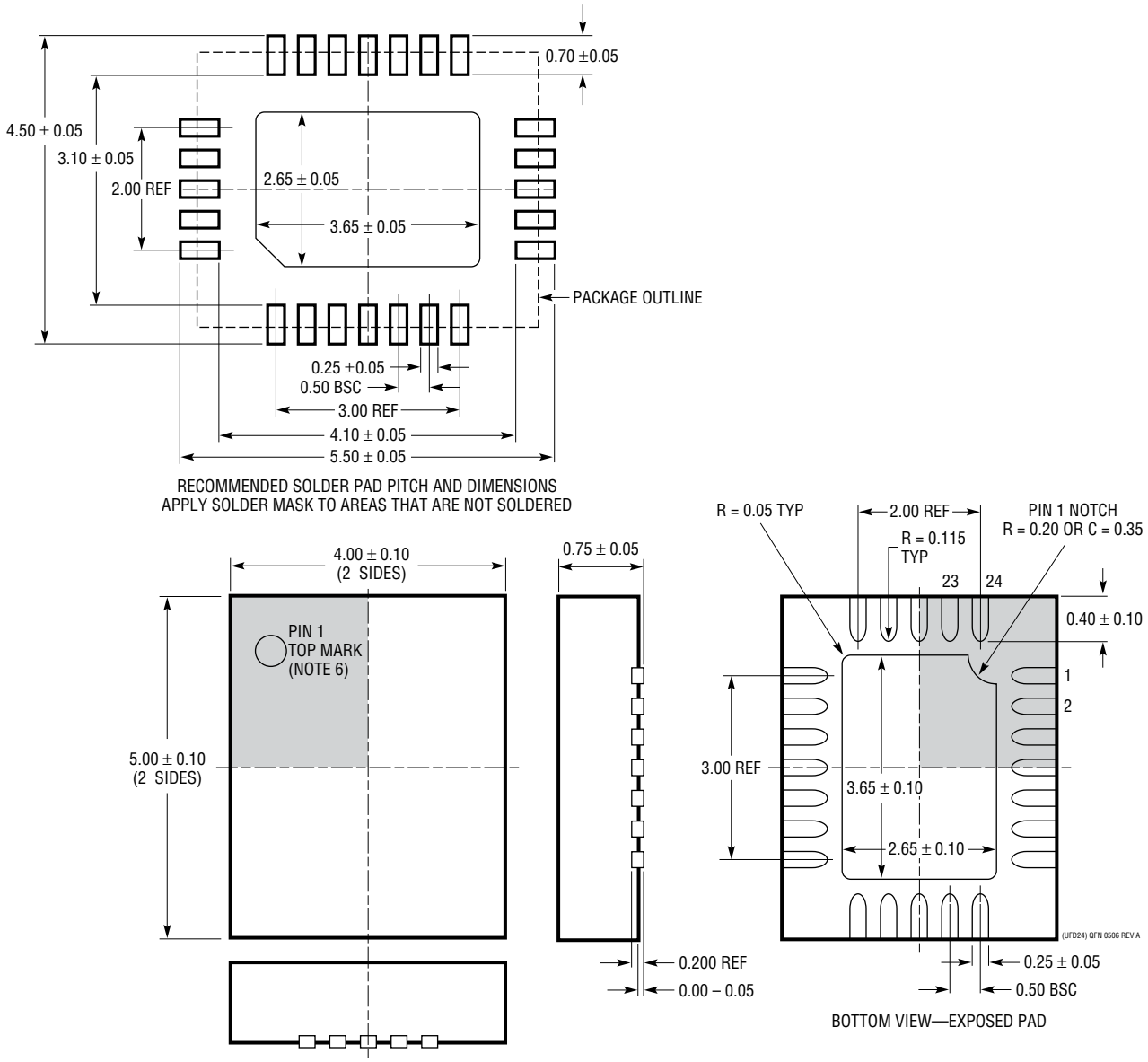
TYPICAL APPLICATIONS

12V Application with High Current Non-Inverting LED Drivers and 8.3A Circuit Breaker



PACKAGE DESCRIPTION

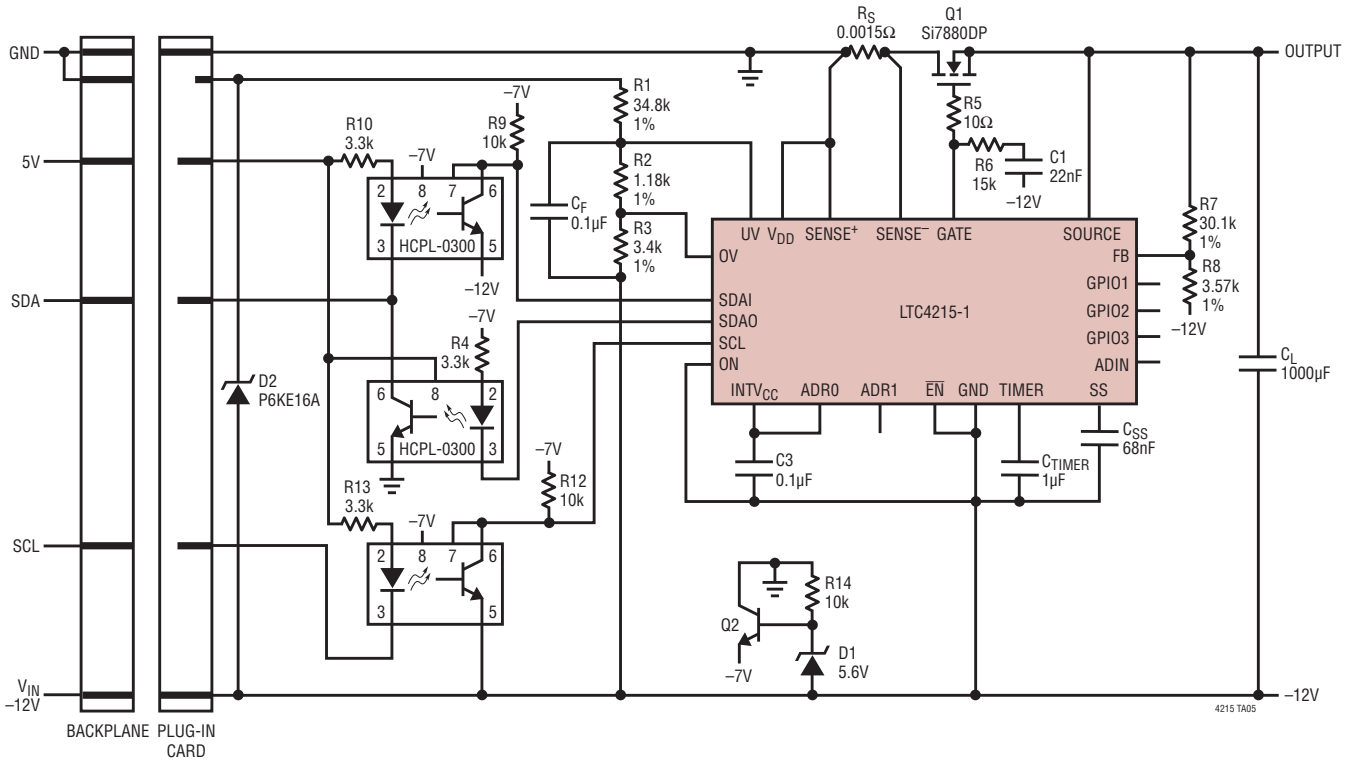
UFD Package
24-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1696 Rev A)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

–12V Card Resident Application with Optically Isolated I²C and 16.6A Current Limit



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1422	Single Channel, Hot Swap Controller	Operates from 2.7V to 12V, SO-8
LTC1642A	Single Channel, Hot Swap Controller	Operates from 3V to 16.5V, Overvoltage Protection up to 33V, SSOP-16
LTC1645	Dual Channel, Hot Swap Controller	Operates from 3V to 12V, Power Sequencing, SO-8 or SO-14
LTC1647	Dual Channel, Hot Swap Controller	Operates from 2.7V to 16.5V, SO-8 or SSOP-16
LTC4210	Single Channel, Hot Swap Controller	Operates from 2.7V to 16.5V, Active Current Limiting, SOT23-6
LTC4211	Single Channel, Hot Swap Controller	Operates from 2.5V to 16.5V, Multifunction Current Control, MSOP-8 or MSOP-10
LTC4212	Single Channel, Hot Swap Controller	Operates from 2.5V to 16.5V, Power-Up Timeout, MSOP-10
LTC4215	Single Channel, Hot Swap Controller with I²C, ADC	Operates from 2.9V to 15V, 27 Device Addresses, Fault Alert Output
LTC4216	Single Channel, Hot Swap Controller	Operates from 0V to 6V, MSOP-10 or 12-Lead (4mm × 3mm) DFN
LT4220	Positive and Negative Voltage, Dual Channel, Hot Swap Controller	Operates from ±2.7V to ±16.5V, SSOP-16
LTC4221	Dual Hot Swap Controller/Sequencer	Operates from 1V to 13.5V, Multifunction Current Control, SSOP-16
LTC4230	Triple Channel, Hot Swap Controller	Operates from 1.7V to 16.5V, Multifunction Current Control, SSOP-20
LTC4260	Single Channel, Hot Swap Controller with I²C, ADC	ADC for Board Power Monitoring, 8.5V to 80V
LTC4261	Negative Voltage, Hot Swap Controller with I²C, ADC	Operates from 9.5V to –100V or More (Shunt Regulated), 24-Lead (4mm × 5mm) QFN or SSOP-28

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