



THE DATASHEET OF LM48100QMHX/NOPB

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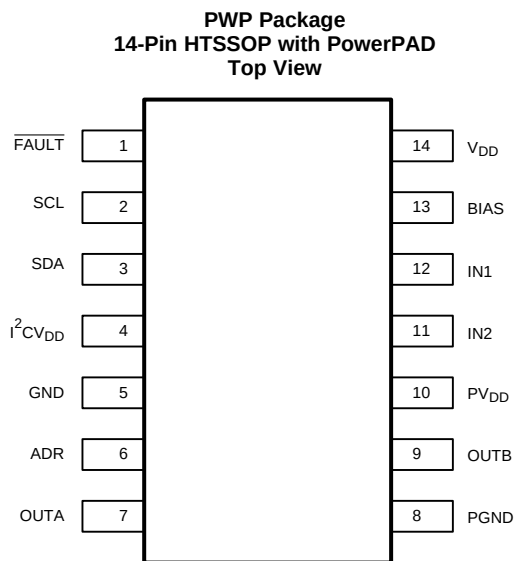
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
10/14/08	1.0	Initial release.
10/20/08	1.01	Text edits.
11/07/08	1.02	Added a column (Limits) in the Electrical tables.
11/12/08	1.03	Text edits.
03/21/2013	D	Changed layout of the National Data Sheet to TI format
11/2015	E	Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section
		Removed LM48100Q-Q1TL Demo board Bill of Materials table.

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	FAULT	O	Open-Drain output fault flag. FAULT = 0 indicates that a fault condition has occurred.
2	SCL	I	I²C Clock Input
3	SDA	I/O	I²C Serial Data Input
4	I²CVDD	—	I²C Interface Power Supply
5	GND	—	Ground
6	ADR	I	I²C Address Bit. Connect to I²CVDD to set address bit, B1 = 1. Connect to GND to set address bit B1 = 0
7	OUTA	O	Non-Inverting Audio Output
8	PGND	—	Power Ground
9	OUTB	O	Inverting Audio Output
10	PVDD	—	Output Amplifier Power Supply
11	IN2	I	Audio Input 2
12	IN1	I	Audio Input 1
13	BIAS	—	Bias Bypass
14	VDD	—	Power Supply
—	Exposed Pad	—	Exposed paddle. Connect to GND.

6 Specifications

6.1 Absolute Maximum Ratings

See ⁽¹⁾⁽²⁾⁽³⁾

	MIN	MAX	UNIT
Supply voltage, continuous		6	V
Input voltage	−0.3	$V_{DD} + 0.3$	°C
Power dissipation ⁽⁴⁾	Internally Limited		
Junction temperature		150	°C
Lead temperature (soldering 4 sec) ⁽⁵⁾		260	°C
Storage temperature	−65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The *Electrical Characteristics* tables found in *Specifications* list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics* Test Conditions, Notes, or both. Typical specifications are estimations only and are not ensured.
- If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- θ_{JA} measured with a 4 layer JEDEC board.
- For detailed information on soldering plastic HTSSOP and LLP packages go to the TI Packaging site, ti.com/packaging.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	2500	V
	Charged-device model (CDM), per AEC Q100-011	300	

- AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Temperature	$T_{MIN} \leq T_A \leq T_{MAX}$	−40	105	°C
Supply voltage	V_{DD} and PV_{DD}	3	5.5	V
I^2C Supply voltage	$I^2C V_{DD}$	1.8	5.5	V
		$I^2C V_{DD}$	V_{DD}	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM48100Q-Q1	UNIT
		PWP (HTSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	—	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

- For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for $V_{DD} = 5\text{ V}$

Programmable Gain = 0 dB, $R_L = 8\ \Omega$, $f = 1\text{ kHz}$, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN ⁽¹⁾	TYP ⁽²⁾	MAX	UNIT
I _{DD}	Quiescent Power Supply Current	V _{IN} = 0 V, Both channels active	R _L = 8 Ω		4.4	9	mA
			R _L = ∞		4.2	6	
I _{DD}	Diagnostic Mode Quiescent Power Supply Current	Diagnostic Mode Enabled, R _L = ∞			12.5	14.5	mA
I _{SD}	Shutdown Current	Shutdown Enabled			0.01	1	μA
V _{OS}	Differential Output Offset Voltage	V _{IN} = 0 V, R _L = 8 Ω			8.8	50	mV
T _{WU}	Wake-Up Time	Time from shutdown to audio available			11.6	50	ms
A _V	Gain	Minimum Gain Setting		−55	−54	−53	dB
		Maximum Gain Setting		17	18	19	
Mute	Mute Attenuation			−80	−77		dB
R _{IN}	Input Resistance	A _V = 18 dB		11.5	12.5	13.5	kΩ
		A _V = −54 dB		98	110	120	
P _O	Output Power	R _L = 8 Ω, f = 1 kHz	THD+N = 10%		1.6		W
			THD+N = 1%	1.05	1.3		
THD+N	Total Harmonic Distortion + Noise	P _O = 850 mW, f = 1 kHz, R _L = 8 Ω			0.04%		
PSRR	Power Supply Rejection Ratio	V _{RI} PPLE = 200 mV _{P-P} Sine, Inputs AC GND, C _{IN} = 1 μF, Input Referred, C _{BIAS} = 2.2 μF	f = 217 Hz	66	79		dB
			f = 1 kHz		74		
SNR	Signal-to-Noise-Ratio	P _{OUT} = 450 mW, f = 1 kHz			104		dB
ε _{OS}	Output Noise	A _V = 0 dB, A-weighted Filter			12		μV
I _{OUT(FAULT)}	FAULT Output Current	FAULT = 0, V _{OUT(FAULT)} = 0.4 V			3		mA
R _{FAULT}	Output to Supply Short Circuit Detection Threshold	Short between either OUTA to V _{DD} or GND, or OUTB to V _{DD} or GND	Short Circuit	3			kΩ
			Open Circuit		7.5		
R _{FAULT}	Output to Supply Short Circuit Detection Threshold	Short between both OUTA and OUTB to V _{DD} or GND	Short Circuit	6			kΩ
			Open Circuit		15		
R _{OPEN}	Open Circuit Detection Threshold	Open circuit between OUTA and OUTB		100		200	Ω
R _{SHT}	Output to Output Short Circuit Detection Threshold	Short circuit between OUTA and OUTB		2		6	Ω
I _{SHTCKT}	Short Circuit Current Limit				1.47	1.67	A
T _{SD}	Thermal Shutdown Threshold				170		°C
t _{DIAG}	Diagnostic Time				58		ms

(1) Datasheet min/max specification limits are specified by test or statistical analysis.

(2) Typical Values are given for $T_A = 25^\circ\text{C}$.

6.6 Electrical Characteristics for $V_{DD} = 5\text{ V}$ at Extended Temperature Limits

Programmable Gain = 0 dB, $R_L = 8\ \Omega$, $f = 1\text{ kHz}$, unless otherwise specified. Limits apply for $T_A = -40^\circ\text{C}$ to 105°C , unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN ⁽¹⁾	TYP ⁽²⁾	MAX	UNIT	
I _{DD}	Quiescent Power Supply Current	V _{IN} = 0 V, Both channels active	R _L = 8 Ω		4.4	10.8	mA	
			R _L = ∞		4.2	7.9		
I _{DD}	Diagnostic Mode Quiescent Power Supply Current	Diagnostic Mode Enabled, R _L = ∞				12.5	mA	
I _{SD}	Shutdown Current	Shutdown Enabled				0.01	μA	
V _{OS}	Differential Output Offset Voltage	V _{IN} = 0 V, R _L = 8 Ω				8.8	75	mV
T _{WU}	Wake-Up Time	Time from shutdown to audio available				11.6		ms
A _V	Gain	Minimum Gain Setting			−56	−54	−52	dB
		Maximum Gain Setting			17	18	19	
Mute	Mute Attenuation					−80	−74	dB

(1) Datasheet min/max specification limits are specified by test or statistical analysis.

(2) Typical Values are given for $T_A = 25^\circ\text{C}$.

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Electrical Characteristics for $V_{DD} = 5\text{ V}$ at Extended Temperature Limits (continued)

Programmable Gain = 0 dB, $R_L = 8\ \Omega$, $f = 1\text{ kHz}$, unless otherwise specified. Limits apply for $T_A = -40^\circ\text{C}$ to 105°C , unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX	UNIT
R_{IN} Input Resistance	$A_V = 18\text{ dB}$		12.5		k Ω
	$A_V = -54\text{ dB}$	89	110	130	
P_O Output Power	$R_L = 8\ \Omega$, $f = 1\text{ kHz}$	THD+N = 10%	1.6		W
		THD+N = 1%	0.96	1.3	
THD+N Total Harmonic Distortion + Noise	$P_O = 850\text{ mW}$, $f = 1\text{ kHz}$, $R_L = 8\ \Omega$		0.04%		
PSRR Power Supply Rejection Ratio	$V_{RIPPLE} = 200\text{ mV}_{P-P}$ Sine, Inputs AC GND, $C_{IN} = 1\ \mu\text{F}$, Input Referred, $C_{BIAS} = 2.2\ \mu\text{F}$	$f = 217\text{ Hz}$	63	79	dB
		$f = 1\text{ kHz}$	74		
SNR Signal-to-Noise-Ratio	$P_{OUT} = 450\text{ mW}$, $f = 1\text{ kHz}$		104		dB
ϵ_{OS} Output Noise	$A_V = 0\text{ dB}$, A-weighted Filter		12		μV
$I_{OUT(FAULT)}$ FAULT Output Current	FAULT = 0, $V_{OUT(FAULT)} = 0.4\text{ V}$		3		mA
R_{FAULT} Output to Supply Short Circuit Detection Threshold	Short between either OUTA to V_{DD} or GND, or OUTB to V_{DD} or GND	Short Circuit	3		k Ω
		Open Circuit		7.5	
I_{SHTCKT} Short Circuit Current Limit			1.47	2	A
T_{SD} Thermal Shutdown Threshold			170		$^\circ\text{C}$
t_{DIAG} Diagnostic Time			58		ms

6.7 Electrical Characteristics for $V_{DD} = 3.6\text{ V}$

Programmable Gain = 0 dB, $R_L = 8\ \Omega$, $f = 1\text{ kHz}$, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX	UNIT
I_{DD} Quiescent Power Supply Current	$V_{IN} = 0\text{ V}$, Both channels active	$R_L = 8\ \Omega$	3.8	8.5	mA
		$R_L = \infty$	3.6	5	
I_{DD} Diagnostic Mode Quiescent Power Supply Current	Diagnostic Mode Enabled, $R_L = \infty$		11.7	14.5	mA
I_{SD} Shutdown Current	Shutdown Enabled		0.01	1	μA
V_{OS} Differential Output Offset Voltage	$V_{IN} = 0\text{ V}$, $R_L = 8\ \Omega$		8.8	50	mV
T_{WU} Wake-Up Time	Time from shutdown to audio available		11.5	50	ms
A_V Gain	Minimum Gain Setting	-55	-54	-53	dB
	Maximum Gain Setting	17	18	19	
Mute Mute Attenuation			-79	-77	dB
R_{IN} Input Resistance	$A_V = 18\text{ dB}$	11.5	12.5	13.5	k Ω
	$A_V = -54\text{ dB}$	98	110	120	
P_O Output Power	$R_L = 8\ \Omega$, $f = 1\text{ kHz}$	THD+N = 10%	820		mW
		THD+N = 1%	480	660	
THD+N Total Harmonic Distortion + Noise	$P_O = 400\text{ mW}$, $f = 1\text{ kHz}$, $R_L = 8\ \Omega$		0.04%		
PSRR Power Supply Rejection Ratio	$V_{RIPPLE} = 200\text{ mV}_{P-P}$ Sine, Inputs AC GND, $C_{IN} = 1\ \mu\text{F}$, Input Referred, $C_{BIAS} = 2.2\ \mu\text{F}$	$f = 217\text{ Hz}$	66	78	dB
		$f = 1\text{ kHz}$	75		
SNR Signal-to-Noise-Ratio	$P_{OUT} = 780\text{ mW}$, $f = 1\text{ kHz}$		106		dB
ϵ_{OS} Output Noise	$A_V = 0\text{ dB}$, A-weighted Filter		12.5		μV
$I_{OUT(FAULT)}$ FAULT Output Current	FAULT = 0, $V_{OUT(FAULT)} = 0.4\text{ V}$		3		mA
R_{FAULT} Output to Supply Short Circuit Detection Threshold	Short between either OUTA to V_{DD} or GND, or OUTB to V_{DD} or GND	Short Circuit	3		k Ω
		Open Circuit		7.5	
R_{FAULT} Output to Supply Short Circuit Detection Threshold	Short between both OUTA and OUTB to V_{DD} or GND	Short Circuit	6		k Ω
		Open Circuit		15	
R_{OPEN} Open Circuit Detection Threshold	Open circuit between OUTA and OUTB	100		200	Ω
R_{SHT} Output to Output Short Circuit Detection Threshold	Short circuit between OUTA and OUTB	2		6	Ω
I_{SHTCKT} Short Circuit Current Limit			1.43		A

(1) Datasheet min/max specification limits are specified by test or statistical analysis.

(2) Typical Values are given for $T_A = 25^\circ\text{C}$.

Electrical Characteristics for $V_{DD} = 3.6\text{ V}$ (continued)

Programmable Gain = 0 dB, $R_L = 8\ \Omega$, $f = 1\text{ kHz}$, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX	UNIT
T_{SD}	Thermal Shutdown Threshold		170		$^\circ\text{C}$
t_{DIAG}	Diagnostic Time		63		ms

6.8 Electrical Characteristics for $V_{DD} = 3.6\text{ V}$ at Extended Temperature Limits

Programmable Gain = 0 dB, $R_L = 8\ \Omega$, $f = 1\text{ kHz}$, unless otherwise specified. Limits apply for $T_A = -40^\circ\text{C}$ to 105°C , unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN ⁽¹⁾	TYP ⁽²⁾	MAX	UNIT
I _{DD}	Quiescent Power Supply Current	V _{IN} = 0 V, Both channels active	R _L = 8 Ω		3.8	10.8	mA
			R _L = ∞		3.6	7	
I _{DD}	Diagnostic Mode Quiescent Power Supply Current	Diagnostic Mode Enabled, R _L = ∞			11.7		mA
I _{SD}	Shutdown Current	Shutdown Enabled			0.01		μA
V _{OS}	Differential Output Offset Voltage	V _{IN} = 0 V, R _L = 8 Ω			8.8	76	mV
T _{WU}	Wake-Up Time	Time from shutdown to audio available			11.5		ms
A _V	Gain	Minimum Gain Setting			−54		dB
		Maximum Gain Setting			18		
Mute	Mute Attenuation				−79		dB
R _{IN}	Input Resistance	A _V = 18 dB			12.5		kΩ
		A _V = −54 dB		89	110	135	
P _O	Output Power	R _L = 8 Ω, f = 1 kHz	THD+N = 10%		820		mW
			THD+N = 1%		660		
THD+N	Total Harmonic Distortion + Noise	P _O = 400 mW, f = 1 kHz, R _L = 8 Ω			0.04%		
PSRR	Power Supply Rejection Ratio	V _{RIPPLE} = 200 mV _{P-P} Sine, Inputs AC GND, C _{IN} = 1 μF, Input Referred, C _{BIAS} = 2.2 μF	f = 217 Hz	60	78		dB
			f = 1 kHz		75		
SNR	Signal-to-Noise-Ratio	P _{OUT} = 780 mW, f = 1 kHz			106		dB
ε _{OS}	Output Noise	A _V = 0 dB, A-weighted Filter			12.5		μV
I _{OUT(FAULT)}	$\overline{\text{FAULT}}$ Output Current	$\overline{\text{FAULT}}$ = 0, V _{OUT(FAULT)} = 0.4 V			3		mA
I _{SHTCKT}	Short Circuit Current Limit				1.43		A
T _{SD}	Thermal Shutdown Threshold				170		°C
t _{DIAG}	Diagnostic Time				63		ms

(1) Datasheet min/max specification limits are specified by test or statistical analysis.

(2) Typical Values are given for $T_A = 25^\circ\text{C}$.

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6.9 I²C Interface Characteristics for $V_{DD} = 5\text{ V}$, $2.2\text{ V} \leq I^2C\ V_{DD} \leq 5.5\text{ V}$
 $A_V = 0\text{ dB}$, $R_L = 8\ \Omega$, $f = 1\text{ kHz}$, unless otherwise specified. Limits apply for $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	MAX	UNIT
t_1 SCL Period		2.5		μs
t_2 SDA Setup Time		100		ns
t_3 SDA Stable Time		0		ns
t_4 Start Condition Time		100		ns
t_5 Stop Condition Time		100		ns
t_6 SDA Data Hold Time		100		ns
V_{IH} Logic High Input Threshold		$0.7 \times I^2C V_{DD}$		V
V_{IL} Logic Low Input Threshold			$0.3 \times I^2C V_{DD}$	V

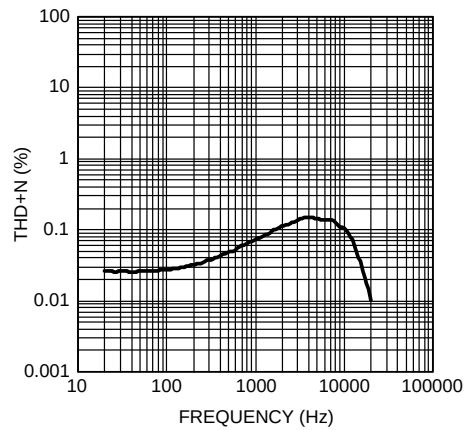
(1) Datasheet min/max specification limits are specified by test or statistical analysis.

6.10 I²C Interface Characteristics for $V_{DD} = 5\text{ V}$, $1.8\text{ V} \leq I^2C\ V_{DD} \leq 2.2\text{ V}$
 $A_V = 0\text{ dB}$, $R_L = 8\ \Omega$, $f = 1\text{ kHz}$, unless otherwise specified. Limits apply for $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	MAX	UNIT
t_1 SCL Period		2.5		μs
t_2 SDA Setup Time		250		ns
t_3 SDA Stable Time		0		ns
t_4 Start Condition Time		250		ns
t_5 Stop Condition Time		250		ns
t_6 SDA Data Hold Time		250		ns
V_{IH} Logic High Input Threshold		$0.7 \times I^2C V_{DD}$		V
V_{IL} Logic Low Input Threshold			$0.3 \times I^2C V_{DD}$	V

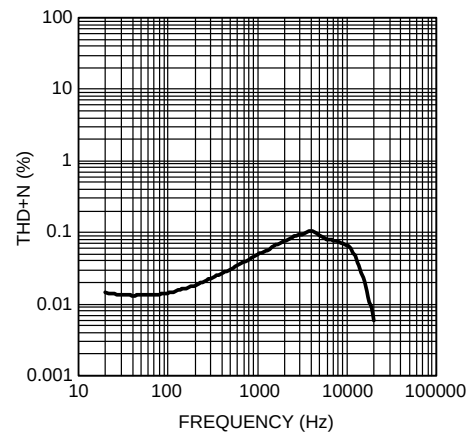
(1) Datasheet min/max specification limits are specified by test or statistical analysis.

6.11 Typical Characteristics



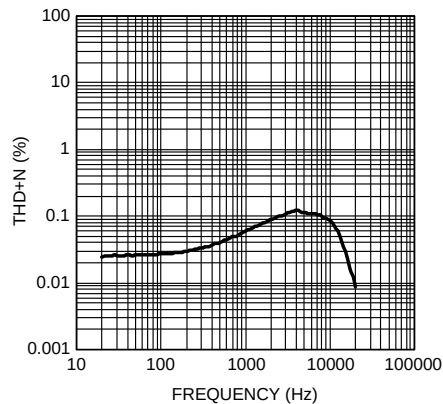
$V_{DD} = 3.6\text{ V}$ $P_{OUT} = 600\text{ mW}$ $R_L = 4\ \Omega$

Figure 1. THD+N vs Frequency



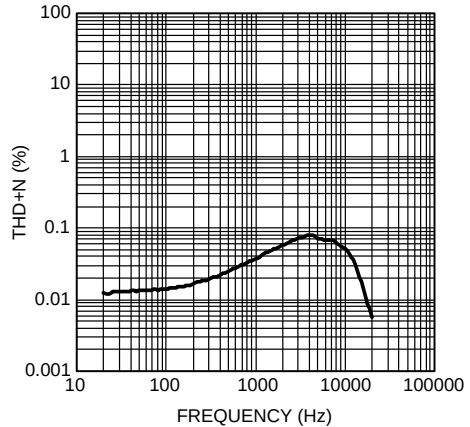
$V_{DD} = 3.6\text{ V}$ $P_{OUT} = 400\text{ mW}$ $R_L = 8\ \Omega$

Figure 2. THD+N vs Frequency



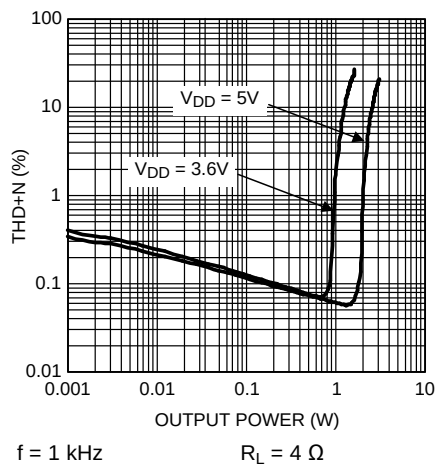
$V_{DD} = 5\text{ V}$ $P_{OUT} = 1.2\text{ W}$ $R_L = 4\ \Omega$

Figure 3. THD+N vs Frequency



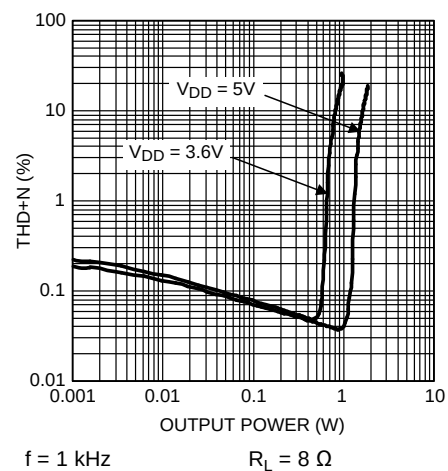
$V_{DD} = 5\text{ V}$ $P_{OUT} = 850\text{ mW}$ $R_L = 8\ \Omega$

Figure 4. THD+N vs Frequency



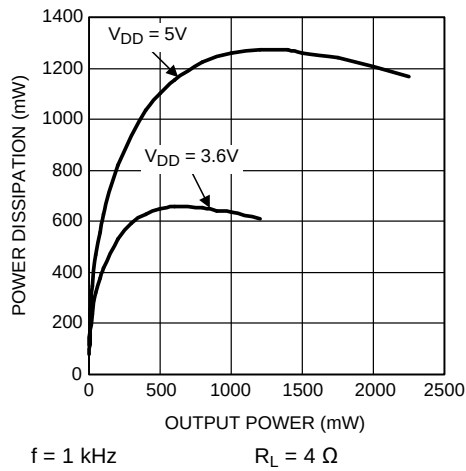
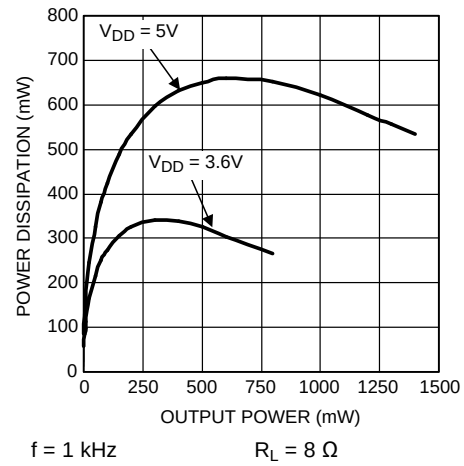
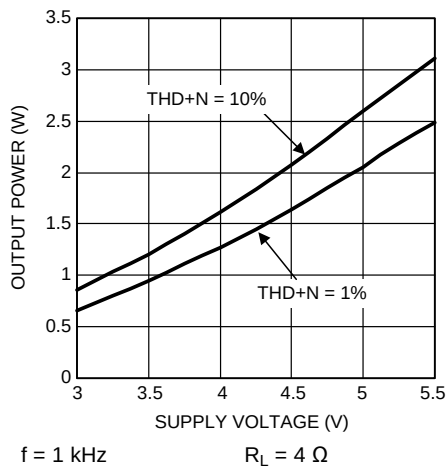
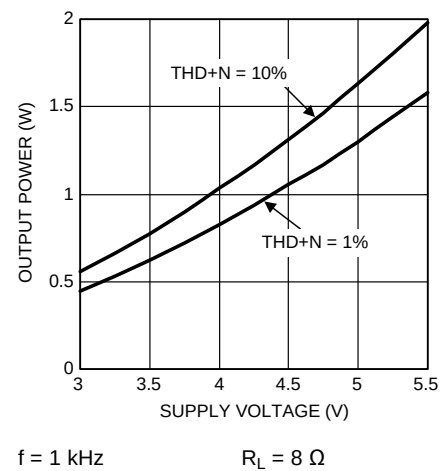
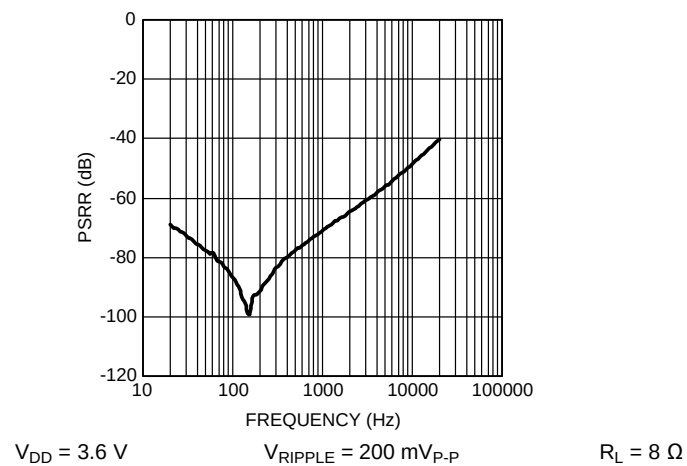
$f = 1\text{ kHz}$ $R_L = 4\ \Omega$

Figure 5. THD+N vs Output Power



$f = 1\text{ kHz}$ $R_L = 8\ \Omega$

Figure 6. THD+N vs Output Power

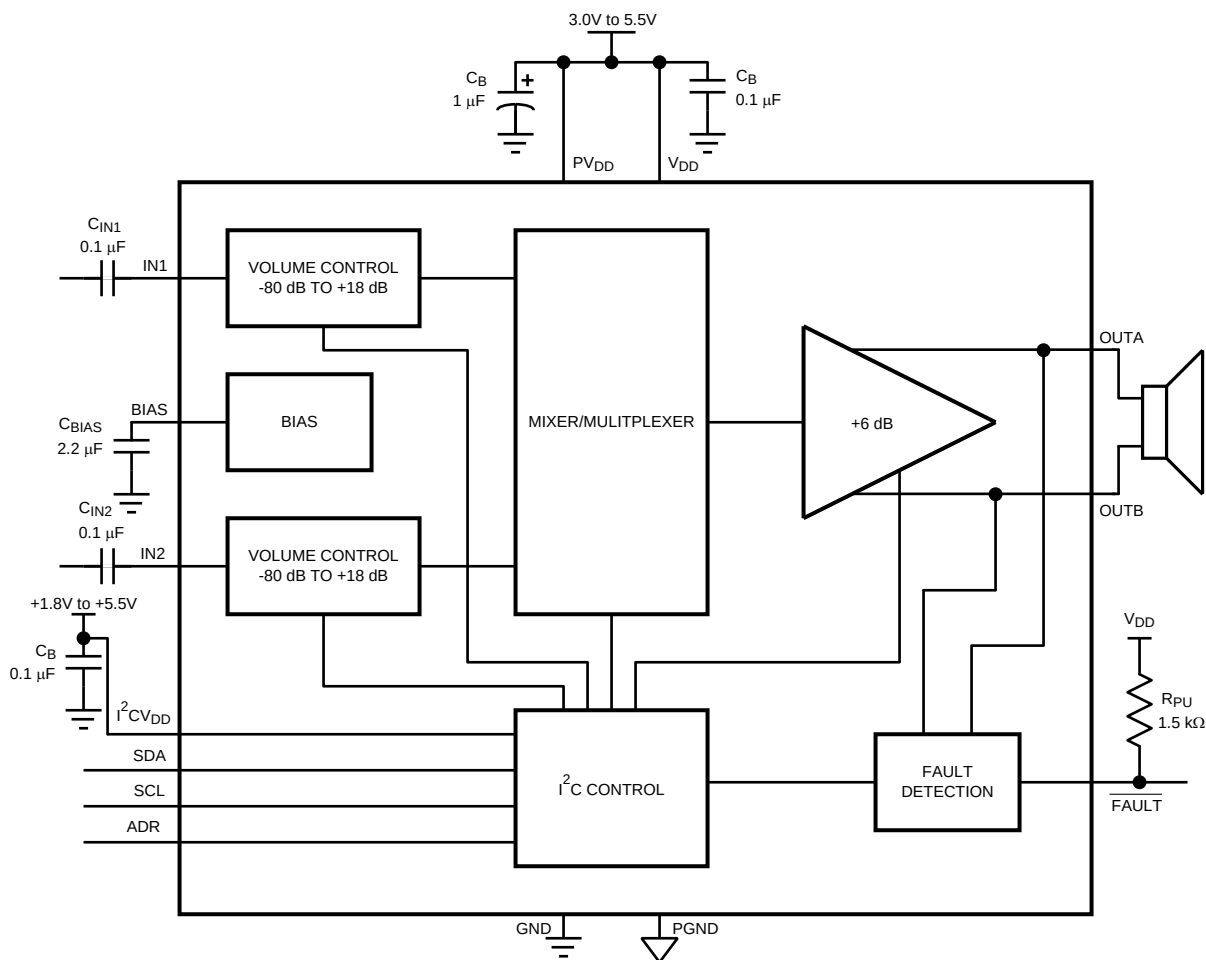
Typical Characteristics (continued)

Figure 7. Power Dissipation vs Output Power

Figure 8. Power Dissipation vs Output Power

Figure 9. Output Power vs Supply Voltage

Figure 10. Output Power vs Supply Voltage

Figure 11. PSRR vs Frequency

7 Detailed Description

7.1 Overview

The LM48100Q-Q1 integrates a comprehensive output fault detection system, which can sense the load conditions, protecting the device during short circuit events and detecting open circuit conditions. High power supply rejection ratio allows the device to operate in noisy environments without additional power supply conditioning. Dual audio inputs can be mixed or multiplexed to the device output. Each input path has its own independent, 32-step volume control. The mixer, volume control and device mode select are controlled through an I²C compatible interface. An open drain FAULT output indicates when a fault has occurred. Comprehensive output short circuit and thermal overload protection prevent the device from damage during fault conditions. Superior click and pop suppression eliminates audible transients on power-up, power-down, and during shutdown.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Diagnostic Control

The LM48100Q-Q1 output fault diagnostics are controlled through the I²C interface. When power is initially applied to the device, the LM48100Q-Q1 initializes, performing the full diagnostic sequence; output short to V_{DD} and GND, outputs shorted together, and no load condition, is performed. The device remains in shutdown while the initial diagnostic check is performed. Any I²C commands written to the device during this time are stored and implemented once the diagnostic check is complete. The initial diagnostic sequence can be terminated by setting DG_RESET = 1.

The Diagnostic Control register, register 1, controls the LM48100Q-Q1 diagnostic process. Bit B4, DG_EN, enables the output fault detection. Set DG_EN = 1 to enable the output diagnostic test sequence. The LM48100Q-Q1 treats the DG_EN bit as rising-edge-sensitive; once DG_EN = 1 is clocked into the device, the diagnostic test is performed. If the LM48100Q-Q1 is in one-shot mode, once the test sequence is performed, the DG_EN bit is ignored and the test sequence will not be run again. Cycle DG_EN from high-to-low-to-high to re-enable the one-shot diagnostic test sequence.

In continuous diagnostic mode, the test sequence is repeated until either a fault condition occurs, DG_RESET is cycled, or the device is taken out of continuous diagnostic mode. Set DG_CONT = 1 before setting DG_EN = 1 to initiate a continuous diagnostic. Set DG-CONT = 0 to disable continuous diagnostic mode. When the device is active and DG_EN = 0, the LM48100Q-Q1 does not perform the output short, or no load diagnostics, however, the thermal overload and output over current protection circuitry remains active, and disables the device should a thermal or over-current fault occur. The initial diagnostic operation when power is applied to the device occurs regardless of the state of DG_EN. The LM48100Q-Q1 output fault detection can be set to either continuous mode where the output diagnostic occurs every 60ms, or a one-shot mode. Set bit B3 (DG_CONT) to 1 for continuous mode, set B3 = 0 for one-shot mode.

Bit B2, DG_RESET, restores the LM48100Q-Q1 to normal operation after an output fault is detected. Toggle DG_RESET to re-enable the device outputs and set FAULT high.

Table 1. Diagnostic Control Register

BIT	NAME	VALUE	DESCRIPTION
B0	RESERVED	0	Unused
B1	ILIMIT	0	Fixed output current limit
		1	Supply dependent output current limit
B2	DG_RESET	0	Normal operation. FAULT remains low and device is disabled once a fault occurs.
		1	Reset FAULT output. Device returns to pre-fault operation.
B3	DG_CONT	0	One shot diagnostic
		1	Continuous diagnostic
B4	DG_EN	0	Disable diagnostic
		1	Enable diagnostic

7.3.2 Fault Detection Control Register

The LM48100Q-Q1 output fault tests are individually controlled through the Fault Detection Control register, register 2. Setting any of the bits in the Fault Detection Control register to 1 causes the FAULT circuitry to ignore the associated test. For example, if B2 (RAIL_SHT) = 1 and the output is shorted to V_{DD}, the FAULT output remains high. Although the FAULT circuitry ignores the selected test, the LM48100Q-Q1 protection circuitry remains active, and disables the device. This feature is useful for diagnosing which fault caused a FAULT condition.

If DG_EN = 1, and a diagnostic sequence is initiated, all the tests are performed regardless of their state in the Fault Detection Control register. If DG_EN = 0, the RAIL_SHT, OUTPUT_OPEN and OUTPUT_SHT tests are not performed, however, the thermal overload and output over-current detection circuitry remains active.

Table 2. Fault Detection Control Register

BIT	NAME	VALUE	DESCRIPTION
B0	OUTPUT_SHT	0	Normal operation
		1	Ignore output short circuit fault (outputs shorted together)
B1	OUTPUT_OPEN	0	Normal operation
		1	Ignore output short circuit fault
B2	RAIL_SHT	0	Normal operation
		1	Ignore output short to V_{DD} or GND fault
B3	OVF	0	Normal operation
		1	Ignore output over-current fault
B4	TSD	0	Normal operation
		1	Ignore thermal overload fault

7.3.3 General Amplifier Function

7.3.3.1 Bridge Configuration Explained

The LM48100Q-Q1 is designed to drive a load differentially, a configuration commonly referred to as a bridge-tied load (BTL). The BTL configuration differs from the single-ended configuration, where one side of the load is connected to ground. A BTL amplifier offers advantages over a single-ended device. By driving the load differentially, the output voltage is doubled, compared to a single-ended amplifier under similar conditions. This doubling of the output voltage leads to a quadrupling of the output power. For example, the theoretical maximum output power for a single-ended amplifier driving 8 Ω and operating from a 5 V supply is 158 mW, while the theoretical maximum output power for a BTL amplifier operating under the same conditions is 633 mW. Since the amplifier outputs are both biased about $V_{DD}/2$, there is no net DC voltage across the load, eliminating the DC blocking capacitors required by single-ended, single-supply amplifiers.

7.3.3.2 Input Mixer/Multiplexer

The LM48100Q-Q1 features an input mixer/multiplexer controlled through the I²C interface. The mixer/multiplexer allows either input, or the combination of both inputs to appear at the device output. Bits B2 (INPUT_1) and B3 (INPUT_2) of the Mode Control Register select the individual input channels. Set INPUT_1 = 1 to select the audio signal on IN1. Set INPUT_2 = 1 to select the audio signal on IN2. Setting both INPUT_1 and INPUT_2 = 1 mixes V_{IN1} and V_{IN2} , and the LM48100Q-Q1 outputs the result as a mono signal (Table 3).

Table 3. Input Multiplexer Control

INPUT_1	INPUT_2	LM48100Q-Q1 OUTPUT
0	0	MUTE. No input selected
1	0	IN1 ONLY
0	1	IN2 ONLY
1	1	IN1 + IN2

7.3.4 Output Fault Detection

7.3.4.1 Output Short to Supplies (V_{DD} or GND)

With a standard speaker load (6 Ω to 100 Ω) connected between OUTA and OUTB, the LM48100Q-Q1 can detect a short between the outputs and either V_{DD} or GND. A short is detected if the impedance between either OUTA or OUTB and V_{DD} or GND is less than 3 k Ω . A short is also detected if the impedance between BOTH OUTA and OUTB and either V_{DD} or GND is less than 6 k Ω . Under either of these conditions, the amplifier outputs are disabled and FAULT is driven low. No short is detected if the impedance between either output and V_{DD} or GND is greater than 7.5 k Ω . Likewise, no short is detected if the impedance between BOTH outputs and V_{DD} or GND is greater than 15 k Ω .

7.3.4.2 Output Short Circuit and Open Circuit Detection

The LM48100Q-Q1 can detect whether the amplifier outputs have been shorted together or, an output open circuit condition has occurred. An output short circuit is detected if the impedance between OUTA and OUTB is less than 2 Ω. An open circuit is detected if the impedance between OUTA and OUTB is greater than 200 Ω. Under either of these conditions, the amplifier outputs are disabled and $\overline{\text{FAULT}}$ is driven low. The device remains in normal operation if the impedance between OUTA and OUTB is in the range of 6 Ω to 100 Ω. The output open circuit test is only performed during the initial diagnostic sequence during power up, or when DG_ENABLE is set to 1.

7.3.4.3 Output Over-Current Detection

The LM48100Q-Q1 has two over current detection modes, a fixed current limit, and a supply dependent current limit. Bit B1 (ILIMIT) of the Diagnostic Control Register selects the over-current detection mode. Set ILIMIT = 0 to select a fixed current limit of 1.47 A (typ). Set ILIMIT = 1 to select the supply dependent current limit mode. In supply dependent mode, the current limit is determined by Equation 1:

$$I_{\text{SH TCKT}} = 0.264 \times V_{\text{DD}} \text{ (A)} \quad (1)$$

If the output current exceeds the current limit, the device outputs are disabled and $\overline{\text{FAULT}}$ is driven low. The output over-current detection circuitry remains active when the diagnostics have been disabled (DG_EN = 0).

7.3.4.4 Thermal Overload Detection

The LM48100Q-Q1 has thermal overload threshold of 170 °C (typ). If the die temperature exceeds 170 °C, the outputs are disabled and $\overline{\text{FAULT}}$ is driven low. The thermal overload detection circuitry remains active when the diagnostics have been disabled (DG_EN = 0).

7.3.5 Open $\overline{\text{FAULT}}$ Output

The LM48100Q-Q1 features an open drain, fault indication output, $\overline{\text{FAULT}}$, that asserts when a fault condition is detected by the device. $\overline{\text{FAULT}}$ goes low when either an output short, output open, over current, or thermal overload fault is detected, and the diagnostic test is not ignored, see [Fault Detection Control Register](#) section. $\overline{\text{FAULT}}$ remains low even after the fault condition has been cleared and the diagnostic tests are repeated. Toggle DG_RESET to clear $\overline{\text{FAULT}}$.

Connect a 1.5-kΩ or higher pullup resistor between $\overline{\text{FAULT}}$ and V_{DD} .

7.3.6 Volume Control

Table 4. Volume Control

VOLUME STEP	VOL4	VOL3	VOL2	VOL1	VOL0	GAIN (dB)
1	0	0	0	0	0	–80
2	0	0	0	0	1	–54
3	0	0	0	1	0	–40.5
4	0	0	0	1	1	–34.5
5	0	0	1	0	0	–30
6	0	0	1	0	1	–27
7	0	0	1	1	0	–24
8	0	0	1	1	1	–21
9	0	1	0	0	0	–18
10	0	1	0	0	1	–15
11	0	1	0	1	0	–13.5
12	0	1	0	1	1	–12
13	0	1	1	0	0	–10.5
14	0	1	1	0	1	–9
15	0	1	1	1	0	–7.5
16	0	1	1	1	1	–6
17	1	0	0	0	0	–4.5

Table 4. Volume Control (continued)

VOLUME STEP	VOL4	VOL3	VOL2	VOL1	VOL0	GAIN (dB)
18	1	0	0	0	1	–3
19	1	0	0	1	0	–1.5
20	1	0	0	1	1	0
21	1	0	1	0	0	1.5
22	1	0	1	0	1	3
23	1	0	1	1	0	4.5
24	1	0	1	1	1	6
25	1	1	0	0	0	7.5
26	1	1	0	0	1	9
27	1	1	0	1	0	10.5
28	1	1	0	1	1	12
29	1	1	1	0	0	13.5
30	1	1	1	0	1	15
31	1	1	1	1	0	16.5
32	1	1	1	1	1	18

7.3.7 Shutdown Function

The LM48100Q-Q1 features an I²C selectable low power shutdown mode that disables the device, reducing quiescent current consumption to 0.01 μ A. Set bit B4 (POWER_ON) in the Mode Control Register to 0 to disable the device. Set B0 to 1 to enable the device.

7.3.8 Power Dissipation

The increase in power delivered by a BTL amplifier leads to a direct increase in internal power dissipation. The maximum power dissipation for a BTL amplifier for a given supply voltage and load is given by [Equation 2](#):

$$P_{DMAX} = 4 \times V_{DD}^2 / 2\pi^2 R_L \text{ (Watts)} \quad (2)$$

The maximum power dissipation of the HTSSOP package is calculated by [Equation 3](#):

$$P_{DMAX} \text{ (PKG)} = T_{JMAX} - T_A / \theta_{JA} \text{ (Watts)}$$

where

- T_{JMAX} is 150 °C
- T_A is the ambient temperature
- θ_{JA} is the thermal resistance specified in the [Absolute Maximum Ratings](#) (3)

If the power dissipation for a given operating condition exceeds the package maximum, either decrease the ambient temperature, increase air flow, add heat sinking to the device, or increase the load impedance and/or supply voltage. The LM48100Q-Q1 HTSSOP package features an exposed die attach pad (DAP) that can be used to increase the maximum power dissipation of the package, see [Exposed DAP Mounting Considerations](#).

The LM48100Q-Q1 features thermal overload protection that disables the amplifier output stage when the die temperature exceeds 170 °C. See the [Thermal Overload Detection](#) section.

7.4 Device Functional Modes

The LM48100Q-Q1 output fault diagnostics support two different modes: one-shot mode and continuous diagnostic mode.

7.4.1 One-Shot Mode

If the LM48100Q-Q1 is in one-shot mode, once the test sequence is performed, the DG_EN bit is ignored and the test sequence will not be run again.

Device Functional Modes (continued)

7.4.2 Continuous Diagnostic Mode

In continuous diagnostic mode, the test sequence is repeated until either a fault condition occurs, DG_RESET is cycled, or the device is taken out of continuous diagnostic mode.

7.5 Programming

7.5.1 Write-Only I²C Compatible Interface

The LM48100Q-Q1 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM48100Q-Q1 and the master can communicate at clock rates up to 400 kHz. Figure 12 shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48100Q-Q1 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 13). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse (Figure 14). The LM48100Q-Q1 device address is 111110X, where X is determined by ADR (Table 6). ADR = 1 sets the device address to 1111101. ADR = 0 sets the device address to 1111100.

7.5.2 I²C Bus Format

The I²C bus format is shown in Figure 14. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/W bit. $\overline{R/W} = 0$ indicates the master is writing to the slave device, $\overline{R/W} = 1$ indicates the master wants to read data from the slave device. Set $\overline{R/W} = 0$; the LM48100Q-Q1 is a WRITE-ONLY device and will not respond the $\overline{R/W} = 1$. The data is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48100Q-Q1 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, the LM48100Q-Q1 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high.

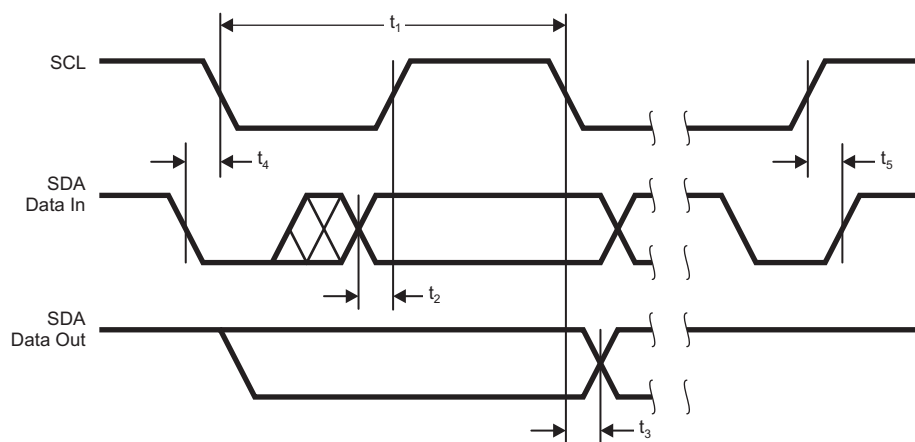


Figure 12. I²C Timing Diagram

Programming (continued)

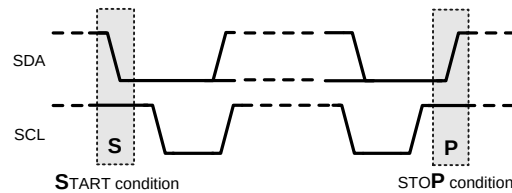


Figure 13. Start and Stop Diagram

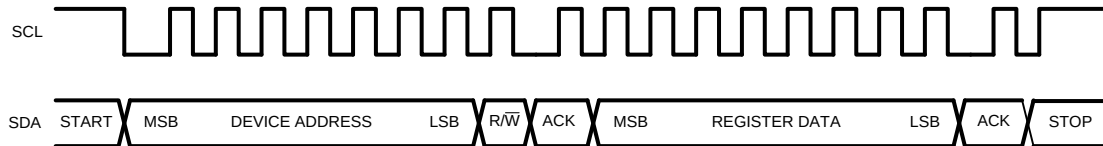


Figure 14. Example Write Sequence

Table 5. Device Address

	B7	B6	B5	B4	B3	B2	B1	B0 R/ $\overline{W}$
ADR = 0	1	1	1	1	1	0	0	0
ADR = 1	1	1	1	1	1	0	1	0

7.6 Register Maps

Table 6. I²C Control Registers

Register Address	Register Name	B7	B6	B5	B4	B3	B2	B1	B0
0	MODE CONTROL	0	0	0	POWER_ON	INPUT_2	INPUT_1	0	0
1	DIAGNOSTIC CONTROL	0	0	1	DG_EN	DG_CONT	DG_RESET	ILIMIT	0
2	FAULT DETECTION CONTROL	0	1	0	TSD	OCF	RAIL_SHT	OUTPUT_OPEN	OUTPUT_SHORT
3	VOLUME CONTROL ₁	0	1	1	VOL1_4	VOL1_3	VOL1_2	VOL1_1	VOL1_0
4	VOLUME CONTROL ₂	1	0	0	VOL2_4	VOL2_3	VOL2_2	VOL_2	VOL2_0

Table 7. Mode Control Registers

BIT	NAME	VALUE	DESCRIPTION
B0, B1	RESERVED	0	Unused
B2	INPUT_1	0	IN1 Input unselected
		1	IN1 Input selected
B3	INPUT_2	0	IN2 Input unselected
		1	IN2 Input selected
B4	POWER_ON	0	Device Disabled
		1	Device Enabled

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM48100Q-Q1 is a single-supply, mono, bridge-tied load amplifier with I2C volume control, ideal for automotive applications. It integrates a comprehensive output fault detection system, which can sense the load conditions, protecting the device during short circuit events and detecting open circuit conditions. High power supply rejection ratio allows the device to operate in noisy environments without additional power supply conditioning. The LM48100Q-Q1 features dual audio inputs that can mixed or multiplexed to the device output. Each input path has its own independent, 32-step volume control. The mixer, volume control and device mode select are controlled through an I2C compatible interface. The LM48100Q-Q1 device has an I2C selectable low power shutdown mode that disables the device, reducing quiescent current consumption to 0.01µA

8.2 Typical Application

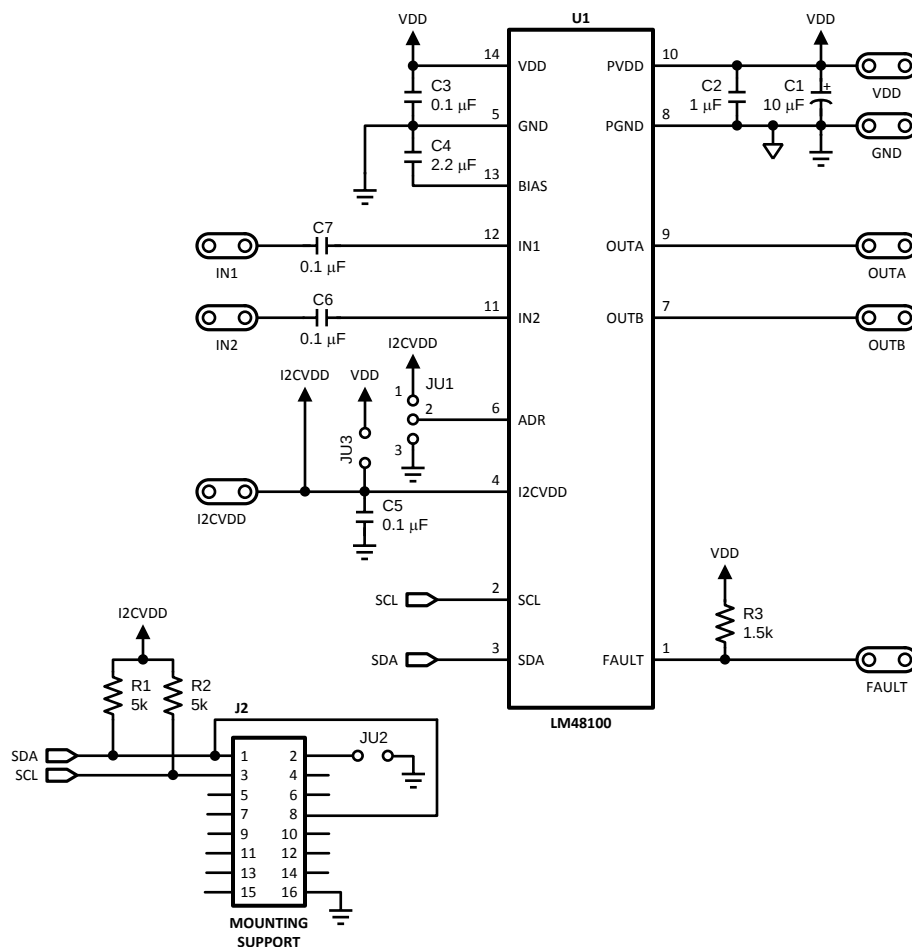


Figure 15. LM48100Q-Q1 Demo Board Schematic

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 8](#) as the input parameters.

Table 8. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Supply Voltage Range	3 V to 5.5 V
I2C Supply Voltage Range	1.8 V to 5.5 V
Temperature Range	–40 °C to 105 °C
Input Voltage Range	–0.3 V to $V_{DD} = 0.3$ V

8.2.2 Detailed Design Procedure

8.2.2.1 Power Supply Bypassing/Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1-μF ceramic capacitor from V_{DD} to GND. Additional bulk capacitance may be added as required.

8.2.2.2 Input Capacitor Selection

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48100Q-Q1. The input capacitors create a high-pass filter with the input resistors R_{IN} . The –3 dB point of the high-pass filter is found using [Equation 4](#).

$$f = 1 / 2\pi R_{IN} C_{IN} \text{ (Hz)}$$

where

- R_{IN} is given in the *Electrical Characteristics tables* found in [Specifications](#) (4)

High pass filtering the audio signal helps protect the speakers. When the LM48100Q-Q1 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved PSRR.

8.2.2.3 Bias Capacitor Selection

The LM48100Q-Q1 internally generates a $V_{DD}/2$ common-mode bias voltage. The BIAS capacitor C_{BIAS} , improves PSRR and THD+N by reducing noise at the BIAS node. Use a 2.2-μF ceramic placed as close to the device as possible.

8.2.3 Application Curve

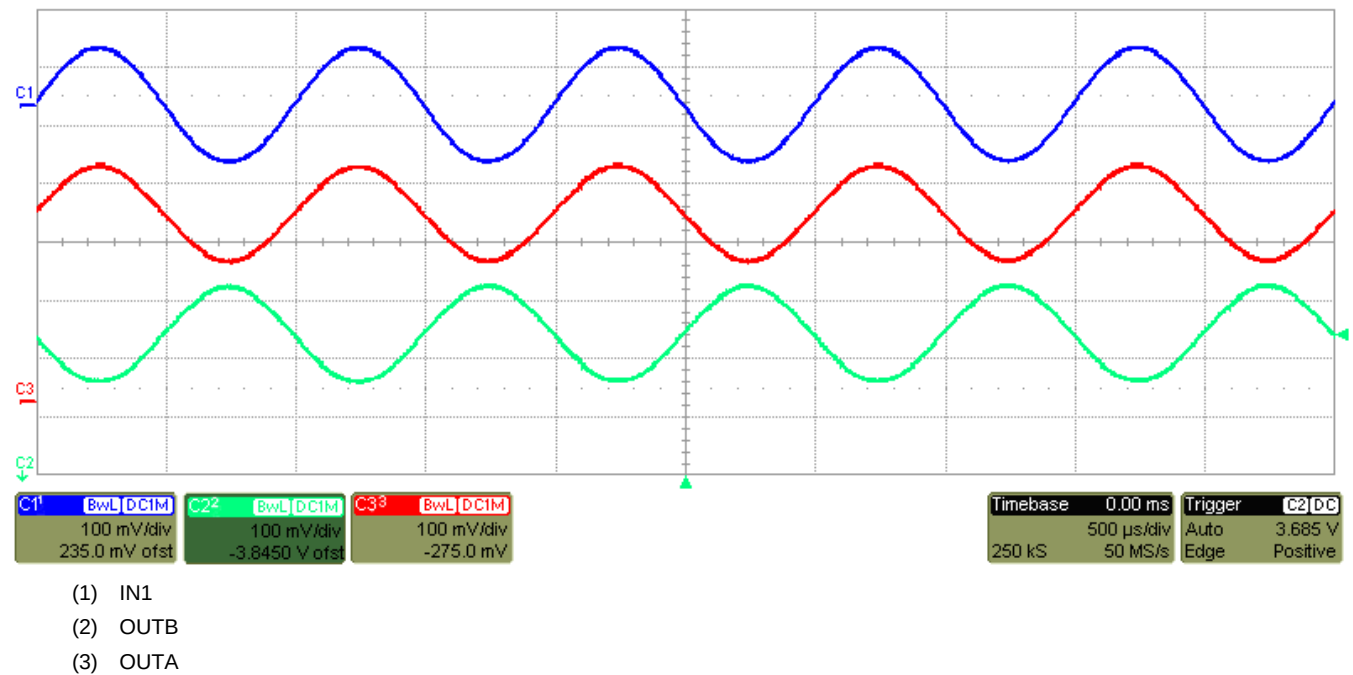


Figure 16. Input and Output Waveforms for a 1kHz Sine Wave

9 Power Supply Recommendations

The LM48100Q-Q1 is designed to operate with a power supply between 3.0 V and 5.5 V. Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1-μF ceramic capacitor from VDD to GND. Additional bulk capacitance may be added as required.

10 Layout

10.1 Layout Guidelines

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM48100Q-Q1 and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents digital noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

10.1.1 Exposed DAP Mounting Considerations

The LM48100Q-Q1 HTSSOP-EP package features an exposed die-attach (thermal) pad on its backside. The exposed pad provides a direct heat conduction path from the die to the PCB, reducing the thermal resistance of the package. Connect the exposed pad to GND with a large pad and via to a large GND plane on the bottom of the PCB for best heat distribution.

10.2 Layout Example

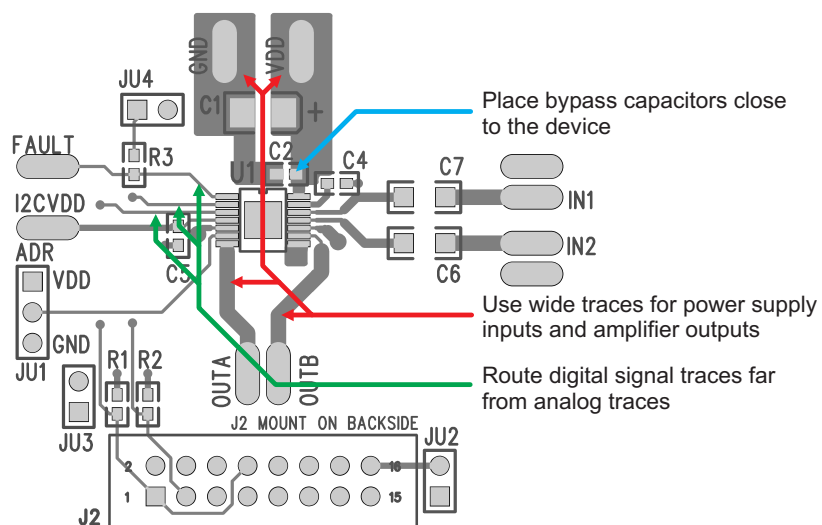


Figure 17. Example Board Layout Implementing Layout Guidelines

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

Boomer, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM48100QMH/NOPB	ACTIVE	HTSSOP	PWP	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	L48100Q	Samples
LM48100QMHE/NOPB	ACTIVE	HTSSOP	PWP	14	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	L48100Q	Samples
LM48100QMHX/NOPB	ACTIVE	HTSSOP	PWP	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	L48100Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

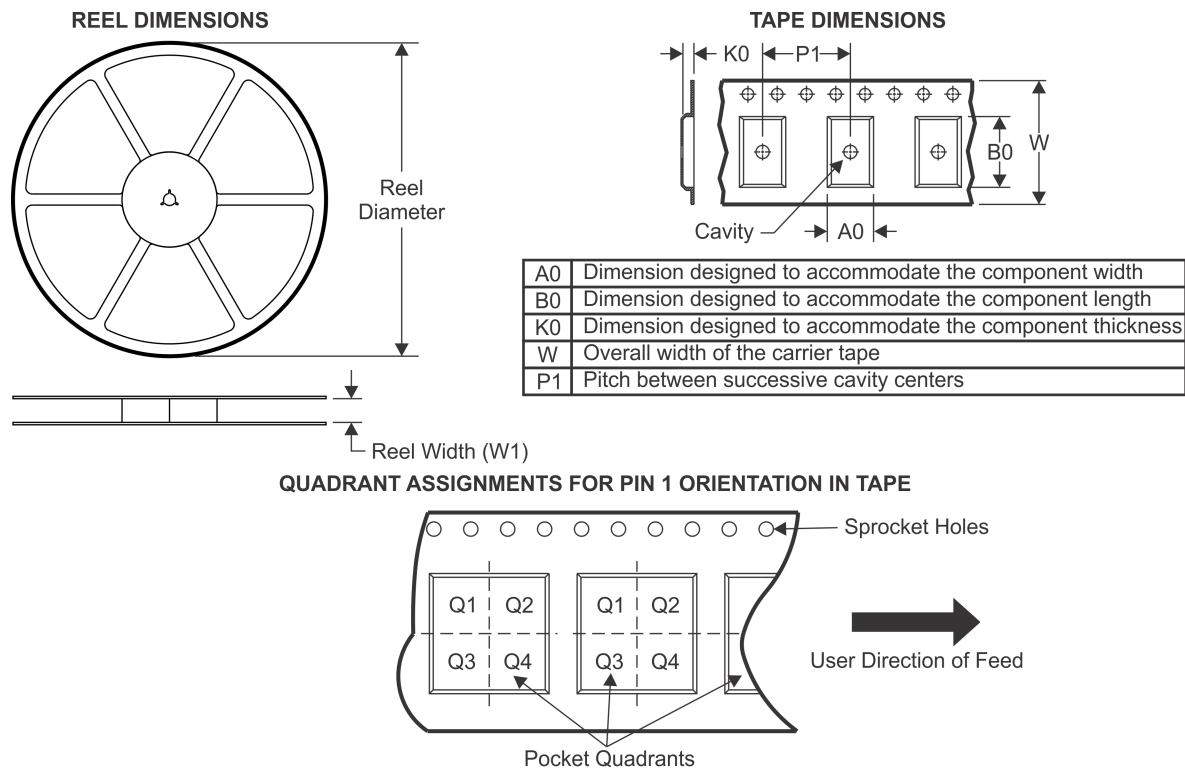
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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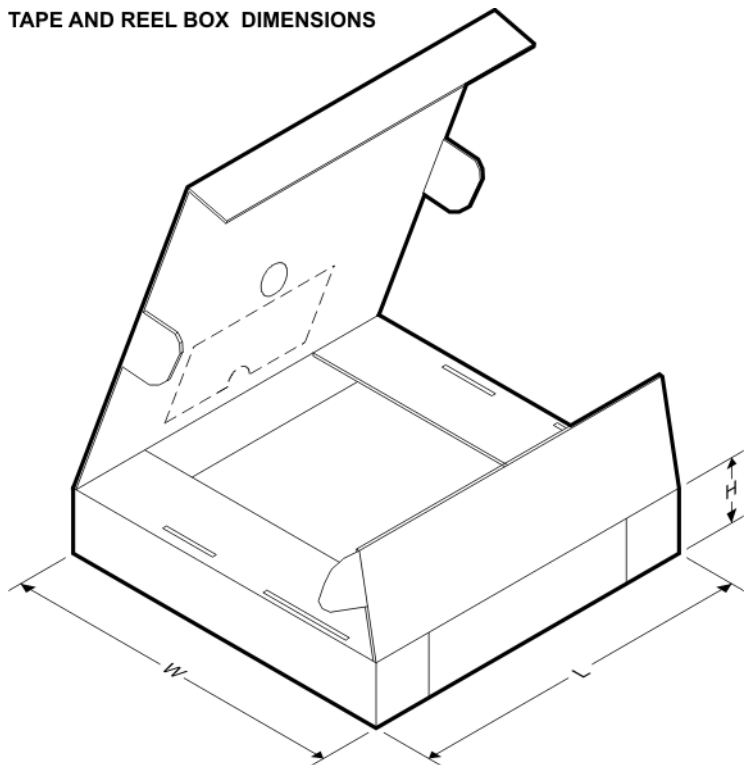
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM48100QMHE/NOPB	HTSSOP	PWP	14	250	178.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM48100QMHX/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM48100QMHE/NOPB	HTSSOP	PWP	14	250	210.0	185.0	35.0
LM48100QMHX/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0



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