THE DATASHEET OF

IR3552MTRPBF

FEATURES

- Peak efficiency up to 94.5% at 12VIN to 1.8VOUT, 93.3% at 1.2VOUT
- 40A PowIRstage® includes: Integrated Driver, Control MOSFET, Synchronous MOSFET and Schottky Diode
- <1uA Disabled ICC Bias Current
- <500uA Enabled ICC Bias Current
- Input voltage (VIN) range of 4.5V to 17V with available 14:1 VIN_DIV monitor pin
- Flexible Drive Voltage (VDRV) from 4.5V to 13.2V to optimize converter efficiency
- Integrated bootstrap PFET for improved high side MOSFET enhancement
- VDRV under voltage lockout protection
- 5V VCC with under voltage lockout protection
- Switching frequency up to 1.5MHz
- Over-temperature TFAULT alert flag with internal temperature exceeds 150°C
- MODE pin selectable 3.3V tri-state PWM logic or IR Active Tri-Level (ATL) PWM logic
- Efficient dual sided cooling
- Small 4mm x 6 mm x 0.9mm PQFN package
- Lead-free RoHS compliant package

APPLICATIONS

- High current solutions with true sleep requirements
- High frequency, low profile DC-DC converters
- Voltage Regulators for CPUs, GPUs, and DDR memory arrays

DESCRIPTION

The IR3552 integrated PowIRstage™ contains a low quiescent current synchronous buck gate driver IC which is co-packed with control and synchronous MOSFETs and low side Schottky diode to further improve efficiency. The package is optimized for PCB layout, heat transfer, driver/MOSFET control timing, and minimal switch node ringing when layout guidelines are followed. The paired gate driver and MOSFET combination enables higher efficiency at lower output voltages required by cutting edge CPU, GPU and DDR memory designs.

The IR3552 also supports <1uA disabled ICC bias current when the ENABLE pin is pulled low. This feature supports ultra-low or "near-off" power shutdown requirements of battery powered devices.

1.5MHz switching frequency enables high performance transient response, allowing miniaturization of output inductors, as well as input and output capacitors while maintaining industry leading efficiency. The IR3552's superior efficiency enables smallest size and lower solution cost.

The IR3552 provides two selectable PWM logic modes, the regular 3.3V tri-state PWM logic or International Rectifier's Active Tri-Level (ATL) PWM logic. The ATL PWM logic eliminates a dedicated Body-braking™ pin and improves the transient response of the converter during load release.

The IR3552 provides a thermal warning output set to 150°C, which makes it possible to protect critical circuits on the PCB.

ORDERING INFORMATION

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR3552MTRPBF	PQFN 4 mm x 6 mm	Tape and Reel	3000	IR3552MTRPBF

PINOUT DIAGRAM

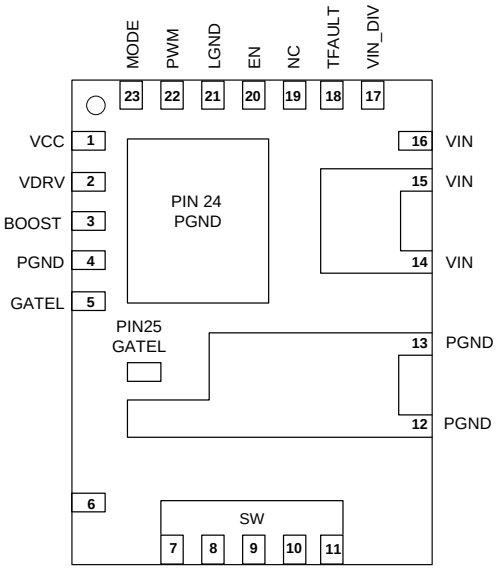


Figure 1: IR3552 Top View

FUNCTIONAL BLOCK DIAGRAM

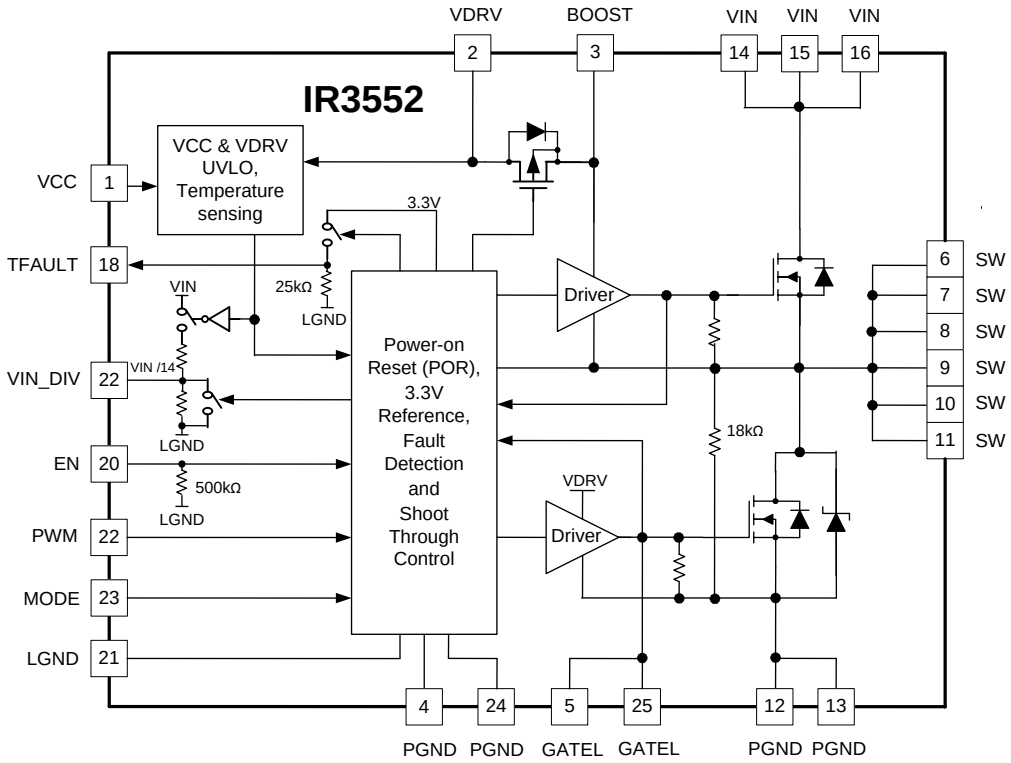


Figure 2: Block Diagram

TYPICAL APPLICATION

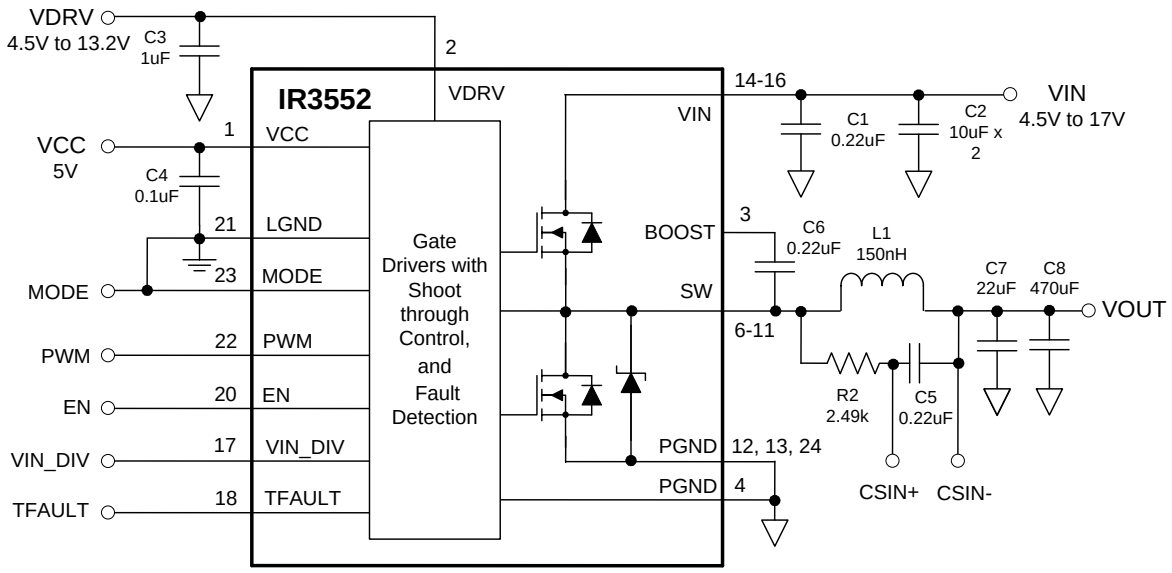


Figure 3: One Phase Voltage Regulator in Standard PWM Mode

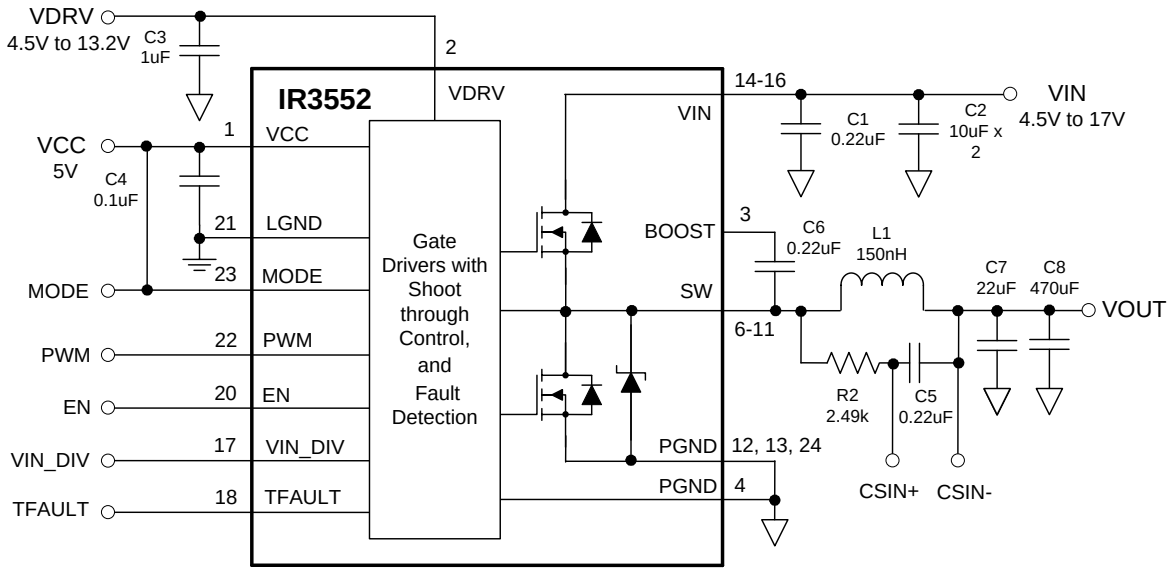


Figure 4: One Phase Voltage Regulator in IR ATL Mode

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	VCC	Connect this pin to a +5V bias supply. Place a 0.1uF high quality low ESR ceramic capacitor from this pin to the LGND pin.
2	VDRV	Connect this pin to a separate supply voltage between 5V and 12V to vary the drive voltage on both control and synchronous MOSFETs. Place a 1uF high quality low ESR ceramic capacitor from this pin to GND. Note that on the control MOSFET, the gate drive voltage is VDRV less the bootstrap diode voltage drop.
3	BOOST	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the SW pin. The bootstrap capacitor provides the charge to turn on the control MOSFET. Connect a 0.22uF capacitor from BOOST to SW pin.
4, 12, 13, 24	PGND	High current power ground. Note all pads are internally connected in the package. Provide low resistance connections to the ground plane and respective output capacitors.
5, 25	GATEL	Gate connection of the synchronous MOSFET.
6-11	SW	High current switch node output.
14-16	VIN	High current input supply pads. Provide low resistance connections to the supply rail. Ensure proper bypass capacitor values and layouts to the PGND pads.
17	VIN_DIV	Output containing divided VIN analog information, (VIN-LGND)/14 with respect to LGND. The internal resistor divider is disconnected from VIN when EN is low. An active pull-down is provided for phase fault communication.
18	TFAULT	Over temperature fault output. TFAULT will pull to 3.3V when the driver exceeds 150ºC and will remain high until 130ºC. It has a 25kΩ pull-down resistor to ground.
19	NC	No Connect.
20	EN	Enable input. Grounding EN places the device in low quiescent mode. It has a 500kΩ pull-down resistor to ground.
21	LGND	Bias and reference ground. All control signals are referenced to this pin.
22	PWM	The PWM signal is the control input for the first driver from either an IR ATL compatible source or an industry standard Tristate PWM source. Connect this pin to the PWM output of the controller.
23	MODE	The MODE pin is used to select between IR ATL mode PWM or standard tristate PWM inputs. It should be tied to LGND or VCC and is sensed at EN enable rising edge or when VCC UVLO is cleared. High = IR ATL mode, and Low = Standard tristate 3.3V and 5V TTL level PWM mode.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PIN Number	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	VCC	6.5V	-0.3V	NA	10mA
2	VDRV	15V	-0.3V	NA	1A for 100ns, 100mA DC
3	BOOST	15V with respect to SW, 35V with respect to PGND	-0.3V with respect to SW	1A for 100ns, 100mA DC	2A for 100ns, 100mA DC
4, 12, 13, 24	PGND	0.3V	-0.3V	20A RMS	45A RMS
5, 25	GATEL	15V with respect to PGND	-5V for <200ns, -0.3V DC with respect to PGND	2A for <100ns, 200mA DC	4A for <100ns, 200mA DC
6-11	SW	25V	-5V for 100ns, 25V for 100ns, -0.3V DC	45A RMS	20A RMS
14-16	VIN	25V	-0.3V	10A RMS	20A RMS
17	VIN_DIV	VCC + 0.3V	-0.3V	1mA	20mA
18	TFAULT	VCC + 0.3V	-0.3V	5mA	1mA
20	EN	VCC + 0.3V	-0.3V	1mA	1mA
21	LGND	0V	0V	50mA	1mA
22	PWM	VCC + 0.3V	-0.3V	5mA	1mA
23	MODE	VCC + 0.3V	-0.3V	1mA	1mA

THERMAL INFORMATION	
Thermal Resistance, Junction to Top (θ_{JC_TOP})	23.3 °C/W
Thermal Resistance, Junction to PCB (Pin 17) (θ_{JB})	2.4 °C/W
Thermal Resistance (θ_{JA})[1]	21.7 °C/W
Maximum Operating Junction Temperature	-40°C to 150°C
Maximum Storage Temperature Range	-65°C to 150°C
ESD rating	HBM Class 1B, JESD22-A114F Standard
	CDM Class III, JESD22-C101 Standard
MSL Rating	3
Reflow Temperature	260°C

Note:
1. Thermal Resistance (θ_{JA}) is measured with the component mounted on a high effective thermal conductivity test board in free air. Refer to International Rectifier Application Note AN-994 for details.

ELECTRICAL SPECIFICATIONS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

PARAMETER	SYMBOL	MIN	MAX	UNIT
Recommended VIN Range	VIN	4.5	17	V
Recommended VCC Range	VCC	4.5	5.5	V
Recommended VDRV Range	VDRV	4.5	13.2	V
Recommended Switching Frequency	f_{SW}	200	1500	kHz
Recommended Operating Junction Temperature	T_J	-40	125	°C

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Efficiency						
PowIRstage Peak Efficiency Note 2	η	VIN=12V, VOUT=1.2V, f_{SW} = 300kHz, L=220nH, 0.29mΩ, VDRV=6.8V, no heat sink, no air flow.		93.3		%
		VIN=12V, VOUT=1.2V, f_{SW} = 400kHz, L=150nH 0.29mΩ, VDRV=6.8V, no heat sink, no air flow.		92.6		%
PWM Input Standard Tri-State Mode (Figure 5)						
PWM Input Rising Threshold	$V_{IH(C\_PWM)}$		2.41	2.55	2.75	V
PWM Input Falling Threshold	$V_{IL(C\_PWM)}$		0.75	0.82	0.89	V
Tri-State LO_GATE Threshold	$V_{TriLoThresh}$		0.95	1.03	1.10	V
Tri-State LO_GATE Hysteresis	$V_{TriLoHyst}$		-	200	-	mV
Tri-State HI_GATE Threshold	$V_{TriHiThresh}$		2.21	2.35	2.48	V
Tri-State HI_GATE Hysteresis	$V_{TriHiHyst}$		-	200	-	mV
Tri-State Hold Off Time	$T_{TriHold}$		-	40	-	ns
PWM Input Pull-Up Voltage	$V_{PWM\_pull\ up}$	PWM Input Floating	-	1.60	-	V
PWM Input Resistance	R_{PWM}	PWM Input Floating	-	3.75	-	kΩ
Minimum Recognized PWM Pulse Width	MinPWM	ATL (IR) and Tri-State Modes	-	20	-	ns
PWM Active Tri-Level (ATL) Mode (Figure 6)						
PWM Input High Threshold	$V_{IH(C\_PWM)}$		0.95	1.03	1.10	V
PWM Input Low Threshold	$V_{IL(C\_PWM)}$		0.75	0.82	0.89	V
PWM Tri-level High Threshold	$V_{TL(C\_PWM)}$		2.41	2.55	2.75	V
PWM Tri-level Low Threshold	$V_{TH(C\_PWM)}$		2.21	2.35	2.48	V
PWM Input Current Low	I_{C_PWMlow}	V_{PWM} = 0V	-	-82	-	uA
PWM Input Current Mid	I_{C_PWMmid}	V_{PWM} = 1.8V	-	-500	-	uA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
PWM Input Current High	$I_{C\_PWMhigh}$	V_{PWM} = 2.7V	-	-1	-	mA
Minimum Recognized PWM Pulse Width	MinPWM	IR ATL and Tri-State Modes	-	20	-	ns
VINDIV						
Divider Ratio	VDIV	(VIN-LGND)/VINDIV	-	14	-	V/V
VINDIV Total Divider Resistance	R_{VINDIV}		-	462	-	kΩ
Fault Pull Down Resistance	VIN_DIV_{fault}		-	300	-	ohm
Enable Input – EN						
Input Voltage High	V_{EN_H}		1.15	2	2.7	V
Input Voltage Low	V_{EN_L}		0.54	0.8	1.2	V
Input Resistance	R_{EN}	Referenced To LGND	-	500	-	kΩ
Thermal Warning - TFAULT Output						
Over Temperature Threshold	OT		-	150	-	°C
Over Temperature Hysteresis	OT_{HYS}		-	-20	-	°C
TFAULT Source Current		V(TFAULT)=2.4V	0.45	1.5	5	mA
TFAULT Output High Voltage			2.4	3.2	3.6	V
Input Resistance	R_{TFLT}	Referenced To LGND	-	25	-	kΩ
Bootstrap Diode						
Forward Voltage	BD_{FV}	I(BOOST) = 35mA	-	595	-	mV
VCC & VDRV Under Voltage Lockout						
VCC Rising Threshold for POR	V_{ccRise}		-	3.90	4.20	V
VCC Falling Threshold for POR	V_{ccFall}		-	3.40	-	V
VDRV Rising Threshold for POR	$V_{drvRise}$		-	3.80	4.20	V
VDRV Falling Threshold for POR	$V_{drvFall}$		-	3.35	-	V
General						
Supply Bias Current Off	$I_{VCC} + I_{VDRV}$	EN=0V	-	0.6	5	uA
VDRV Supply Bias Current	$I_{drv400k}$	f_{PWM} = 400kHz, 10% Duty Cycle, VDRV=5V	-	12.5	-	mA
	I_{drv5V}	PWM Float	-	85	-	uA
	I_{drv12V}	PWM Float	-	140	-	uA
VCC Supply Bias Current	I_{vccAtl}	ATL PWM Mode, PWM Float	0.2	0.48	1.2	mA
	I_{vccTri}	Tri-state PWM Mode, PWM Float	0.2	0.43	1.2	mA

Notes

1. Guaranteed by design but not tested in production
2. Applies to IR3552 4mm x 6mm Package on IR approved PCB layout. Controller loss and Inductor loss are not included.

PWM TIMING DIAGRAM

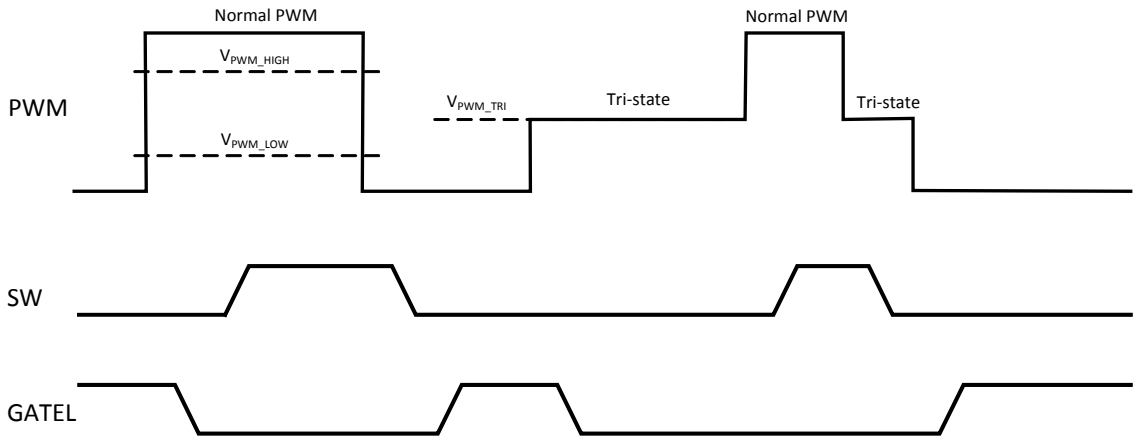


Figure 5: IR3552 Timing When Configured in 3.3V Tri-state Standard PWM Mode

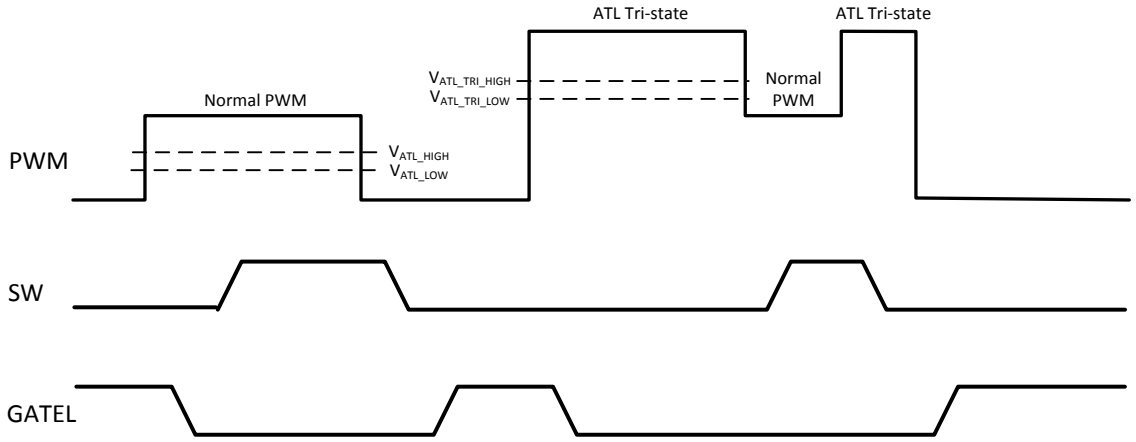


Figure 6: IR3552 Timing Diagram When Configured in IR ATL PWM Mode

TYPICAL OPERATING CHARACTERISTICS

Circuit of Figure 31, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), PWM Mode, Vcc= 5V, VDRV=7V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7"(L) x 2.6"(W), no PWM controller loss, no inductor loss, unless specified otherwise.

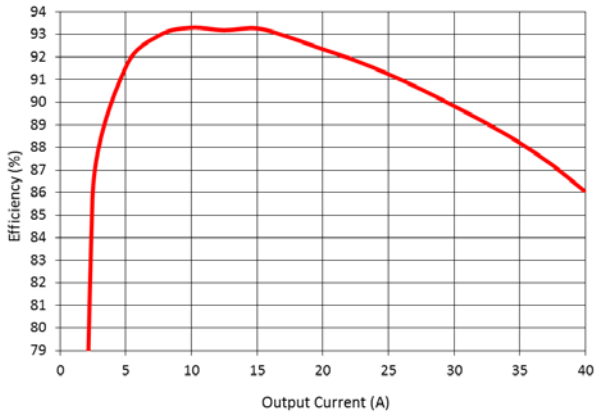


Figure 7: Typical IR3552 Efficiency, 300kHz

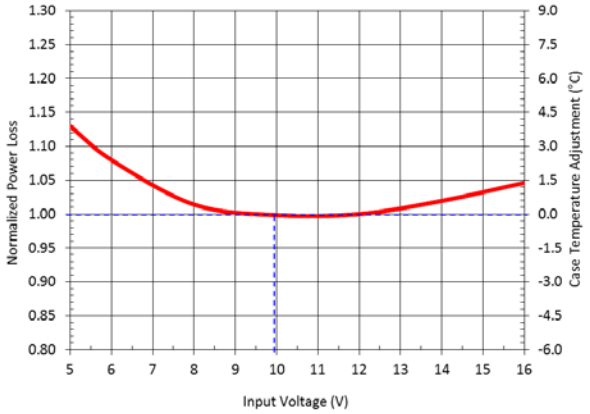


Figure 10: Normalized Power Loss vs. Input Voltage

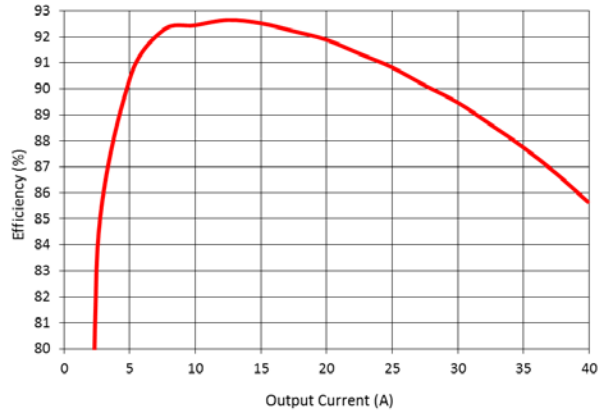


Figure 8: Typical IR3552 Efficiency, 400kHz

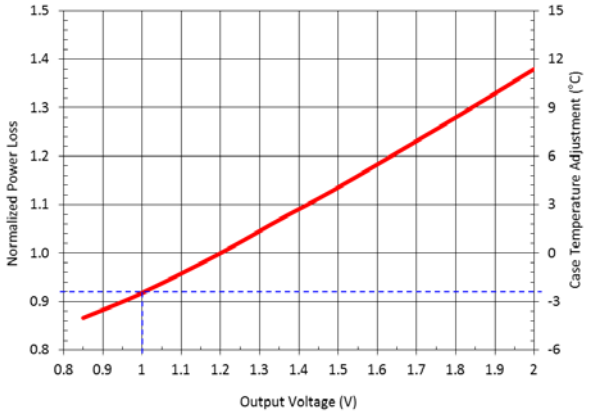


Figure 11: Normalized Power Loss vs. Output Voltage

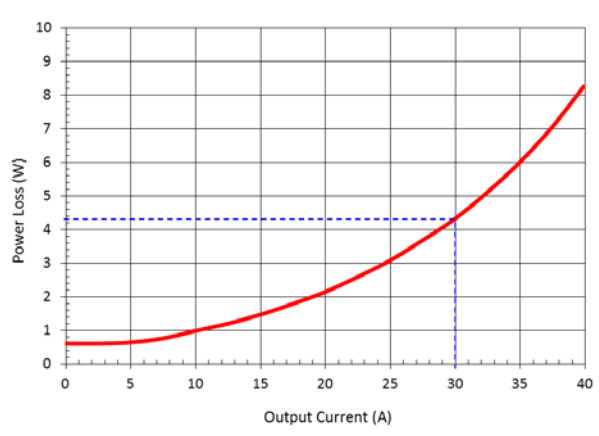


Figure 9: Typical IR3552 Power Loss, 400kHz

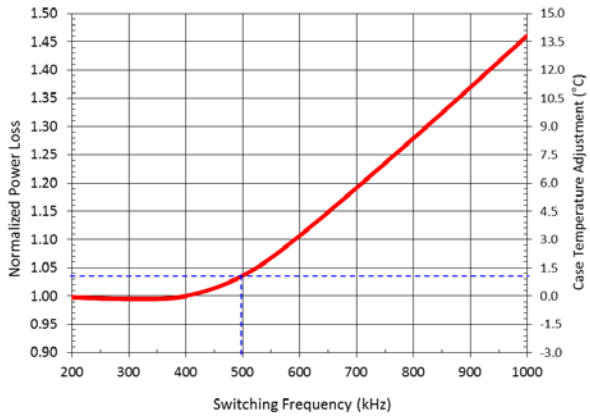


Figure 12: Normalized Power Loss vs. Switching Frequency

TYPICAL OPERATING CHARACTERISTICS

Circuit of Figure 3, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), PWM Mode, Vcc= 5V, VDRV=7V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7"(L) x 2.6"(W), no PWM controller loss, no inductor loss, unless specified otherwise.

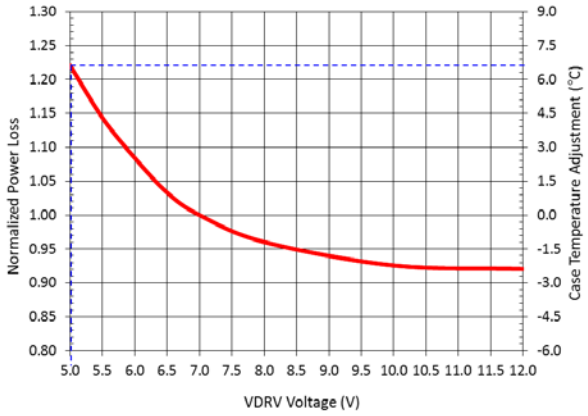


Figure 13: Normalized Power Loss vs. VDRV Voltage (Circuit of Figure 31)

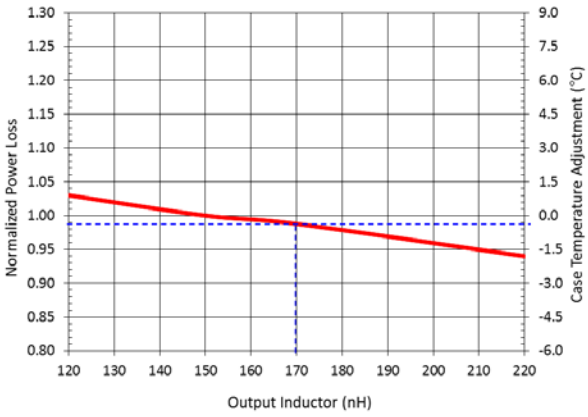


Figure 14: Normalized Power Loss vs. Output Inductor (Circuit of Figure 31)

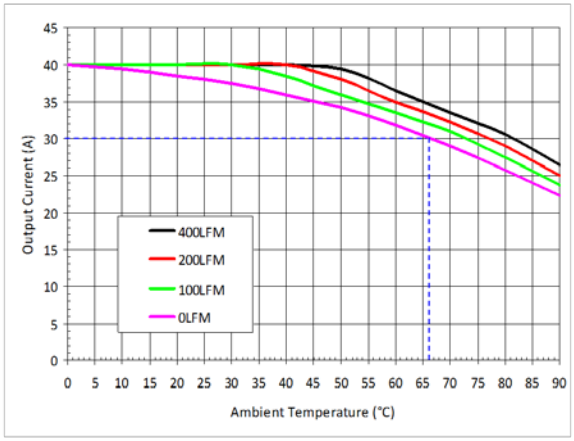


Figure 15: Thermal Derating Curve

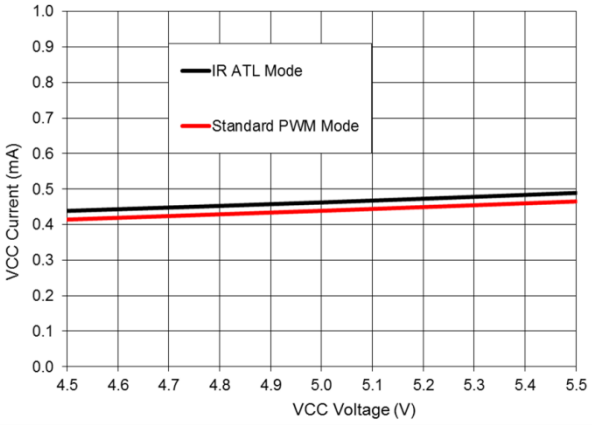


Figure 16: Vcc Current in Tristate

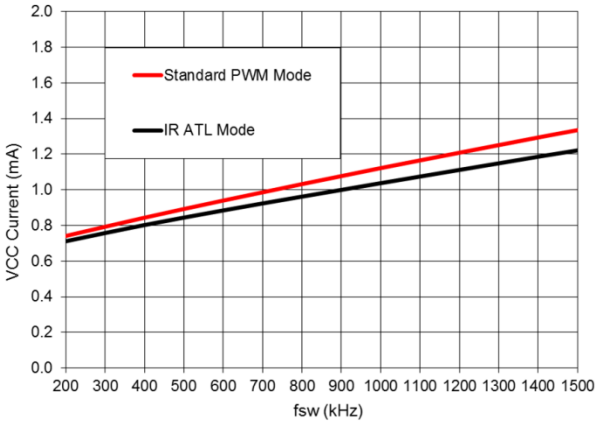


Figure 17: Vcc Current vs. Switching Frequency

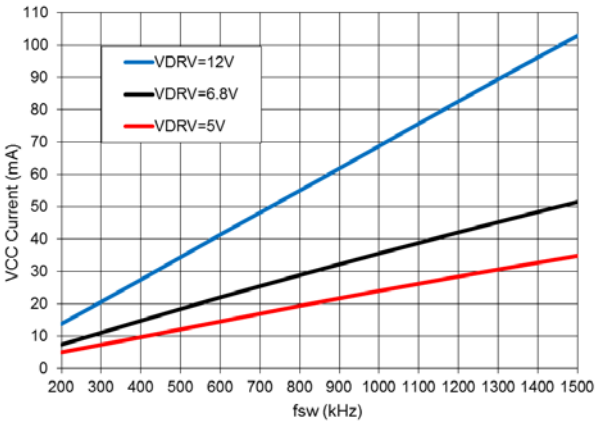


Figure 18: VDRV Current vs. Switching Frequency

TYPICAL OPERATING CHARACTERISTICS

Circuit of Figure 3, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), PWM Mode, Vcc= 5V, VDRV=7V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7"(L) x 2.6"(W), no PWM controller loss, no inductor loss, unless specified otherwise.

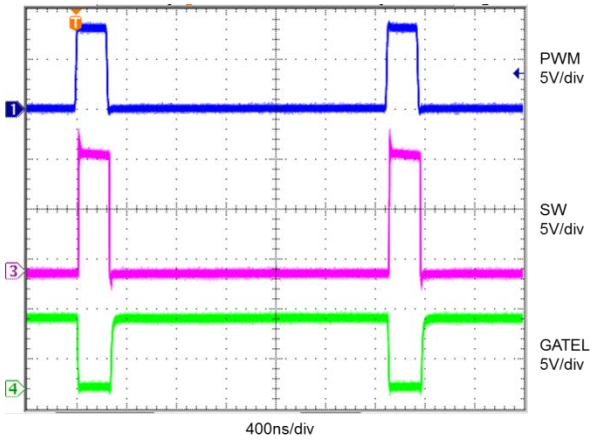


Figure 19: Switching Waveform in Standard PWM Mode, 0A

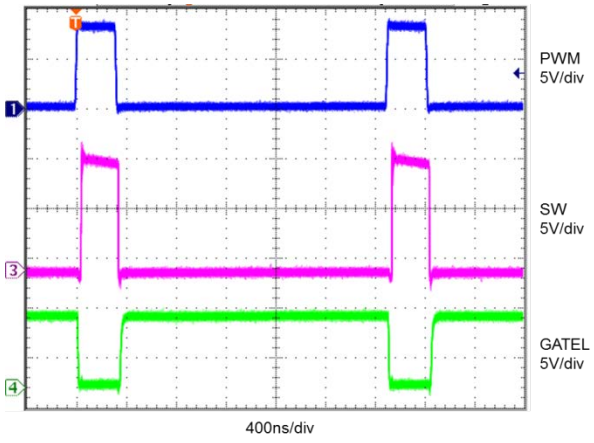


Figure 20: Switching Waveform in Standard PWM Mode, 40A

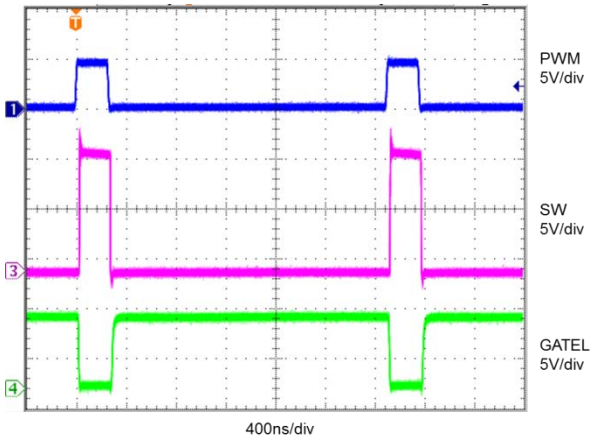


Figure 21: Switching Waveform in IR ATLPWM Mode, 0A (Circuit of Figure 4)

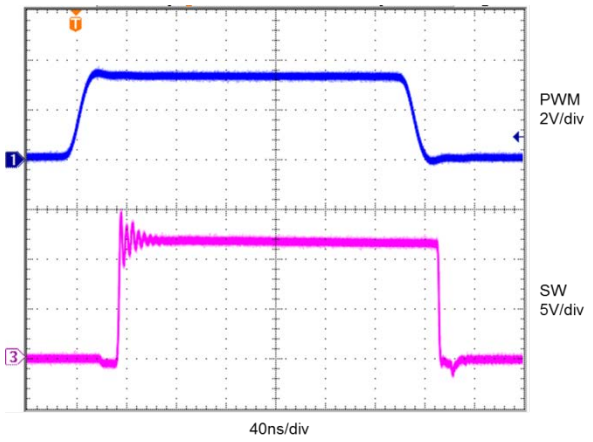


Figure 22: PWM to Switching Delay in PWM Mode, 10A

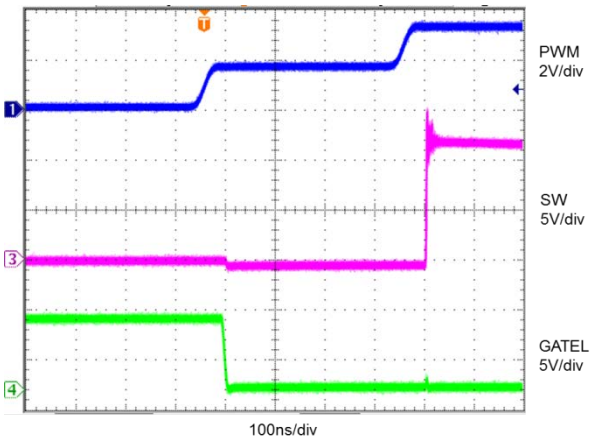


Figure 23: Tristate Delay in PWM Mode, 10A

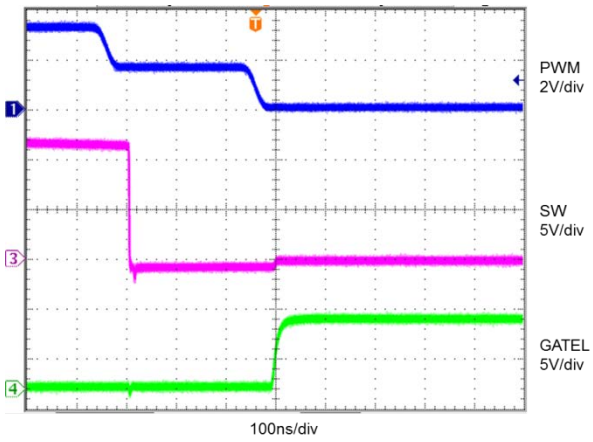


Figure 24: Tristate Delay in PWM Mode, 10A

TYPICAL OPERATING CHARACTERISTICS

Circuit of Figure 3, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), PWM Mode, Vcc= 5V, VDRV=7V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7"(L) x 2.6"(W), no PWM controller loss, no inductor loss, unless specified otherwise.

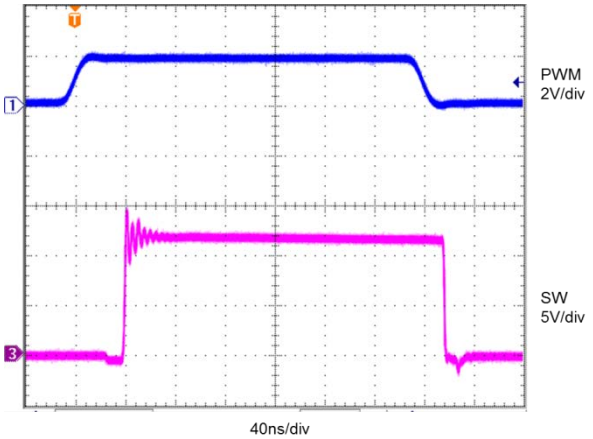


Figure 25: PWM to Switching Delay in IR ATL Mode, 10A (Circuit of Figure 4)

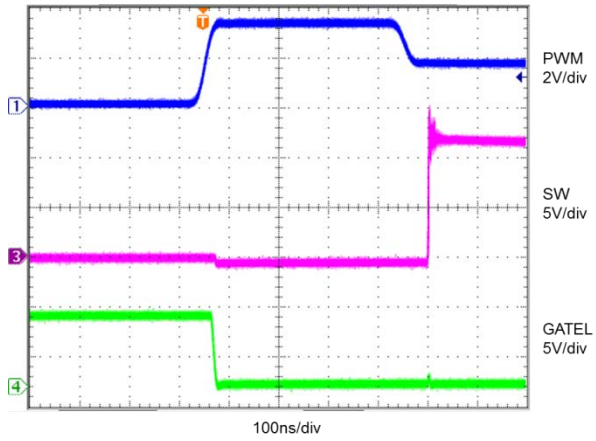


Figure 26: Tristate Delay in IR ATLMode, 10A (Circuit of Figure 4)

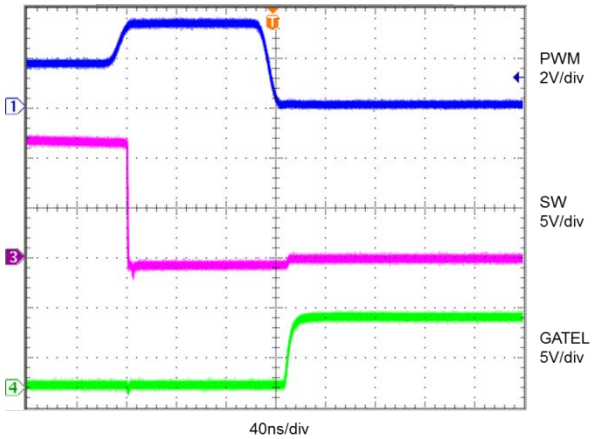


Figure 27: Tristate Delay in IR ATLMode, 10A (Circuit of Figure 4)

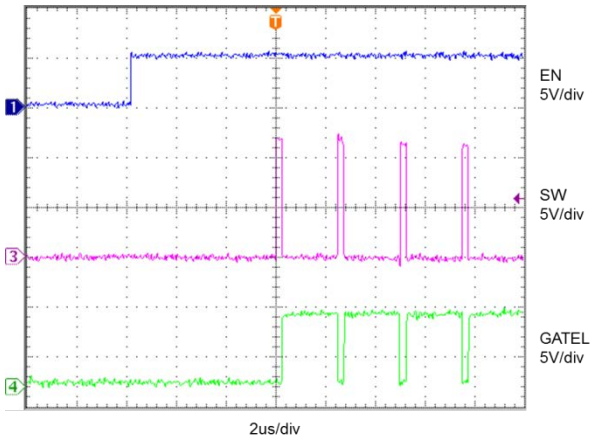


Figure 28: Enable (EN) Delay, 0A

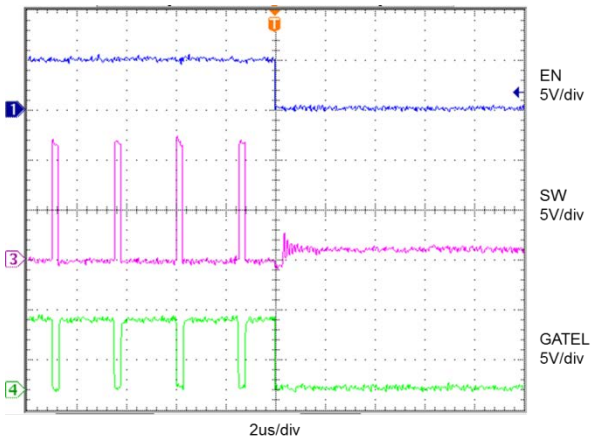


Figure 29: Enable (EN) Delay, 0A

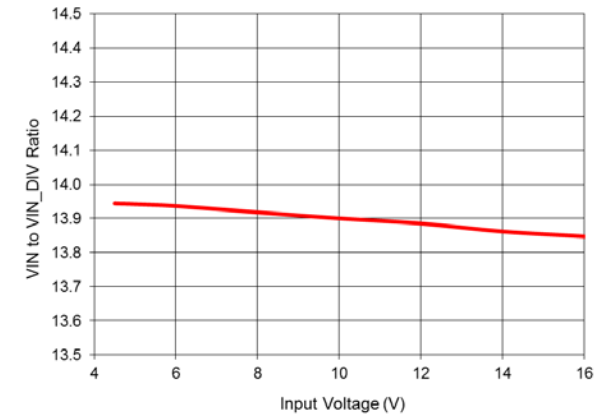


Figure 30: VIN to VIN_DIV Ratio

GENERAL DESCRIPTION

The IR3552 contains a high-efficiency and high speed MOSFET driver optimized to drive a pair of integrated control and synchronous N-channel MOSFETs up to 1.5MHz. The patented IR Active Tri-Level (ATL) feature allows complete enable and disable control of both MOSFET pairs through the PWM input signal from the controller. The timing and voltage levels of ATL are shown in Figure 6.

During normal operation the PWM transitions between low and high voltage levels to drive the synchronous and control MOSFETs. The PWM signal falling edge transition to a low voltage threshold initiates the high-side driver turn off after a short propagation delay. The dead time control circuit monitors the internal high gate signals and respective SW voltages to ensure the control MOSFET is turned off before turning on the synchronous MOSFET.

The PWM rising edge transition through the high-side turn on threshold initiates the turn off of the synchronour MOSFET after a small propagation delay. The adaptive dead time circuit provides the appropriate dead time by determining if the synchronous MOSFET gate voltage has crossed the lower threshold before allowing the High Gate voltage to rise and turn on the control MOSFET.

THEORY OF OPERATION

POWER-ON RESET (POR)

The IR3552 incorporates a power-on reset protection. This ensures that both the high- and low-side output drivers are active only after the device supply voltage VCC and VDRV both have exceeded a certain minimum operating threshold. The VCC and VDRV supplies are monitored and both the drivers are set to the low state, holding both external MOSFETs off. Once both VCC and VDRV cross the rising POR threshold and if the IR3552 is in IR ATL mode, the outputs are held in the low state until a transition from tri-state to active operation is detected at the PWM input. For standar Tri-state PWM mode, the POR operation is the same except the driver does not look for an input tri-state before functioning. During normal operation the drivers continue to remain active until VCC or VDRV fall below their respective falling POR thresholds.

INTEGRATED BOOTSTRAP PFET

The IR3552 features an integrated bootstrap PFET to reduce external component count. This enables the IR3552 to be used effectively in cost and space sensitive designs.

The bootstrap circuit is used to establish the high side MOSFET gate driver bias voltage and consists of a PFET (which includes a body diode in parallel) and an external capacitor connected between the SW and BOOST pins. The external bootstrap capacitor is charged through the PFET when the SW node is low.

STANDARD PWM TRISTATE MODE

If the MODE pin is grounded, the IR3552 accepts regular three-level 3.3V PWM input signals. As shown in Figure 5, when PWM input is above V_{PWM_HIGH}, the synchronous MOSFET is turned off and the control MOSFET is turned on. When PWM input is below V_{PWM_LOW}, the control MOSFET is turned off and synchronous MOSFET is turned on. If PWM pin is floated, the built-in resistors pull the PWM pin into a tri-state region centered around 1.6V.

IR ACTIVE TRI-LEVEL (ATL) PWM INPUT SIGNAL

When the MODE pin is tied to VCC, the IR3552 gate drivers are driven by a patented tri-level PWM control signal provided by the IR digital PWM controllers, as shown in Figure 4. During normal operation, the rising and falling edges of the PWM signal transition between 0V and 1.8V to control pulse width modulation of the integrated MOSFETs. To force both MOSFETs off simultaneously, the PWM signal crosses a tri-state voltage level higher than the tri-state high threshold. This threshold based tri-state results in a very fast disable for both the MOSFET pairs with only a small tri-state propagation delay. MOSFET switching resumes when the PWM signal falls below the tri-state threshold into the normal operating voltage range.

This fast tri-state operation eliminates the need for any tri-state hold-off time of the PWM signal to dwell in the shutdown window. Dedicated disable or

enable pins are not required which simplifies the routing and layout in applications with a limited number of board layers. It also provides switching free of shoot-through for slow PWM transition times of up to 20ns. The IR3552 is therefore tolerant of stray capacitance on the PWM signal lines.

The IR3552 provides a pull-up bias current to drive the PWM input to the tri-state condition of 3.3V when the PWM controller output is in its high impedance state. Multi-level pull-up currents are designed to drive worst case stray capacitances and allows for PWM transitions into the tri-state condition rapidly to avoid a prolonged period of MOSFET conduction during faults. The pull-up currents are disabled once the PWM pin exceeds the tri-state threshold to conserve power.

START UP IN IR ATL MODE

During initial startup in IR ATL mode, the IR3552 holds both high- and low-side MOSFETs off, even after POR thresholds are reached. This mode is maintained while the PWM signal is pulled to the tri-state threshold level greater than the tri-state high threshold and until it transitions out of tri-state. It is this initial transition out of the tri-state which enables both drivers to switch based on the normal PWM voltage levels. This startup configuration also ensures that any undetermined PWM signal levels from a controller in pre-POR state will not result in high- or low-side MOSFET turn on until the controller is out of its POR.

For Tri-state mode, the POR operation is the same except the driver does not look for an input tri-state before functioning.

HIGH-SIDE DRIVER

Each high-side driver controls an internal floating N-channel MOSFET which can be switched at 1.5MHz. The external bootstrap BOOST pin capacitor referenced to the SW node is used to bias the internal MOSFET gate. When the SW node is at ground, the bootstrap capacitor is charged to the supply voltage using the BOOST PFET and this stored charge is used to bias the internal MOSFET when the PWM signal goes high. Once the high-side MOSFET is turned on, the SW voltage is driven to the VIN supply voltage and the BOOST pin voltage is equal to VIN plus the VDRV voltage (note: without any diode voltage drop).

When the PWM signal goes low, the high side MOSFET is turned off by pulling the gate to the SW voltage.

LOW-SIDE DRIVER

The IR3552 low-side driver is designed to drive the internal N-channel MOSFET to frequencies of 1.5MHz. The low-side driver is biased from the VDRV supply voltage to turn the MOSFET on.

When the low-side MOSFET is turned on the SW node is pulled to ground. This allows recharging of the bootstrap capacitor for the next high-side MOSFET drive event.

ADAPTIVE DEAD TIME ADJUSTMENT

In a synchronous buck configuration care should be taken to prevent both high and low side MOSFETs from being on simultaneously. Such an event could result in very large shoot-through currents and could lead to long term degradation of the power stage. A fixed dead time does not provide optimal performance due to variations in converter duty cycles, bias voltages and temperature.

The IR3552 provides an adaptive dead time adjustment to minimize dead time to an optimum duration which allows for maximum efficiency. The ‘break before make’ adaptive design is achieved by monitoring gate and SW voltages to determine the ON or OFF status of a MOSFET. Adaptive dead time also provides zero-voltage switching (ZVS) of the low-side MOSFET with minimum current conduction through its body-diode.

When operating in IR ATL mode, the PWM input switches between 1.8V and 0V. The PWM falling edge transition turns off the high-side MOSFET and turns on the low-side MOSFET. The adaptive dead time circuit ensures the internal high side MOSFET Vgs is below 1.25V and the SW node voltage is below 1.38V before the low side MOSFET is turned on.

The PWM rising edge transition turns off the low-side MOSFET and turns on the high-side MOSFET. The adaptive dead time circuit ensures the internal low side MOSFET Vgs is below 1.25V before the high side MOSFET is turned on.

FREQUENCY RANGE

The IR3552 is designed to operate over a wide frequency range. The lower limit of the output frequency range is dictated by the size of the BOOST capacitor which provides bias to the high-side MOSFET driver during the entire on-time. The upper limit of frequency is determined by thermal limitations as well as pulse width limitations. The IR3552 is designed to operate with output frequencies as low as 200kHz and in excess of 1.5MHz.

ENABLE

The IR3552 has its own enable input (EN). Respective high and low MOSFETS are held off while EN is low. This allows for low quiescent current operation, which is required for next generation portable devices to improve battery life.

The IR3552 is ready to accept PWM activity in less than 10usec after the part is enabled via EN.

OVERTEMPERATURE ALERT

The IR3552 provides an over-temperature alert signal, TFAULT. This signal will pull to 3.3V when the temperature of the device reaches 150ºC. The signal will then be cleared when the temperature has reduced to 130ºC.

APPLICATION INFORMATION

Figure 3 shows a typical single phase, high density application circuit for the IR3552 with tristate standard PWM mode.

CONFIGURING THE PWM MODE

The PWM mode is programmed using the MODE pin. A HIGH on this pin sets IR ATL mode. A LOW sets standard 3.3V tri-state mode.

The MODE selection pin is latched into the IR3552 at power up and during EN cycling and cannot be changed after these events.

POWER LOSS CALCULATION

The single-phase IR3552 efficiency and power loss measurement circuit is shown in Figure 31.

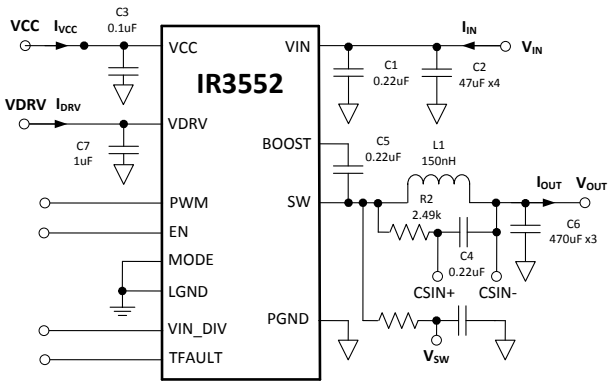


Figure 31: IR3552 Power Loss Measurement

The IR3552 power loss is determined by,

$$P_{LOSS} = V_{IN} \times I_{IN} + V_{CC} \times I_{VCC} + V_{DRV} \times I_{VDRV} - V_{SW} \times I_{OUT}$$

Where both MOSFET loss and the driver loss are included, but the PWM controller and the inductor losses are not.

Figure 8 shows the measured single-phase IR3552 efficiency under the default test conditions, V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH (0.29mΩ), VCC=7V, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow.

The efficiency of an interleaved multiphase IR3552 converter is always higher than that of a single-phase under the same conditions due to the reduced input RMS current and more input/output capacitors.

The measured single-phase IR3552 power loss under the same conditions is provided in Figure 9.

If any of the application condition, i.e. input voltage, output voltage, switching frequency, VCC MOSFET driver voltage or inductance, is different from those of Figure 9, a set of normalized power loss curves should be used. Obtain the normalizing factors from Figure 10 to Figure 14 for the new application conditions; multiply these factors by the power loss obtained from Figure 9 for the required load current.

As an example, the power loss calculation procedures under different conditions, V_{IN}=10V, V_{OUT}=1V, f_{SW} = 500kHz, VCC=5V, L=170nH, VCC=5V, I_{OUT}=30A, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow, are as follows.

1) Determine the power loss at 30A under the default test conditions of V_{IN}=12V, V_{OUT}=1.2V, f_{SW} = 400kHz, L=150nH, VCC=7V, $T_{AMBIENT}$ = 25°C, no heat sink, and no air flow. It is 4.3W from Figure 9.

2) Determine the input voltage normalizing factor with V_{IN}=10V, which is 1.0 based on the dashed lines in Figure 10.

3) Determine the output voltage normalizing factor with V_{OUT}=1V, which is 0.92 based on the dashed lines in Figure 11.

4) Determine the switching frequency normalizing factor with f_{SW} = 500kHz, which is 1.035 based on the dashed lines in Figure 12.

5) Determine the MOSFET drive voltage normalizing factor with VDRV=5V, which is 1.22 based on the dashed lines in Figure 13.

6) Determine the inductance normalizing factor with L=170nH, which is 0.985 based on the dashed lines in Figure 14.

7) Multiply the power loss under the default conditions by the five normalizing factors to obtain the power loss under the new conditions, which is 4.3W x 1.02 x 0.90 x 0.99 x 1.18 x 0.94 = 4.8W.

THERMAL DERATING

Figure 15 shows the IR3552 thermal derating curve with the case temperature controlled at or below 125°C. The test conditions are V_{IN}=12V, V_{OUT}=1.2V, f_{SW}=400kHz, L=150nH (0.29mΩ), VCC=7V, $T_{AMBIENT}$ = 0°C to 90°C, no heat sink, and Airflow = 0LFM / 100LFM / 200LFM / 400LFM.

If any of the application condition, i.e. input voltage, output voltage, switching frequency, VDRV MOSFET driver voltage, or inductance is different from those of Figure 15, a set of IR3552 case temperature adjustment curves should be used. Obtain the temperature deltas from Figure 10 to Figure 14 for the new application conditions; sum these deltas and then subtract from the IR3552 case temperature obtained from Figure 9 for the required load current.

8) From Figure 15, determine the highest ambient temperature at the required load current under the default conditions, which is 66°C at 30A with 0LFM airflow and the IR3552 case temperature of 125°C.

9) Determine the case temperature with V_{IN}=10V, which is +0.0° based on the dashed lines in Figure 10.

10) Determine the case temperature with V_{OUT}=1V, which is -2.4° based on the dashed lines in Figure 11.

11) Determine the case temperature with f_{SW} = 500kHz, which is +1.1° based on the dashed lines in Figure 12.

12) Determine the case temperature with VDRV = 5V, which is +6.5° based on the dashed lines in Figure 13.

13) Determine the case temperature with L=170nH, which is -0.4° based on the dashed lines in Figure 14.

14) Sum the case temperature adjustment from 9) to 13), +0.0° -2.4° +1.1° +6.5° -0.4° = +4.8°. Deduct the delta from the highest ambient temperature in step 8), 66°C – (+4.8°C) = 61.2°C.

BOOTSTRAP CIRCUIT

The integrated bootstrap PFET of the IR3552 reduces the external component count, cost and space. The bootstrap capacitor CBoot stores the charge and provides the voltage required to drive the external high-side MOSFET gate. A minimum 0.1uF capacitor value is recommended with a provisional series resistor in case PCB layouts or operating environments need a slower switch node rise time.

SUPPLY DECOUPLING CAPACITOR

Vcc decoupling to the IR3552 is provided by a 0.1uF bypass capacitor C_{Vcc} located close to the supply input pin. A series resistor Rvcc, typically 10Ω, is added in series with the supply voltage to filter high frequency ringing and noise. A 1uF capacitor is recommended for the VDRV decoupling capacitor, CDRV.

PCB LAYOUT CONSIDERATIONS

PCB layout and design is important to driver performance in voltage regulator circuits due to the high current slew rate (di/dt) during MOSFET switching.

- Locate all power components in each phase as close to each other as practically possible in order to minimize parasitics and losses, allowing for reasonable airflow.
- Input supply decoupling and bootstrap capacitors should be physically located close to their respective IC pins.
- High current paths like the gate driver traces should be as wide and short as practically possible.
- The ground connection of the IC should be as close as possible to the low-side MOSFET source.
- Use of a copper plane under and around the IC and thermal vias to connect to buried copper layers improves the thermal performance substantially.

* Contact International Rectifier for a layout example suitable for your specific application.

METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to prevent shorting.
- Lead land length should be equal to maximum part lead length +0.15 - 0.3 mm outboard extension and 0 to + 0.05mm inboard extension. The outboard extension ensures a large and visible toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width.
- Only 0.30mm diameter via shall be placed in the area of the power pad lands and connected to power planes to minimize the noise effect on the IC and to improve thermal performance.

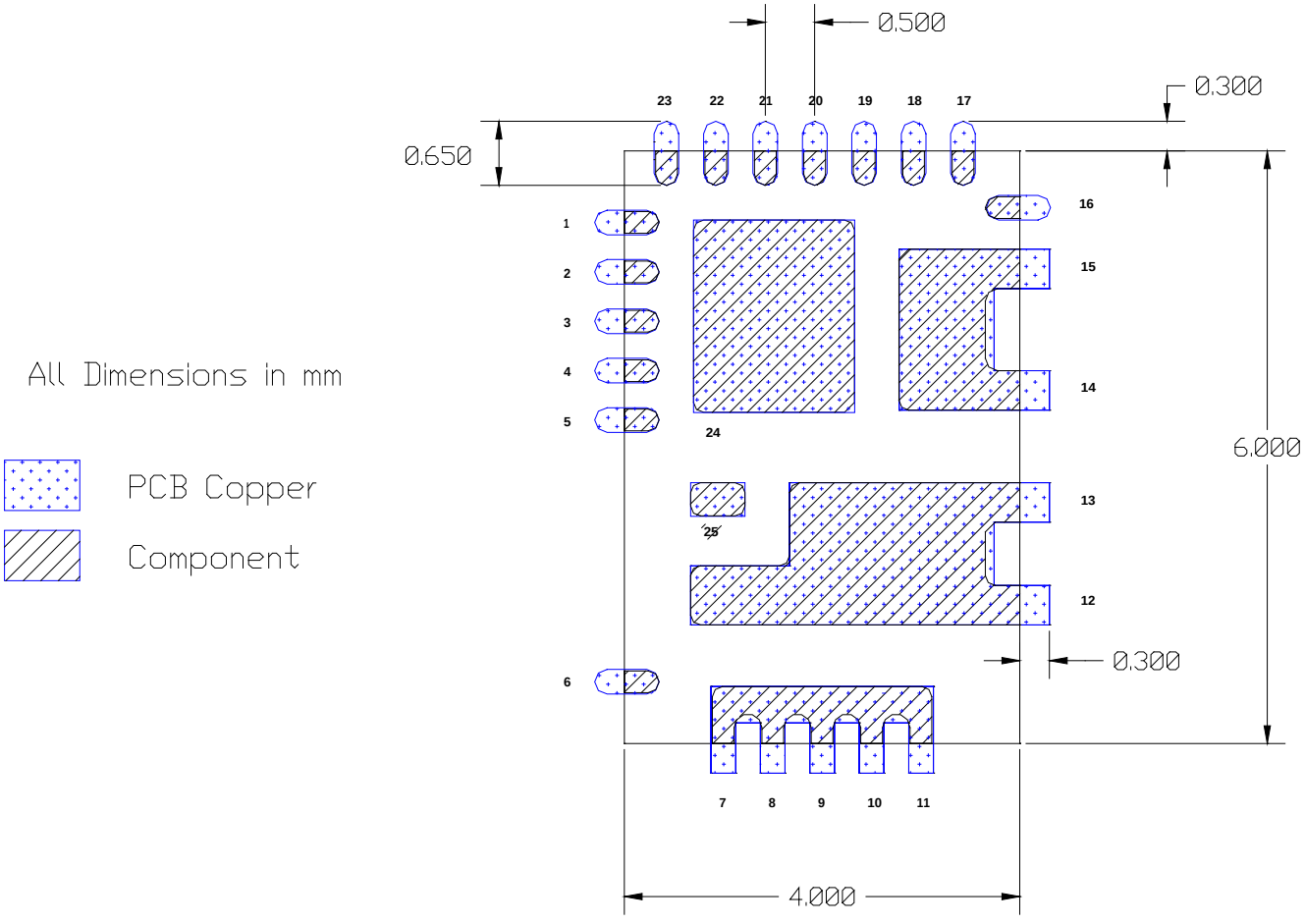


Figure 32: IR3552 Metal and Component Placement

SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist miss-alignment is a maximum of 0.05mm and it is recommended that the low power signal lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensures NSMD pads.
- The minimum solder resist width is 0.13mm typical.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The power land pads VIN, PGND, and SW should be Solder Mask Defined (SMD).
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

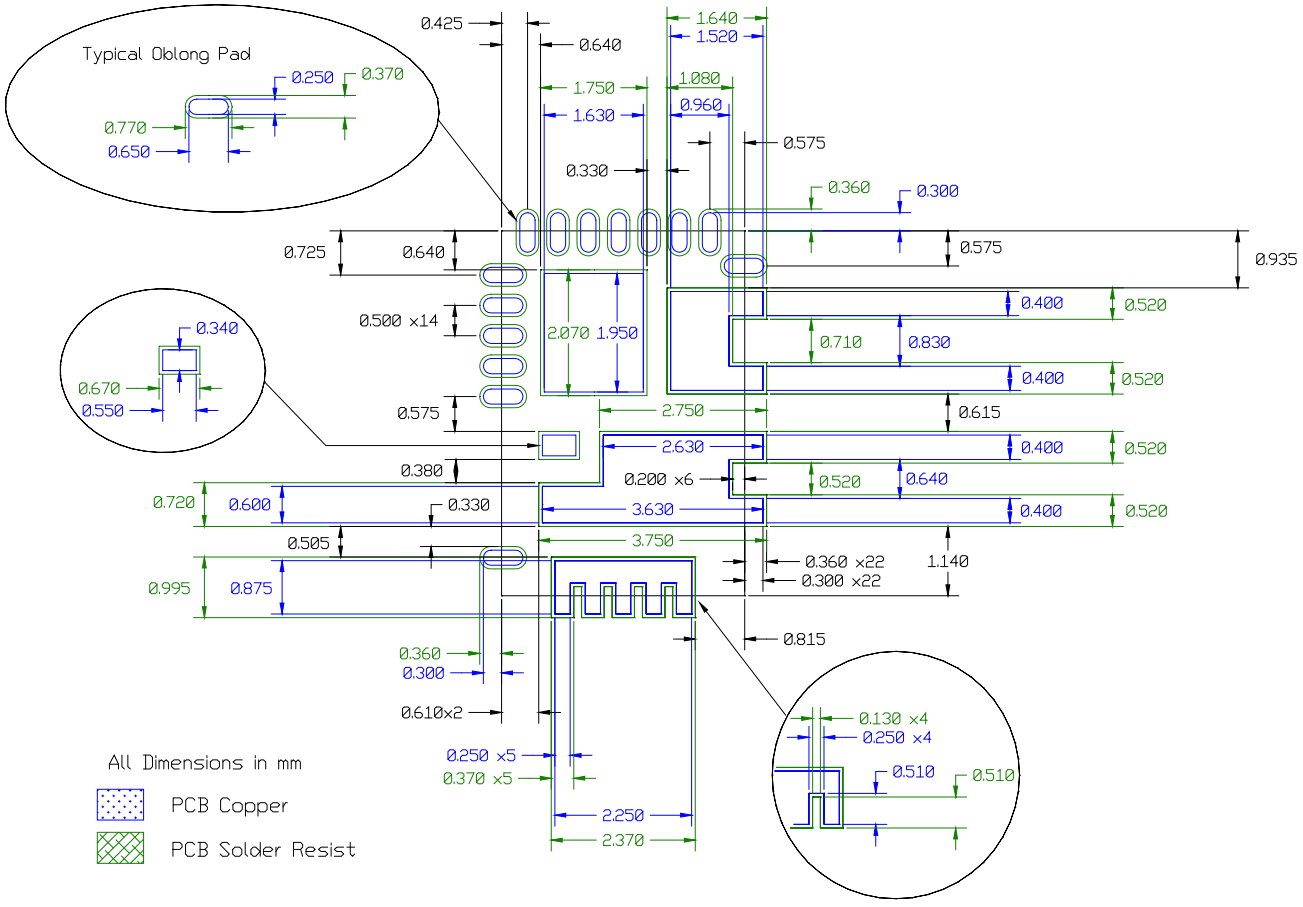


Figure 33: IR3552 Solder Resist

STENCIL DESIGN

- The stencil apertures for the lead lands should be approximately 65% to 75% of the area of the lead lands depending on stencil thickness. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The low power signal stencil lead land apertures should therefore be shortened in length to keep area ratio of 65% to 75% while centered on lead land.
- The power pads VIN, PGND and SW, land pad apertures should be approximately 65% to 75% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open. Solder paste on large pads is broken down into small sections with a minimum gap of 0.2mm between allowing for out-gassing during solder reflow.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.

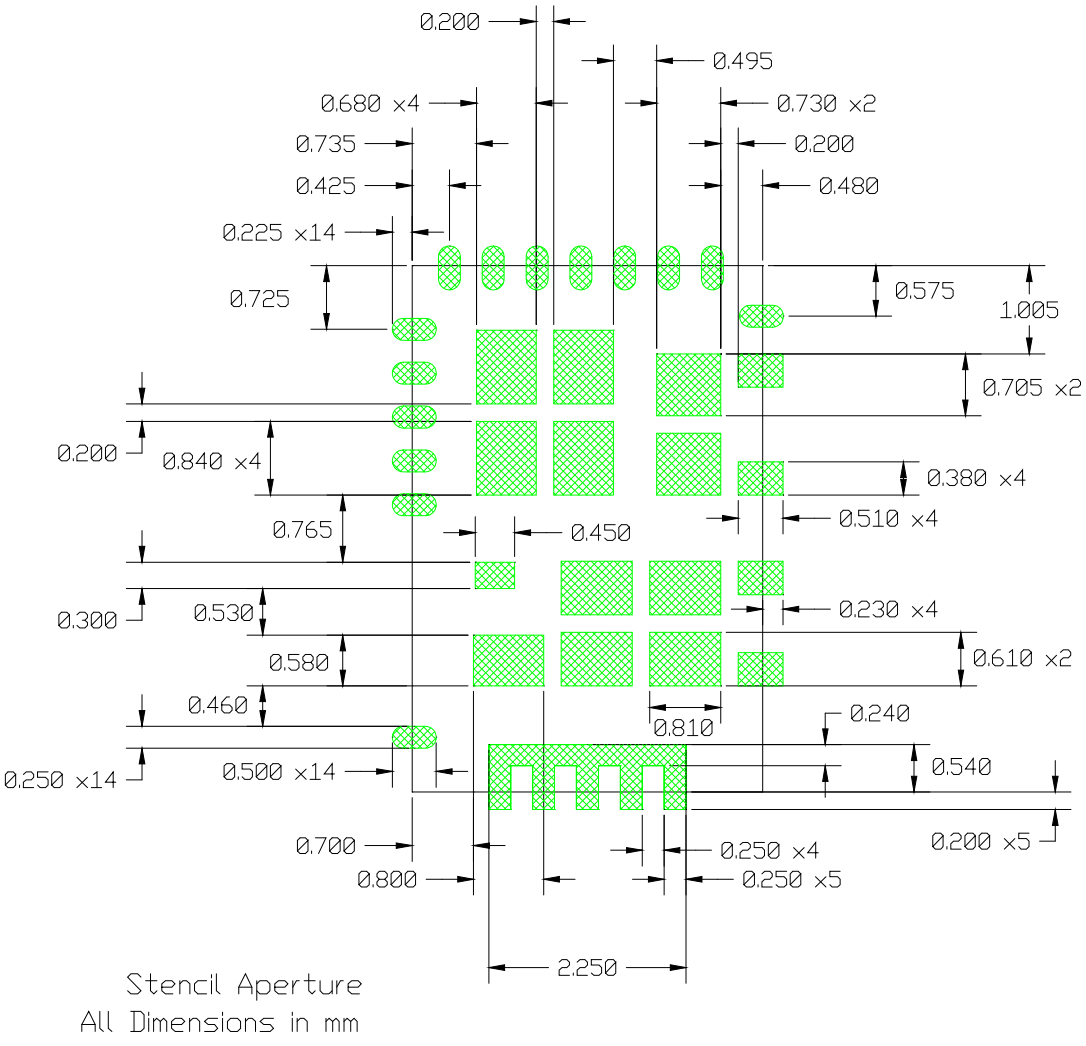


Figure 34: IR3552 Stencil Design

* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

MARKING INFORMATION

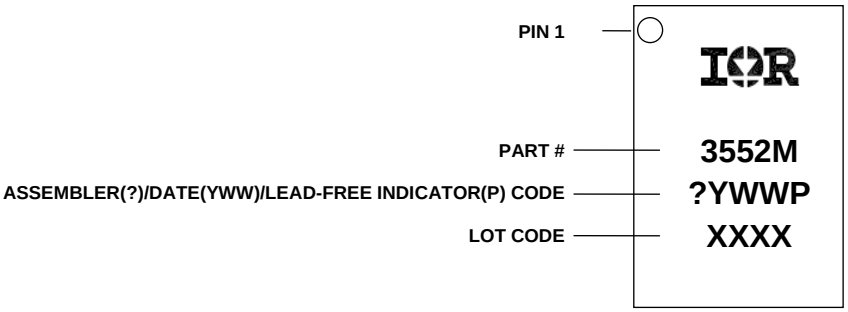
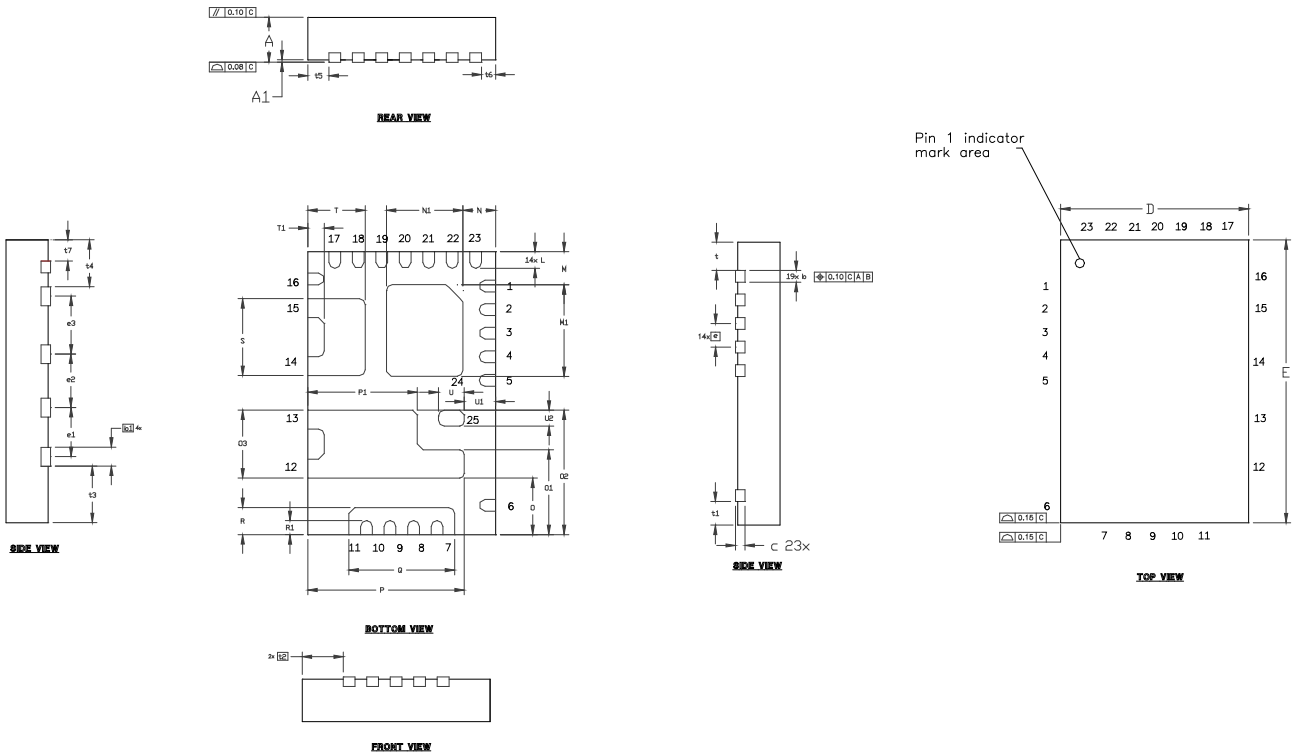


Figure 35: PQFN 4mm x 6mm

PACKAGE INFORMATION



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	1.000	.0315	.0394
A1	0.000	0.050	.0000	.0020
b	0.20	0.30	.0079	.0118
b1	0.350	0.450	.0138	.0177
c	0.203 REF.		.0080 REF.	
D	4.000 BASIC		.1575 BASIC	
E	6.000 BASIC		.2362 BASIC	
e	0.500 BASIC		.0197 BASIC	
e1	1.041 BASIC		.0410 BASIC	
e2	1.134 BASIC		.0446 BASIC	
e3	1.230 BASIC		.0484 BASIC	
t	0.600 BASIC		.0236 BASIC	
t1	0.500 BASIC		.0197 BASIC	
t2	0.875 BASIC		.0344 BASIC	
t3	1.200 BASIC		.0472 BASIC	
t4	0.996 BASIC		.0392 BASIC	
t5	0.450 BASIC		.0177 BASIC	
t6	0.300 BASIC		.0118 BASIC	
t7	0.450 BASIC		.0177 BASIC	

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
L	0.300	0.400	.0118	.0157
M	0.650	0.750	.0256	.0295
M1	1.896	1.996	.0747	.0786
N	0.650	0.750	.0256	.0296
N1	1.577	1.677	.0621	.0660
O	1.150	1.250	.0453	.0492
O1	1.750	1.850	.0689	.0728
O2	2.591	2.691	.1020	.1060
O3	1.391	1.491	.0548	.0587
P	3.281	3.381	.1292	.1331
P1	2.281	2.381	.0898	.0937
Q	2.200	2.300	.0866	.0906
R	0.525	0.625	.0207	.0246
R1	0.250	0.350	.0098	.0138
S	1.580	1.680	.0622	.0661
T	1.173	1.273	.0462	.0501
T1	0.300	0.400	.0118	.0157
U	0.500	0.600	.0197	.0236
U1	0.619	0.719	.0244	.0283
U2	0.287	0.387	.0130	.0152

Figure 36: PQFN 4mm x 6mm

Data and specifications subject to change without notice.
This product will be designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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- Alternative Solution
- Excess Inventory Management