



**THE DATASHEET OF
LT1193IS8#TRPBF**



FEATURES

- Differential or Single-Ended Gain Block (Adjustable)
- -3dB Bandwidth, $A_V = \pm 2$: 80MHz
- Slew Rate: 500V/ μs
- Low Cost
- Output Current: $\pm 50\text{mA}$
- Settling Time: 180ns to 0.1%
- CMRR at 10MHz: $> 40\text{dB}$
- Differential Gain Error: 0.2%
- Differential Phase Error: 0.08°
- Single 5V Operation
- Drives Cables Directly
- Output Shutdown

APPLICATIONS

- Line Receivers
- Video Signal Processing
- Cable Drivers
- Oscillators
- Tape and Disc Drive Systems

DESCRIPTION

The LT[®]1193 is a video difference amplifier optimized for operation on $\pm 5\text{V}$ and a single 5V supply. This versatile amplifier features uncommitted high input impedance (+) and (–) inputs, and can be used in differential or single-ended configurations. Additionally, a second set of inputs give gain adjustment and DC control to the differential amplifier.

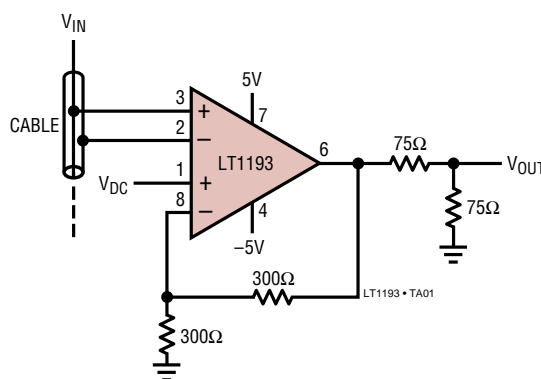
The LT1193's high slew rate, 500V/ μs , wide bandwidth, 80MHz, and $\pm 50\text{mA}$ output current make it ideal for driving cables directly. The shutdown feature reduces the power dissipation to a mere 15mW and allows multiple amplifiers to drive the same cable.

The LT1193 is available in 8-pin PDIP and SO packages.

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TYPICAL APPLICATION

Cable Sense Amplifier for Loop Through Connections with DC Adjust



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V ⁺ to V ⁻)	18V
Differential Input Voltage	±6V
Input Voltage	±V _S
Output Short-Circuit Duration (Note 2)	Continuous
Operating Temperature Range	
LT1193M (OBSOLETE)	-55°C to 125°C
LT1193C	0°C to 70°C
LT1193I	-40°C to 85°C
Maximum Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>N8 PACKAGE 8-LEAD PDIP S8 PACKAGE 8-LEAD PLASTIC SO</p> <p>T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N8) T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S8)</p> <p>J8 PACKAGE 8-LEAD CERDIP T_{JMAX} = 150°C, θ_{JA} = 100°C/W</p> <p>OBSOLETE PACKAGE Consider the N8 or S8 Packages for Alternate Source</p>	ORDER PART NUMBER
	LT1193CN8 LT1193CS8 LT1193IS8
	S8 PART MARKING
	1193 1193I
	LT1193MJ8 LT1193CJ8

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_S = ±5V, V_{REF} = 0V, R_{FB1} = 900Ω from Pins 6 to 8, R_{FB2} = 100Ω from Pin 8 to ground, R_L = R_{FB1} + R_{FB2} = 1k (Note 3), T_A = 25°C, C_L ≤ 10pF, Pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1193M/C/I			UNITS
			MIN	TYP	MAX	
V _{OS}	Input Offset Voltage	Both Inputs (Note 4) All Packages		2	12	mV
I _{OS}	Input Offset Current	Either Input		0.2	3	μA
I _B	Input Bias Current	Either Input		±0.5	±3.5	μA
e _n	Input Noise Voltage	f ₀ = 10kHz		50		nV/√Hz
i _n	Input Noise Current	f ₀ = 10kHz		4		pA/√Hz
R _{IN}	Input Resistance	Either Input		100		kΩ
C _{IN}	Input Capacitance	Either Input		2		pF
V _{IN(LIM)}	Input Voltage Limit	(Note 5)		1.3		V
	Input Voltage Range		-2.5		3.5	V
CMRR	Common Mode Rejection Ratio	V _{CM} = -2.5V to 3.5V	60	75		dB
PSRR	Power Supply Rejection Ratio	V _S = ±2.375V to ±8V	60	75		dB
V _{OUT}	Output Voltage Swing	V _S = ±5V, R _L = 1k V _S = ±8V, R _L = 1k V _S = ±8V, R _L = 100Ω	±3.8 ±6.8 6.4	±4 ±7 6.6		V V V
G _E	Gain Error	V _O = ±3V, R _L = 1k R _L = 100Ω		0.1 0.1	1.0 1.2	% %
SR	Slew Rate	V _O = ±2V, R _L = 300Ω (Notes 6, 11)	350	500		V/μs
FPBW	Full-Power Bandwidth	V _O = 6V _{P-P} (Note 7)	18.5	26.5		MHz
BW	Small-Signal Bandwidth			9		MHz
t _r , t _f	Rise Time, Fall Time	A _V = 50, V _O = ±1.5V, 20% to 80% (Note 11)	110	160	210	ns
t _{PD}	Propagation Delay	R _L = 1k, V _O = ±125mV, 50% to 50%		15		ns
	Overshoot	V _O = ±50mV		0		%
t _s	Settling Time	3V Step, 0.1% (Note 8)		180		ns
Diff A _V	Differential Gain	R _L = 150Ω, A _V = 2 (Note 9)		0.2		%
Diff Ph	Differential Phase	R _L = 150Ω, A _V = 2 (Note 9)		0.08		Deg _{P-P}

1193fb

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from Pins 6 to 8, $R_{FB2} = 100\Omega$ from Pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$ (Note 3), $T_A = 25^\circ C$, $C_L \leq 10pF$, Pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1193M/C/I			UNITS
			MIN	TYP	MAX	
I_S	Supply Current			35	43	mA
	Shutdown Supply Current	Pin 5 at V^-		1.3	2	mA
I_{SHDN}	Shutdown Pin Current	Pin 5 at V^-		20	50	μA
t_{ON}	Turn On Time	Pin 5 from V^- to Ground, $R_L = 1k$		300		ns
t_{OFF}	Turn Off Time	Pin 5 from Ground to V^- , $R_L = 1k$		200		ns

$V_S^+ = 5V$, $V_S^- = 0V$, $V_{REF} = 2.5V$, $R_{FB1} = 900\Omega$ from Pins 6 to 8, $R_{FB2} = 100\Omega$ from Pin 8 to V_{REF} , $R_L = R_{FB1} + R_{FB2} = 1k$ (Note 3), $T_A = 25^\circ C$, $C_L \leq 10pF$, Pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1193M/C/I			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	Both Inputs (Note 4) All Packages		3	15	mV
I_{OS}	Input Offset Current	Either Input		0.2	3	μA
I_B	Input Bias Current	Either Input		± 0.5	± 3.5	μA
	Input Voltage Range		2		3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 2V$ to $3.5V$	55	70		dB
V_{OUT}	Output Voltage Swing	$R_L = 100\Omega$ to Ground	V_{OUT} High	3.6	3.8	V
			V_{OUT} Low		0.25	0.4
SR	Slew Rate	$V_O = 1V$ to $3V$		250		$V/\mu s$
BW	Small-Signal Bandwidth			8		MHz
I_S	Supply Current			32	40	mA
	Shutdown Supply Current	Pin 5 at V^-		1.3	2	mA
I_{SHDN}	Shutdown Pin Current	Pin 5 at V^-		20	50	μA

The ● denotes the specifications which apply over the full operating temperature range of $-55^\circ C \leq T_A \leq 125^\circ C$. $V_S = \pm 5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from Pins 6 to 8, $R_{FB2} = 100\Omega$ from Pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$ (Note 3), $C_L \leq 10pF$, Pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1193M			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	2	16	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●	20		$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	0.8	5	μA
I_B	Input Bias Current		●	± 1	± 5.5	μA
	Input Voltage Range		●	-2.5	3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $3.5V$	●	53	70	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 5V$	●	53	70	dB
V_{OUT}	Output Voltage Swing	$R_L = 1k$	●	3.6	4	V
		$V_S = \pm 8V$, $R_L = 100\Omega$	●	6	6.5	
G_E	Gain Error	$V_O = \pm 3V$, $R_L = 1k$	●	0.2	1.2	%
I_S	Supply Current		●	35	43	mA
	Shutdown Supply Current	Pin 5 at V^- (Note 10)	●	1.3	2.2	mA
I_{SHDN}	Shutdown Pin Current	Pin 5 at V^-	●	20		μA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. $V_S = \pm 5\text{V}$, $V_{\text{REF}} = 0\text{V}$, $R_{\text{FB1}} = 900\Omega$ from Pins 6 to 8, $R_{\text{FB2}} = 100\Omega$ from Pin 8 to ground, $R_L = R_{\text{FB2}} = 1\text{k}$ (Note 3), $C_L \leq 10\text{pF}$, Pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1193I			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	SO-8 Package	●	2	20	mV
$\Delta V_{\text{OS}}/\Delta T$	Input V_{OS} Drift		●	20		$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		●	0.8	5	μA
I_{B}	Input Bias Current		●	± 1	± 5.5	μA
	Input Voltage Range		●	-2.5	3.5	V
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -2.5\text{V}$ to 3.5V	●	53	70	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.375\text{V}$ to $\pm 5\text{V}$	●	53	70	dB
V_{OUT}	Output Voltage Swing	$R_L = 1\text{k}$	●	3.6	4	V
		$V_S = \pm 8\text{V}$, $R_L = 100\Omega$	●	6	6.5	
G_E	Gain Error	$V_O = \pm 3\text{V}$, $R_L = 1\text{k}$	●	0.2	1.2	%
I_S	Supply Current		●	35	43	mA
	Shutdown Supply Current	Pin 5 at V^- (Note 10)	●	1.3	2.2	mA
I_{SHDN}	Shutdown Pin Current	Pin 5 at V^-	●	20		μA

The ● denotes the specifications which apply over the full operating temperature range of $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$. $V_S = \pm 5\text{V}$, $V_{\text{REF}} = 0\text{V}$, $R_{\text{FB1}} = 900\Omega$ from Pins 6 to 8, $R_{\text{FB2}} = 100\Omega$ from Pin 8 to ground, $R_L = R_{\text{FB1}} + R_{\text{FB2}} = 1\text{k}$ (Note 3), $C_L \leq 10\text{pF}$, Pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1193C			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	N8 Package SO-8 Package	● ●	2	14 20	mV mV
$\Delta V_{\text{OS}}/\Delta T$	Input V_{OS} Drift		●	20		$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		●	0.2	3.5	μA
I_{B}	Input Bias Current		●	± 0.5	± 4	μA
	Input Voltage Range		●	-2.5	3.5	V
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -2.5\text{V}$ to 3.5V	●	55	70	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.375\text{V}$ to $\pm 5\text{V}$	●	55	70	dB
V_{OUT}	Output Voltage Swing	$R_L = 1\text{k}$	●	3.7	4	V
		$R_L = 100\Omega$	●	6.2	6.6	V
G_E	Gain Error	$V_O = \pm 3\text{V}$, $R_L = 1\text{k}$	●	0.2	1.2	%
I_S	Supply Current		●	35	43	mA
	Shutdown Supply Current	Pin 5 at V^- (Note 10)	●	1.3	2.1	mA
I_{SHDN}	Shutdown Pin Current	Pin 5 at V^-	●	20		μA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

Note 3: When $R_L = 1\text{k}$ is specified, the load resistor is $R_{\text{FB1}} + R_{\text{FB2}}$, but when $R_L = 100\Omega$ is specified, then an additional 100Ω is added to the output.

Note 4: V_{OS} measured at the output (Pin 6) is the contribution from both input pair, and is input referred.

Note 5: $V_{\text{IN LIM}}$ is the maximum voltage between $-V_{\text{IN}}$ and $+V_{\text{IN}}$ (Pin 2 and Pin 3) for which the output can respond.

Note 6: Slew rate is measured between $\pm 2\text{V}$ on the output, with a $\pm 1\text{V}$ input step, $A_V = 3$.

Note 7: Full-power bandwidth is calculated from the slew rate measurement:

$$\text{FPBW} = \text{SR}/2\pi V_p.$$

Note 8: Settling time measurement techniques are shown in "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985.

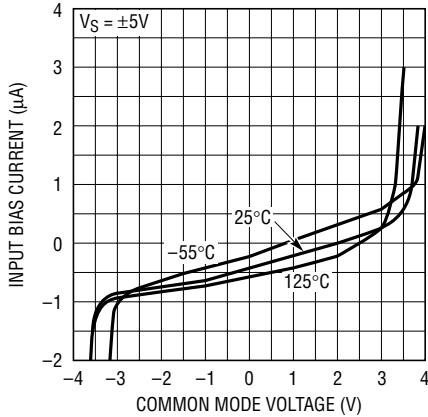
Note 9: NTSC (3.58MHz).

Note 10: See Applications section for shutdown at elevated temperatures. Do not operate the shutdown above $T_J > 125^{\circ}\text{C}$.

Note 11: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J and N suffix) and are sample tested on every lot of the SO packaged parts (S suffix).

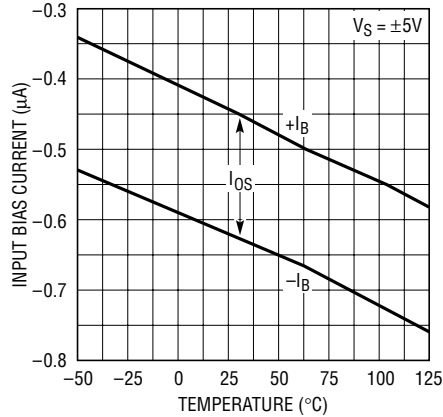
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Common Mode Voltage



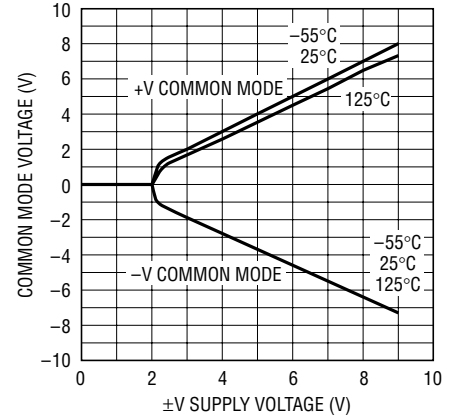
LT1193 • TPC01

Input Bias Current vs Temperature



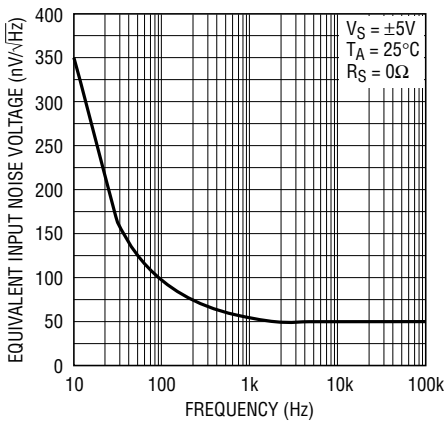
LT1193 • TPC02

Common Mode Voltage vs Supply Voltage



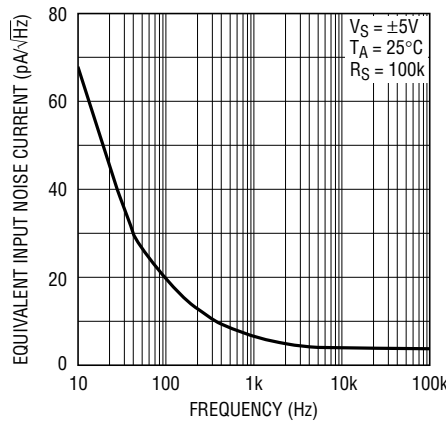
LT1193 • TPC03

Equivalent Input Noise Voltage vs Frequency



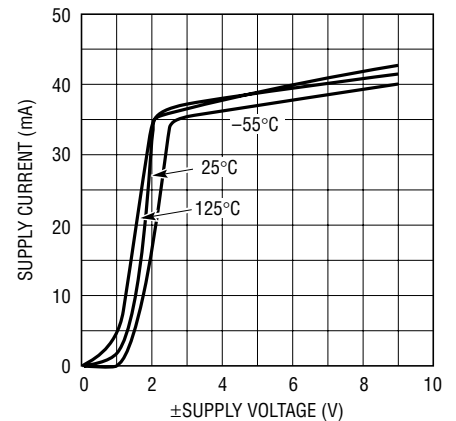
LT1193 • TPC04

Equivalent Input Noise Current vs Frequency



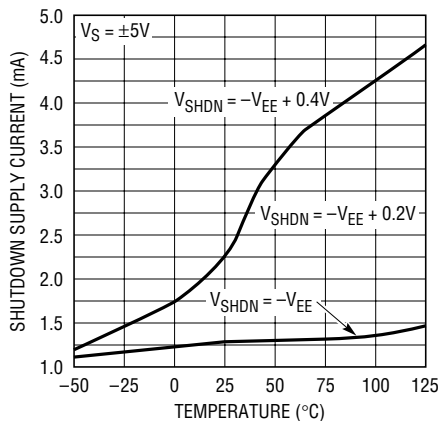
LT1193 • TPC05

Supply Current vs Supply Voltage



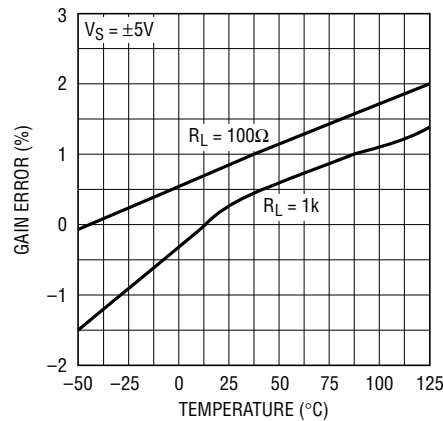
LT1193 • TPC06

Shutdown Supply Current vs Temperature



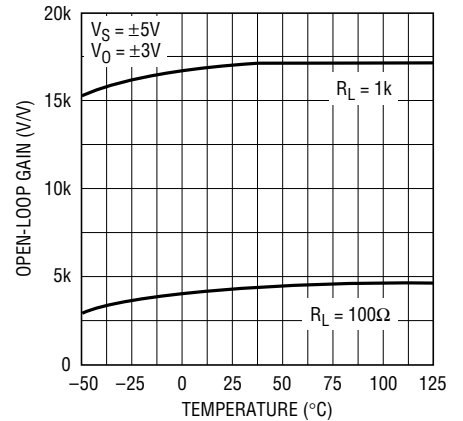
LT1193 • TPC07

Gain Error vs Temperature



LT1193 • TPC08

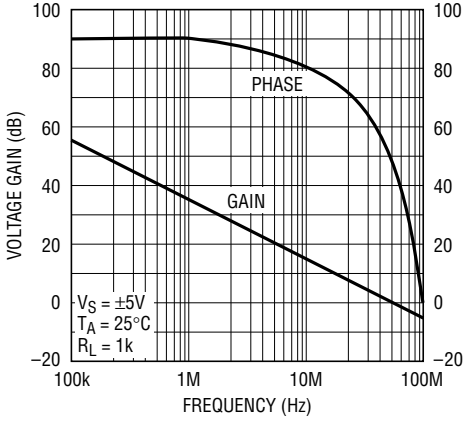
Open-Loop Gain vs Temperature



LT1193 • TPC09

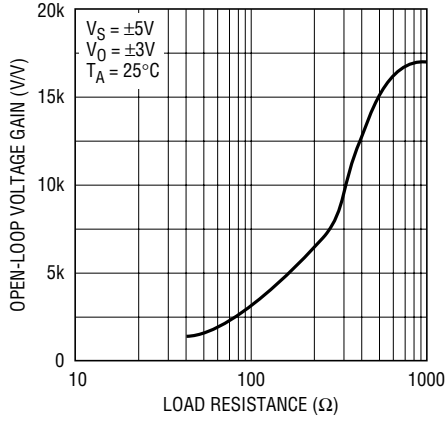
TYPICAL PERFORMANCE CHARACTERISTICS

Gain, Phase vs Frequency



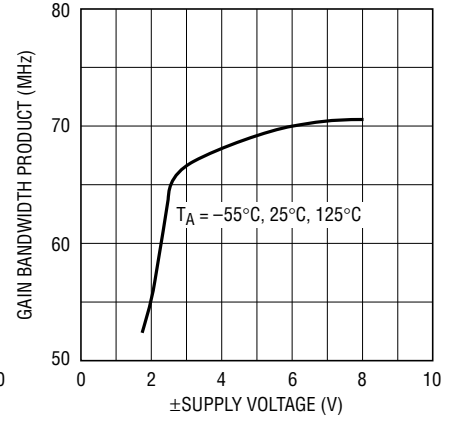
LT1193 • TPC11

Open-Loop Voltage Gain vs Load Resistance



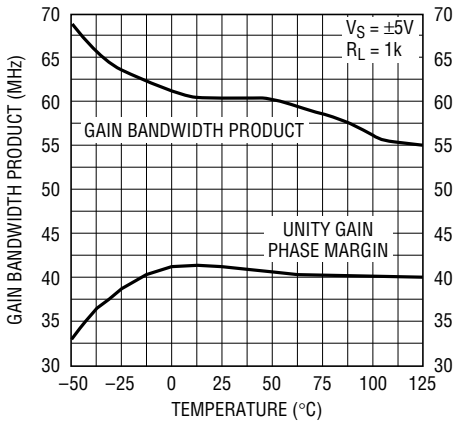
LT1193 • TPC10

Gain Bandwidth Product vs Supply Voltage



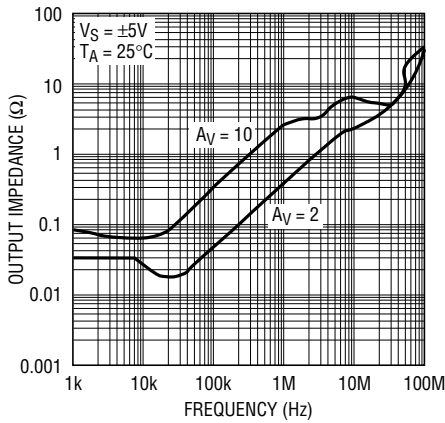
LT1193 • TPC12

Gain Bandwidth Product and Unity Gain Phase Margin vs Temperature



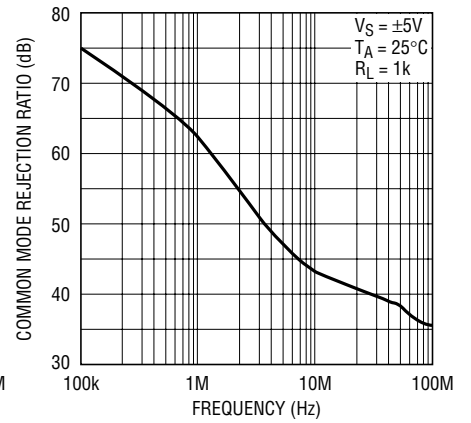
LT1193 • TPC13

Output Impedance vs Frequency



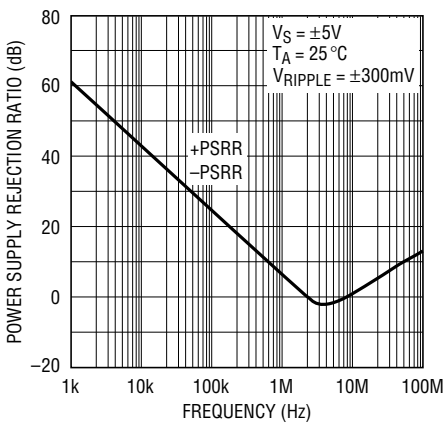
LT1193 • TPC14

Common Mode Rejection Ratio vs Frequency



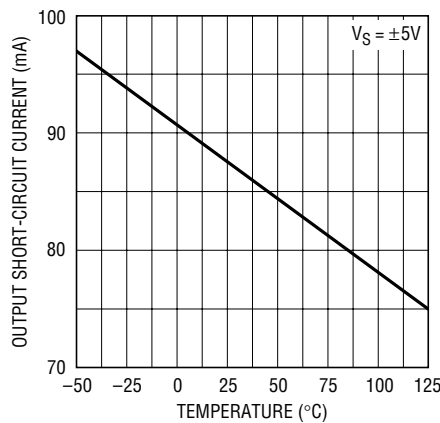
LT1193 • TPC15

Power Supply Rejection Ratio vs Frequency



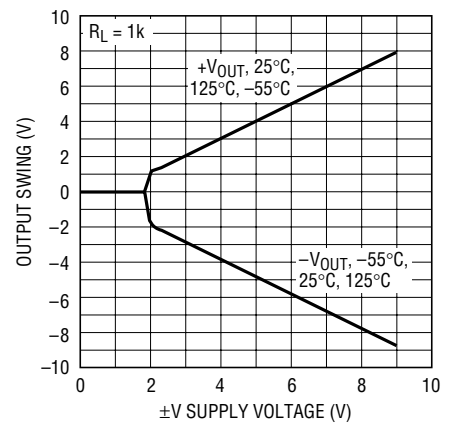
LT1193 • TPC16

Output Short-Circuit Current vs Temperature



LT1193 • TPC17

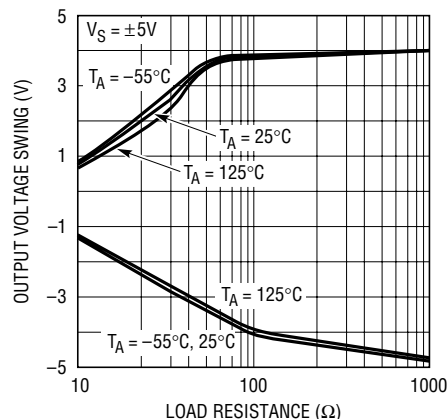
Output Swing vs Supply Voltage



LT1193 • TPC18

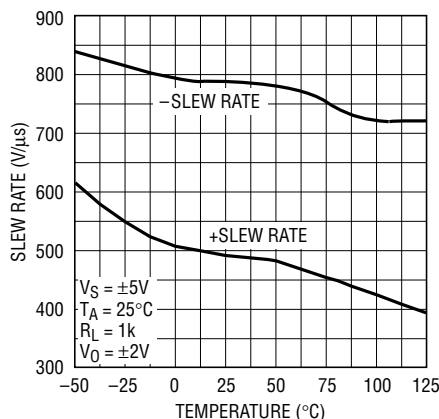
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Swing vs Load Resistance



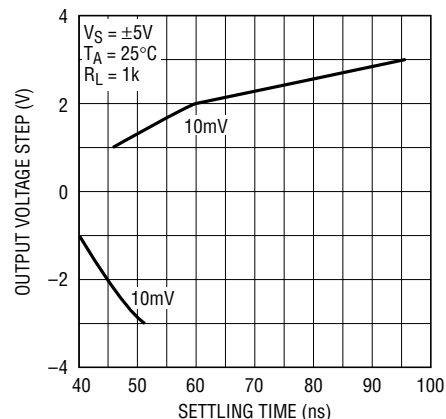
LT1193 • TPC19

Slew Rate vs Temperature



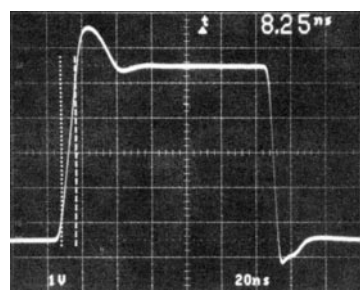
LT1193 • TPC20

Output Voltage Step vs Settling Time, $A_V = 2$



LT1193 • TPC21

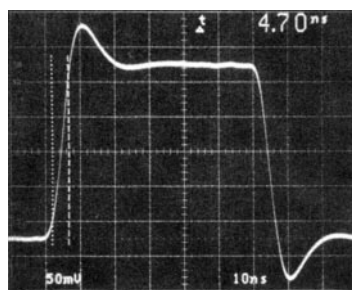
Large-Signal Transient Response



LT1193 • TPC22

$A_V = 2$, $R_L = 150\Omega$, $R_{FB} = 300\Omega$, $R_G = 300\Omega$

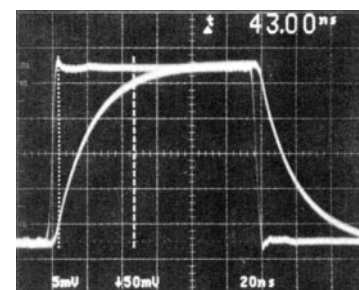
Small-Signal Transient Response



LT1193 • TPC23

$A_V = -10$, SMALL-SIGNAL RISE TIME = 43ns

Small-Signal Transient Response



LT1193 • TPC24

$A_V = 2$, $R_{FB} = 300\Omega$, $R_G = 300\Omega$,
OVERSHOOT = 25%, RISE TIME = 4.7ns

APPLICATIONS INFORMATION

The LT1193 is a video difference amplifier which has two uncommitted high input impedance (+) and (-) inputs. The amplifier has one set of inputs that can be used for reference and feedback. Additionally, this set of inputs give gain adjust and DC control to the differential amplifier. The voltage gain of the LT1193 is set like a conventional operational amplifier. Feedback is applied to Pin 8 and it is optimized for gains of 2 or greater. The amplifier can be operated single-ended by connecting either the (+) or (-) inputs to +/REF, Pin 1. The voltage gain is set by the resistors: $(R_{FB} + R_G)/R_G$.

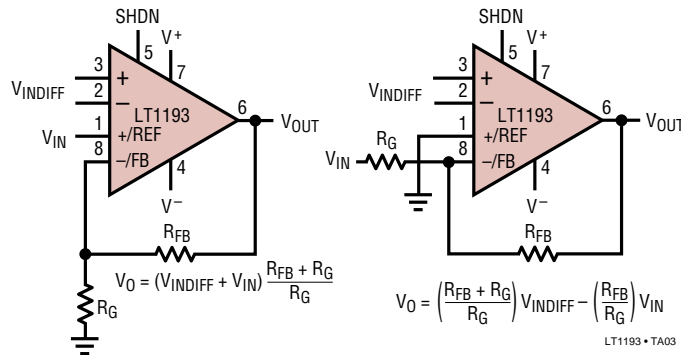
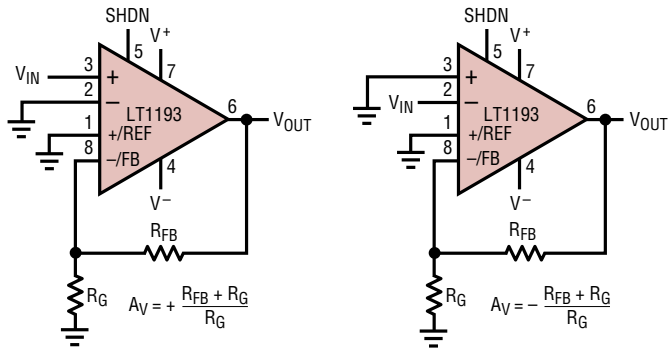
The primary usefulness of the LT1193 is in converting high speed differential signals to a single-ended output. The amplifier has common mode rejection beyond 50MHz

and a full-power bandwidth of 40MHz at 4V_{p-p}. Like the single-ended case, the differential voltage gain is set by the external resistors: $(R_{FB} + R_G)/R_G$. The maximum input differential signal for which the output will respond is approximately $\pm 1.3V$.

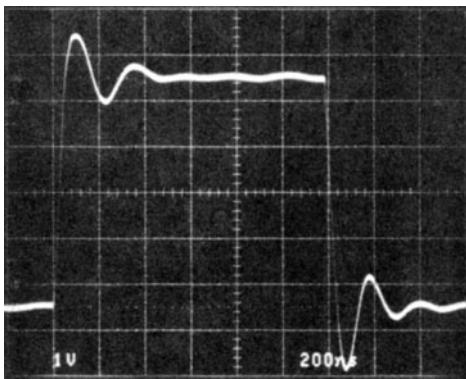
Power Supply Bypassing

The LT1193 is quite tolerant of power supply bypassing. In some applications a 0.1 μF ceramic disc capacitor placed 1/2 inch from the amplifier is all that is required. A scope photo of the amplifier output with no supply bypassing is used to demonstrate this bypassing tolerance, $R_L = 1k$.

APPLICATIONS INFORMATION



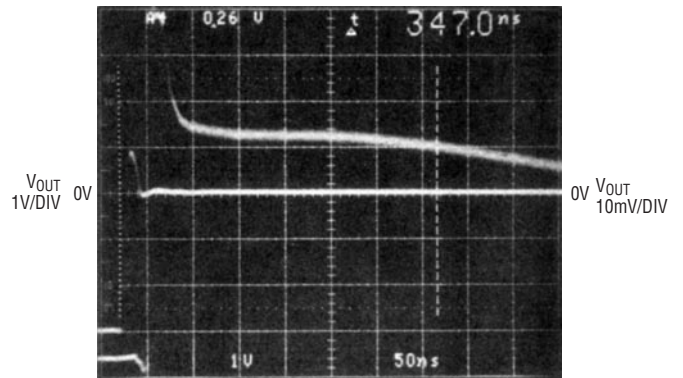
No Supply Bypass Capacitors



$A_V = 10$, IN DEMO BOARD, $R_L = 1k$

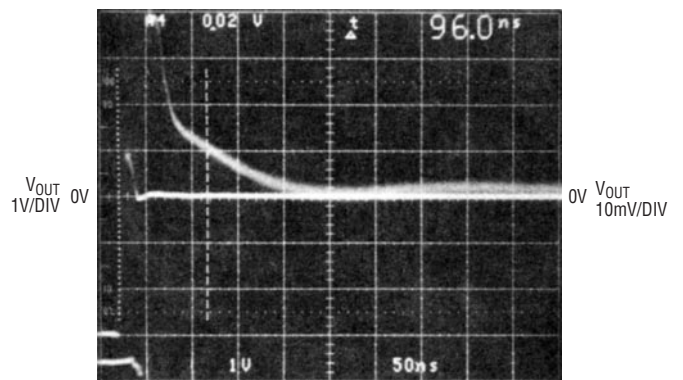
In many applications and those requiring good settling time it is important to use multiple bypass capacitors. A $0.1\mu F$ ceramic disc in parallel with a $4.7\mu F$ tantalum is recommended. Two oscilloscope photos with different bypass conditions are used to illustrate the settling time characteristics of the amplifier. Note that although the output waveform looks acceptable at 1V/DIV, when amplified to 10mV/DIV the settling time to 10mV is 347ns for the $0.1\mu F$ bypass; the time drops to 96ns with multiple bypass capacitors.

Settling Time Poor Bypass



SETTLING TIME TO 10mV, $A_V = 2$
SUPPLY BYPASS CAPACITORS = $0.1\mu F$

Settling Time Good Bypass



SETTLING TIME TO 10mV, $A_V = 2$
SUPPLY BYPASS CAPACITORS = $0.1\mu F + 4.7\mu F$ TANTALUM

Operating With Low Closed-Loop Gains

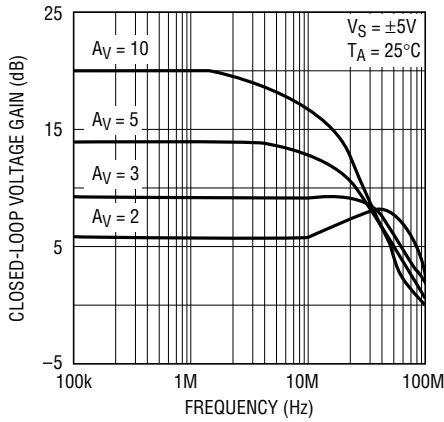
The LT1193 has been optimized for closed-loop gains of 2 or greater; the frequency response illustrates the obtainable closed-loop bandwidths. For a closed-loop gain of 2 the response peaks about 2dB. Peaking can be minimized by keeping the feedback elements below $1k\Omega$, and can be eliminated by placing a capacitor across the feedback resistor, (feedback zero). This peaking shows up as time domain overshoot of about 40%. With the feedback capacitor it is eliminated.

Cable Terminations

The LT1193 video difference amplifier has been optimized as a low cost cable driver. The $\pm 50mA$ guaranteed output current enables the LT1193 to easily deliver $7.5V_{P-P}$ into

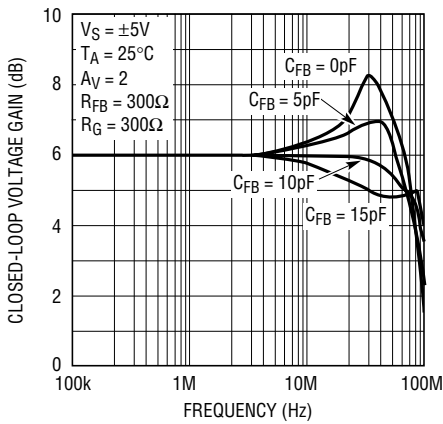
APPLICATIONS INFORMATION

Closed-Loop Voltage Gain vs Frequency



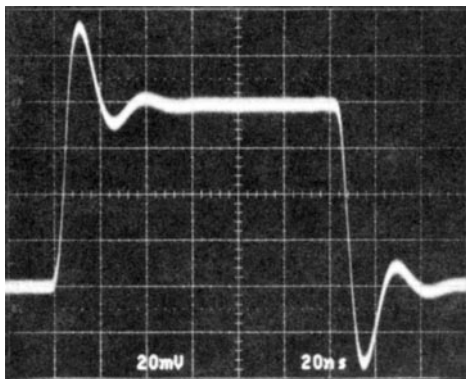
LT1193 • TA07

Closed-Loop Voltage Gain vs Frequency



LT1193 • TA08

Small-Signal Transient Response

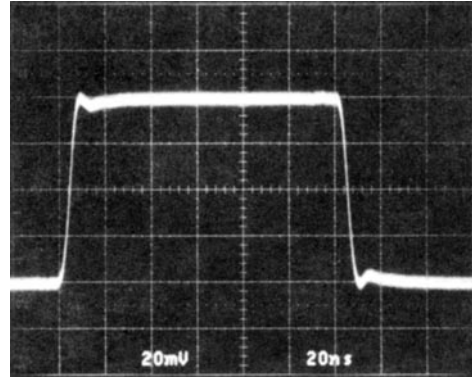


LT1193 • TA09

$A_V = 2$, OVERSHOOT = 40%, $R_{FB} = 1k$, $R_G = 1k$

100Ω, while operating on ±5V supplies and gains >3. On a single 5V supply, the LT1193 can swing 2.6V_{P-P} for gains ≥2.

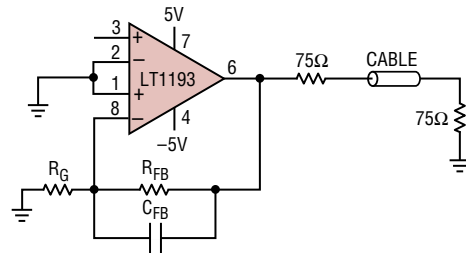
Small-Signal Transient Response



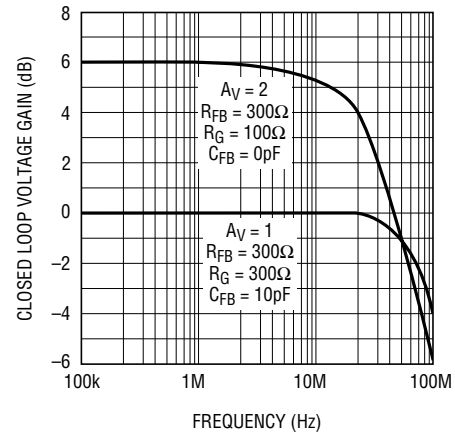
LT1193 • TA10

$A_V = 2$ WITH 8pF FEEDBACK CAPACITOR
RISE TIME = 3.75ns, $R_{FB} = 1k$, $R_G = 1k$

Double Terminated Cable Driver



Closed-Loop Voltage Gain vs Frequency



LT1193 • TA11

When driving a cable it is important to terminate the cable to avoid unwanted reflections. This can be done in one of two ways: single termination or double termination. With single termination, the cable must be terminated at the receiving end (75Ω to ground) to absorb unwanted energy. The best performance can be obtained by double termination (75Ω in series with the output of the amplifier, and 75Ω to ground at the other end of the cable). This

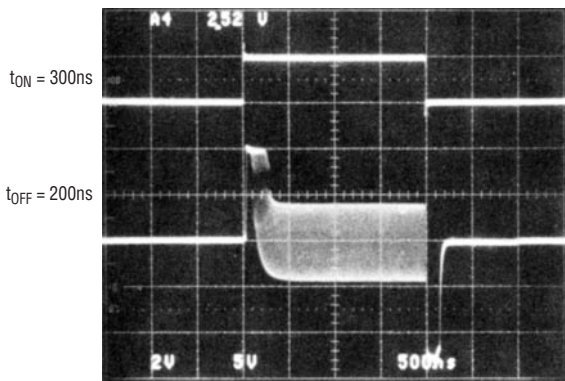
APPLICATIONS INFORMATION

termination is preferred because reflected energy is absorbed at each end of the cable. When using the double termination technique it is important to note that the signal is attenuated by a factor of 2, or 6dB. The cable driver has a -3dB bandwidth of 80MHz while driving a 150Ω load.

Using the Shutdown Feature

The LT1193 has a unique feature that allows the amplifier to be shut down for conserving power or for multiplexing several amplifiers onto a common cable. The amplifier will shut down by taking Pin 5 to V^- . In shutdown, the amplifier dissipates 15mW while maintaining a true high impedance output state of $15\text{k}\Omega$ in parallel with the feedback resistors. The amplifiers may be connected inverting, noninverting or differential for MUX applications. When the output is loaded with as little as $1\text{k}\Omega$ from the amplifier's feedback resistors, the amplifier shuts off in 200ns . This shutoff can be under the control of HC CMOS operating between 0V and -5V .

Output Shutdown



1MHz SINE WAVE GATED OFF WITH SHUTDOWN PIN, $A_V = 3$, $R_{FB} = 1\text{k}$, $R_G = 500\Omega$

The ability to maintain shutoff is shown on the curve Shutdown Supply Current vs Temperature in the Typical Performance Characteristics section. At very high elevated temperatures it is important to hold the SHDN pin close to the negative supply to keep the supply current from increasing.

Murphy Circuits

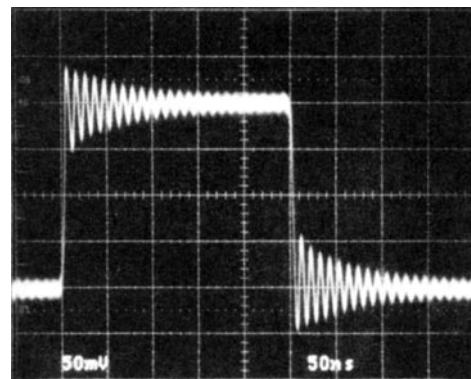
There are several precautions the user should take when using the LT1193 in order to realize its full capability. Although the LT1193 can drive a 30pF in gains as low as 2,

isolating the capacitance with 10Ω can be helpful. Precautions primarily have to do with driving large capacitive loads.

Other precautions include:

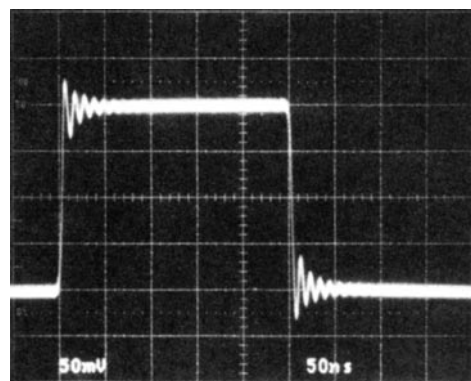
1. Use a ground plane (see Design Note 50, High Frequency Amplifier Evaluation Board).
2. Do not use high source impedances. The input capacitance of 2pF , and $R_S = 10\text{k}$ for instance, will give an $8\text{MHz} - 3\text{dB}$ bandwidth.
3. PC board socket may reduce stability.
4. A feedback resistor of 1k or lower reduces the effects of stray capacitance at the inverting input. (For instance, closed-loop gain of ± 2 can use $R_{FB} = 300\Omega$ and $R_G = 300\Omega$.)

Driving Capacitive Load



$A_V = 2$, IN DEMO BOARD, $C_L = 30\text{pF}$, $R_{FB} = 1\text{k}$, $R_G = 1\text{k}$

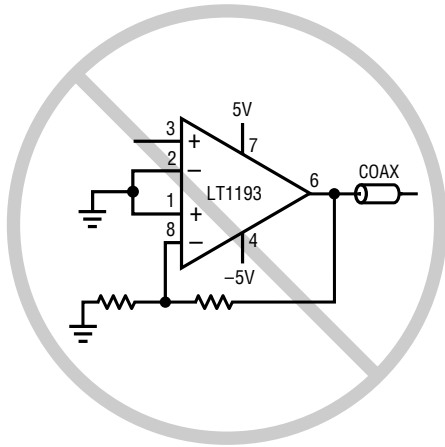
Driving Capacitive Load



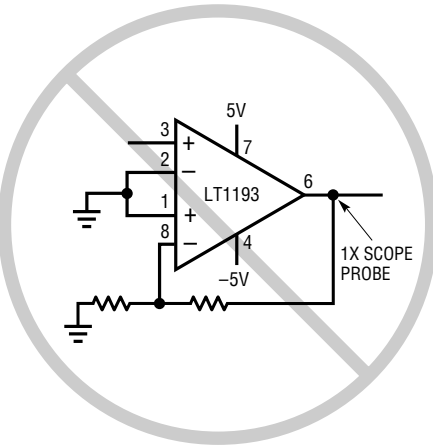
$A_V = 2$, IN DEMO BOARD, $C_L = 30\text{pF}$ WITH 10Ω ISOLATING RESISTOR

APPLICATIONS INFORMATION

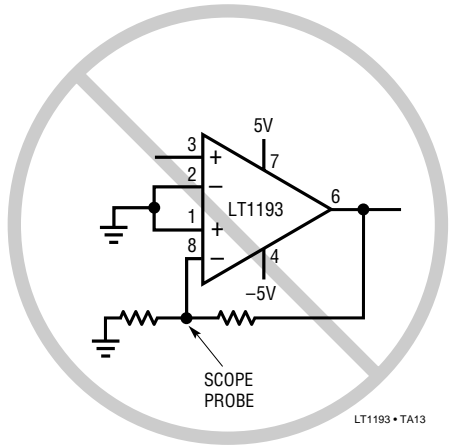
Murphy Circuits



An unterminated cable is a large capacitive load



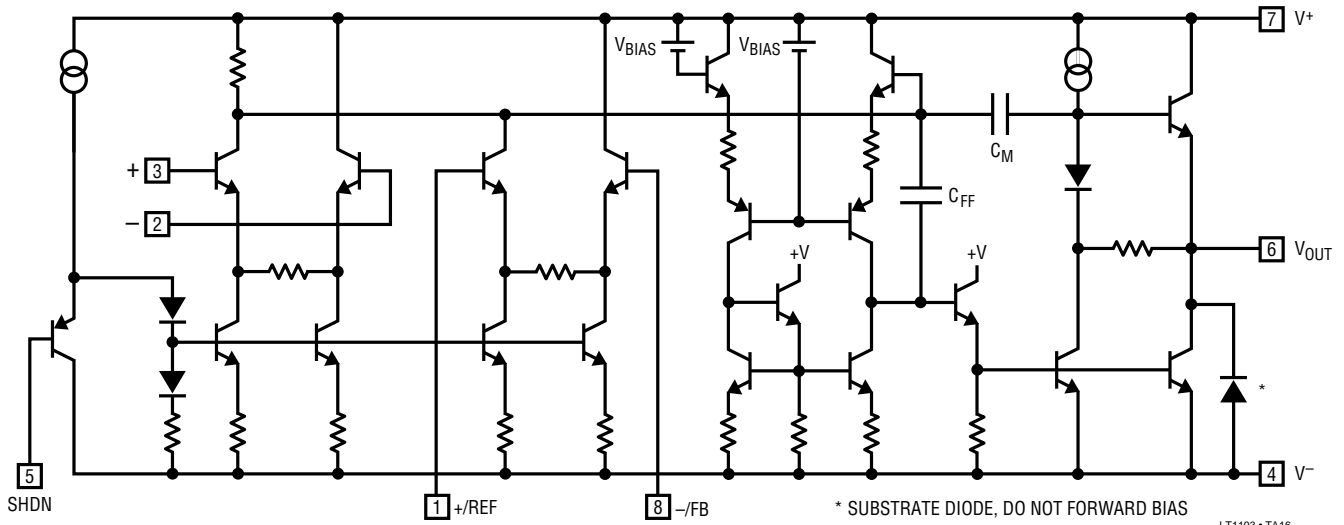
A 1X scope probe is a large capacitive load



A scope probe on the inverting input reduces phase margin

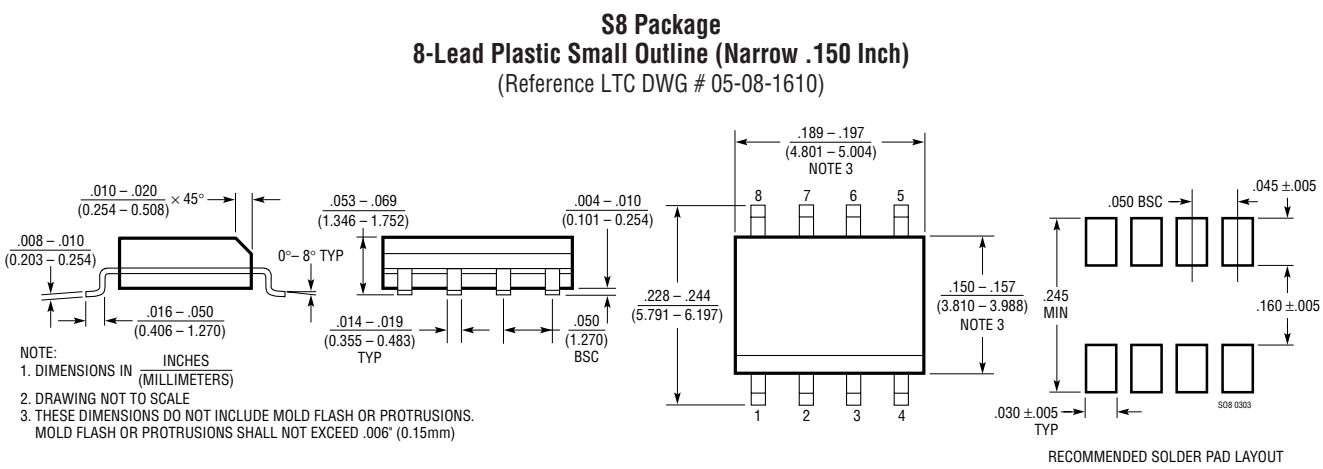
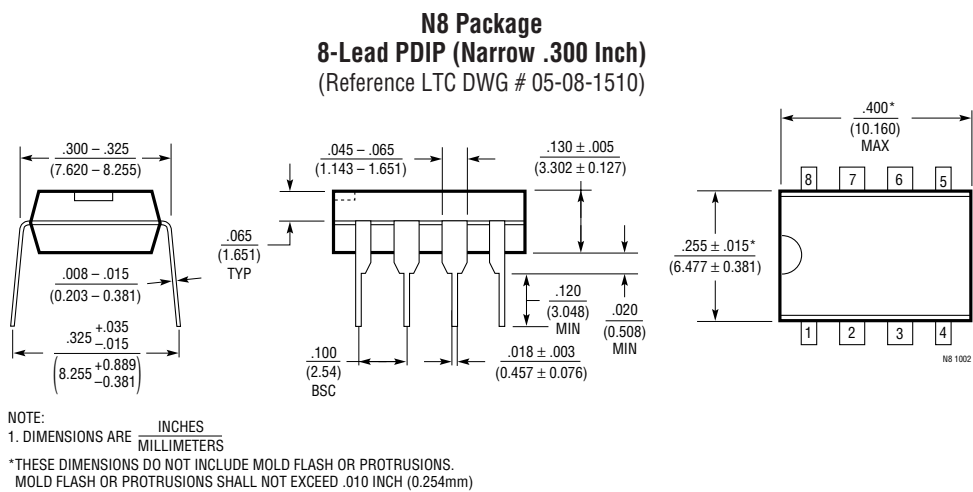
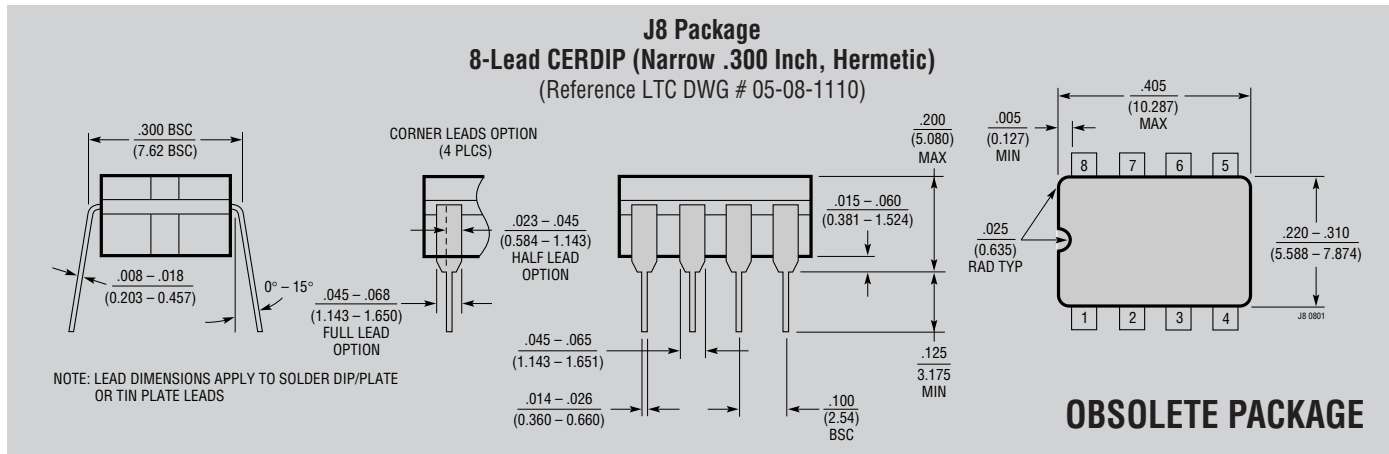
LT1193 • TA13

SIMPLIFIED SCHEMATIC



LT1193 • TA16

PACKAGE DESCRIPTION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1194	Video Difference Amp	A _V = 10 Version of the LT1193

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