



**THE DATASHEET OF
TL331IDBVRQ1**

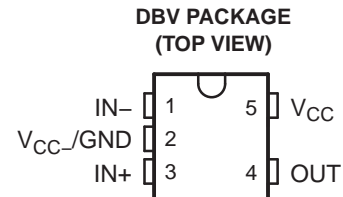


SINGLE DIFFERENTIAL COMPARATOR

 Check for Samples: [TL331-Q1](#)

FEATURES

- Qualified for Automotive Applications
- Single Supply or Dual Supplies
- Wide Range of Supply Voltage: 2 V to 36 V
- Low Supply-Current Drain Independent of Supply Voltage: 0.4 mA Typ.
- Low Input Bias Current: 25 nA Typ.
- Low Input Offset Voltage: 2 mV Typ.
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: ± 36 V
- Low Output Saturation Voltage
- Output Compatible With TTL, MOS, and CMOS



DESCRIPTION AND ORDERING INFORMATION

This device consists of a single voltage comparator designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible if the difference between the two supplies is 2 V to 36 V and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. To achieve wired-AND relationships, one can connect the output to other open-collector outputs.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOT-23 – DBV	Reel of 3000	TL331IDBVRQ1	TQ1U
-40°C to 125°C	SOT-23 – DBV	Reel of 3000	TL331QDBVRQ1	T1RU

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

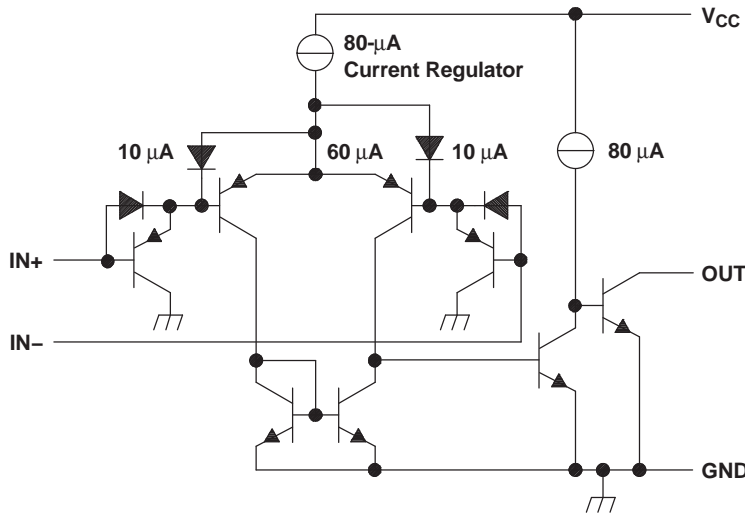


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LOGIC DIAGRAM



SCHEMATIC



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	1
Transistors	20

Note: Current values shown are nominal.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage ⁽²⁾	36 V
V_{ID}	Differential input voltage ⁽³⁾	± 36 V
V_I	Input voltage range (either input)	-0.3 V to 36 V
V_O	Output voltage	36 V
I_O	Output current	20 mA
	Duration of output short-circuit to ground ⁽⁴⁾	Unlimited
T_J	Operating virtual junction temperature	150°C
T_{stg}	Storage temperature range	-65°C to 150°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TL331-Q1	
		DBV	
		5 PINS	
		UNIT	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	218.3 °C/W	
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽³⁾	87.3 °C/W	
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	44.9 °C/W	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	4.3 °C/W	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	44.1 °C/W	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	N/A °C/W	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{CC} = 5\text{ V}$ to 30 V , $V_O = 1.4\text{ V}$, $V_{IC} = V_{IC(min)}$	25°C		2	5	mV
			–40°C to 125°C			9	
I_{IO}	Input offset current	$V_O = 1.4\text{ V}$	25°C		5	50	nA
			–40°C to 125°C			250	
I_{IB}	Input bias current	$V_O = 1.4\text{ V}$	25°C		–25	–250	nA
			–40°C to 125°C			–400	
V_{ICR}	Common-mode input voltage range ⁽²⁾		25°C	0 to $V_{CC} - 1.5$			V
			–40°C to 125°C	0 to $V_{CC} - 2$			
A_{VD}	Large-signal differential-voltage amplification	$V_{CC} = 15\text{ V}$, $V_O = 1.4\text{ V}$ to 11.4 V , $R_L \geq 15\text{ k}\Omega$ to V_{CC}	25°C	50	200		V/mV
I_{OH}	High-level output current	$V_{OH} = 5\text{ V}$, $V_{ID} = 1\text{ V}$	25°C		0.1	50	nA
		$V_{OH} = 30\text{ V}$, $V_{ID} = 1\text{ V}$	–40°C to 125°C			1	μA
V_{OL}	Low-level output voltage	$I_{OL} = 4\text{ mA}$, $V_{ID} = -1\text{ V}$	25°C		150	400	mV
			–40°C to 125°C			700	
I_{OL}	Low-level output current	$V_{OL} = 1.5\text{ V}$, $V_{ID} = -1\text{ V}$	25°C	6			mA
I_{CC}	Supply current	$R_L = \infty$, $V_{CC} = 5\text{ V}$	25°C		0.4	0.7	mA

- (1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$ at 25°C, but either or both inputs can go to 30 V without damage.

SWITCHING CHARACTERISTICS

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
Response time	R_L connected to 5 V through 5.1 k Ω , $C_L = 15\text{ pF}$ ^{(1) (2)}	100-mV input step with 5-mV overdrive	1.3
		TTL-level input step	0.3

- (1) C_L includes probe and jig capacitance.
- (2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

REVISION HISTORY

Changes from Revision B (September 2012) to Revision C	Page
• Added a Thermal Information table	3
• Changed V_{ICR} in the Electrical Characteristics	3
• Changed test conditions of I_{OL} in the Electrical Characteristics	3

Changes from Revision A (July 2010) to Revision B	Page
• Changed V_{ICR} in the Electrical Characteristics	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TL331IDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TQ1U	Samples
TL331QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1RU	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL331-Q1 :

- Catalog: [TL331](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL331IDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

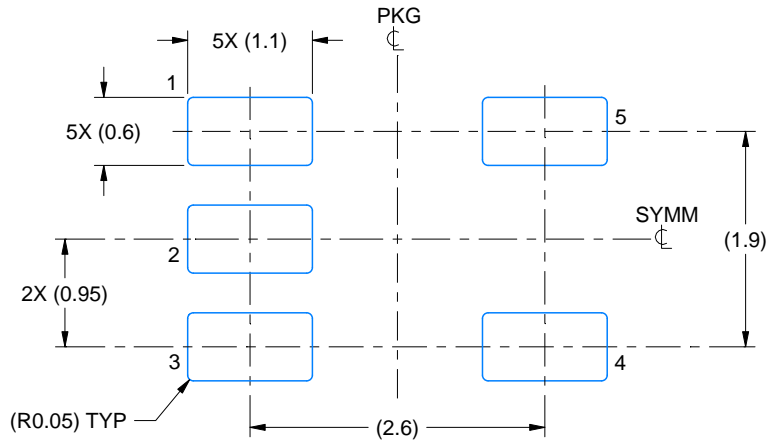
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL331IDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0
TL331QDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0

EXAMPLE BOARD LAYOUT

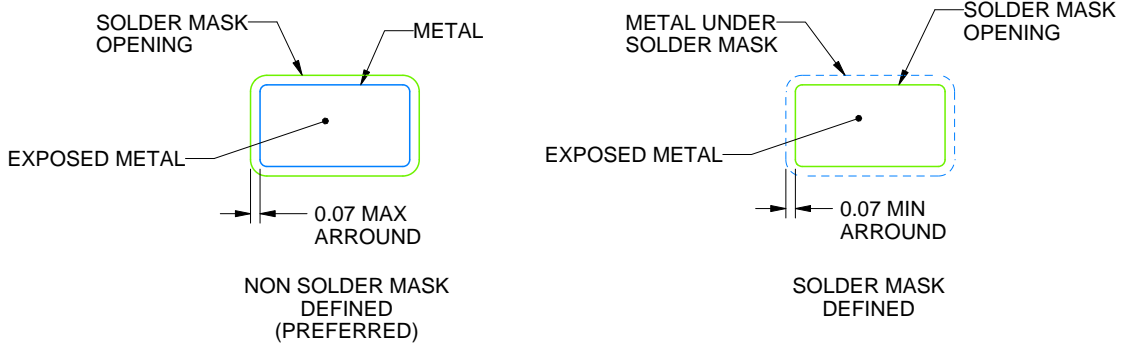
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

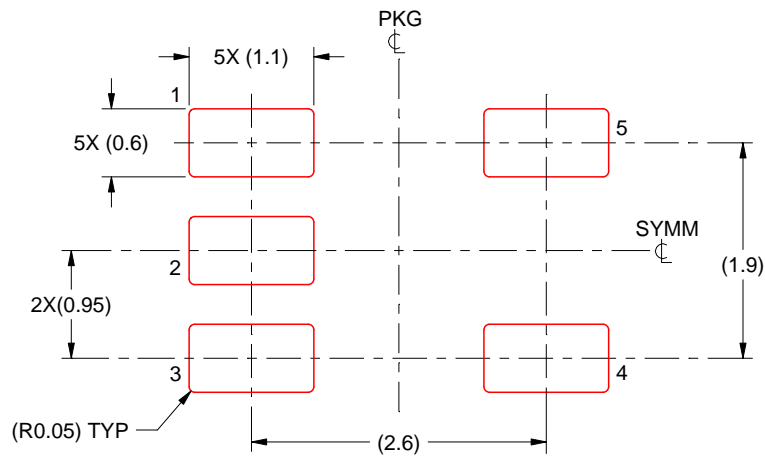
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View TL331IDBVRQ1 on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management