



THE DATASHEET OF CD74HC192PWT



Features

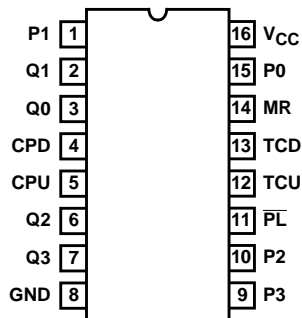
- Synchronous Counting and Asynchronous Loading
- Two Outputs for N-Bit Cascading
- Look-Ahead Carry for High-Speed Counting
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The 'HC192, 'HC193 and 'HCT193 are asynchronously presettable BCD Decade and Binary Up/Down synchronous counters, respectively.

Pinout

CD54HC192, CD54HC193, CD54HCT193 (CERDIP)
 CD74HC192 (PDIP, SOP, TSSOP)
 CD74HC193 (PDIP, SOIC)
 CD74HCT193 (PDIP)
 TOP VIEW



Presetting the counter to the number on the preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input (\overline{PL}). The counter is incremented on the low-to-high transition of the Clock-Up input (and a high level on the Clock-Down input) and decremented on the low to high transition of the Clock-Down input (and a high level on the Clock-up input). A high level on the MR input overrides any other input to clear the counter to its zero state. The Terminal Count up (carry) goes low half a clock period before the zero count is reached and returns to a high level at the zero count. The Terminal Count Down (borrow) in the count down mode likewise goes low half a clock period before the maximum count (9 in the 192 and 15 in the 193) and returns to high at the maximum count. Cascading is effected by connecting the carry and borrow outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

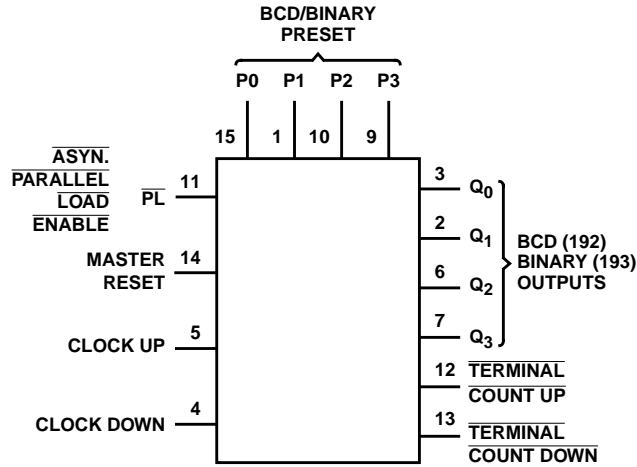
If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|---------------|------------------|--------------|
| CD54HC192F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HC193F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HCT193F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC192E | -55 to 125 | 16 Ld PDIP |
| CD74HC192NSR | -55 to 125 | 16 Ld SOP |
| CD74HC192PW | -55 to 125 | 16 Ld TSSOP |
| CD74HC192PWR | -55 to 125 | 16 Ld TSSOP |
| CD74HC192PWT | -55 to 125 | 16 Ld TSSOP |
| CD74HC193E | -55 to 125 | 16 Ld PDIP |
| CD74HC193M | -55 to 125 | 16 Ld SOIC |
| CD74HC193MT | -55 to 125 | 16 Ld SOIC |
| CD74HC193M96 | -55 to 125 | 16 Ld SOIC |
| CD74HCT193E | -55 to 125 | 16 Ld PDIP |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

Functional Diagram



TRUTH TABLE

| CLOCK UP | CLOCK DOWN | RESET | PARALLEL LOAD | FUNCTION |
|----------|------------|-------|---------------|--------------------|
| ↑ | H | L | H | Count Up |
| H | ↑ | L | H | Count Down |
| X | X | H | X | Reset |
| X | X | L | L | Load Preset Inputs |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level

CD54/74HC192, CD54/74HC193, CD54/74HCT193

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC V_{CC} or Ground Current, I_{CC} or I_{GND} | $\pm 50mA$ |

Thermal Information

| | |
|--|----------------|
| Package Thermal Impedance, θ_{JA} (see Note 1): | |
| E (PDIP) Package | 67°C/W |
| M (SOIC) Package | 73°C/W |
| NS (SOP) Package | 64°C/W |
| PW (TSSOP) Package | 108°C/W |
| Maximum Junction Temperature | 150°C |
| Maximum Storage Temperature Range | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C |
| (SOIC - Lead Tips Only) | |

Operating Conditions

| | |
|---|----------------|
| Temperature Range (T_A) | -55°C to 125°C |
| Supply Voltage Range, V_{CC} | |
| HC Types | .2V to 6V |
| HCT Types | 4.5V to 5.5V |
| DC Input or Output Voltage, V_I , V_O | 0V to V_{CC} |
| Input Rise and Fall Time | |
| 2V | 1000ns (Max) |
| 4.5V | 500ns (Max) |
| 6V | 400ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|----------|-------------------------|------------|--------------|------|-----|-----------|---------------|---------|----------------|---------|---------|
| | | V_I (V) | I_O (mA) | V_{CC} (V) | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | V_{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I_I | V_{CC} or GND | 0 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Quiescent Device Current | I_{CC} | V_{CC} or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | μA |
| | | | - | 6 | - | - | ± 0.1 | - | ± 1 | - | ± 1 | μA |

CD54/74HC192, CD54/74HC193, CD54/74HCT193

DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|------------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
| | | V _I (V) | I _O (mA) | V _{CC} (V) | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HCT TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | V _{OH} | V _{IH} or V _{IL} | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | V _{OL} | V _{IH} or V _{IL} | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I _I | V _{CC} to GND | - | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | - | 5.5 | - | - | 8 | - | 80 | - | 160 | μA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI _{CC} (Note 2) | V _{CC} - 2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | μA |

NOTE:

- For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

| INPUT | UNIT LOADS |
|----------|------------|
| P0-P3 | 0.4 |
| MR | 1.45 |
| PL | 0.85 |
| CPU, CPD | 1.45 |

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360μA max at 25°C.

CD54/74HC192, CD54/74HC193, CD54/74HCT193

Prerequisite For Switching Specifications

| PARAMETER | SYMBOL | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|------------------|------------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | |
| Pulse Width CPU, CPD 192 | t _W | 2 | 115 | - | - | 145 | - | 175 | - | ns |
| | | 4.5 | 23 | - | - | 29 | - | 35 | - | ns |
| | | 6 | 20 | - | - | 25 | - | 30 | - | ns |
| CPU, CPD 193 | t _W | 2 | 100 | - | - | 125 | - | 150 | - | ns |
| | | 4.5 | 20 | - | - | 25 | - | 30 | - | ns |
| | | 6 | 17 | - | - | 21 | - | 26 | - | ns |
| \overline{PL} | t _W | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| MR | t _W | 2 | 100 | - | - | 125 | - | 150 | - | ns |
| | | 4.5 | 20 | - | - | 25 | - | 30 | - | ns |
| | | 6 | 17 | - | - | 21 | - | 26 | - | ns |
| Set-up Time Pn to \overline{PL} | t _{SU} | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| Hold Time Pn to \overline{PL} | t _H | 2 | 0 | - | - | 0 | - | 0 | - | ns |
| | | 4.5 | 0 | - | - | 0 | - | 0 | - | ns |
| | | 6 | 0 | - | - | 0 | - | 0 | - | ns |
| Hold Time CPD to CPU or CPU to CPD | t _H | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| Recovery Time \overline{PL} to CPU, CPD | t _{REC} | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| MR to CPU, CPD | t _{REC} | 2 | 5 | - | - | 5 | - | 5 | - | ns |
| | | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |
| | | 6 | 5 | - | - | 5 | - | 5 | - | ns |
| Maximum Frequency CPU, CPD 192 | f _{MAX} | 2 | 5 | - | - | 4 | - | 3 | - | MHz |
| | | 4.5 | 22 | - | - | 18 | - | 15 | - | MHz |
| | | 6 | 24 | - | - | 21 | - | 18 | - | MHz |
| CPU, CPD 193 | f _{MAX} | 2 | 5 | - | - | 4 | - | 3 | - | MHz |
| | | 4.5 | 25 | - | - | 20 | - | 17 | - | MHz |
| | | 6 | 29 | - | - | 24 | - | 20 | - | MHz |
| HCT TYPES | | | | | | | | | | |
| Pulse Width CPU, CPD 192 | t _W | 2 | - | - | - | - | - | - | - | ns |
| | | 4.5 | 23 | - | - | 29 | - | 35 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| CPU, CPD 193 | t _W | 2 | - | - | - | - | - | - | - | ns |
| | | 4.5 | 23 | - | - | 29 | - | 35 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |

CD54/74HC192, CD54/74HC193, CD54/74HCT193

Prerequisite For Switching Specifications (Continued)

| PARAMETER | SYMBOL | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|------------------|------------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| \overline{PL} | t _W | 2 | - | - | - | - | - | - | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| MR | t _W | 2 | - | - | - | - | - | - | - | ns |
| | | 4.5 | 20 | - | - | 25 | - | 30 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| Set-up Time P _n to \overline{PL} | t _{SU} | 2 | - | - | - | - | - | - | - | ns |
| | | 4.5 | 15 | - | - | 19 | - | 22 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| Hold Time P _n to \overline{PL} | t _H | 2 | - | - | - | - | - | - | - | ns |
| | | 4.5 | 0 | - | - | 0 | - | 0 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| Hold Time CPD to CPU or CPU to CPD | t _H | 2 | - | - | - | - | - | - | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| Recovery Time \overline{PL} to CPU, CPD | t _{REC} | 2 | - | - | - | - | - | - | - | ns |
| | | 4.5 | 15 | - | - | 19 | - | 22 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| MR to CPU, CPD | t _{REC} | 2 | - | - | - | - | - | - | - | ns |
| | | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |
| | | 6 | - | - | - | - | - | - | - | ns |
| Maximum Frequency CPU, CPD 192 | f _{MAX} | 2 | - | - | - | - | - | - | - | MHz |
| | | 4.5 | 22 | - | - | 18 | - | 15 | - | MHz |
| | | 6 | - | - | - | - | - | - | - | MHz |
| CPU, CPD 193 | f _{MAX} | 2 | - | - | - | - | - | - | - | MHz |
| | | 4.5 | 22 | - | - | 18 | - | 15 | - | MHz |
| | | 6 | - | - | - | - | - | - | - | MHz |

Switching Specifications Input t_r, t_f = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|-------------------------------------|-----------------------|------------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | |
| Propagation Delay CPU to \overline{TCU} | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 125 | - | 155 | - | 190 | ns |
| | | C _L = 50pF | 4.5 | - | - | 25 | - | 31 | - | 38 | ns |
| | | C _L = 15pF | 5 | - | 10 | - | - | - | - | - | ns |
| | | C _L = 50pF | 6 | - | - | 21 | - | 26 | - | 32 | ns |
| CPD to \overline{TCU} | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 125 | - | 155 | - | 190 | ns |
| | | C _L = 50pF | 4.5 | - | - | 25 | - | 31 | - | 38 | ns |
| | | C _L = 15pF | 5 | - | 10 | - | - | - | - | - | ns |
| | | C _L = 50pF | 6 | - | - | 21 | - | 26 | - | 32 | ns |
| CPU to Q _n | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 220 | - | 270 | - | 325 | ns |
| | | C _L = 50pF | 4.5 | - | - | 43 | - | 54 | - | 65 | ns |
| | | C _L = 15pF | 5 | - | 18 | - | - | - | - | - | ns |
| | | C _L = 50pF | 6 | - | - | 37 | - | 46 | - | 55 | ns |

CD54/74HC192, CD54/74HC193, CD54/74HCT193

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|-------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| CPD to Q _n | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 220 | - | 270 | - | 325 | ns |
| | | C _L = 50pF | 4.5 | - | - | 43 | - | 54 | - | 65 | ns |
| | | C _L = 15pF | 5 | - | 18 | - | - | - | - | - | ns |
| | | C _L = 50pF | 6 | - | - | 37 | - | 46 | - | 55 | ns |
| P _L to Q _n | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 220 | - | 275 | - | 330 | ns |
| | | C _L = 50pF | 4.5 | - | - | 44 | - | 55 | - | 66 | ns |
| | | C _L = 15pF | 5 | - | 18 | - | - | - | - | - | ns |
| | | C _L = 50pF | 6 | - | - | 37 | - | 47 | - | 56 | ns |
| MR to Q _n | t _{PHL} | C _L = 50pF | 2 | - | - | 200 | - | 250 | - | 300 | ns |
| | | C _L = 50pF | 4.5 | - | - | 40 | - | 50 | - | 60 | ns |
| | | C _L = 15pF | 5 | - | 17 | - | - | - | - | - | ns |
| | | C _L = 50pF | 6 | - | - | 34 | - | 43 | - | 51 | ns |
| Transition Time Q, TCU, TCD | t _{TLH} , t _{THL} | C _L = 50pF | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Input Capacitance | C _{IN} | C _L = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | C _{PD} | C _L = 15pF | 5 | - | 40 | - | - | - | - | - | pF |
| HCT TYPES | | | | | | | | | | | |
| Propagation Delay CPU to TCU | t _{PLH} , t _{PHL} | C _L = 50pF | 4.5 | - | - | 27 | - | 34 | - | 41 | ns |
| | | C _L = 15pF | 5 | - | 11 | - | - | - | - | - | ns |
| CPU to TCD | t _{PLH} , t _{PHL} | C _L = 50pF | 4.5 | - | - | 27 | - | 34 | - | 41 | ns |
| | | C _L = 15pF | 5 | - | 11 | - | - | - | - | - | ns |
| CPU to Q _n | t _{PLH} , t _{PHL} | C _L = 50pF | 4.5 | - | - | 40 | - | 50 | - | 60 | ns |
| | | C _L = 15pF | 5 | - | 17 | - | - | - | - | - | ns |
| CPD to Q _n | t _{PLH} , t _{PHL} | C _L = 50pF | 4.5 | - | - | 40 | - | 50 | - | 60 | ns |
| | | C _L = 15pF | 5 | - | 17 | - | - | - | - | - | ns |
| P _L to Q _n | t _{PLH} , t _{PHL} | C _L = 50pF | 4.5 | - | - | 46 | - | 58 | - | 69 | ns |
| | | C _L = 15pF | 5 | - | 21 | - | - | - | - | - | ns |
| MR to Q _n | t _{PHL} | C _L = 50pF | 4.5 | - | - | 43 | - | 54 | - | 65 | ns |
| | | C _L = 15pF | 5 | - | 18 | - | - | - | - | - | ns |
| Transition Time Q, TCU, TCD | t _{TLH} , t _{THL} | C _L = 50pF | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| Input Capacitance | C _{IN} | C _L = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | C _{PD} | C _L = 15pF | 5 | - | 50 | - | - | - | - | - | pF |

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per gate.
- $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

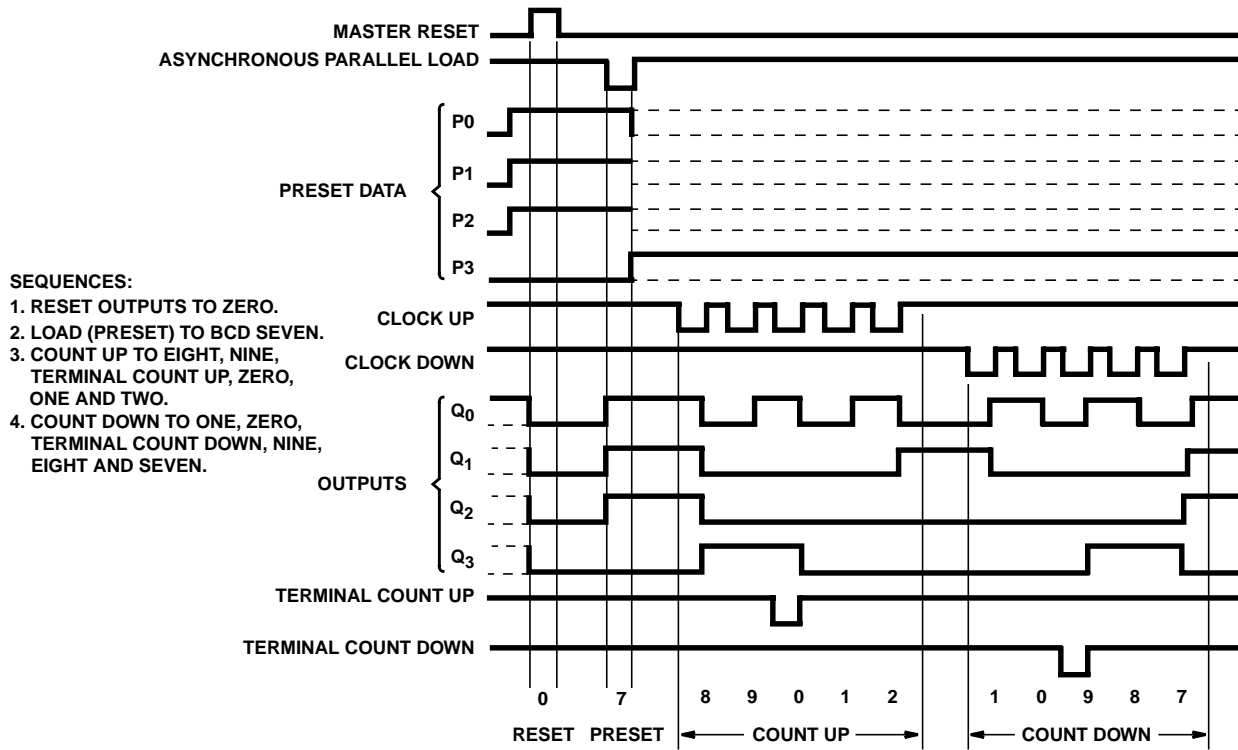


FIGURE 1. 'HC192 SYNCHRONOUS DECADE COUNTERS, TYPICAL RESET, PRESET AND COUNT SEQUENCES

Test Circuits and Waveforms (Continued)

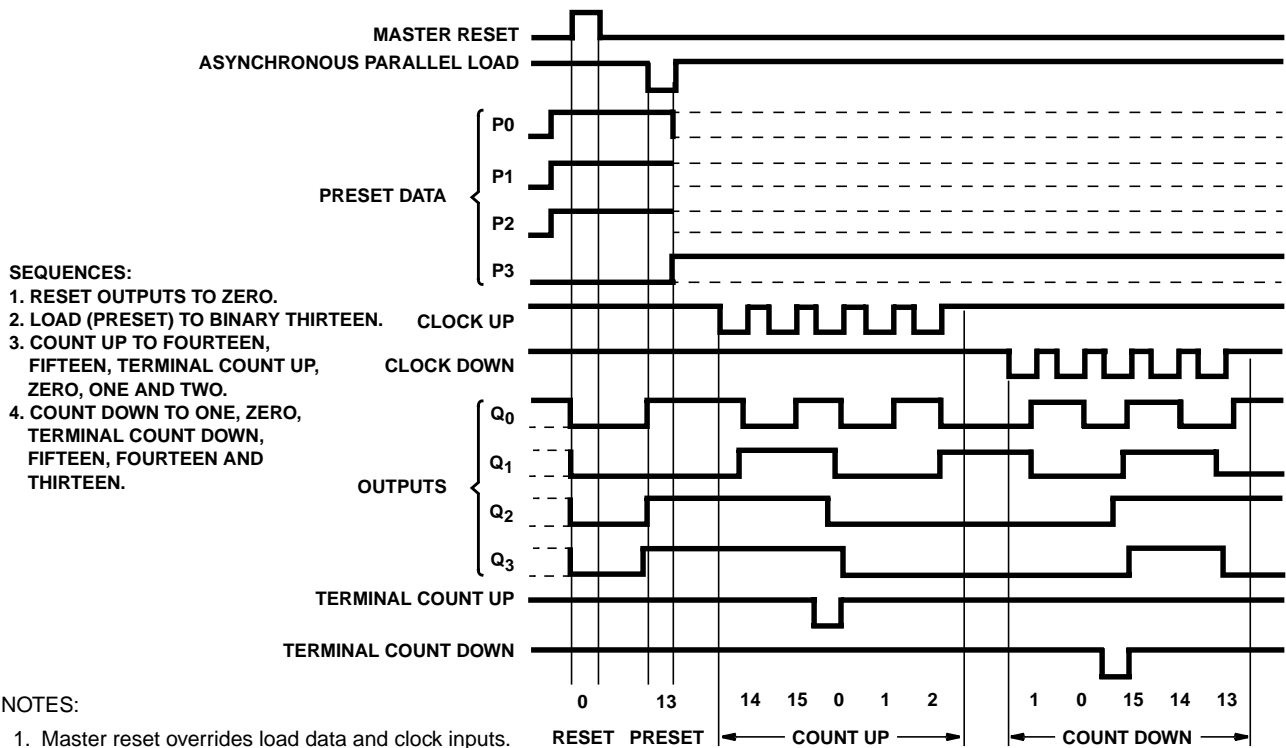


FIGURE 2. 'HC193 SYNCHRONOUS BINARY COUNTERS, TYPICAL RESET, PRESET AND COUNT SEQUENCES

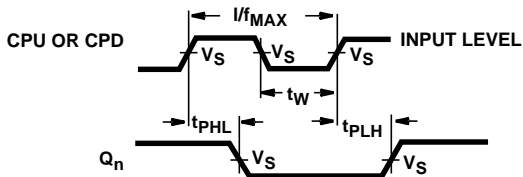


FIGURE 3. CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH

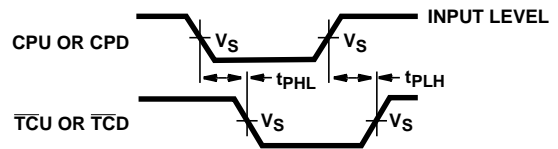


FIGURE 4. CLOCK TO TERMINAL COUNT DELAYS

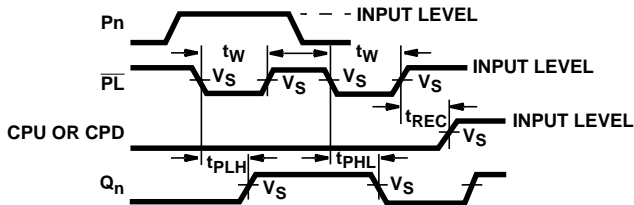


FIGURE 5. PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAYS, AND PARALLEL LOAD TO CLOCK RECOVERY TIME

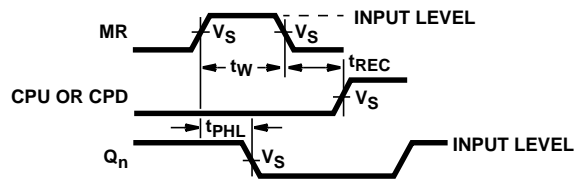


FIGURE 6. MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

Test Circuits and Waveforms (Continued)

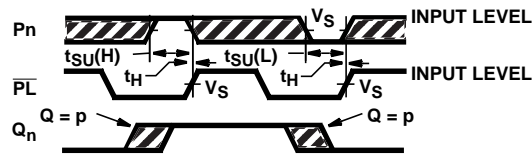


FIGURE 7. SET-UP AND HOLD TIMES DATA TO PARALLEL LOAD (PL)

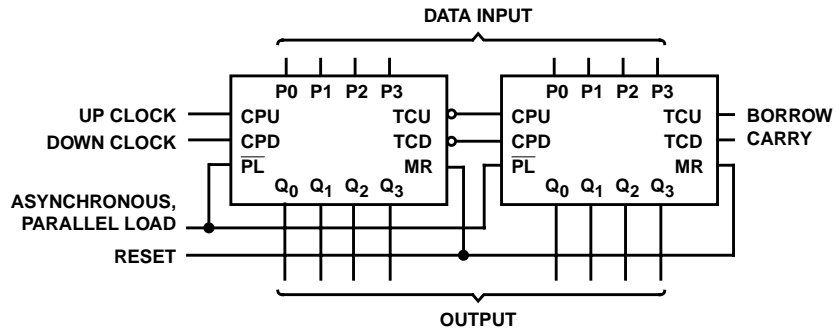
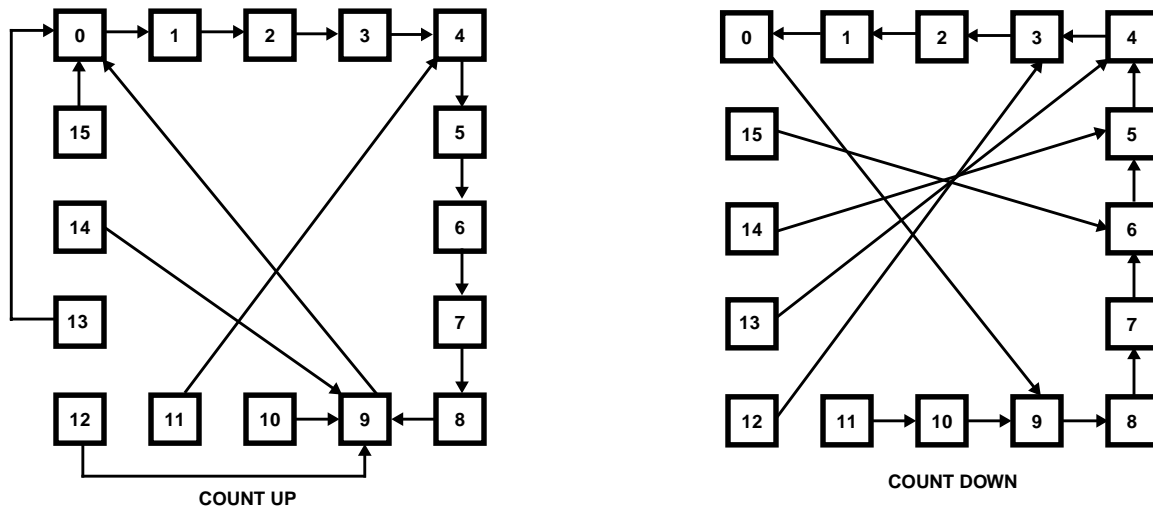


FIGURE 8. CASCADED UP/DOWN COUNTER WITH PARALLEL LOAD



NOTE: Illegal states in BCD counters corrected in one count.

NOTE: Illegal states in BCD counters corrected in one or two counts.

FIGURE 9. 'HC192, 'HCT193 STATE DIAGRAMS

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|--------------------------------------|-------------------------|
| 5962-8780801EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8780801EA CD54HC192F3A | Samples |
| 5962-9084801MEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9084801ME A CD54HCT193F3A | Samples |
| CD54HC192F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8780801EA CD54HC192F3A | Samples |
| CD54HC193F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8772401EA CD54HC193F3A | Samples |
| CD54HCT193F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9084801ME A CD54HCT193F3A | Samples |
| CD74HC192E | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC192E | Samples |
| CD74HC192NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC192M | Samples |
| CD74HC192NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC192M | Samples |
| CD74HC192PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ192 | Samples |
| CD74HC192PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ192 | Samples |
| CD74HC192PWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ192 | Samples |
| CD74HC193E | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC193E | Samples |
| CD74HC193M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC193M | Samples |
| CD74HC193M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC193M | Samples |
| CD74HC193M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC193M | Samples |
| CD74HC193MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC193M | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|----------------|
| CD74HCT193E | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT193E | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC192, CD54HC193, CD54HCT193, CD74HC192, CD74HC193, CD74HCT193 :

● Catalog: [CD74HC192](#), [CD74HC193](#), [CD74HCT193](#)

- Military: [CD54HC192](#), [CD54HC193](#), [CD54HCT193](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC192NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD74HC192PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC192PWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC193M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC192NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| CD74HC192PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| CD74HC192PWT | TSSOP | PW | 16 | 250 | 367.0 | 367.0 | 35.0 |
| CD74HC193M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

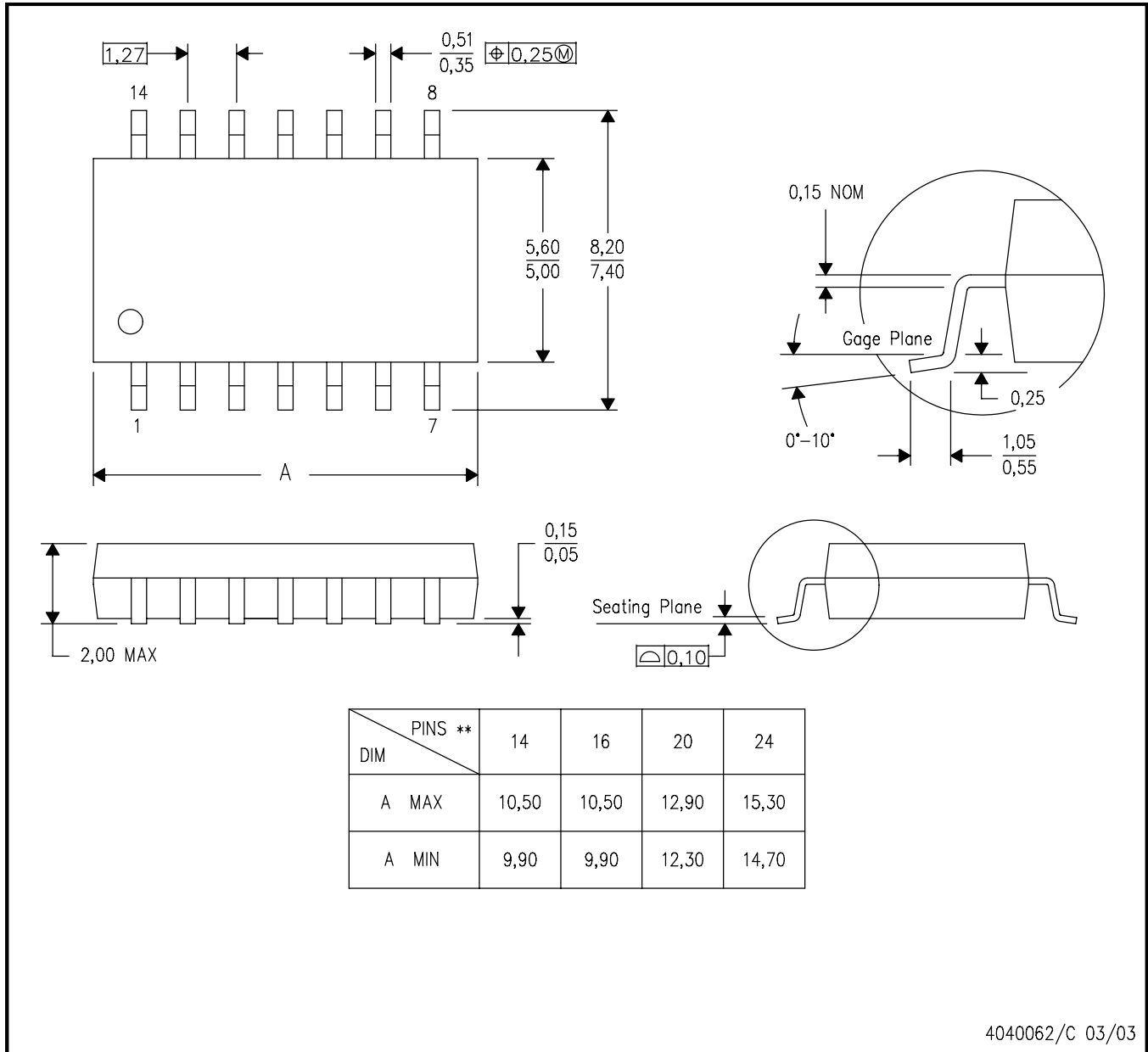
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View CD74HC192PWT](#) on WIN SOURCE

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management