



**THE DATASHEET OF  
UCC27211AQDDARQ1**



# UCC27211A-Q1 120-V Boot, 4-A Peak, High-Frequency High-Side and Low-Side Driver

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade  $-40^{\circ}\text{C}$  to  $+140^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM Classification Level 2
  - Device CDM Classification Level C6
- Drives Two N-Channel MOSFETs in High-Side and Low-Side Configuration With Independent Inputs
- Maximum Boot Voltage 120-V DC
- 4-A Sink, 4-A Source Output Currents
- $0.9\text{-}\Omega$  Pullup and Pulldown Resistance
- Input Pins Can Tolerate  $-10\text{ V}$  to  $+20\text{ V}$  and are Independent of Supply Voltage Range
- TTL Compatible Inputs
- 8-V to 17-V VDD Operating Range, (20-V ABS MAX)
- 7.2-ns Rise and 5.5-ns Fall Time With 1000-pF Load
- Fast Propagation Delay Times (20-ns typical)
- 4-ns Delay Matching
- Symmetrical Undervoltage Lockout for High-Side and Low-Side Driver
- Available in the Industry Standard SO-PowerPAD SOIC-8 Package
- Specified from  $-40$  to  $+140^{\circ}\text{C}$

## 2 Applications

- Power Supplies for Telecom, Datacom, and Merchant
- Half-Bridge and Full-Bridge Converters
- Push-Pull Converters
- High Voltage Synchronous-Buck Converters
- Two-Switch Forward Converters
- Active-Clamp Forward Converters
- Class-D Audio Amplifiers

## 3 Description

The UCC27211A-Q1 device driver is based on the popular UCC27201 MOSFET drivers; but, this device offers several significant performance improvements.

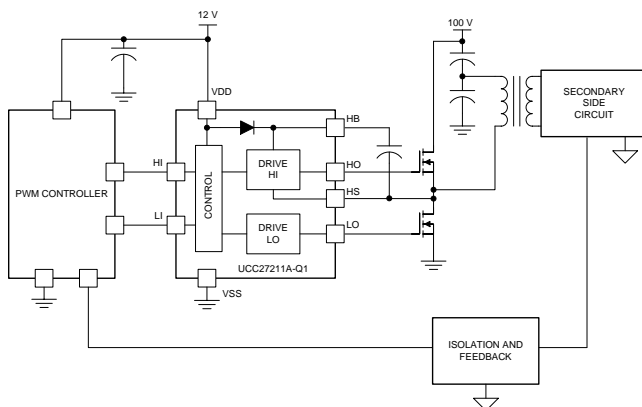
The peak output pullup and pulldown current has been increased to 4-A source and 4-A sink, and pullup and pulldown resistance have been reduced to  $0.9\ \Omega$ , and thereby allows for driving large power MOSFETs with minimized switching losses during the transition through the Miller Plateau of the MOSFET. The input structure can directly handle  $-10\text{ VDC}$ , which increases robustness and also allows direct interface to gate-drive transformers without using rectification diodes. The inputs are also independent of supply voltage and have a 20-V maximum rating.

### Device Information<sup>(1)</sup>

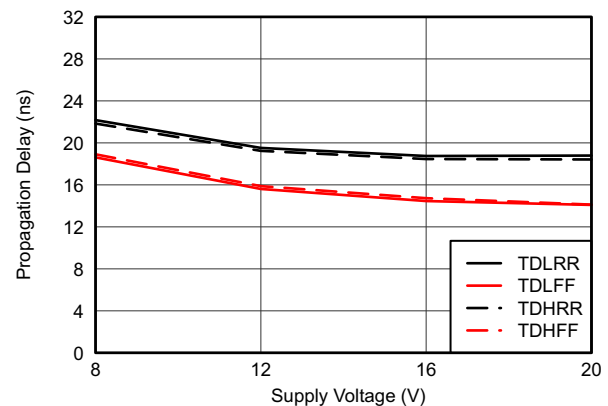
PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27211A-Q1	SO PowerPAD™ (8)	4.89 mm x 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Typical Application Diagram



### Propagation Delays vs Supply Voltage $T = 25^{\circ}\text{C}$



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2016	*	Initial release.

## 5 Description (continued)

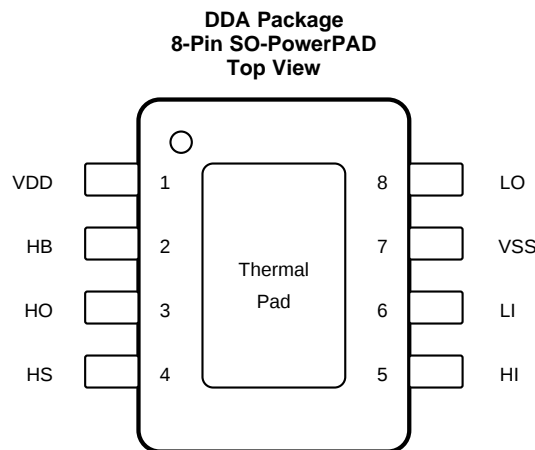
The switching node of the UCC27211A-Q1 (HS pin) can handle –18-V maximum, which allows the high-side channel to be protected from inherent negative voltages caused by parasitic inductance and stray capacitance. The UCC27211A-Q1 has increased hysteresis that allows for interface to analog or digital PWM controllers with enhanced noise immunity.

The low-side and high-side gate drivers are independently controlled and matched to 2 ns between the turn on and turn off of each other.

An on-chip 120-V rated bootstrap diode eliminates the external discrete diodes. Undervoltage lockout is provided for both the high-side and the low-side drivers which provides symmetric turn on and turn off behavior and forces the outputs low if the drive voltage is below the specified threshold.

The UCC27211A-Q1 device is offered in an 8-Pin SO-PowerPAD package.

## 6 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
HB	2	P	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 $\mu\text{F}$ to 0.1 $\mu\text{F}$ . The capacitor value is dependant on the gate charge of the high-side MOSFET and must also be selected based on speed and ripple criteria.
HI	5	I	High-side input. <sup>(1)</sup>
HO	3	O	High-side output. Connect to the gate of the high-side power MOSFET.
HS	4	P	High-side source connection. Connect to source of high-side power MOSFET. Connect the negative side of bootstrap capacitor to this pin.
LI	6	I	Low-side input. <sup>(1)</sup>
LO	8	O	Low-side output. Connect to the gate of the low-side power MOSFET.
VDD	1	P	Positive supply to the lower-gate driver. De-couple this pin to $V_{SS}$ (GND). Typical decoupling capacitor range is 0.22 $\mu\text{F}$ to 4.7 $\mu\text{F}$ (See <sup>(2)</sup> ).
VSS	7	—	Negative supply terminal for the device that is generally grounded.
Thermal pad <sup>(3)</sup>		—	Electrically referenced to $V_{SS}$ (GND). Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

- (1) HI or LI input is assumed to connect to a low impedance source signal. The source output impedance is assumed less than 100  $\Omega$ . If the source impedance is greater than 100  $\Omega$ , add a bypassing capacitor, each, between HI and VSS and between LI and VSS. The added capacitor value depends on the noise levels presented on the pins, typically from 1 nF to 10 nF should be effective to eliminate the possible noise effect. When noise is present on two pins, HI or LI, the effect is to cause HO and LO malfunctions to have wrong logic outputs.
- (2) For cold temperature applications TI recommends the upper capacitance range. Follow the [Layout Guidelines](#) for PCB layout.
- (3) The thermal pad is not directly connected to any leads of the package; however, it is electrically and thermally connected to the substrate which is the ground of the device.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{DD}^{(2)}$ , $V_{HB} - V_{HS}$	Supply voltage range	-0.3	20	V
$V_{LI}$ , $V_{HI}$	Input voltages on LI and HI	-10	20	V
$V_{LO}$	Output voltage on LO	DC	$V_{DD} + 0.3$	V
		Repetitive pulse < 100 ns <sup>(3)</sup>	$V_{DD} + 0.3$	
$V_{HO}$	Output voltage on HO	DC	$V_{HS} - 0.3$	V
		Repetitive pulse < 100 ns <sup>(3)</sup>	$V_{HS} - 2$	
$V_{HS}$	Voltage on HS	DC	115	V
		Repetitive pulse < 100 ns <sup>(3)</sup>	$-(24\text{ V} - V_{DD})$	
$V_{HB}$	Voltage on HB	-0.3	120	V
$T_J$	Operating virtual junction temperature range	-40	150	°C
$T_{STG}$	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to VSS unless otherwise noted. Currents are positive into and negative out of the specified terminal.
- (3) Verified at bench characterization. VDD is the value used in an application design.

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	V
		Charged-device model (CDM), per AEC Q100-011	
		All pins	±1500

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

all voltages are with respect to VSS; currents are positive into and negative out of the specified terminal.  $-40^{\circ}\text{C} < T_J = T_A < 140^{\circ}\text{C}$  (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD}$ , $V_{HB} -$ $V_{HS}$	Supply voltage range	8	12	17	V
$V_{HS}$	Voltage on HS	-1		105	V
$V_{HS}$	Voltage on HS (repetitive pulse < 100 ns)	$-(24\text{ V} - V_{DD})$		110	V
$V_{HB}$	Voltage on HB	$V_{HS} + 8,$ $V_{DD} - 1$		$V_{HS} + 17,$ 115	V
	Voltage slew rate on HS			50	V/ns
	Operating junction temperature	-40		140	°C

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		UCC27211A-Q1	
		DDA (SO-PowerPAD)	
		8 PINS	
Symbol	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	2.8	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	9.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

$V_{DD} = V_{HB} = 12\text{ V}$ ,  $V_{HS} = V_{SS} = 0\text{ V}$ , no load on LO or HO,  $T_A = T_J = -40^\circ\text{C}$  to  $140^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENTS</b>						
$I_{DD}$	$V_{DD}$ quiescent current	$V(LI) = V(HI) = 0\text{ V}$	0.05	0.085	0.17	mA
$I_{DDO}$	$V_{DD}$ operating current	$f = 500\text{ kHz}$ , $C_{LOAD} = 0$	2.1	2.5	6.5	mA
$I_{HB}$	Boot voltage quiescent current	$V(LI) = V(HI) = 0\text{ V}$	0.015	0.065	0.1	mA
$I_{HBO}$	Boot voltage operating current	$f = 500\text{ kHz}$ , $C_{LOAD} = 0$	1.5	2.5	5.1	mA
$I_{HBS}$	HB to $V_{SS}$ quiescent current	$V(HS) = V(HB) = 115\text{ V}$		0.0005	1	$\mu\text{A}$
$I_{HBSO}$	HB to $V_{SS}$ operating current	$f = 500\text{ kHz}$ , $C_{LOAD} = 0$		0.07	1.2	mA
<b>INPUT</b>						
$V_{HIT}$	Input voltage threshold		1.7	2.3	2.55	V
$V_{LIT}$	Input voltage threshold		1.2	1.6	1.9	V
$V_{IHYS}$	Input voltage hysteresis			700		mV
$R_{IN}$	Input pulldown resistance			68		k $\Omega$
<b>UNDER-VOLTAGE LOCKOUT (UVLO)</b>						
$V_{DDR}$	$V_{DD}$ turnon threshold		6.2	7	7.8	V
$V_{DDHYS}$	Hysteresis			0.5		V
$V_{HBR}$	$V_{HB}$ turnon threshold		5.6	6.7	7.9	V
$V_{HBHYS}$	Hysteresis			1.1		V
<b>BOOTSTRAP DIODE</b>						
$V_F$	Low-current forward voltage	$I_{VDD-HB} = 100\text{ }\mu\text{A}$		0.65	0.8	V
$V_{FI}$	High-current forward voltage	$I_{VDD-HB} = 100\text{ mA}$		0.85	0.95	V
$R_D$	Dynamic resistance, $\Delta V_F/\Delta I$	$I_{VDD-HB} = 100\text{ mA}$ and $80\text{ mA}$	0.3	0.5	0.85	$\Omega$
<b>LO GATE DRIVER</b>						
$V_{LOL}$	Low-level output voltage	$I_{LO} = 100\text{ mA}$	0.05	0.1	0.19	V
$V_{LOH}$	High level output voltage	$I_{LO} = -100\text{ mA}$ , $V_{LOH} = V_{DD} - V_{LO}$	0.1	0.16	0.29	V
	Peak pullup current <sup>(1)</sup>	$V_{LO} = 0\text{ V}$		3.7		A
	Peak pulldown current <sup>(1)</sup>	$V_{LO} = 12\text{ V}$		4.5		A
<b>HO GATE DRIVER</b>						
$V_{HOL}$	Low-level output voltage	$I_{HO} = 100\text{ mA}$	0.05	0.1	0.19	V
$V_{HOH}$	High-level output voltage	$I_{HO} = -100\text{ mA}$ , $V_{HOH} = V_{HB} - V_{HO}$	0.1	0.16	0.29	V
	Peak pullup current <sup>(1)</sup>	$V_{HO} = 0\text{ V}$		3.7		A
	Peak pulldown current <sup>(1)</sup>	$V_{HO} = 12\text{ V}$		4.5		A

(1) Ensured by design.

## 7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
<b>PROPAGATION DELAYS</b>							
$T_{DLFF}$	$V_{LI}$ falling to $V_{LO}$ falling	$C_{LOAD} = 0$		10	16	30	ns
$T_{DHFF}$	$V_{HI}$ falling to $V_{HO}$ falling	$C_{LOAD} = 0$		10	16	30	ns
$T_{DLRR}$	$V_{LI}$ rising to $V_{LO}$ rising	$C_{LOAD} = 0$		10	20	42	ns
$T_{DHRR}$	$V_{HI}$ rising to $V_{HO}$ rising	$C_{LOAD} = 0$		10	20	42	ns
<b>DELAY MATCHING</b>							
$T_{MON}$	From HO OFF to LO ON	$T_J = 25^\circ\text{C}$		4	9.5	ns	
		$T_J = -40^\circ\text{C to } 140^\circ\text{C}$		4	17	ns	
$T_{MOFF}$	From LO OFF to HO ON	$T_J = 25^\circ\text{C}$		4	9.5	ns	
		$T_J = -40^\circ\text{C to } 140^\circ\text{C}$		4	17	ns	
<b>OUTPUT RISE AND FALL TIME</b>							
$t_R$	LO rise time	$C_{LOAD} = 1000 \text{ pF, from } 10\% \text{ to } 90\%$		7.2		ns	
$t_R$	HO rise time	$C_{LOAD} = 1000 \text{ pF, from } 10\% \text{ to } 90\%$		7.2		ns	
$t_F$	LO fall time	$C_{LOAD} = 1000 \text{ pF, from } 90\% \text{ to } 10\%$		5.5		ns	
$t_F$	HO fall time	$C_{LOAD} = 1000 \text{ pF, from } 90\% \text{ to } 10\%$		5.5		ns	
$t_R$	LO, HO	$C_{LOAD} = 0.1 \text{ }\mu\text{F, (3 V to 9 V)}$		0.36	0.6	$\mu\text{s}$	
$t_F$	LO, HO	$C_{LOAD} = 0.1 \text{ }\mu\text{F, (9 V to 3 V)}$		0.15	0.4	$\mu\text{s}$	
<b>MISCELLANEOUS</b>							
Minimum input pulse width that changes the output				50		ns	
Bootstrap diode turnoff time <sup>(1)(2)</sup>		$I_F = 20 \text{ mA, } I_{REV} = 0.5 \text{ A}^{(3)}$		20		ns	

(1) Ensured by design.

(2)  $I_F$ : Forward current applied to bootstrap diode,  $I_{REV}$ : Reverse current applied to bootstrap diode.

(3) Typical values for  $T_A = 25^\circ\text{C}$ .

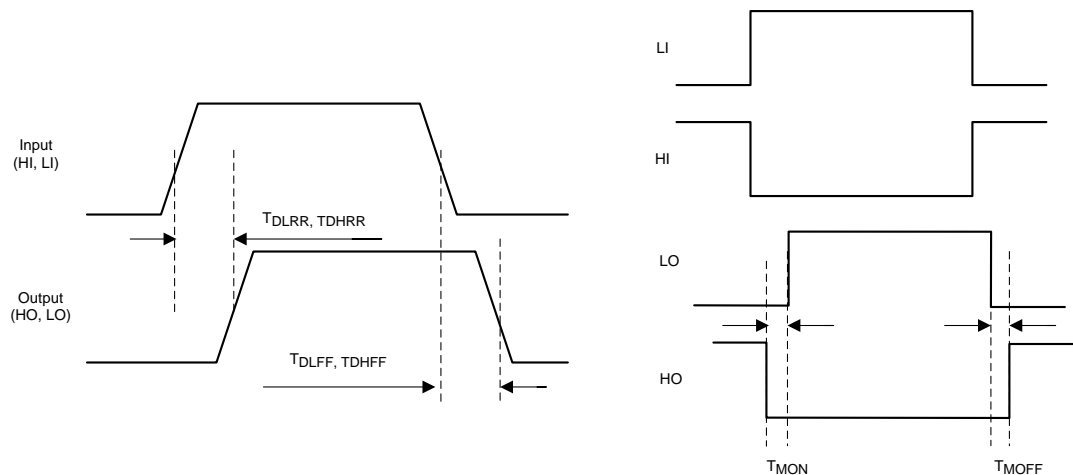


Figure 1. Timing Diagram

### 7.7 Typical Characteristics

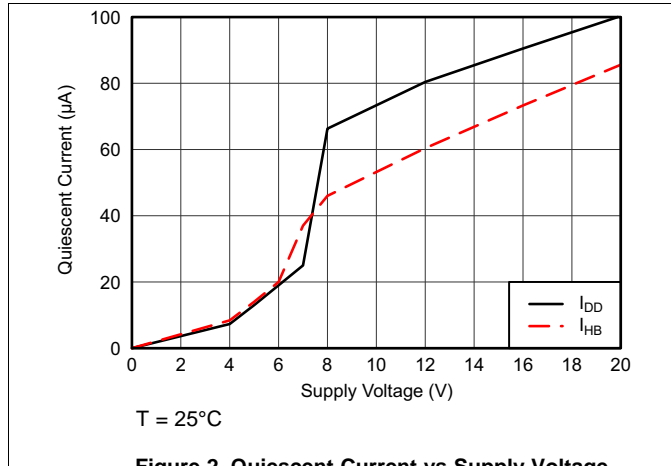


Figure 2. Quiescent Current vs Supply Voltage

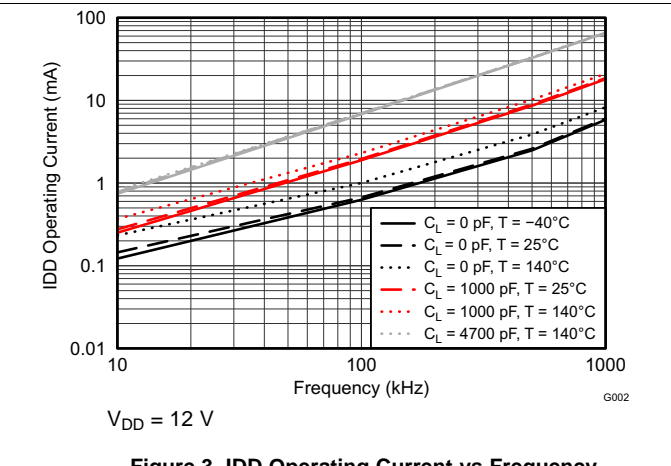


Figure 3. IDD Operating Current vs Frequency

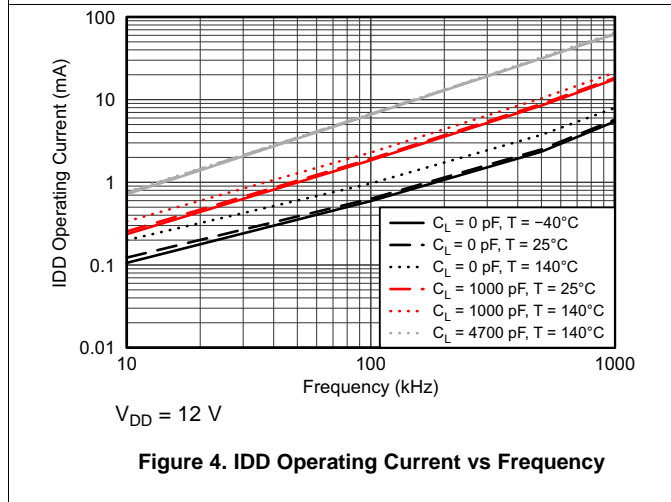


Figure 4. IDD Operating Current vs Frequency

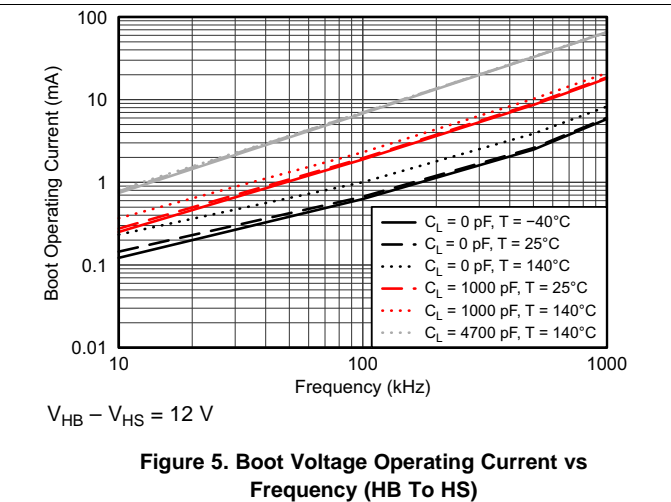


Figure 5. Boot Voltage Operating Current vs Frequency (HB To HS)

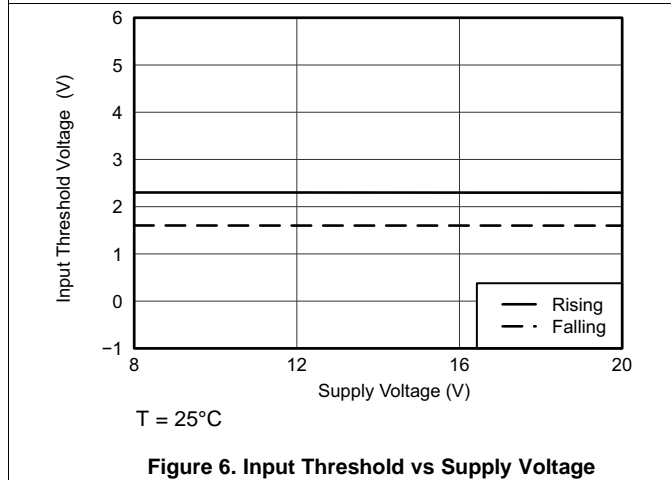


Figure 6. Input Threshold vs Supply Voltage

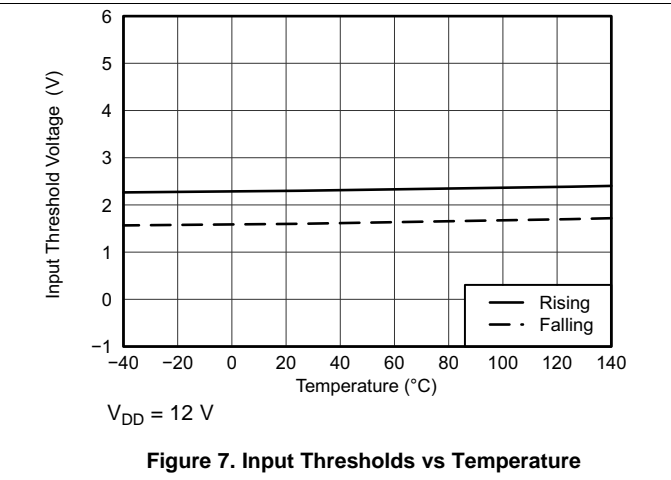
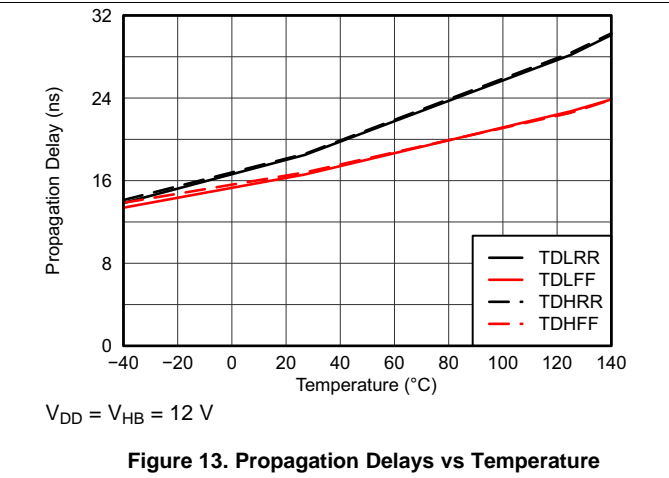
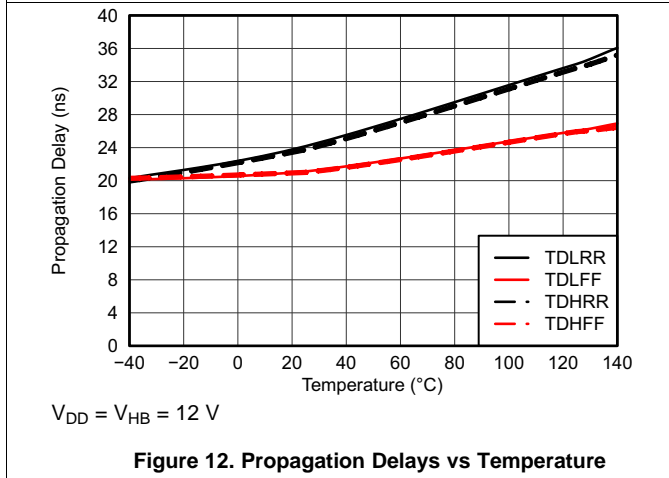
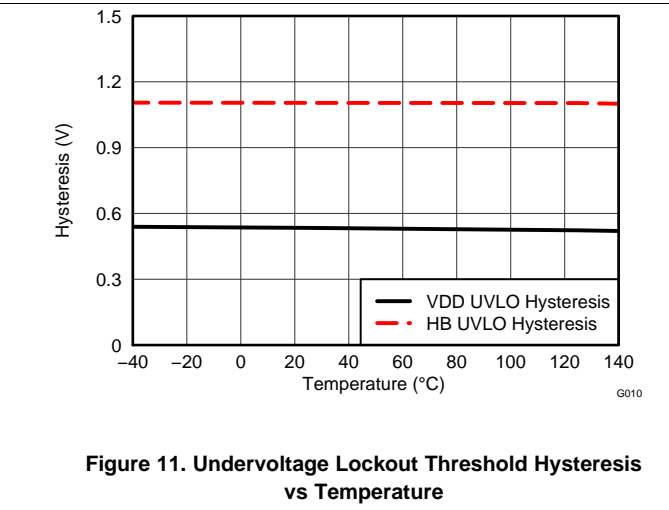
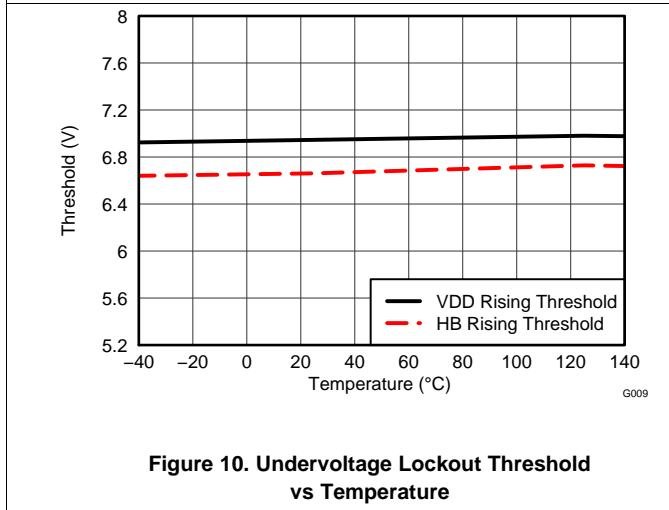
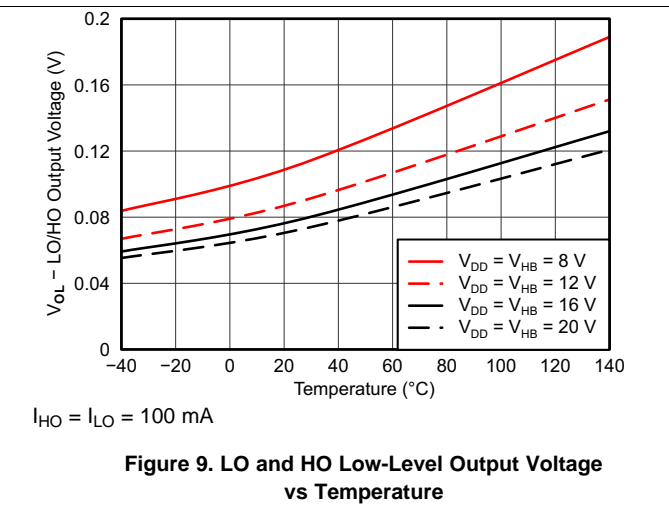
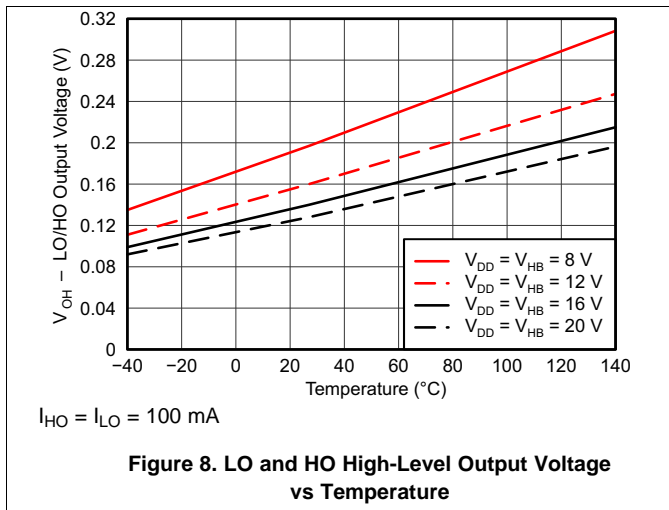
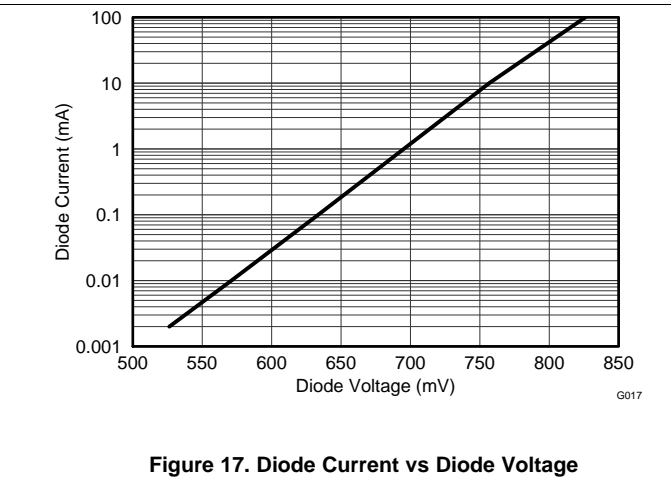
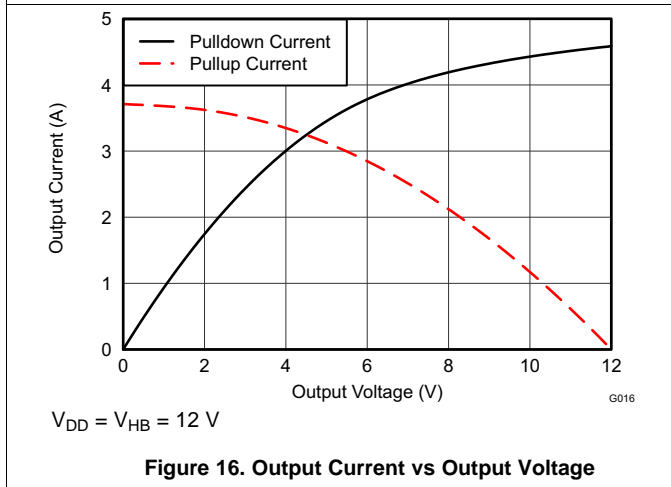
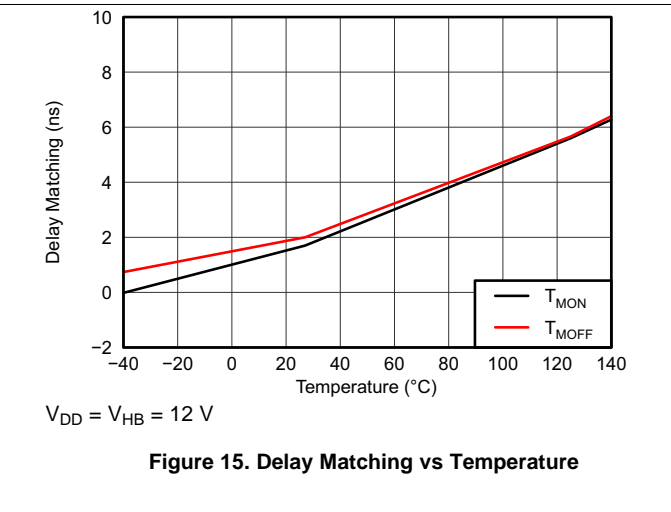
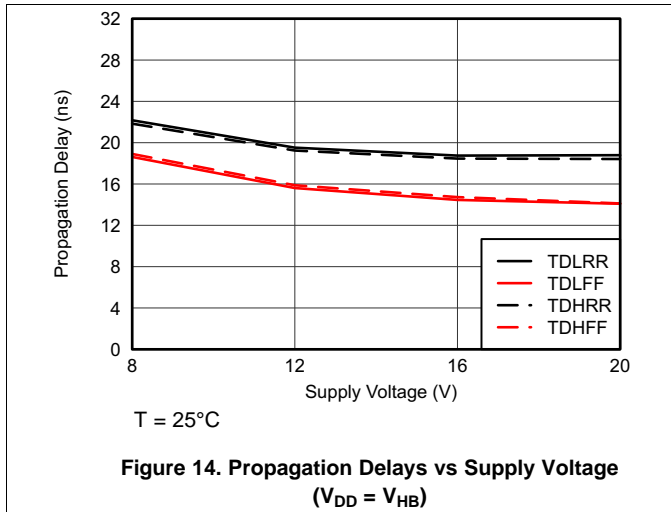


Figure 7. Input Thresholds vs Temperature

Typical Characteristics (continued)



Typical Characteristics (continued)



## 8 Detailed Description

### 8.1 Overview

The UCC27211A-Q1 device represents Texas Instruments' latest generation of high-voltage gate drivers, which are designed to drive both the high-side and low-side of N-Channel MOSFETs in a half- and full-bridge or synchronous-buck configuration. The floating high-side driver can operate with supply voltages of up to 120 V, which allows for N-Channel MOSFET control in half-bridge, full-bridge, push-pull, two-switch forward, and active clamp forward converters.

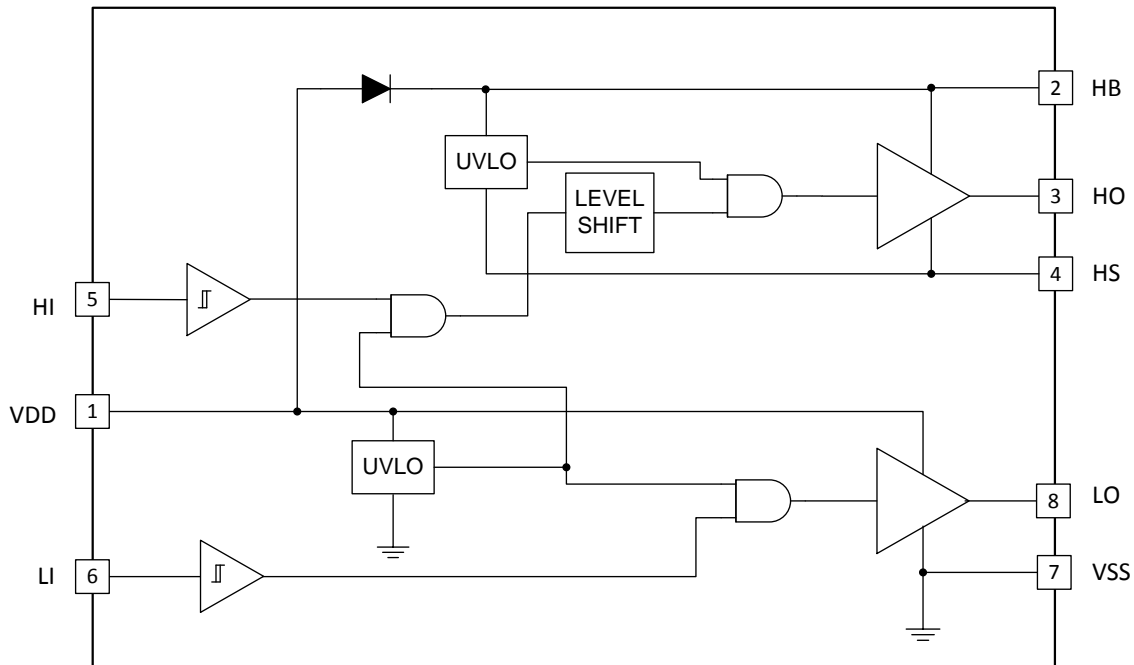
The UCC27211A-Q1 device features 4-A source and sink capability, industry best-in-class switching characteristics and a host of other features listed in [Table 1](#). These features combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

**Table 1. UCC27211A-Q1 Highlights**

FEATURE	BENEFIT
4-A source and sink current with 0.9-Ω output resistance	High peak current ideal for driving large power MOSFETs with minimal power loss (fast-drive capability at Miller plateau)
Input pins (HI and LI) can directly handle –10 VDC up to 20 VDC	Increased robustness and ability to handle undershoot and overshoot can interface directly to gate-drive transformers without having to use rectification diodes.
120-V internal boot diode	Provides voltage margin to meet telecom 100-V surge requirements
Switch node (HS pin) able to handle –18 V maximum for 100 ns	Allows the high-side channel to have extra protection from inherent negative voltages caused by parasitic inductance and stray capacitance
Robust ESD circuitry to handle voltage spikes	Excellent immunity to large dV/dT conditions
18-ns propagation delay with 7.2-ns rise time and 5.5-ns fall time	Best-in-class switching characteristics and extremely low-pulse transmission distortion
2-ns (typical) delay matching between channels	Avoids transformer volt-second offset in bridge
Symmetrical UVLO circuit	Ensures high-side and low-side shut down at the same time
TTL optimized thresholds with increased hysteresis	Complementary to analog or digital PWM controllers; increased hysteresis offers added noise immunity

In the UCC27211A-Q1 device, the high side and low side each have independent inputs that allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27211A. The UCC27211A is a TTL or logic compatible device. The high-side driver is referenced to the switch node (HS), which is typically the source pin of the high-side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to  $V_{SS}$ , which is typically ground. The UCC27211A-Q1 functions are divided into the input stages, UVLO protection, level shift, boot diode, and output driver stages.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Input Stages

The input stages of the UCC27211A-Q1 device have impedance of 70-k $\Omega$  nominal and input capacitance is approximately 2 pF. Pulldown resistance to  $V_{SS}$  (ground) is 70 k $\Omega$ . The logic level compatible input provides a rising threshold of 2.3 V and a falling threshold of 1.6 V.

### 8.3.2 Undervoltage Lockout (UVLO)

The bias supplies for the high-side and low-side drivers have UVLO protection.  $V_{DD}$  as well as  $V_{HB}$  to  $V_{HS}$  differential voltages are monitored. The  $V_{DD}$  UVLO disables both drivers when  $V_{DD}$  is below the specified threshold. The rising  $V_{DD}$  threshold is 7 V with 0.5-V hysteresis. The VHB UVLO disables only the high-side driver when the  $V_{HB}$  to  $V_{HS}$  differential voltage is below the specified threshold. The  $V_{HB}$  UVLO rising threshold is 6.7 V with 1.1-V hysteresis.

## Feature Description (continued)

### 8.3.3 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

### 8.3.4 Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC27211A-Q1 family of drivers. The diode anode is connected to  $V_{DD}$  and cathode connected to  $V_{HB}$ . With the  $V_{HB}$  capacitor connected to HB and the HS pins, the  $V_{HB}$  capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

### 8.3.5 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from  $V_{DD}$  to  $V_{SS}$  and the high side is referenced from  $V_{HB}$  to  $V_{HS}$ .

## 8.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See the [Undervoltage Lockout \(UVLO\)](#) section for information on UVLO operation mode. In the normal mode the output state is dependent on states of the HI and LI pins. [Table 2](#) lists the output states for different input pin combinations.

**Table 2. Device Logic Table**

HI PIN	LI PIN	HO <sup>(1)</sup>	LO <sup>(2)</sup>
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

(1) HO is measured with respect to HS.

(2) LO is measured with respect to VSS.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

To affect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers, and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

Finally, emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. Gate-driver devices are extremely important components in switching power, and they combine the benefits of high-performance, low-cost component count and board-space reduction as well as simplified system design.

### 9.2 Typical Application

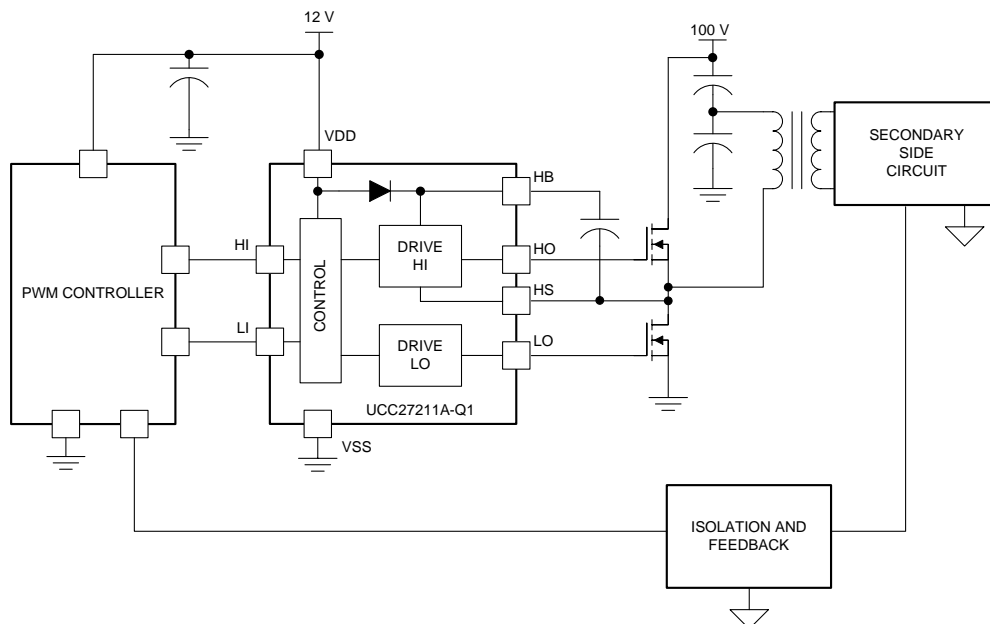
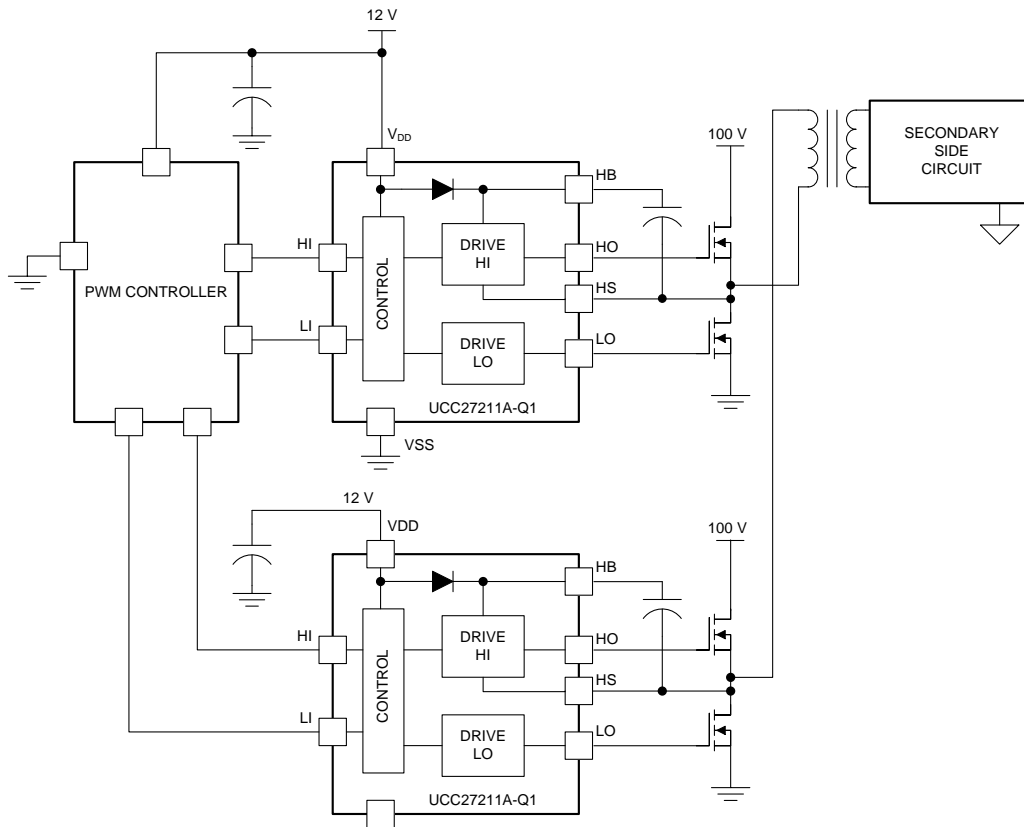


Figure 18. UCC27211A-Q1 Typical Application Diagram

**Typical Application (continued)**

**Figure 19. UCC27211-Q1 Typical Application Diagram**
**9.2.1 Design Requirements**

 For this design example, use the parameters listed in [Table 3](#).

**Table 3. Design Specifications**

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, VDD	12 V
Voltage on HS, VHS	0 V to 100 V
Voltage on HB, VHB	12 V to 112 V
Output current rating, IO	–4 A to 4 A
Operating frequency	500 kHz

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Input Threshold Type

The UCC27211A-Q1 device has an input maximum voltage range from  $-10\text{ V}$  to  $20\text{ V}$ . This increased robustness means that both parts can be directly interfaced to gate drive transformers. The UCC27211A-Q1 device features TTL compatible input threshold logic with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See the [Electrical Characteristics](#) table for the actual input threshold voltage levels and hysteresis specifications for the UCC27211A-Q1 device.

### 9.2.2.2 $V_{DD}$ Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the [Absolute Maximum Ratings](#) table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With a wide operating range from  $8\text{ V}$  to  $17\text{ V}$ , the UCC27211A-Q1 device can be used to drive a variety of power switches, such as Si MOSFETs, IGBTs, and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than  $6\text{ V}$  to be applied to the gate terminals).

### 9.2.2.3 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible in order to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds with the targeted power MOSFET. The system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as  $dV_{DS}/dt$ ). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned-on with a  $dV_{DS}/dt$  of  $20\text{ V/ns}$  or higher with a DC bus voltage of  $400\text{ V}$  in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from  $400\text{ V}$  in the OFF state to  $V_{DS(on)}$  in on state) must be completed in approximately  $20\text{ ns}$  or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in the SPP20N60C3 data sheet is  $33\text{ nC}$  typical) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET,  $V_{GS(TH)}$ .

To achieve the targeted  $dV_{DS}/dt$ , the gate driver must be capable of providing the  $Q_{GD}$  charge in  $20\text{ ns}$  or less. In other words a peak current of  $1.65\text{ A}$  ( $= 33\text{ nC} / 20\text{ ns}$ ) or higher must be provided by the gate driver. The UCC27211A gate driver is capable of providing  $4\text{-A}$  peak sourcing current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The  $2.4\times$  overdrive capability provides an extra margin against part-to-part variations in the  $Q_{GD}$  parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the  $dI/dt$  of the output current pulse of the gate driver. In order to illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle ( $\frac{1}{2} \times I_{PEAK} \times \text{time}$ ) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET datasheet =  $87\text{ nC}$  typical). If the parasitic trace inductance limits the  $dI/dt$  then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words the time parameter in the equation would dominate and the  $I_{PEAK}$  value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

### 9.2.2.4 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27211A-Q1 device features 16-ns (typical) propagation delays, which ensures very little pulse distortion and allows operation at very high-frequencies. See the [Electrical Characteristics](#) table for the propagation and switching characteristics of the UCC27211A-Q1 device.

### 9.2.2.5 Power Dissipation

Power dissipation of the gate driver has two portions as shown in [Equation 1](#).

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

Use [Equation 2](#) to calculate the DC portion of the power dissipation (PDC).

$$PDC = I_Q \times V_{DD}$$

where

- $I_Q$  is the quiescent current for the driver. (2)

The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through, and so forth). The UCC27211A-Q1 features very low quiescent currents (less than 0.17 mA, refer to the [Electrical Characteristics](#) table and contain internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the PDC on the total power dissipation within the gate driver can be safely assumed to be negligible. The power dissipated in the gate-driver package during switching (PSW) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage  $V_G$ , which is very close to input bias supply voltage  $V_{DD}$ )
- Switching frequency
- Use of external gate resistors. When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by [Equation 3](#).

$$EG = \frac{1}{2} C_{LOAD} \times V_{DD}^2$$

where

- $C_{LOAD}$  is load capacitor
- $V_{DD}$  is bias voltage feeding the driver (3)

There is an equal amount of energy dissipated when the capacitor is charged and when it is discharged. This leads to a total power loss given by [Equation 4](#).

$$PG = C_{LOAD} \times V_{DD}^2 \times f_{SW}$$

where

- $f_{SW}$  is the switching frequency (4)

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge  $Q_G$ , determine the power that must be dissipated when switching a capacitor which is calculated using the equation  $Q_G = C_{LOAD} \times V_{DD}$  to provide [Equation 5](#) for power.

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} = Q_G \times V_{DD} \times f_{SW} \quad (5)$$

This power  $P_G$  is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on and off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor.

### 9.2.3 Application Curves

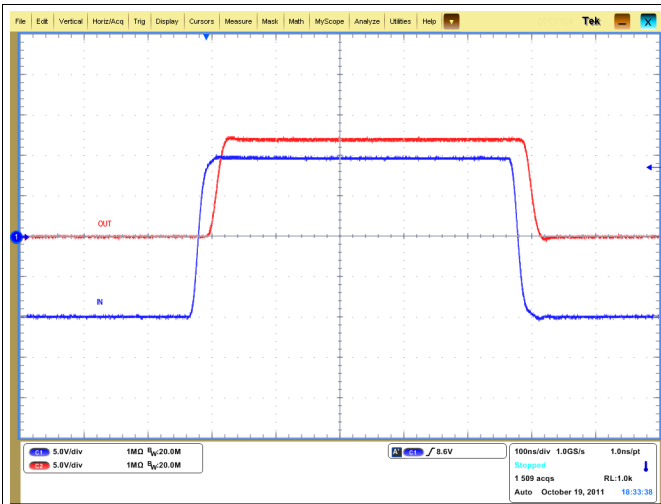


Figure 20. Negative 10-V Input

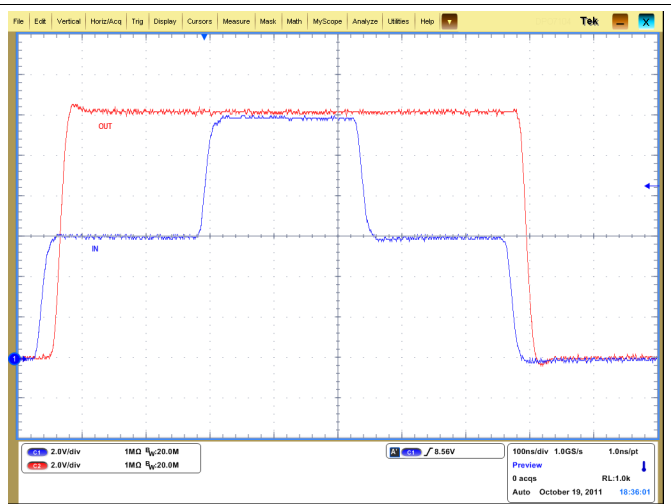


Figure 21. Step Input

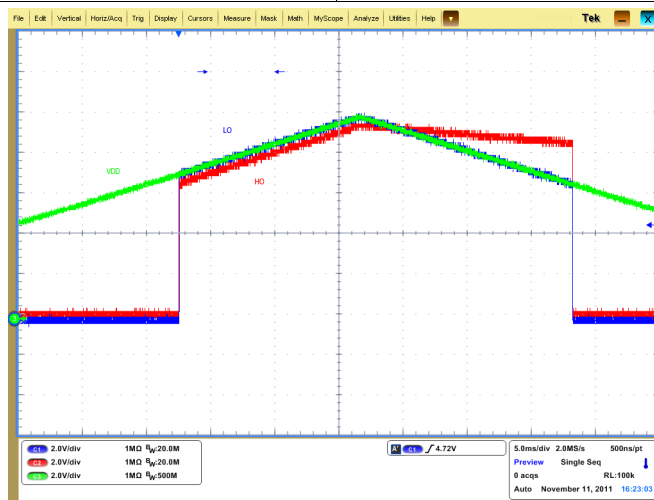


Figure 22. Symmetrical UVLO

## 10 Power Supply Recommendations

The bias supply voltage range for which the UCC27211A-Q1 device is recommended to operate is from 8 V to 17 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the  $V_{DD}$  pin supply circuit blocks. Whenever the driver is in UVLO condition when the  $V_{DD}$  pin voltage is below the  $V_{(ON)}$  supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the  $V_{DD}$  pin of the device (which is a stress rating). Keeping a 3-V margin to allow for transient voltage spikes, the maximum recommended voltage for the  $V_{DD}$  pin is 17 V. The UVLO protection feature also involves a hysteresis function, which means that when the  $V_{DD}$  pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification  $V_{DD(hys)}$ . Therefore, ensuring that, while operating at or near the 8-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the  $V_{DD}$  pin voltage has dropped below the  $V_{(OFF)}$  threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up the device does not begin operation until the  $V_{DD}$  pin voltage has exceeded the  $V_{(ON)}$  threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the  $V_{DD}$  pin. Although this fact is well known, it is important to recognize that the charge for source current pulses delivered by the HO pin is also supplied through the same  $V_{DD}$  pin. As a result, every time a current is sourced out of the HO pin, a corresponding current pulse is delivered into the device through the  $V_{DD}$  pin. Thus, ensure that a local bypass capacitor is provided between the  $V_{DD}$  and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is required. TI recommends using a capacitor in the range 0.22  $\mu$ F to 4.7  $\mu$ F between  $V_{DD}$  and GND. In a similar manner, the current pulses delivered by the LO pin are sourced from the HB pin. Therefore a 0.022- $\mu$ F to 0.1- $\mu$ F local decoupling capacitor is recommended between the HB and HS pins.

## 11 Layout

### 11.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules must be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the  $V_{DD} - V_{SS}$  and  $V_{HB} - V_{HS}$  (bootstrap) capacitors as close as possible to the device (see [Figure 23](#)).
- Pay close attention to the GND trace. Use the thermal pad of the DRM package as GND by connecting it to the VSS pin (GND). The GND trace from the driver goes directly to the source of the MOSFET, but must not be in the high current path of the MOSFET drain or source current.
- Use similar rules for the HS node as for GND for the high-side driver.
- For systems using multiple UCC27211A-Q1 device, TI recommends that dedicated decoupling capacitors be located at  $V_{DD} - V_{SS}$  for each device.
- Care must be taken to avoid placing VDD traces close to LO, HS, and HO signals.
- Use wide traces for LO and HO closely following the associated GND or HS traces. A width of 60 to 100 mils is preferable where possible.
- Use as least two or more vias if the driver outputs or SW node must be routed from one layer to another. For GND, the number of vias must be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid LI and HI (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.

A poor layout can cause a significant drop in efficiency or system malfunction, and it can even lead to decreased reliability of the whole system.

## 11.2 Layout Example

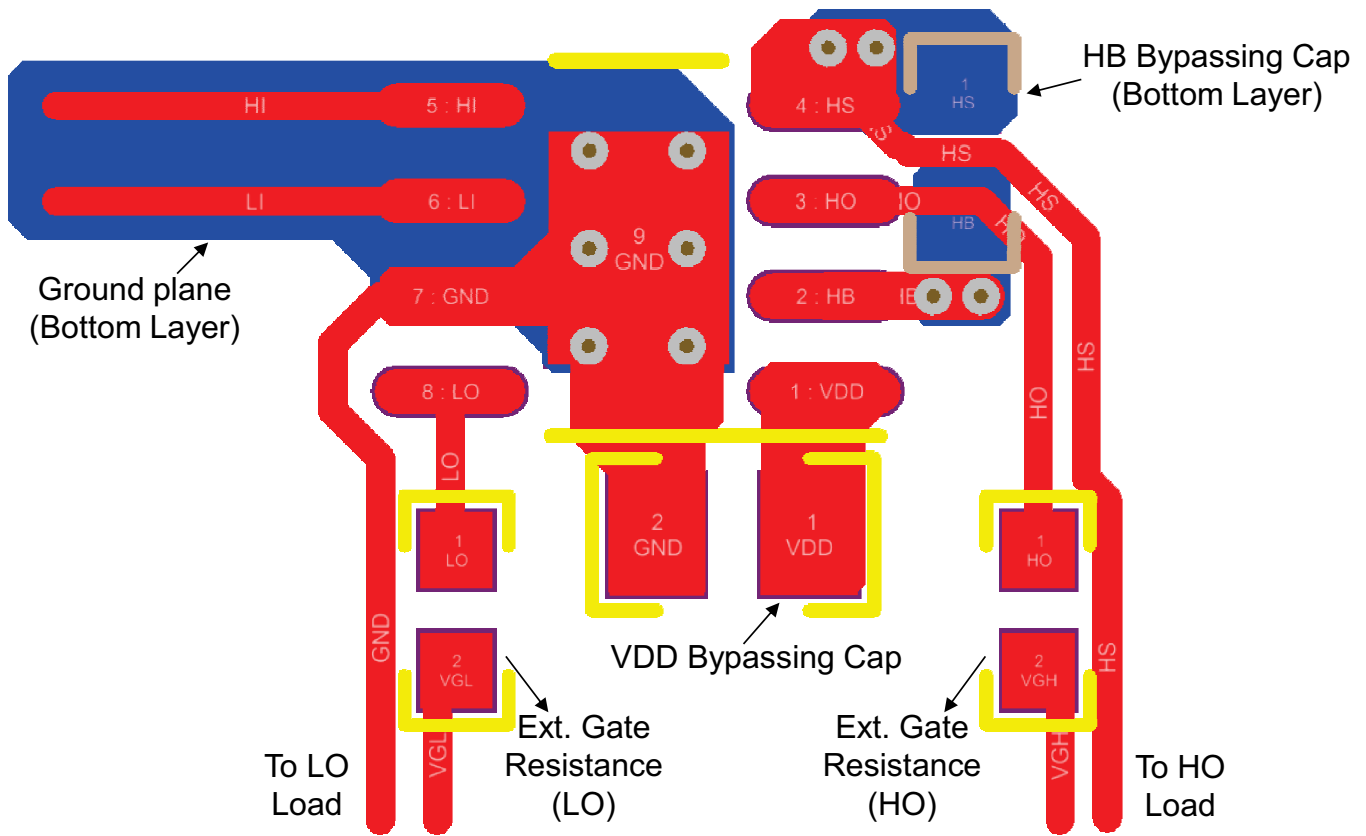


Figure 23. UCC27211A-Q1 PCB Layout Example

## 11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. For a gate driver to be useful over a particular temperature range, the package must allow for efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package are listed in . For detailed information regarding the table, refer to the Application Note from Texas Instruments entitled *Semiconductor and IC Package Thermal Metrics* (SPRA953). The UCC27211A-Q1 device is offered in an 8-pin SO-PowerPAD package.

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

*PowerPAD™ Thermally Enhanced Package*, Application Report ([SLMA002](#))

*PowerPAD™ Made Easy*, Application Report ([SLMA004](#))

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27211AQDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 140	27211Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

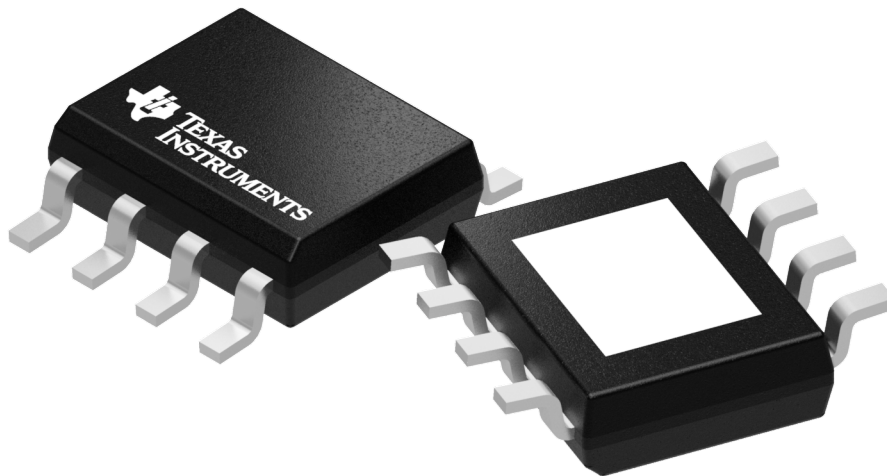

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27211AQDDARQ1	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

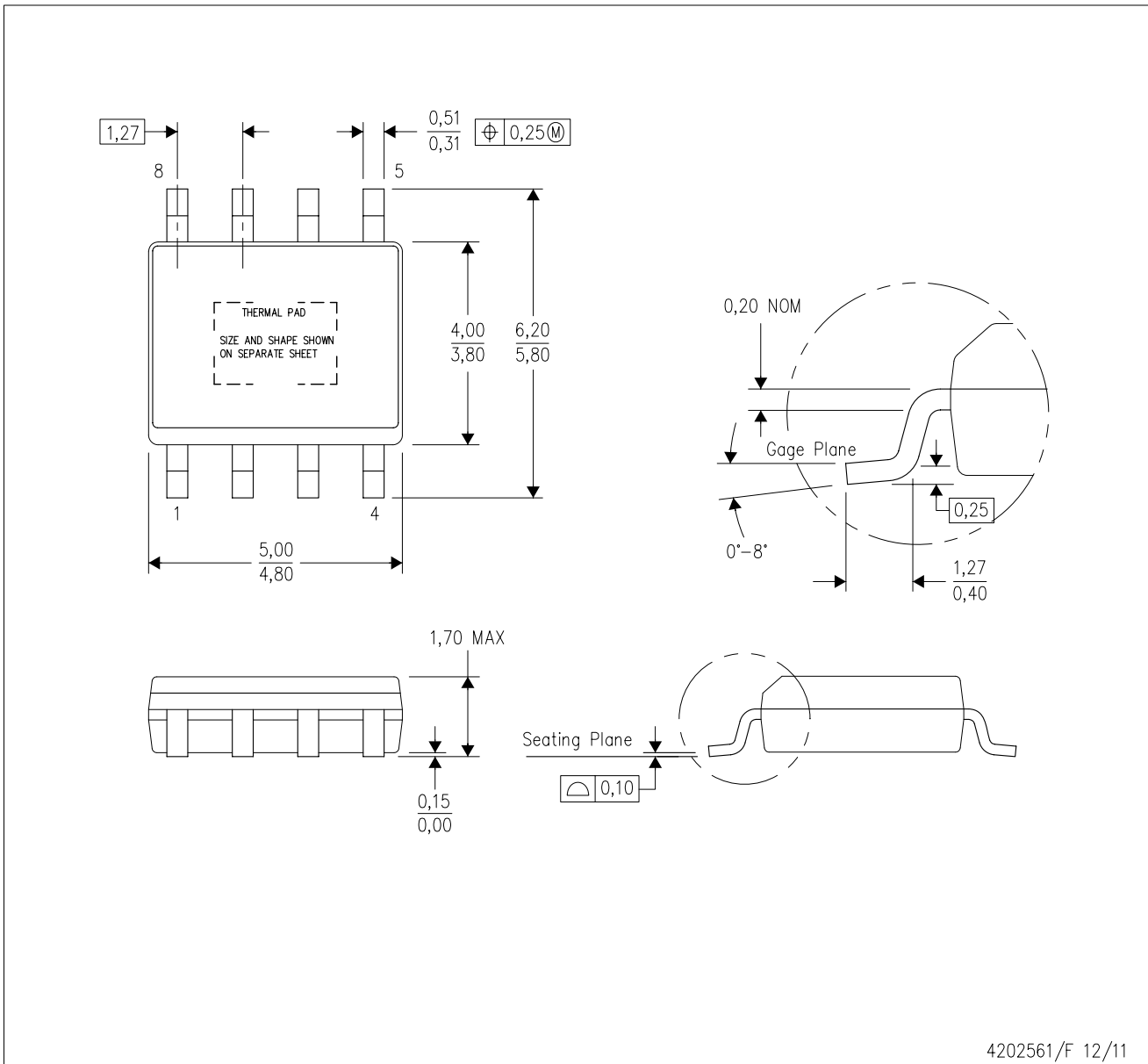
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27211AQDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



4202561/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R-PDSO-G8)

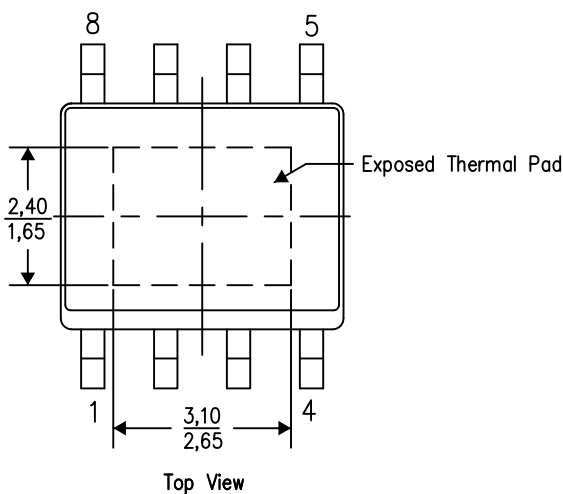
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

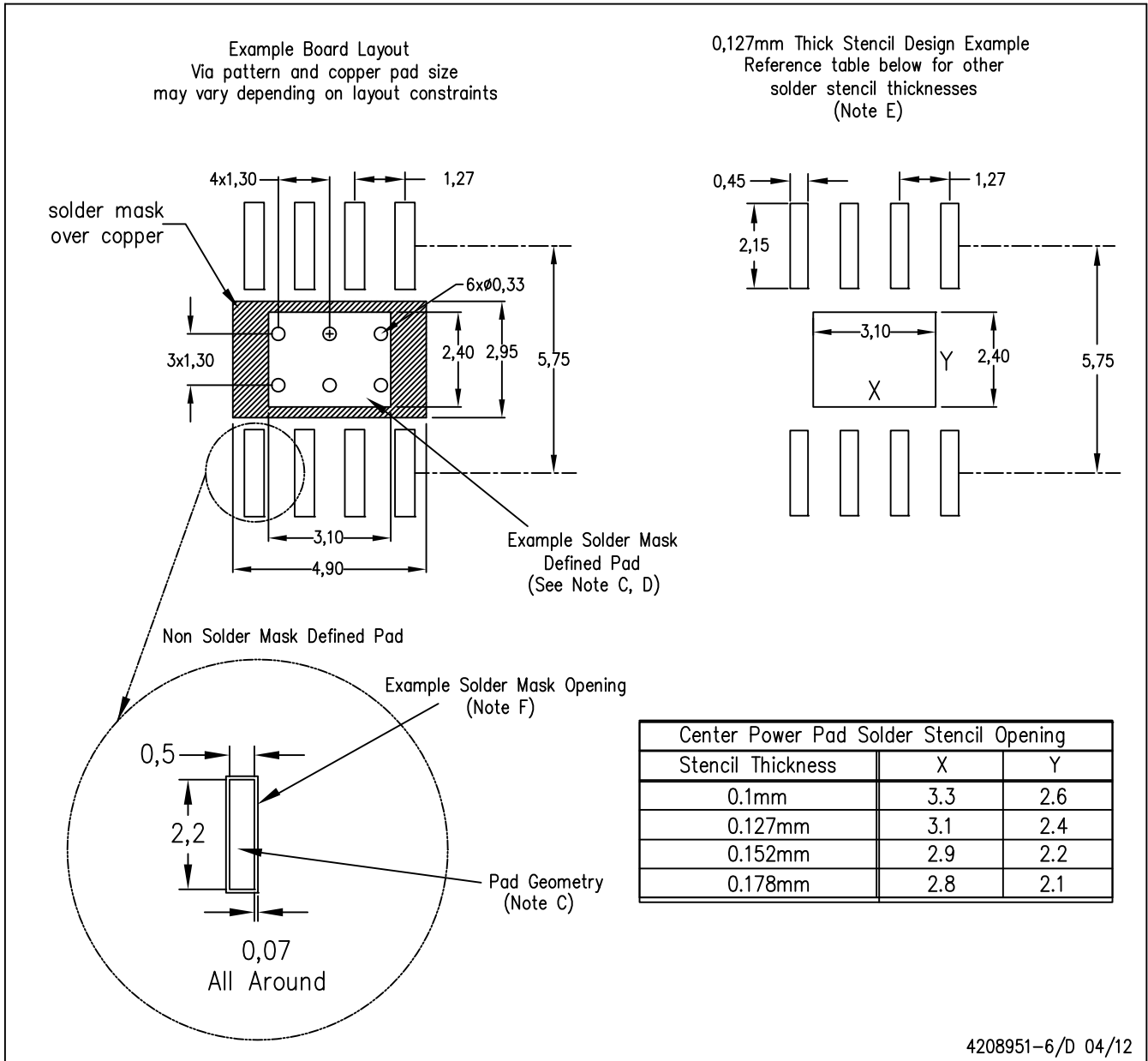


Exposed Thermal Pad Dimensions

4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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