



**THE DATASHEET OF  
MAX9113ESA+T**



## MAX9111/MAX9113

## Single/Dual LVDS Line Receivers with Ultra-Low Pulse Skew in SOT23

### General Description

The MAX9111/MAX9113 single/dual low-voltage differential signaling (LVDS) receivers are designed for high-speed applications requiring minimum power consumption, space, and noise. Both devices support switching rates exceeding 500Mbps while operating from a single +3.3V supply, and feature ultra-low 300ps (max) pulse skew required for high-resolution imaging applications such as laser printers and digital copiers.

The MAX9111 is a single LVDS receiver, and the MAX9113 is a dual LVDS receiver.

Both devices conform to the EIA/TIA-644 LVDS standard and convert LVDS to LVTTTL/CMOS-compatible outputs. A fail-safe feature sets the outputs high when the inputs are undriven and open, terminated, or shorted. The MAX9111/MAX9113 are available in space-saving 8-pin SOT23 and SO packages. Refer to the MAX9110/MAX9112 data sheet for single/dual LVDS line drivers.

### Applications

- Laser Printers
- Digital Copiers
- Cellular Phone Base Stations
- Telecom Switching Equipment
- Network Switches/Routers
- LCD Displays
- Backplane Interconnect
- Clock Distribution
- Automotive

### Features

- Low 300ps (max) Pulse Skew for High-Resolution Imaging and High-Speed Interconnect
- Space-Saving 8-Pin SOT23 and SO Packages
- Pin-Compatible Upgrades to DS90LV018A and DS90LV028A (SO Packages Only)
- Guaranteed 500Mbps Data Rate
- Low 29mW Power Dissipation at 3.3V
- Conform to EIA/TIA-644 Standard
- Single +3.3V Supply
- Flow-Through Pinout Simplifies PCB Layout
- Fail-Safe Circuit Sets Output High for Undriven Inputs
- High-Impedance LVDS Inputs when Powered Off
- AEC-Q100 Qualified, Refer to [Ordering Information](#) for the Specific /V Versions

[Typical Operating Circuit](#) appears at end of data sheet.

**Absolute Maximum Ratings**

V <sub>CC</sub> to GND.....	-0.3V to +4V	8-Pin SO (derate 5.88mW/°C above +70°C).....	471mW
IN_ to GND .....	-0.3V to +3.9V	8-Pin TDFN (derate 6.20mW/°C above +70°C) .....	496mW
OUT_ to GND.....	-0.3V to (V <sub>CC</sub> + 0.3V)	<b>Operating Temperature Ranges</b>	
<b>ESD Protection All Pins</b>		MAX911_E.....	-40°C to +85°C
(Human Body Model, IN_+, IN_-).....		MAX911_A .....	-40°C to +125°C
<b>Continuous Power Dissipation (T<sub>A</sub> = +70°C)</b>		<b>Storage Temperature Range .....</b>	
8-Pin SOT23 (derate 5.10mW/°C above +70°C) ...		-65°C to +150°C	
408.60mW		<b>Lead Temperature (soldering, 10s) .....</b>	
		+300°C	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Package Information**

**SOT23-8**

PACKAGE CODE	K8+1
Outline Number	<a href="#">21-0078</a>
Land Pattern Number	<a href="#">90-0176</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	195.80°C/W
Junction to Case (θ <sub>JC</sub> )	70°C/W

**SO-8**

PACKAGE CODE	S8-2/S8+2
Outline Number	<a href="#">21-0041</a>
Land Pattern Number	<a href="#">90-0096</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	170°C/W
Junction to Case (θ <sub>JC</sub> )	40°C/W
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	136°C/W
Junction to Case (θ <sub>JC</sub> )	38°C/W

**TDFN-8**

PACKAGE CODE	T822CY+2
Outline Number	<a href="#">21-100341</a>
Land Pattern Number	<a href="#">90-100117</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	162°C/W
Junction to Case (θ <sub>JC</sub> )	20°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

**Electrical Characteristics**

( $V_{CC} = +3.0V$  to  $+3.6V$ , magnitude of input voltage,  $|V_{ID}| = +0.1V$  to  $+1.0V$ ,  $V_{CM} = |V_{ID}|/2$  to  $(2.4V - (|V_{ID}|/2))$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ . Typical values are at  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$ , unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input High Threshold (Note 3)	$V_{TH}$	$V_{CM} = 0.05V, 1.2V, 2.75V$ at 3.3V			100	mV
Differential Input Low Threshold (Note 3)	$V_{TL}$	$V_{CM} = 0.05V, 1.2V, 2.75V$ at 3.3V	-100			mV
Differential Input Resistance	$R_{DIFF}$	$V_{CM} = 0.2V$ or $2.2V$ , $V_{ID} = \pm 0.4V$ , $V_{CC} = 0$ or $3.6V$	5	18		k $\Omega$
Output High Voltage (OUT_)	$V_{OH}$	$I_{OH} = -4mA$	$V_{ID} = +200mV$	2.7		V
			Inputs shorted, undriven	2.7		
			100 $\Omega$ parallel termination, undriven	2.7		
Output Low Voltage (OUT_)	$V_{OL}$	$I_{OL} = 4mA$ , $V_{ID} = -200mV$			0.4	
Output Short-Circuit Current	$I_{OS}$	$V_{ID} = +200mV$ , $V_{OUT\_} = 0$			-100	mA
		MAX9113ATA/VY+			-120	
No-Load Supply Current	$I_{CC}$	MAX9111		4.2	6	mA
		MAX9113		8.7	11	
		MAX9113ATA/VY+		8.7	16	

Switching Characteristics

(V<sub>CC</sub> = +3.0V to +3.6V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>. Typical values are at V<sub>CC</sub> = +3.3V and T<sub>A</sub> = +25°C, unless otherwise noted.) (Notes 4, 5, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Differential Propagation Delay High to Low	t <sub>PHLD</sub>	C <sub>L</sub> = 15pF, V <sub>ID</sub> = ±200mV, V <sub>CM</sub> = 1.2V (Figures 1, 2)	T <sub>A</sub> = +85°C	1.0	1.77	2.5	ns
			T <sub>A</sub> = +125°C			3.0	
			T <sub>A</sub> = +125°C MAX9113ATA/VY+			3.5	
Differential Propagation Delay Low to High	t <sub>PLHD</sub>	C <sub>L</sub> = 15pF, V <sub>ID</sub> = ±200mV, V <sub>CM</sub> = 1.2V (Figures 1, 2)	T <sub>A</sub> = +85°C	1.0	1.68	2.5	ns
			T <sub>A</sub> = +125°C			3.0	
			T <sub>A</sub> = +125°C MAX9113ATA/VY+			3.5	
Differential Pulse Skew  t <sub>PLHD</sub> - t <sub>PHLD</sub>   (Note 7)	t <sub>SKD1</sub>	C <sub>L</sub> = 15pF, V <sub>ID</sub> = ±200mV, V <sub>CM</sub> = 1.2V (Figures 1, 2)		90	300	ps	
Differential Channel-to-Channel Skew; Same Device (MAX9113 only) (Note 8)	t <sub>SKD2</sub>			140	400	ps	
			MAX9113ATA/VY+		900		
Differential Part-to-Part Skew (Note 9)	t <sub>SKD3</sub>				1		ns
			MAX9113ATA/VY+		1200		
Differential Part-to-Part Skew (MAX9113 only) (Note 10)	t <sub>SKD4</sub>	MAX9113ATA/VY+		1.5	2000	ns	
Rise Time	t <sub>TLH</sub>	C <sub>L</sub> = 15pF, V <sub>ID</sub> = ±200mV, V <sub>CM</sub> = 1.2V (Figures 1, 2)	T <sub>A</sub> = +85°C	0.6	0.8	ns	
			T <sub>A</sub> = +125°C		1.0		
			T <sub>A</sub> = +125°C (MAX9113ATA/VY+)		1.6		
Fall Time	t <sub>THL</sub>	C <sub>L</sub> = 15pF, V <sub>ID</sub> = ±200mV, V <sub>CM</sub> = 1.2V (Figures 1, 2)	T <sub>A</sub> = +85°C	0.6	0.8	ns	
			T <sub>A</sub> = +125°C		1.0		
			T <sub>A</sub> = +125°C (MAX9113ATA/VY+)		1.8		
Maximum Operating Frequency	f <sub>MAX</sub>	All channels switching, C <sub>L</sub> = 15pF, V <sub>OL</sub> (max) = 0.4V, V <sub>OH</sub> (min) = 2.7V, 40% < duty cycle < 60% (Note 6)		250	300	MHz	
			MAX9113ATA/VY+T only		300		

- Note 1:** Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T<sub>A</sub> = +25°C.
- Note 2:** Current into the device is defined as positive. Current out of the devices is defined as negative. All voltages are referenced to ground except V<sub>TH</sub> and V<sub>TL</sub>.
- Note 3:** Guaranteed by design, not production tested.
- Note 4:** AC parameters are guaranteed by design and characterization.
- Note 5:** C<sub>L</sub> includes probe and test jig capacitance.
- Note 6:** f<sub>MAX</sub> generator output conditions: t<sub>R</sub> = t<sub>F</sub> < 1ns (0 to 100%), 50% duty cycle, V<sub>OH</sub> = 1.3V, V<sub>OL</sub> = 1.1V.
- Note 7:** t<sub>SKD1</sub> is the magnitude difference of differential propagation delays in a channel. t<sub>SKD1</sub> = |t<sub>PLHD</sub> - t<sub>PHLD</sub>|.
- Note 8:** t<sub>SKD2</sub> is the magnitude difference of the t<sub>PLHD</sub> or t<sub>PHLD</sub> of one channel and the t<sub>PLHD</sub> or t<sub>PHLD</sub> of the other channel on the same device.
- Note 9:** t<sub>SKD3</sub> is the magnitude difference of any differential propagation delays between devices at the same V<sub>CC</sub> and within 5°C of each other.
- Note 10:** t<sub>SKD4</sub>, is the magnitude difference of any differential propagation delays between devices operating over the rated supply and temperature ranges.

Test Circuit Diagrams

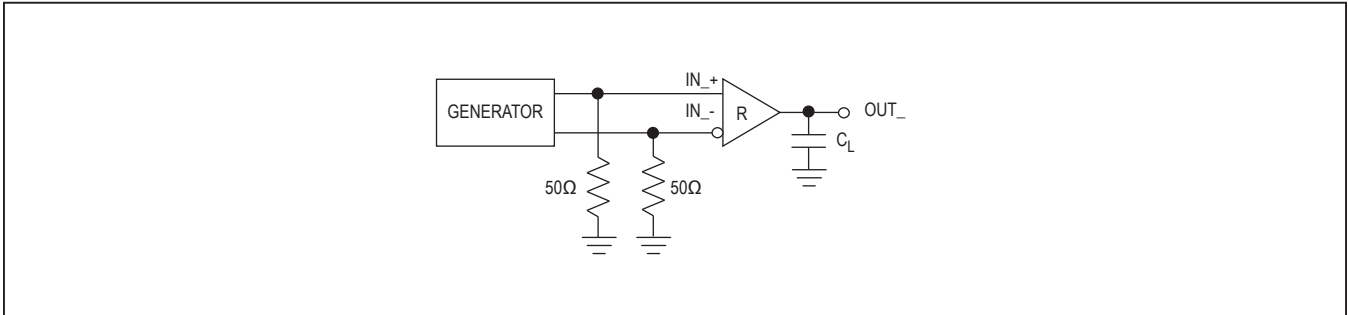


Figure 1. Receiver Propagation Delay and Transition Time Test Circuit

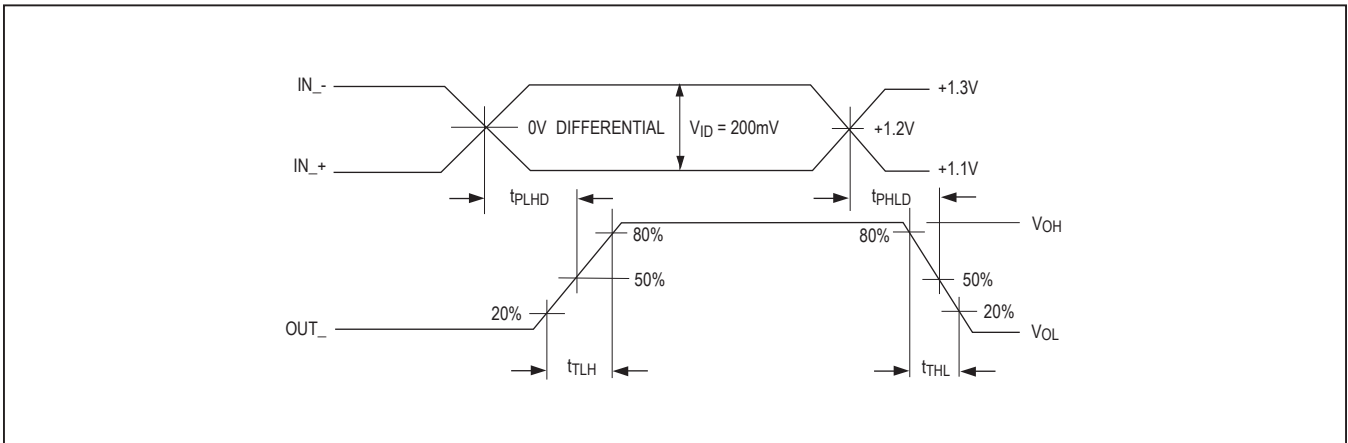
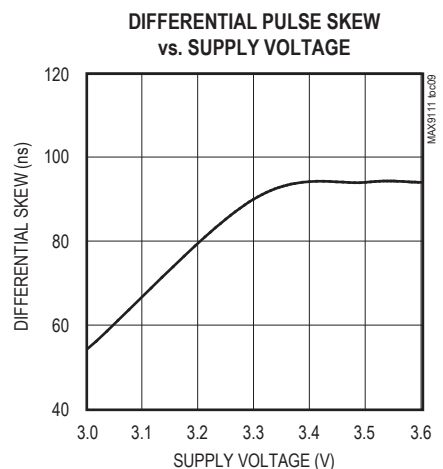
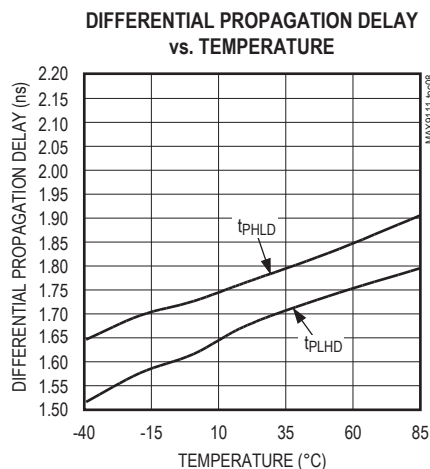
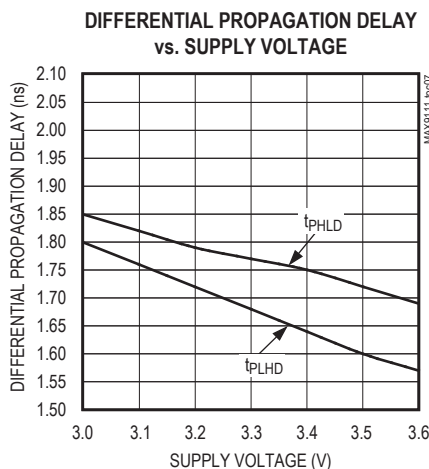
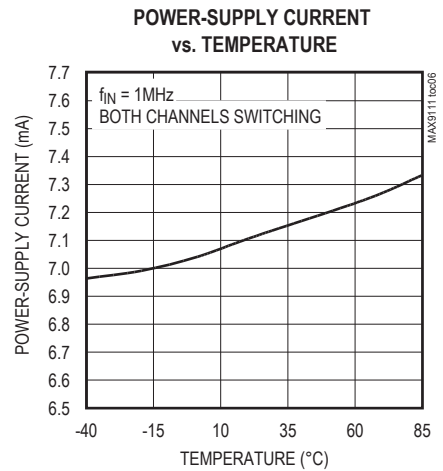
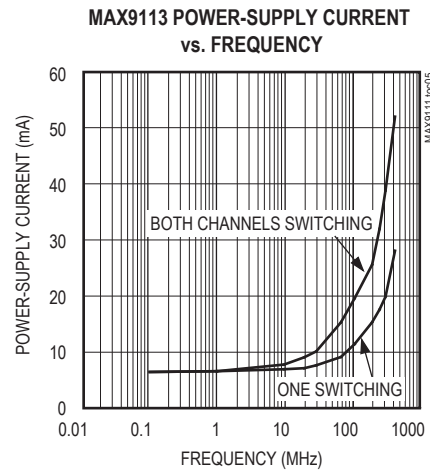
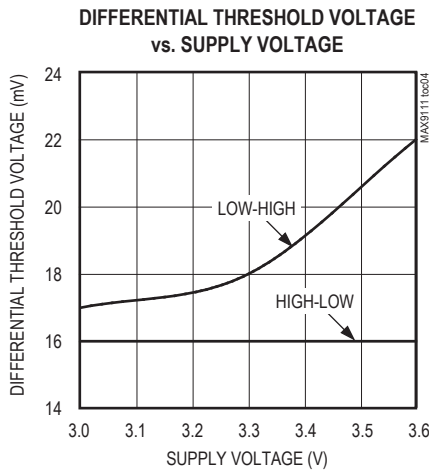
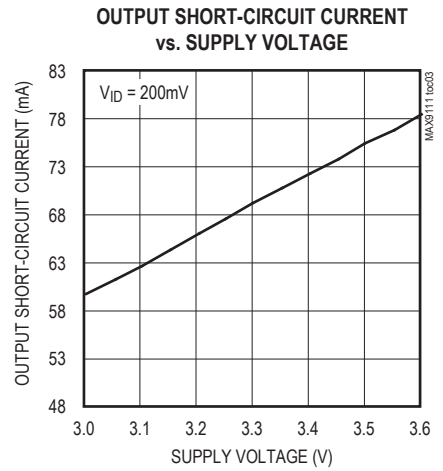
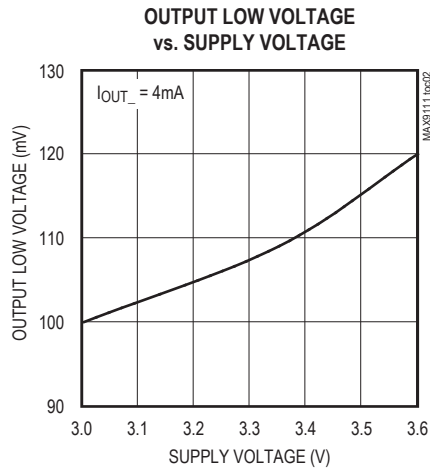
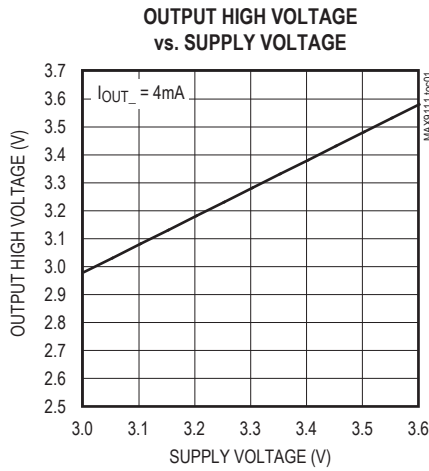


Figure 2. Receiver Propagation Delay and Transition Time Waveforms

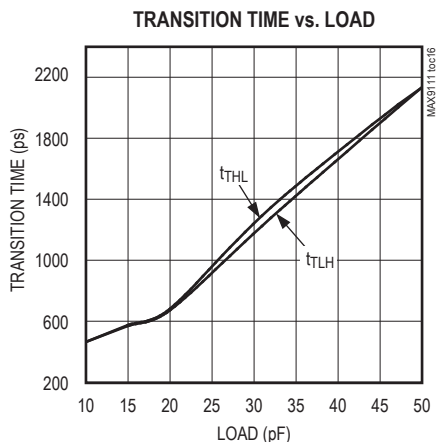
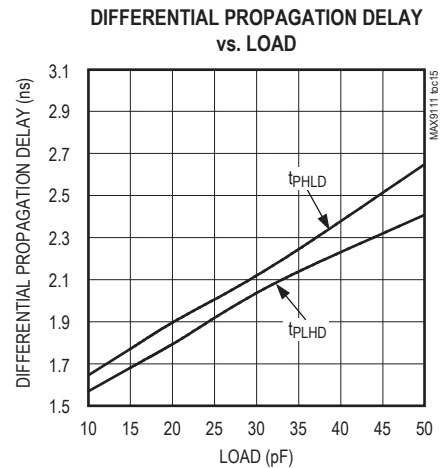
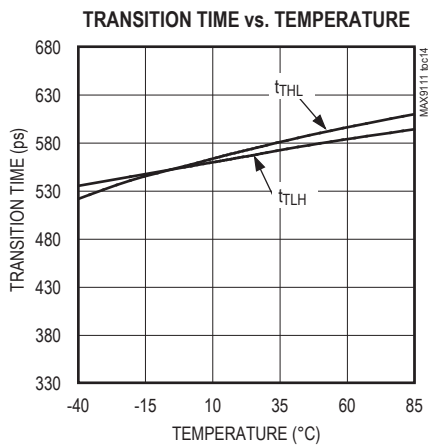
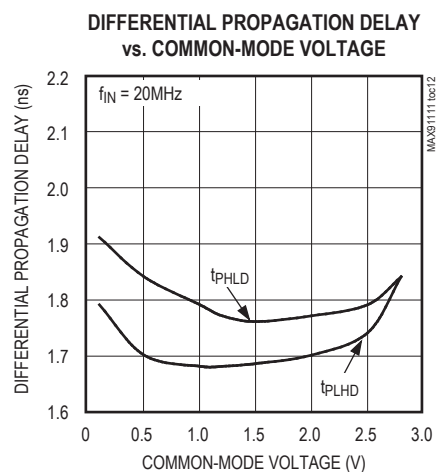
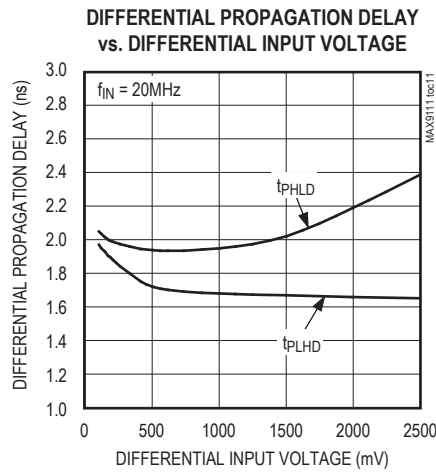
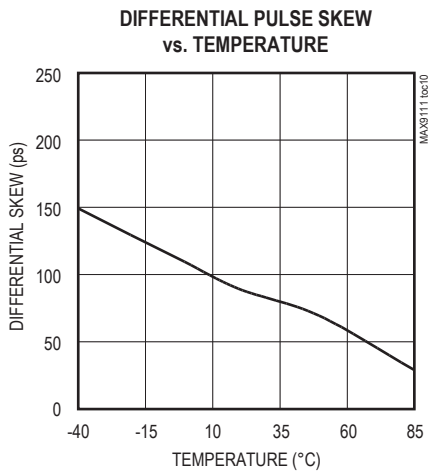
Typical Operating Characteristics

( $V_{CC} = 3.3V$ ,  $|V_{ID}| = 200mV$ ,  $V_{CM} = 1.2V$ ,  $f_{IN} = 200MHz$ ,  $C_L = 15pF$ ,  $T_A = +25^\circ C$  and over recommended operating conditions, unless otherwise specified.)



Typical Operating Characteristics (continued)

( $V_{CC} = 3.3V$ ,  $|V_{ID}| = 200mV$ ,  $V_{CM} = 1.2V$ ,  $f_{IN} = 200MHz$ ,  $C_L = 15pF$ ,  $T_A = +25^\circ C$  and over recommended operating conditions, unless otherwise specified.)



Pin Configurations/Functional Diagrams/Truth Table

TOP VIEW

(IN <sub>+</sub> ) - (IN <sub>-</sub> )	OUT <sub>-</sub>
≥ 100mV	H
≤ -100mV	L
OPEN	H
SHORT	H
100Ω PARALLEL TERMINATION (UNDRIVEN)	H

H = LOGIC LEVEL HIGH  
L = LOGIC LEVEL LOW

Pin Description

PIN				NAME	FUNCTION
MAX9111		MAX9113			
SOT23-8	SO-8	SOT23-8	SO-8		
1	8	1	8	V <sub>CC</sub>	Power Supply
2	5	2	5	GND	Ground
8	1	8	1	IN-/IN1-	Receiver Inverting Differential Input
7	2	7	2	IN+/IN1+	Receiver Noninverting Differential Input
—	—	5	4	IN2-	Receiver Inverting Differential Input
—	—	6	3	IN2+	Receiver Noninverting Differential Input
3	7	3	7	OUT/OUT1	Receiver Output
—	—	4	6	OUT2	Receiver Output
4, 5, 6	3, 4, 6	—	—	N.C.	No Connection. Not internally connected.

Detailed Description

LVDS Inputs

The MAX9111/MAX9113 feature LVDS inputs for interfacing high-speed digital circuitry. The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled impedance media, as defined by the ANSI/EIA/TIA-644 standards. The technology uses low-voltage signals to achieve fast transition times, minimize power dissipation, and noise immunity. Receivers such as the MAX9111/MAX9113 convert LVDS signals to CMOS/LVTTL signals at rates in excess of 500Mbps. The devices are capable of detecting differential signals as low as 100mV and as high as 1V within a 0V to 2.4V input voltage range. The LVDS standard specifies an input voltage range of 0 to 2.4V referenced to ground.

Fail-Safe

The fail-safe feature sets the output to a high state when the inputs are undriven and open, terminated, or shorted. When using one channel in the MAX9113, leave the unused channel open. The fail-safe feature is not guaranteed to be operational above +85°C.

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The receiver inputs of the MAX9111/MAX9113 have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±11kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down.

ESD protection can be tested in various ways; the receiver inputs of this product family are characterized for protection to the limit of ±11kV using the Human Body Model.

Human Body Model

Figure 3a shows the Human Body Model, and Figure 3b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

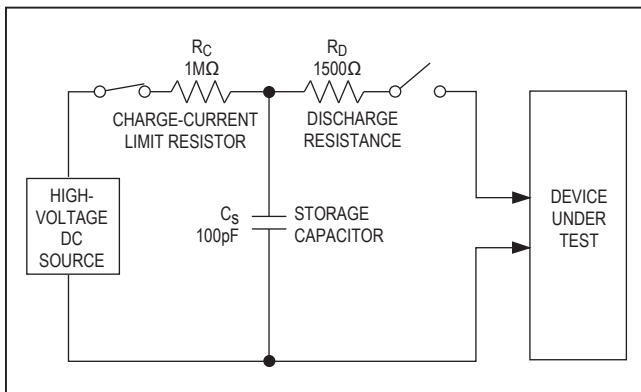


Figure 3a. Human Body ESD Test Modules

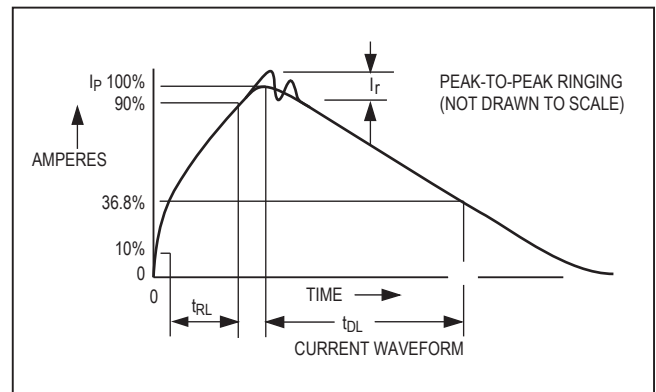


Figure 3b. Human Body Current Waveform

## Applications Information

### Supply Bypassing

Bypass  $V_{CC}$  with high-frequency surface-mount ceramic  $0.1\mu\text{F}$  and  $0.001\mu\text{F}$  capacitors in parallel, as close to the device as possible, with the  $0.001\mu\text{F}$  valued capacitor the closest to the device. For additional supply bypassing, place a  $10\mu\text{F}$  tantalum or ceramic capacitor at the point where power enters the circuit board.

### Differential Traces

Output trace characteristics affect the performance of the MAX9111/MAX9113. Use controlled impedance traces to match trace impedance to both transmission medium impedance and the termination resistor. Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Maintain the distance between the differential traces to avoid discontinuities in differential impedance. Avoid  $90^\circ$  turns and minimize the number of vias to further prevent impedance discontinuities.

### Cables and Connectors

Transmission media should have a differential characteristic impedance of about  $100\Omega$ . Use cables and connectors that have matched impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

### Termination

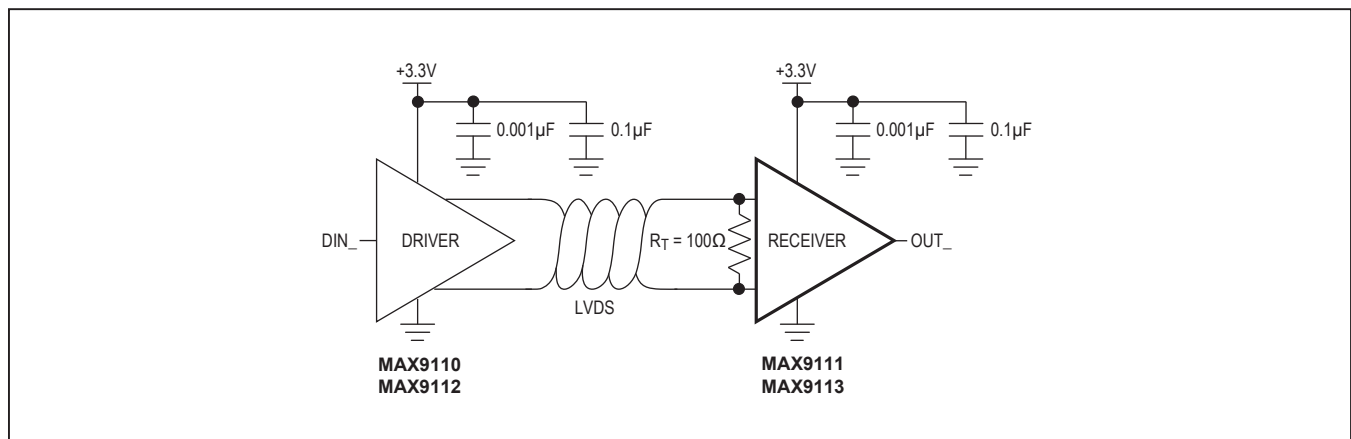
The MAX9111/MAX9113 input differential voltage depends on the driver current and termination resistance. Refer to the MAX9110/MAX9112 differential driver data sheet for this information.

Minimize the distance between the termination resistor and receiver inputs. Use a single 1% to 2% surface-mount resistor across the receiver inputs.

### Board Layout

For LVDS applications, a four-layer PCB that provides separate power, ground, LVDS signals, and input signals is recommended. Isolate the input and LVDS signals from each other to prevent coupling. For best results, separate the input and LVDS signal planes with the power and ground planes.

## Typical Operating Circuit



## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX9111EKA	-40°C to +85°C	8 SOT23	AAEE
MAX9111ESA	-40°C to +85°C	8 SO	—
MAX9113EKA	-40°C to +85°C	8 SOT23	AAED
MAX9113ESA	-40°C to +85°C	8 SO	—
MAX9113ASA/V+	-40°C to +125°C	8 SO	—
MAX9113ATA/VY+T	-40°C to +125°C	8 TDFN	+BST

/V denotes an automotive qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

## Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.
8 SOT23	K8+1	<a href="#">21-0078</a>
8 SO	S8+2	<a href="#">21-0041</a>
8 TDFN	T822CY+2	<a href="#">21-100341</a>

## Chip Information

PROCESS: CMOS

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	—	Initial release	—
1	2/07	—	1, 2, 8, 10, 11
2	12/07	Updated <i>Ordering Information</i> , temperature, <i>Switching Characteristics</i> , <i>Fail-Safe</i> section.	1, 2, 3, 7
3	3/09	Added <i>IV</i> designation to <i>Ordering Information</i> and updated <i>Termination</i> section.	1, 8
4	1/19	Updated <i>Ordering Information</i> , <i>Applications</i> , <i>Pin Configuration</i> , <i>Absolute Maximum Rating</i> , <i>Package Information</i>	1, 2, 9
5	5/19	Updated <i>Pin Configuration</i> and <i>Ordering Information</i> table	1, 8, 11
6	5/19	Updated <i>Electrical Characteristics</i> table	3
7	6/19	Updated <i>Electrical Characteristics</i> table	4

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- ✓ Alternative Solution
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