THE DATASHEET OF

N25Q00AA13GSF40F TR

www.win-source.net 0086-755-83957316

Micron Serial NOR Flash Memory

3V, Multiple I/O, 4KB Sector Erase

N25Q00AA

Features

- Stacked device (four 256Mb die)
- SPI-compatible serial bus interface
- Double transfer rate (DTR) mode
- 2.7–3.6V single supply voltage
- 108 MHz (MAX) clock frequency supported for all protocols in single transfer rate (STR) mode
- 54 MHz (MAX) clock frequency supported for all protocols in DTR mode
- Dual/quad I/O instruction provides increased throughput up to 54 MB/s
- Supported protocols
  - Extended SPI, dual I/O, and quad I/O
  - DTR mode supported on all
- Execute-in-place (XIP) mode for all three protocols
  - Configurable via volatile or nonvolatile registers
  - Enables memory to work in XIP mode directly after power-on
- PROGRAM/ERASE SUSPEND operations
- Available protocols
  - Available READ operations
  - Quad or dual output fast read
  - Quad or dual I/O fast read
- Flexible to fit application
  - Configurable number of dummy cycles
  - Output buffer configurable
- Software reset
- 3-byte and 4-byte addressability mode supported
- 64-byte, user-lockable, one-time programmable (OTP) dedicated area
- Erase capability
  - Subsector erase 4KB uniform granularity blocks
  - Sector erase 64KB uniform granularity blocks
  - Single die erase (32MB)
- Write protection
  - Software write protection applicable to every 64KB sector via volatile lock bit
  - Hardware write protection: protected area size defined by five nonvolatile bits (BP0, BP1, BP2, BP3, and TB)
  - Additional smart protections, available upon request
- Electronic signature
  - JEDEC-standard 2-byte signature (BA21h)
  - Unique ID code (UID): 17 read-only bytes, including: Two additional extended device ID bytes to identify device factory options; and customized factory data (14 bytes)
- Minimum 100,000 ERASE cycles per sector
- More than 20 years data retention
- Packages – JEDEC-standard, all RoHS-compliant
  - L-PBGA-24b05/6mm x 8mm (also known as LBGA24)
  - SOP2-16/300 mils (also known as SO16W, SO16-Wide, SOIC-16)

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Device Description

N25Q is a high-performance multiple input/output serial Flash memory device manufactured on 65nm NOR technology. It features execute-in-place (XIP) functionality, advanced write protection mechanisms, and a high-speed SPI-compatible bus interface. Innovative, high-performance, dual and quad input/output instructions enable double or quadruple the transfer bandwidth for READ and PROGRAM operations.

Features

The 1Gb N25Q is a stacked device that contains four 256Mb die. From a user standpoint this stacked device behaves as a monolithic device, except with regard to READ MEMORY and ERASE operations and status polling. The device contains a single chip select (S#).

The memory is organized as 2048 (64KB) main sectors that are further divided into 16 subsectors each (32,768 subsectors in total). The memory can be erased one 4KB subsector at a time, 64KB sectors at a time, or single die (256Mb) at a time.

The memory can be write protected by software through volatile and nonvolatile protection features, depending on the application needs. The protection granularity is of 64KB (sector granularity) for volatile protections

The device has 64 one-time programmable (OTP) bytes that can be read and programmed with the READ OTP and PROGRAM OTP commands. These 64 bytes can also be permanently locked with a PROGRAM OTP command.

The device also has the ability to pause and resume PROGRAM and ERASE cycles by using dedicated PROGRAM/ERASE SUSPEND and RESUME instructions.

3-Byte Address and 4-Byte Address Modes

The device features 3-byte or 4-byte address modes to access memory beyond 128Mb.

When 4-byte address mode is enabled, all commands requiring an address must be entered and exited with a 4-byte address mode command: ENTER 4-BYTE ADDRESS MODE command and EXIT 4-BYTE ADDRESS MODE command. The 4-byte address mode can also be enabled through the nonvolatile configuration register. See Registers for more information.

Operating Protocols

The memory can be operated with three different protocols:

- Extended SPI (standard SPI protocol upgraded with dual and quad operations)
- Dual I/O SPI
- Quad I/O SPI

The standard SPI protocol is extended and enhanced by dual and quad operations. In addition, the dual SPI and quad SPI protocols improve the data access time and throughput of a single I/O device by transmitting commands, addresses, and data across two or four data lines.

Each protocol contains unique commands to perform READ operations in DTR mode. This enables high data throughput while running at lower clock frequencies.

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XIP Mode

XIP mode requires only an address (no instruction) to output data, improving random access time and eliminating the need to shadow code onto RAM for fast execution.

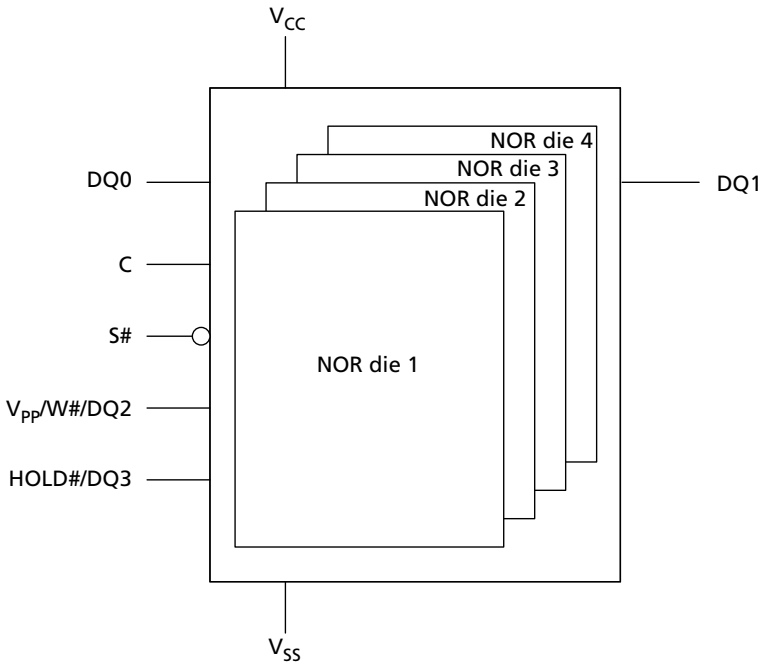
All protocols support XIP operation. For flexibility, multiple XIP entry and exit methods are available. For applications that must enter XIP mode immediately after power-up, nonvolatile configuration register bit settings can enable XIP as the default mode.

Device Configurability

The N25Q family offers additional features that are configured through the nonvolatile configuration register for default and/or nonvolatile settings. Volatile settings can be configured through the volatile and volatile-enhanced configuration registers. These configurable features include the following:

- Number of dummy cycles for the fast READ commands
- Output buffer impedance
- SPI protocol types (extended SPI, DIO-SPI, or QIO-SPI)
- Required XIP mode
- Enabling/disabling HOLD (RESET function)
- Enabling/disabling wrap mode

Figure 1: Logic Diagram



Note: 1. Reset functionality is available in devices with a dedicated part number. See Part Number Ordering Information for more details.

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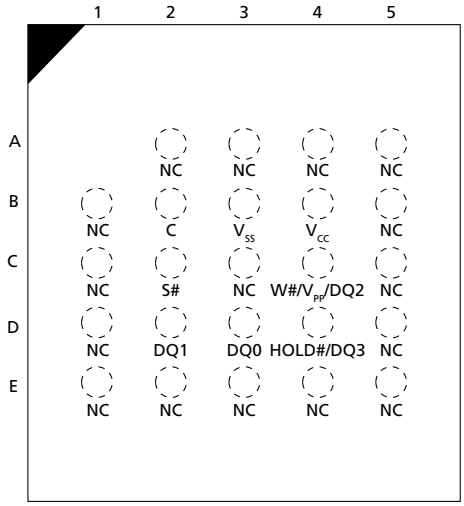
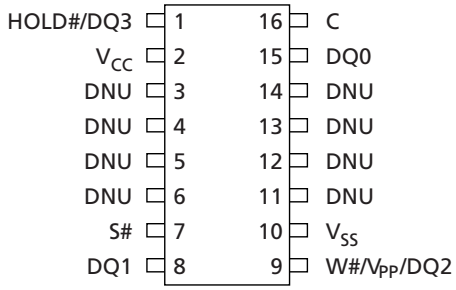
Signal Assignments

Figure 2: 24-Ball LBGA (Balls Down)



Note: 1. See Part Number Ordering Information for complete package names and details.

Figure 3: 16-Pin, Plastic Small Outline — SO16 (Top View)



Note: 1. Reset functionality is available in devices with a dedicated part number. See Part Number Ordering Information for complete package names and details.

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Signal Descriptions

The signal description table below is a comprehensive list of signals for the N25 family devices. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 1: Signal Descriptions

Symbol	Type	Description
C	Input	**Clock:** Provides the timing of the serial interface. Commands, addresses, or data present at serial data inputs are latched on the rising edge of the clock. Data is shifted out on the falling edge of the clock.
S#	Input	**Chip select:** When S# is HIGH, the device is deselected and DQ1 is at High-Z. When in extended SPI mode, with the device deselected, DQ1 is tri-stated. Unless an internal PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress, the device enters standby power mode (not deep power-down mode). Driving S# LOW enables the device, placing it in the active power mode. After power-up, a falling edge on S# is required prior to the start of any command.
DQ0	Input and I/O	**Serial data:** Transfers data serially into the device. It receives command codes, addresses, and the data to be programmed. Values are latched on the rising edge of the clock. DQ0 is used for input/output during the following operations: DUAL OUTPUT FAST READ, QUAD OUTPUT FAST READ, DUAL INPUT/OUTPUT FAST READ, and QUAD INPUT/OUTPUT FAST READ. When used for output, data is shifted out on the falling edge of the clock. In DIO-SPI, DQ0 always acts as an input/output. In QIO-SPI, DQ0 always acts as an input/output, with the exception of the PROGRAM or ERASE cycle performed with V_{PP}. The device temporarily enters the extended SPI protocol and then returns to QIO-SPI as soon as V_{PP} goes LOW.
DQ1	Output and I/O	**Serial data:**Transfers data serially out of the device. Data is shifted out on the falling edge of the clock. DQ1 is used for input/output during the following operations: DUAL INPUT FAST PROGRAM, QUAD INPUT FAST PROGRAM, DUAL INPUT EXTENDED FAST PROGRAM, and QUAD INPUT EXTENDED FAST PROGRAM. When used for input, data is latched on the rising edge of the clock. In DIO-SPI, DQ1 always acts as an input/output. In QIO-SPI, DQ1 always acts as an input/output, with the exception of the PROGRAM or ERASE cycle performed with the enhanced program supply voltage (V_{PP}). In this case the device temporarily enters the extended SPI protocol and then returns to QIO-SPI as soon as V_{PP} goes LOW.
DQ2	Input and I/O	**DQ2:** When in QIO-SPI mode or in extended SPI mode using QUAD FAST READ commands, the signal functions as DQ2, providing input/output. All data input drivers are always enabled except when used as an output. Micron recommends customers drive the data signals normally (to avoid unnecessary switching current) and float the signals before the memory device drives data on them.
DQ3	Input and I/O	**DQ3:** When in quad SPI mode or in extended SPI mode using quad FAST READ commands, the signal functions as DQ3, providing input/output. HOLD# is disabled and RESET# is disabled if the device is selected.
RESET#	Control Input	**RESET:** This is a hardware RESET# signal. When RESET# is driven HIGH, the memory is in the normal operating mode. When RESET# is driven LOW, the memory enters reset mode and output is High-Z. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost.

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Table 1: Signal Descriptions (Continued)

Symbol	Type	Description
HOLD#	Control Input	**HOLD:** Pauses any serial communications with the device without deselecting the device. DQ1 (output) is High-Z. DQ0 (input) and the clock are "Don't Care." To enable HOLD, the device must be selected with S# driven LOW. HOLD# is used for input/output during the following operations: QUAD OUTPUT FAST READ, QUAD INPUT/OUTPUT FAST READ, QUAD INPUT FAST PROGRAM, and QUAD INPUT EXTENDED FAST PROGRAM. In QIO-SPI, HOLD# acts as an I/O (DQ3 functionality), and the HOLD# functionality is disabled when the device is selected. When the device is deselected (S# is HIGH) in parts with RESET# functionality, it is possible to reset the device unless this functionality is not disabled by means of dedicated registers bits. The HOLD# functionality can be disabled using bit 4 of the NVCR or bit 4 of the VECR. On devices that include DTR mode capability, the HOLD# functionality is disabled as soon as a DTR operation is recognized.
W#	Control Input	**Write protect:** W# can be used as a protection control input or in QIO-SPI operations. When in extended SPI with single or dual commands, the WRITE PROTECT function is selectable by the voltage range applied to the signal. If voltage range is low (0V to V_{CC}), the signal acts as a write protection control input. The memory size protected against PROGRAM or ERASE operations is locked as specified in the status register block protect bits 3:0. W# is used as an input/output (DQ2 functionality) during QUAD INPUT FAST READ and QUAD INPUT/OUTPUT FAST READ operations and in QIO-SPI.
V_{PP}	Power	**Supply voltage:** If V_{PP} is in the voltage range of V_{PPH}, the signal acts as an additional power supply, as defined in the AC Measurement Conditions table. During QIFP, QIEFP, and QIO-SPI PROGRAM/ERASE operations, it is possible to use the additional V_{PP} power supply to speed up internal operations. However, to enable this functionality, it is necessary to set bit 3 of the VECR to 0. In this case, V_{PP} is used as an I/O until the end of the operation. After the last input data is shifted in, the application should apply V_{PP} voltage to V_{PP} within 200ms to speed up the internal operations. If the V_{PP} voltage is not applied within 200ms, the PROGRAM/ERASE operations start at standard speed. The default value of VECR bit 3 is 1, and the V_{PP} functionality for quad I/O modify operations is disabled.
V_{CC}	Power	**Device core power supply:** Source voltage.
V_{SS}	Ground	**Ground:** Reference for the V_{CC} supply voltage.
DNU	–	Do not use.
NC	–	No connect.

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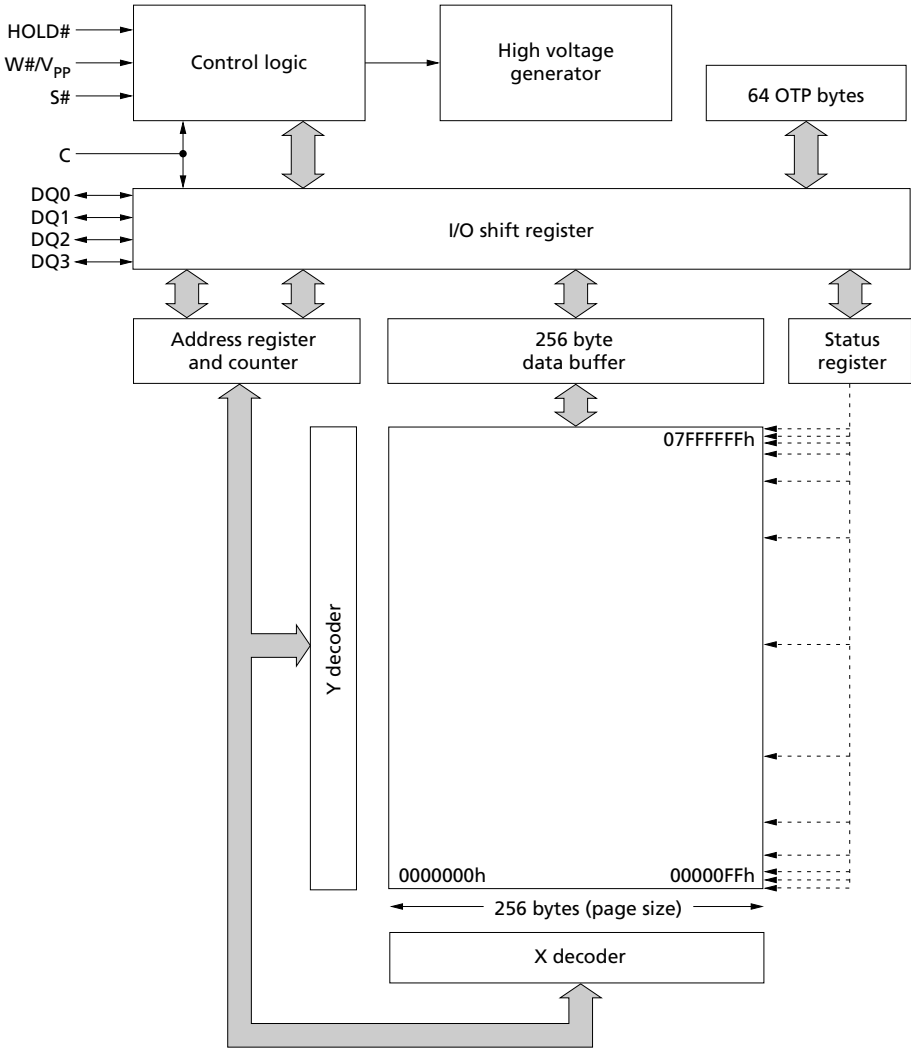
Memory Organization

Memory Configuration and Block Diagram

The memory is a stacked device comprised of four 256Mb chips. Each chip is internally partitioned into two 128Mb segments. Each page of memory can be individually programmed. Bits are programmed from one through zero. The device is subsector, sector, or single 256Mb chip erasable, but not page-erasable. Bits are erased from zero through one. The memory is configured as 134,217,728 bytes (8 bits each); 2048 sectors (64KB each); 32,768 subsectors (4KB each); and 524,288 pages (256 bytes each); and 64 OTP bytes are located outside the main memory array.

Figure 4: Block Diagram



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Memory Map – 1Gb Density

Table 2: Sectors[2047:0]

Sector	Subsector	Address Range	
		Start	End
2047	32767	07FFF000h	07FFFFFFh
	⋮	⋮	⋮
	32750	07FF0000h	07FF0FFFh
⋮	⋮	⋮	⋮
1023	16383	03FF F000h	03FF FFFFh
	⋮	⋮	⋮
	16368	03FF 0000h	03FF 0FFFh
⋮	⋮	⋮	⋮
511	8191	01FF F000h	01FF FFFFh
	⋮	⋮	⋮
	8176	01FF 0000h	01FF 0FFFh
⋮	⋮	⋮	⋮
255	4095	00FF F000h	00FF FFFFh
	⋮	⋮	⋮
	4080	00FF 0000h	00FF 0FFFh
⋮	⋮	⋮	⋮
127	2047	007F F000h	007F FFFFh
	⋮	⋮	⋮
	2032	007F 0000h	007F 0FFFh
⋮	⋮	⋮	⋮
63	1023	003F F000h	003F FFFFh
	⋮	⋮	⋮
	1008	003F 0000h	003F 0FFFh
⋮	⋮	⋮	⋮
0	15	0000 F000h	0000 FFFFh
	⋮	⋮	⋮
	0	0000 0000h	0000 0FFFh

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Device Protection

Table 3: Data Protection Using Device Protocols

Note 1 applies to the entire table

Protection by:	Description
Power-on reset and internal timer	Protects the device against inadvertent data changes while the power supply is outside the operating specification.
Command execution check	Ensures that the number of clock pulses is a multiple of one byte before executing a PROGRAM or ERASE command, or any command that writes to the device registers.
WRITE ENABLE operation	Ensures that commands modifying device data must be preceded by a WRITE ENABLE command, which sets the write enable latch bit in the status register.

Note: 1. Extended, dual, and quad SPI protocol functionality ensures that device data is protected from excessive noise.

Table 4: Memory Sector Protection Truth Table

Note 1 applies to the entire table

Sector Lock Register		
Sector Lock Down Bit	Sector Write Lock Bit	Memory Sector Protection Status
0	0	Sector unprotected from PROGRAM and ERASE operations. Protection status reversible.
0	1	Sector protected from PROGRAM and ERASE operations. Protection status reversible.
1	0	Sector unprotected from PROGRAM and ERASE operations. Protection status not reversible except by power cycle or reset.
1	1	Sector protected from PROGRAM and ERASE operations. Protection status not reversible except by power cycle or reset.

Note: 1. Sector lock register bits are written to when the WRITE TO LOCK REGISTER command is executed. The command will not execute unless the sector lock down bit is cleared (see the WRITE TO LOCK REGISTER command).

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Table 5: Protected Area Sizes – Upper Area

Note 1 applies to the entire table

Status Register Content					Memory Content	
Top/ Bottom Bit	BP3	BP2	BP1	BP0	Protected Area	Unprotected Area
0	0	0	0	0	None	All sectors
0	0	0	0	1	Sector 2047	Sectors (0 to 2046)
0	0	0	1	0	Sectors (2046 to 2047)	Sectors (0 to 2045)
0	0	0	1	1	Sectors (2044 to 2047)	Sectors (0 to 2043)
0	0	1	0	0	Sectors (2040 to 2047)	Sectors (0 to 2039)
0	0	1	0	1	Sectors (2032 to 2047)	Sectors (0 to 2031)
0	0	1	1	0	Sectors (2016 to 2047)	Sectors (0 to 2015)
0	0	1	1	1	Sectors (1984 to 2047)	Sectors (0 to 1983)
0	1	0	0	0	Sectors (1920 to 2047)	Sectors (0 to 1919)
0	1	0	0	1	Sectors (1792 to 2047)	Sectors (0 to 1791)
0	1	0	1	0	Sectors (1536 to 2047)	Sectors (0 to 1535)
0	1	0	1	1	Sectors (1024 to 2047)	Sectors (0 to 1023)
0	1	1	0	0	All sectors	None
0	1	1	0	1	All sectors	None
0	1	1	1	0	All sectors	None
0	1	1	1	1	All sectors	None

Note: 1. See the Status Register for details on the top/bottom bit and the BP 3:0 bits.

Table 6: Protected Area Sizes – Lower Area

Note 1 applies to the entire table

Status Register Content					Memory Content	
Top/ Bottom Bit	BP3	BP2	BP1	BP0	Protected Area	Unprotected Area
1	0	0	0	0	None	All sectors
1	0	0	0	1	Sector 0	Sectors (1 to 2047)
1	0	0	1	0	Sectors (0 to 1)	Sectors (2 to 2047)
1	0	0	1	1	Sectors (0 to 3)	Sectors (4 to 2047)
1	0	1	0	0	Sectors (0 to 7)	Sectors (8 to 2047)
1	0	1	0	1	Sectors (0 to 15)	Sectors (16 to 2047)
1	0	1	1	0	Sectors (0 to 31)	Sectors (32 to 2047)
1	0	1	1	1	Sectors (0 to 63)	Sectors (64 to 2047)
1	1	0	0	0	Sectors (0 to 127)	Sectors (128 to 2047)
1	1	0	0	1	Sectors (0 to 255)	Sectors (256 to 2047)

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Table 6: Protected Area Sizes – Lower Area (Continued)

Note 1 applies to the entire table

Status Register Content					Memory Content	
Top/ Bottom Bit	BP3	BP2	BP1	BP0	Protected Area	Unprotected Area
1	1	0	1	0	Sectors (0 to 511)	Sectors (512 to 2047)
1	1	0	1	1	Sectors (0 to 1023)	Sectors (1024 to 2047)
1	1	1	0	0	All sectors	None
1	1	1	0	1	All sectors	None
1	1	1	1	0	All sectors	None
1	1	1	1	1	All sectors	None

Note: 1. See the Status Register for details on the top/bottom bit and the BP 3:0 bits.

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Serial Peripheral Interface Modes

The device can be driven by a microcontroller while its serial peripheral interface is in either of the two modes shown here. The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring data. Input data is latched in on the rising edge of the clock, and output data is available from the falling edge of the clock.

Table 7: SPI Modes

Note 1 applies to the entire table

SPI Modes	Clock Polarity
CPOL = 0, CPHA = 0	C remains at 0 for (CPOL = 0, CPHA = 0)
CPOL = 1, CPHA = 1	C remains at 1 for (CPOL = 1, CPHA = 1)

Note: 1. The listed SPI modes are supported in extended, dual, and quad SPI protocols.

Shown below is an example of three memory devices in extended SPI protocol in a simple connection to an MCU on an SPI bus. Because only one device is selected at a time, that one device drives DQ1, while the other devices are High-Z.

Resistors ensure the device is not selected if the bus master leaves S# High-Z. The bus master might enter a state in which all input/output is High-Z simultaneously, such as when the bus master is reset. Therefore, the serial clock must be connected to an external pull-down resistor so that S# is pulled HIGH while the serial clock is pulled LOW. This ensures that S# and the serial clock are not HIGH simultaneously and that ^{t}SHCH is met. The typical resistor value of 100kΩ, assuming that the time constant R × Cp (Cp = parasitic capacitance of the bus line), is shorter than the time the bus master leaves the SPI bus in High-Z.

Example: Cp = 50pF, that is R × Cp = 5µs. The application must ensure that the bus master never leaves the SPI bus High-Z for a time period shorter than 5µs. W# and HOLD# should be driven either HIGH or LOW, as appropriate.

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Figure 5: Bus Master and Memory Devices on the SPI Bus

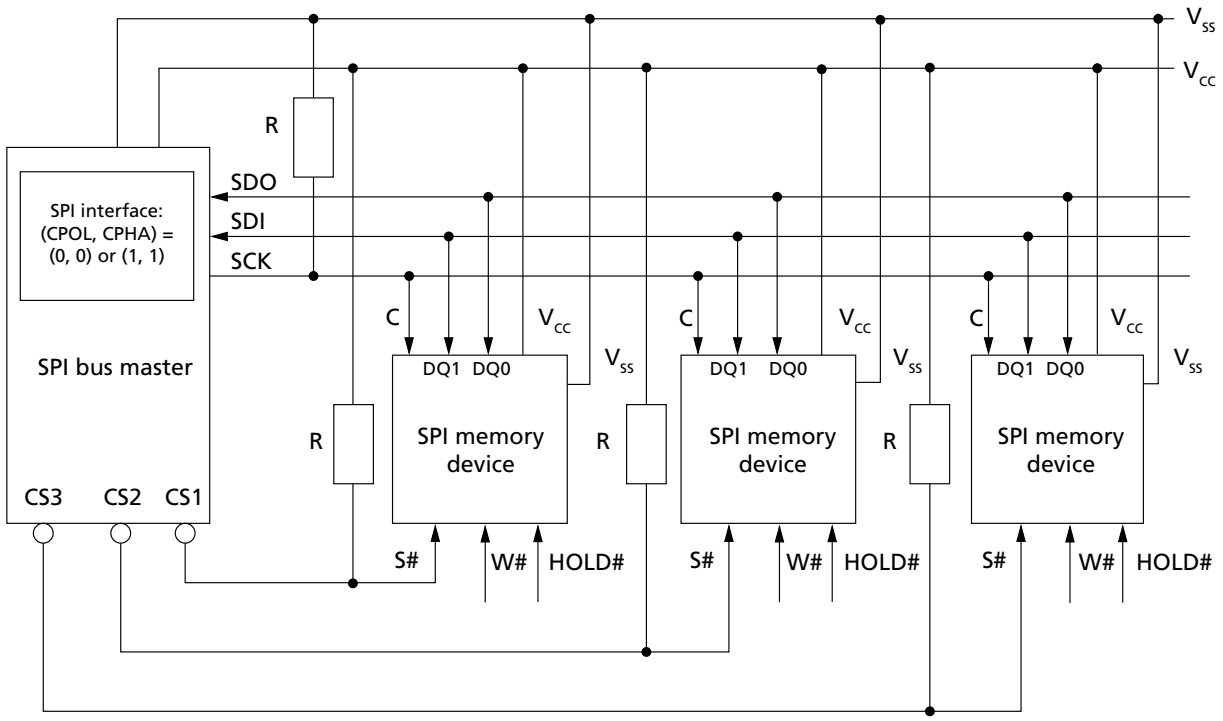
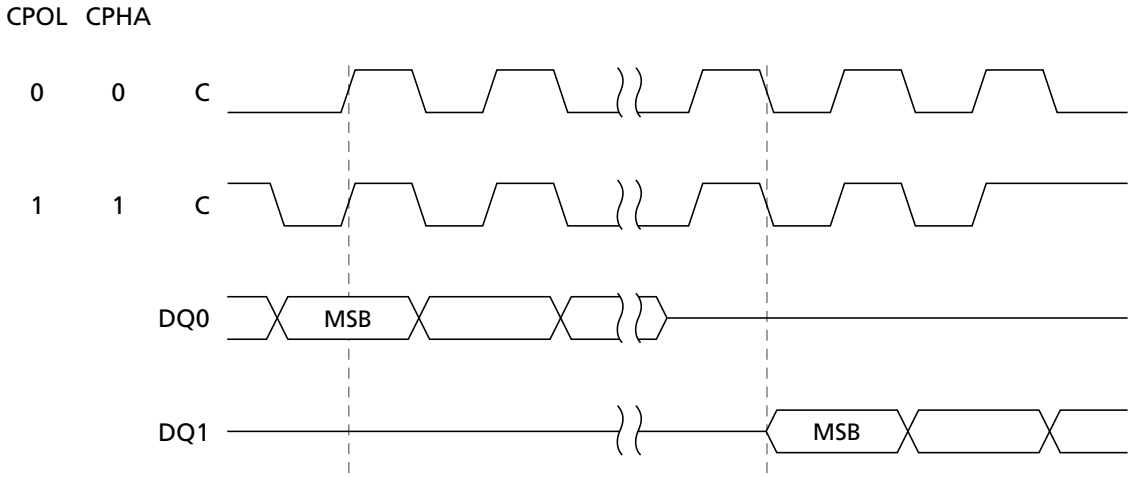


Figure 6: SPI Modes



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SPI Protocols

Table 8: Extended, Dual, and Quad SPI Protocols

Protocol Name	Command Input	Address Input	Data Input/Output	Description
Extended	DQ0	Multiple DQ*n* lines, depending on the command	Multiple DQ*n* lines, depending on the command	Device default protocol from the factory. Additional commands extend the standard SPI protocol and enable address or data transmission on multiple DQ*n* lines.
Dual	DQ[1:0]	DQ[1:0]	DQ[1:0]	**Volatile selectable:** When the enhanced volatile configuration register bit 6 is set to 0 and bit 7 is set to 1, the device enters the dual SPI protocol immediately after the WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command. The device returns to the default protocol after the next power-on. In addition, the device can return to default protocol using the rescue sequence or through new WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command, without power-off or power-on. **Nonvolatile selectable:** When nonvolatile configuration register bit 2 is set, the device enters the dual SPI protocol after the next power-on. Once this register bit is set, the device defaults to the dual SPI protocol after all subsequent power-on sequences until the nonvolatile configuration register bit is reset to 1.
Quad[1]	DQ[3:0]	DQ[3:0]	DQ[3:0]	**Volatile selectable:** When the enhanced volatile configuration register bit 7 is set to 0, the device enters the quad SPI protocol immediately after the WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command. The device returns to the default protocol after the next power-on. In addition, the device can return to default protocol using the rescue sequence or through new WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command, without power-off or power-on. **Nonvolatile selectable:** When nonvolatile configuration register bit 3 is set to 0, the device enters the quad SPI protocol after the next power-on. Once this register bit is set, the device defaults to the quad SPI protocol after all subsequent power-on sequences until the nonvolatile configuration register bit is reset to 1.

Note: 1. In quad SPI protocol, all command/address input and data I/O are transmitted on four lines except during a PROGRAM and ERASE cycle performed with V_{PP}. In this case, the device enters the extended SPI protocol to temporarily allow the application to perform a PROGRAM/ERASE SUSPEND operation or to check the write-in-progress bit in the status register or the program/erase controller bit in the flag status register. Then, when V_{PP} goes LOW, the device returns to the quad SPI protocol.

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Nonvolatile and Volatile Registers

The device features the following volatile and nonvolatile registers that users can access to store device parameters and operating configurations:

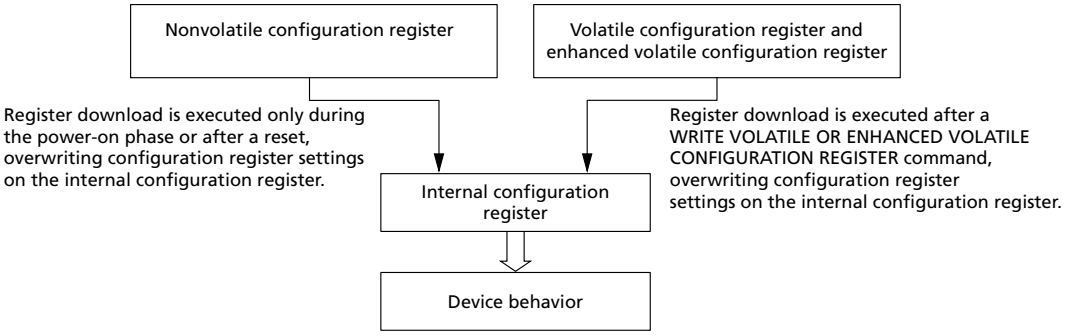
- Status register
- Nonvolatile and volatile configuration registers
- Extended address register
- Enhanced volatile configuration register
- Flag status register
- Lock register

Note: The lock register is defined in READ LOCK REGISTER Command.

The working condition of memory is set by an internal configuration register that is not directly accessible to users. As shown below, parameters in the internal configuration register are loaded from the nonvolatile configuration register during each device boot phase or power-on reset. In this sense, then, the nonvolatile configuration register contains the default settings of memory.

Also, during the life of an application, each time a WRITE VOLATILE or ENHANCED VOLATILE CONFIGURATION REGISTER command executes to set configuration parameters in these respective registers, these new settings are copied to the internal configuration register. Therefore, memory settings can be changed in real time. However, at the next power-on reset, the memory boots according to the memory settings defined in the nonvolatile configuration register parameters.

Figure 7: Internal Configuration Register



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Status Register

Table 9: Status Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
7	Status register write enable/disable	0 = Enabled 1 = Disabled	**Nonvolatile bit:** Used with the W# signal to enable or disable writing to the status register.	3
5	Top/bottom	0 = Top 1 = Bottom	**Nonvolatile bit:** Determines whether the protected memory area defined by the block protect bits starts from the top or bottom of the memory array.	4
6, 4:2	Block protect 3–0	See Protected Area Sizes – Upper Area and Lower Area tables in Device Protection	**Nonvolatile bit:** Defines memory to be software protected against PROGRAM or ERASE operations. When one or more block protect bits is set to 1, a designated memory area is protected from PROGRAM and ERASE operations.	4
1	Write enable latch	0 = Cleared (Default) 1 = Set	**Volatile bit:** The device always powers up with this bit cleared to prevent inadvertent WRITE STATUS REGISTER, PROGRAM, or ERASE operations. To enable these operations, the WRITE ENABLE operation must be executed first to set this bit.	2, 5
0	Write in progress	0 = Ready 1 = Busy	**Volatile bit:** Indicates if one of the following command cycles is in progress: WRITE STATUS REGISTER WRITE NONVOLATILE CONFIGURATION REGISTER PROGRAM ERASE	2, 6

Notes:
1. Bits can be read from or written to using READ STATUS REGISTER or WRITE STATUS REGISTER commands, respectively.
2. Volatile bits are cleared to 0 by a power cycle or reset.
3. The status register write enable/disable bit, combined with the W#/V_{PP} signal as described in the Signal Descriptions, provides hardware data protection for the device as follows: When the enable/disable bit is set to 1, and the W#/V_{PP} signal is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not execute. The only way to exit this hardware-protected mode is to drive W#/V_{PP} HIGH.
4. See Protected Area Sizes tables. The DIE ERASE command is executed only if all bits are 0.
5. In case of protection error this volatile bit is set and can be reset only by means of a CLEAR FLAG STATUS REGISTER command.
6. Program or erase controller bit = NOT (write in progress bit).

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Nonvolatile and Volatile Configuration Registers

Table 10: Nonvolatile Configuration Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
15:12	Number of dummy clock cycles	0000 (identical to 1111) 0001 0010 . . 1101 1110 1111	Sets the number of dummy clock cycles subsequent to all FAST READ commands. The default setting targets the maximum allowed frequency and guarantees backward compatibility.	2, 3
11:9	XIP mode at power-on reset	000 = XIP: Fast Read 001 = XIP: Dual Output Fast Read 010 = XIP: Dual I/O Fast Read 011 = XIP: Quad Output Fast Read 100 = XIP: Quad I/O Fast Read 101 = Reserved 110 = Reserved 111 = Disabled (Default)	Enables the device to operate in the selected XIP mode immediately after power-on reset.	
8:6	Output driver strength	000 = Reserved 001 = 90 Ohms 010 = 60 Ohms 011 = 45 Ohms 100 = Reserved 101 = 20 Ohms 110 = 15 Ohms 111 = 30 (Default)	Optimizes impedance at $V_{CC}/2$ output voltage.	
5	Reserved	X	"Don't Care."	
4	Reset/hold	0 = Disabled 1 = Enabled (Default)	Enables or disables hold or reset. (Available on dedicated part numbers.)	
3	Quad I/O protocol	0 = Enabled 1 = Disabled (Default, Extended SPI protcocol)	Enables or disables quad I/O protocol.	4
2	Dual I/O protocol	0 = Enabled 1 = Disabled (Default, Extended SPI protocol)	Enables or disables dual I/O protocol.	4
1	128Mb segment select	0 = Upper 128Mb segment 1 = Lower 128Mb segment (Default)	Selects a 128Mb segment as default for 3B address operations. See also the extended address register.	
0	Address bytes	0 = Enable 4B address 1 = Enable 3B address (Default)	Defines the number of address bytes for a command.	

Notes: 1. Settings determine device memory configuration after power-on. The device ships from the factory with all bits erased to 1 (FFFFh). The register is read from or written to by READ NONVOLATILE CONFIGURATION REGISTER or WRITE NONVOLATILE CONFIGURATION REGISTER commands, respectively.

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2. The 0000 and 1111 settings are identical in that they both define the default state, which is the maximum frequency of ^{f}c = 108 MHz. This ensures backward compatibility.
3. If the number of dummy clock cycles is insufficient for the operating frequency, the memory reads wrong data. The number of cycles must be set according to and sufficient for the clock frequency, which varies by the type of FAST READ command, as shown in the Supported Clock Frequencies table.
4. If bits 2 and 3 are both set to 0, the device operates in quad I/O. When bits 2 or 3 are reset to 0, the device operates in dual I/O or quad I/O respectively, after the next power-on.

Table 11: Volatile Configuration Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
7:4	Number of dummy clock cycles	0000 (identical to 1111) 0001 0010 . . 1101 1110 1111	Sets the number of dummy clock cycles subsequent to all FAST READ commands. The default setting targets maximum allowed frequency and guarantees backward compatibility.	2, 3
3	XIP	0 1	Enables or disables XIP. For device part numbers with feature digit equal to 2 or 4, this bit is always "Don't Care," so the device operates in XIP mode without setting this bit.	
2	Reserved	x = Default	0b = Fixed value.	
1:0	Wrap	00 = 16-byte boundary aligned	16-byte wrap: Output data wraps within an aligned 16-byte boundary starting from the address (3-byte or 4-byte) issued after the command code.	4
		01 = 32-byte boundary aligned	32-byte wrap: Output data wraps within an aligned 32-byte boundary starting from the address (3-byte or 4-byte) issued after the command code.	
		10 = 64-byte boundary aligned	64-byte wrap: Output data wraps within an aligned 64-byte boundary starting from the address (3-byte or 4-byte) issued after the command code.	
		11 = sequential (default)	Continuous reading (default): All bytes are read sequentially.	

Notes:
1. Settings determine the device memory configuration upon a change of those settings by the WRITE VOLATILE CONFIGURATION REGISTER command. The register is read from or written to by READ VOLATILE CONFIGURATION REGISTER or WRITE VOLATILE CONFIGURATION REGISTER commands respectively.
2. The 0000 and 1111 settings are identical in that they both define the default state, which is the maximum frequency of ^{f}c = 108 MHz. This ensures backward compatibility.
3. If the number of dummy clock cycles is insufficient for the operating frequency, the memory reads wrong data. The number of cycles must be set according to and be sufficient for the clock frequency, which varies by the type of FAST READ command, as shown in the Supported Clock Frequencies table.
4. See the Sequence of Bytes During Wrap table.

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Table 12: Sequence of Bytes During Wrap

Starting Address	16-Byte Wrap	32-Byte Wrap	64-Byte Wrap
0	0-1-2- . . . -15-0-1- . .	0-1-2- . . . -31-0-1- . .	0-1-2- . . . -63-0-1- . .
1	1-2- . . . -15-0-1-2- . .	1-2- . . . -31-0-1-2- . .	1-2- . . . -63-0-1-2- . .
15	15-0-1-2-3- . . . -15-0-1- . .	15-16-17- . . . -31-0-1- . .	15-16-17- . . . -63-0-1- . .
31	31-16-17- . . . -31-16-17- . .	31-0-1-2-3- . . . -31-0-1- . .	31-32-33- . . . -63-0-1- . .
63	63-48-49- . . . -63-48-49- . .	63-32-33- . . . -63-32-33- . .	63-0-1- . . . -63-0-1- . .

Table 13: Supported Clock Frequencies – STR

Note 1 applies to entire table

Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ
1	90	80	50	43	30
2	100	90	70	60	40
3	108	100	80	75	50
4	108	105	90	90	60
5	108	108	100	100	70
6	108	108	105	105	80
7	108	108	108	108	86
8	108	108	108	108	95
9	108	108	108	108	105
10	108	108	108	108	108

Note: 1. Values are guaranteed by characterization and not 100% tested in production.

Table 14: Supported Clock Frequencies – DTR

Note 1 applies to entire table

Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ
1	45	40	25	30	15
2	50	45	35	38	20
3	54	50	40	45	25
4	54	53	45	47	30
5	54	54	50	50	35
6	54	54	53	53	40
7	54	54	54	54	43
8	54	54	54	54	48
9	54	54	54	54	53
10	54	54	54	54	54

Note: 1. Values are guaranteed by characterization and not 100% tested in production.

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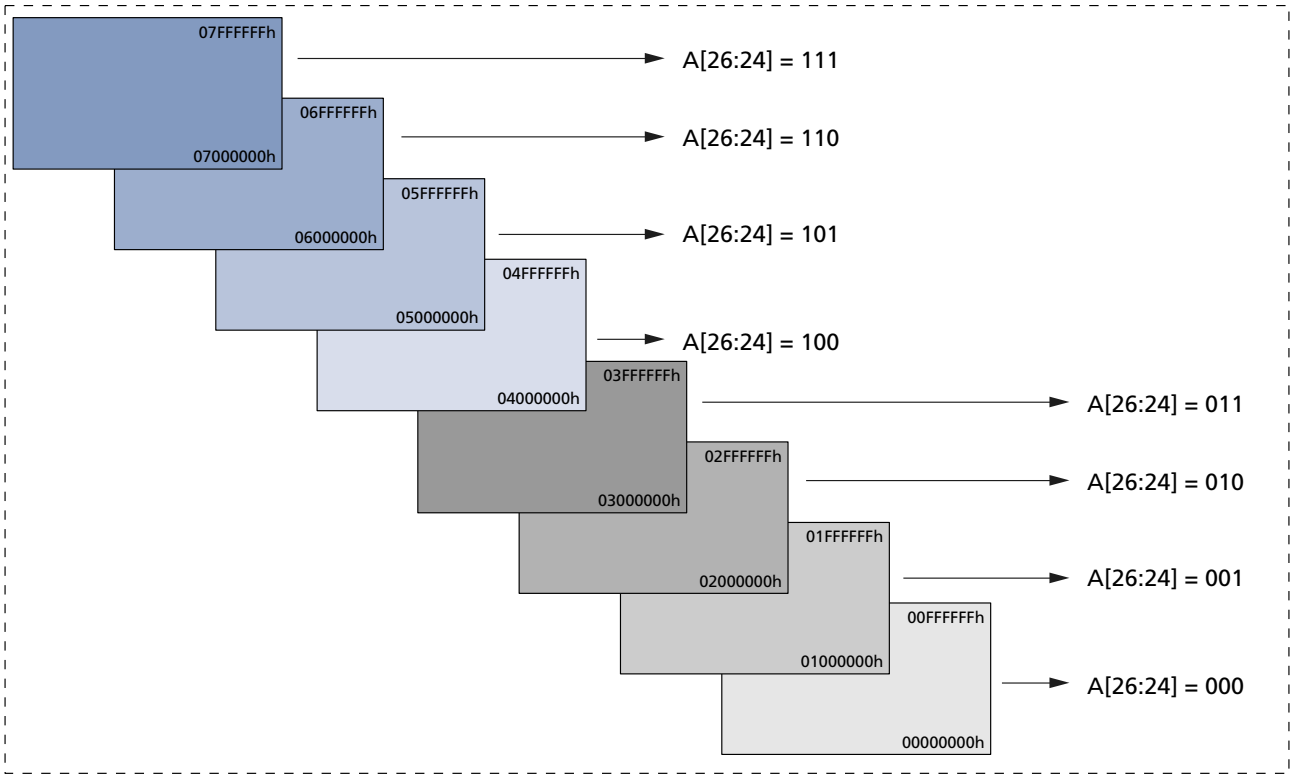
Extended Address Register

In the case of 3-byte addressability mode, the device includes an extended address register that provides a fourth address byte A[31:24], enabling access to memory beyond 128Mb. The extended address register bits [2:0] are used to select one of the eight 128Mb segments of the memory array.

Figure 8: Upper and Lower Memory Array Segments



The PROGRAM and ERASE operations act upon the 128Mb segment selected in the extended address register.

The READ operation begins reading in the selected 128Mb segment. It is bound by the 256Mb (die segment) to which the 128Mb segment belongs. In a continuos read, when the last byte of the die segment selected is read, the next byte output is the first byte of the same die segment; therefore, a download of the whole array is not possible with one READ operation. The value of the extended address register does not change when a READ operation crosses the selected 128Mb boundary.

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Table 15: Extended Address Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description
7	A[31:27]	0 = Reserved	–
6			
5			
4			
3			
2	A[26:24]	111 = Upper 128Mb segment 110 = Seventh 128Mb segment 101 = Sixth 128Mb segment 100 = Fifth 128Mb segment 011 = Fourth 128Mb segment 010 = Third 128Mb segment 001 = Second 128Mb segment 000 = Lower 128Mb segment (default)	Enable selecting 128Mb segmentation. For A[26:24], the default setting is determined by bit 1 of the nonvolatile configuration register. However, this setting can be changed using the WRITE EXTENDED ADDRESS REGISTER command.
1			
0			

Note: 1. The extended address register is for an application that supports only 3-byte addressing. It extends the device's first three address bytes A[23:0] to a fourth address byte A[31:24] to enable memory access beyond 128Mb. The extended address register bits [2:0] are used to select one of the eight 128Mb segments of the memory array. If 4-byte addressing is enabled, extended address register settings are ignored.

Enhanced Volatile Configuration Register

Table 16: Enhanced Volatile Configuration Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
7	Quad I/O protocol	0 = Enabled 1 = Disabled (Default, extended SPI protocol)	Enables or disables quad I/O protocol.	2
6	Dual I/O protocol	0 = Enabled 1 = Disabled (Default, extended SPI protocol)	Enables or disables dual I/O protocol.	2
5	Reserved	x = Default	0b = Fixed value.	
4	Reset/hold	0 = Disabled 1 = Enabled (Default)	Enables or disables hold or reset. (Available on dedicated part numbers.)	
3	V_{PP} accelerator	0 = Enabled 1 = Disabled (Default)	Enables or disables V_{PP} acceleration for QUAD INPUT FAST PROGRAM and QUAD INPUT EXTENDED FAST PROGRAM OPERATIONS.	

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Table 16: Enhanced Volatile Configuration Register Bit Definitions (Continued)

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
2:0	Output driver strength	000 = Reserved 001 = 90 Ohms 010 = 60 Ohms 011 = 45 Ohms 100 = Reserved 101 = 20 Ohms 110 = 15 Ohms 111 = 30 (Default)	Optimizes impedance at $V_{CC}/2$ output voltage.	

Notes:
1. Settings determine the device memory configuration upon a change of those settings by the WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command. The register is read from or written to in all protocols by READ ENHANCED VOLATILE CONFIGURATION REGISTER or WRITE ENHANCED VOLATILE CONFIGURATION REGISTER commands, respectively.
2. If bits 6 and 7 are both set to 0, the device operates in quad I/O. When either bit 6 or 7 is reset to 0, the device operates in dual I/O or quad I/O respectively following the next WRITE ENHANCED VOLATILE CONFIGURATION command.

Flag Status Register

Table 17: Flag Status Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
7	Program or erase controller	0 = Busy 1 = Ready	**Status bit:** Indicates whether one of the following command cycles is in progress: WRITE STATUS REGISTER, WRITE NONVOLATILE CONFIGURATION REGISTER, PROGRAM, or ERASE.	2, 5
6	Erase suspend	0 = Not in effect 1 = In effect	**Status bit:** Indicates whether an ERASE operation has been or is going to be suspended.	2
5	Erase	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether an ERASE operation has succeeded or failed.	3, 4
4	Program	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether a PROGRAM operation has succeeded or failed; also an attempt to program a 0 to a 1 when $V_{PP} = V_{PPH}$ and the data pattern is a multiple of 64 bits.	3, 4
3	V_{PP}	0 = Enabled 1 = Disabled (Default)	**Error bit:** Indicates an invalid voltage on V_{PP} during a PROGRAM or ERASE operation.	3, 4
2	Program suspend	0 = Not in effect 1 = In effect	**Status bit:** Indicates whether a PROGRAM operation has been or is going to be suspended.	2
1	Protection	0 = Clear 1 = Failure or protection error	**Error bit:** Indicates whether an ERASE or PROGRAM operation has attempted to modify the protected array sector, or whether a PROGRAM operation has attempted to access the locked OTP space.	3, 4

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Table 17: Flag Status Register Bit Definitions (Continued)

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
0	Addressing	0 = 3 bytes addressing 1 = 4 bytes addressing	**Status bit:** Indicates whether 3-byte or 4-byte address mode is enabled.	2

Notes:
1. Register bits are read by READ FLAG STATUS REGISTER command. All bits are volatile.
2. Status bits are reset automatically.
3. Error bits must be cleared through the CLEAR FLAG STATUS REGISTER command.
4. These error flags are "sticky." They must be cleared through the CLEAR STATUS REGISTER command.
5. Program or erase controller bit = NOT (write in progress bit).

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Command Definitions

Table 18: Command Set

Note 1 applies to entire table

Command	Code	Extended	Dual I/O	Quad I/O	Data Bytes	Notes
RESET Operations						
RESET ENABLE	66h	Yes	Yes	Yes	0	2
RESET MEMORY	99h					
IDENTIFICATION Operations						
READ ID	9E/9Fh	Yes	No	No	1 to 20	2
MULTIPLE I/O READ ID	AFh	No	Yes	Yes	1 to 3	2
READ SERIAL FLASH DISCOVERY PARAMETER	5Ah	Yes	Yes	Yes	1 to ∞	3
READ Operations						
READ	03h	Yes	No	No	1 to ∞	4
FAST READ	0Bh	Yes	Yes	Yes		5
DUAL OUTPUT FAST READ	3Bh	Yes	Yes	No	1 to ∞	5
DUAL INPUT/OUTPUT FAST READ	0Bh 3Bh BBh	Yes	Yes	No		5, 11
QUAD OUTPUT FAST READ	6Bh	Yes	No	Yes	1 to ∞	5
QUAD INPUT/OUTPUT FAST READ	0Bh 6Bh EBh	Yes	No	Yes		5, 12
FAST READ – DTR	0Dh	Yes	Yes	Yes	1 to ∞	6
DUAL OUTPUT FAST READ – DTR	3Dh	Yes	Yes	No	1 to ∞	6
DUAL INPUT/OUTPUT FAST READ – DTR	0Dh 3Dh BDh	Yes	Yes	No	1 to ∞	6
QUAD OUTPUT FAST READ – DTR	6Dh	Yes	No	Yes	1 to ∞	6
QUAD INPUT/OUTPUT FAST READ – DTR	0Dh 6Dh EDh	Yes	No	Yes	1 to ∞	7
4-BYTE READ	13h	Yes	Yes	Yes	1 to ∞	8
4-BYTE FAST READ	0Ch					9
4-BYTE DUAL OUTPUT FAST READ	3Ch	Yes	Yes	No	1 to ∞	9
4-BYTE DUAL INPUT/OUTPUT FAST READ	BCh	Yes	Yes	No		9, 11
4-BYTE QUAD OUTPUT FAST READ	6Ch	Yes	No	Yes	1 to ∞	9
4-BYTE QUAD INPUT/OUTPUT FAST READ	ECh	Yes	No	Yes		10, 12
WRITE Operations						

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Table 18: Command Set (Continued)

Note 1 applies to entire table

Command	Code	Extended	Dual I/O	Quad I/O	Data Bytes	Notes
WRITE ENABLE	06h	Yes	Yes	Yes	0	2
WRITE DISABLE	04h					
REGISTER Operations						
READ STATUS REGISTER	05h	Yes	Yes	Yes	1 to ∞	2
WRITE STATUS REGISTER	01h				1	2, 13, 15
READ LOCK REGISTER	E8h	Yes	Yes	Yes	1 to ∞	4
WRITE LOCK REGISTER	E5h				1	4, 13
READ FLAG STATUS REGISTER	70h	Yes	Yes	Yes	1 to ∞	2
CLEAR FLAG STATUS REGISTER	50h				0	
READ NONVOLATILE CONFIGURATION REGISTER	B5h	Yes	Yes	Yes	2	2
WRITE NONVOLATILE CONFIGURATION REGISTER	B1h					2, 13, 15
READ VOLATILE CONFIGURATION REGISTER	85h	Yes	Yes	Yes	1 to ∞	2
WRITE VOLATILE CONFIGURATION REGISTER	81h				1	2, 13
READ ENHANCED VOLATILE CONFIGURATION REGISTER	65h	Yes	Yes	Yes	1 to ∞	2
WRITE ENHANCED VOLATILE CONFIGURATION REGISTER	61h				1	2, 13
READ EXTENDED ADDRESS REGISTER	C8h	Yes	Yes	Yes	0	2
WRITE EXTENDED ADDRESS REGISTER	C5h					2, 13
PROGRAM Operations						
PAGE PROGRAM	02h	Yes	Yes	Yes	1 to 256	4, 13, 14
DUAL INPUT FAST PROGRAM	A2h	Yes	Yes	No	1 to 256	4, 13, 14
EXTENDED DUAL INPUT FAST PROGRAM	02h A2h D2h	Yes	Yes	No		4, 11, 13, 14
QUAD INPUT FAST PROGRAM	32h	Yes	No	Yes	1 to 256	4, 13, 14
EXTENDED QUAD INPUT FAST PROGRAM	02h 32h 12h	Yes	No	Yes		4, 12, 13, 14
ERASE Operations						
SUBSECTOR ERASE	20h	Yes	Yes	Yes	0	4, 13, 14
SECTOR ERASE	D8h					4, 13, 14
DIE ERASE	C4h					4, 13, 14
PROGRAM/ERASE RESUME	7Ah	Yes	Yes	Yes	0	2, 13, 14
PROGRAM/ERASE SUSPEND	75h					

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Table 18: Command Set (Continued)

Note 1 applies to entire table

Command	Code	Extended	Dual I/O	Quad I/O	Data Bytes	Notes
ONE-TIME PROGRAMMABLE (OTP) Operations						
READ OTP ARRAY	4Bh	Yes	Yes	Yes	1 to 64	5
PROGRAM OTP ARRAY	42h					4, 13, 14
4-BYTE ADDRESS MODE Operations						
ENTER 4-BYTE ADDRESS MODE	B7h	Yes	Yes	Yes	0	2, 13
EXIT 4-BYTE ADDRESS MODE	E9h					

Notes:
1. *Yes* in the protocol columns indicates that the command is supported and has the same functionality and command sequence as other commands marked *Yes*.
2. Address bytes = 0. Dummy clock cycles = 0.
3. Address bytes = 3. Dummy clock cycles default = 8.
4. Address bytes default = 3; address bytes = 4 (extended address). Dummy clock cycles = 0.
5. Address bytes default = 3; address bytes = 4 (extended address). Dummy clock cycles default = 8. Dummy clock cycles default = 10 (when quad SPI protocol is enabled). Dummy clock cycles are configurable by the user.
6. Address bytes default = 3; address bytes = 4 (extended address). Dummy clock cycles default = 6. Dummy clock cycles default = 8 when quad SPI protocol is enabled. Dummy clock cycles are configurable by the user.
7. Address bytes default = 3; address bytes = 4 (extended address). Dummy clock cycles default = 8. Dummy clock cycles are configurable by the user.
8. Address bytes = 4. Dummy clock cycles = 0.
9. Address bytes = 4. Dummy clock cycles default = 8. Dummy clock cycles default = 10 (when quad SPI protocol is enabled). Dummy clock cycles are configurable by the user.
10. Address bytes = 4. Dummy clock cycles default = 10. Dummy clock cycles is configurable by the user.
11. When the device is in dual SPI protocol, the command can be entered with any of these three codes. The different codes enable compatibility between dual SPI and extended SPI protocols.
12. When the device is in quad SPI protocol, the command can be entered with any of these three codes. The different codes enable compatibility between quad SPI and extended SPI protocols.
13. The WRITE ENABLE command must be issued first before this command can be executed.
14. Requires the READ FLAG STATUS REGISTER command being issued with at least one byte output. (After code, at least 8 clock pulses in extended SPI, 4 clock pulses in dual I/O SPI, and 2 clock pulses in quad I/O SPI.) The cycle is not complete until bit 7 of the flag status register outputs 1.
15. The end of operation can be detected by means of a READ FLAG STATUS REGISTER command being issued four times, S# toggled between each command execution, and bit 7 of the flag status register outputs 1 for all four READ operations.

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READ REGISTER and WRITE REGISTER Operations

READ STATUS REGISTER or FLAG STATUS REGISTER Command

To initiate a READ STATUS REGISTER command, S# is driven LOW. For extended SPI protocol, the command code is input on DQ0, and output on DQ1. For dual SPI protocol, the command code is input on DQ[1:0], and output on DQ[1:0]. For quad SPI protocol, the command code is input on DQ[3:0], and is output on DQ[3:0]. The operation is terminated by driving S# HIGH at any time during data output.

The status register can be read continuously and at any time, including during a PROGRAM, ERASE, or WRITE operation.

The flag status register can be read continuously and at any time, including during an ERASE or WRITE operation.

If one of these operations is in progress, checking the write in progress bit or program or erase controller bit is recommended before executing the command.

The flag status register must be read any time a PROGRAM, ERASE, or SUSPEND/RESUME command is issued, or after a RESET command while device is busy. The cycle is not complete until bit 7 of the flag status register outputs 1. Refer to Command Definitions for more information.

Note: The end of an operation (such as a power-up, WRITE STATUS REGISTER, or WRITE NONVOLATILE CONFIGURATION REGISTER) is determined by issuing the READ FLAG STATUS REGISTER command once for each die in the device, with S# toggled between commands until each die is ready. Bit 7 of the flag status register outputs a value of 1 each time.

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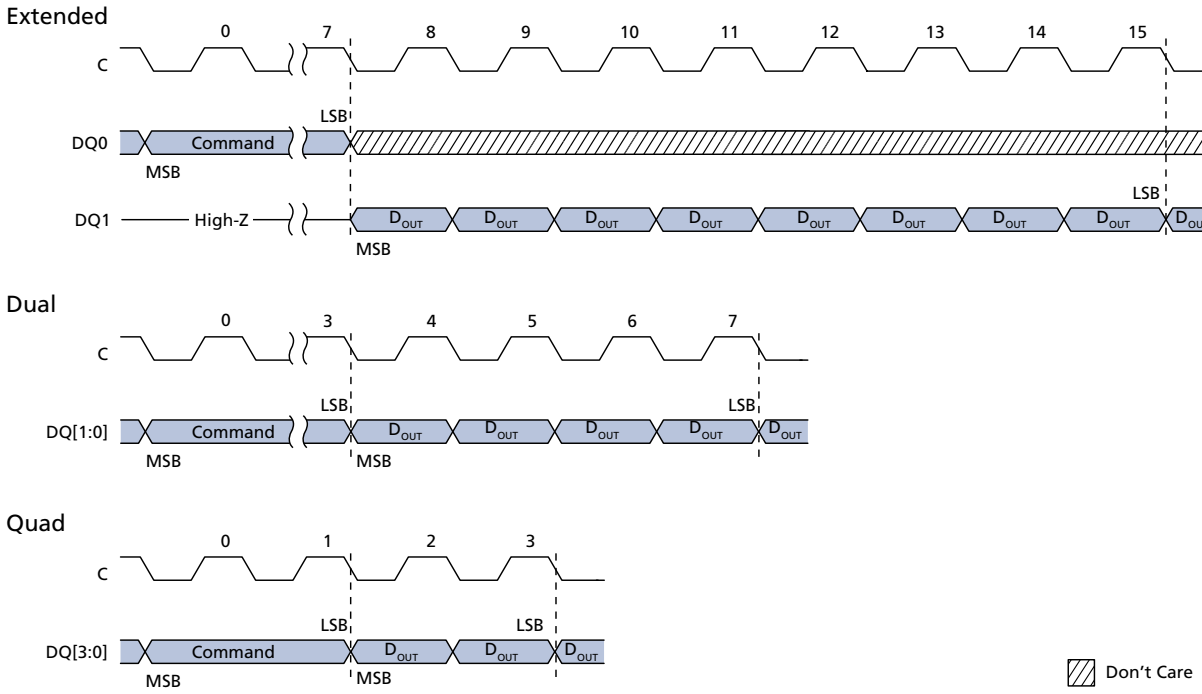
Figure 9: READ REGISTER Command



Notes:
1. Supports all READ REGISTER commands except READ LOCK REGISTER.
2. A READ NONVOLATILE CONFIGURATION REGISTER operation will output data starting from the least significant byte.

READ NONVOLATILE CONFIGURATION REGISTER Command

To execute a READ NONVOLATILE CONFIGURATION REGISTER command, S# is driven LOW. For extended SPI protocol, the command code is input on DQ0, and output on DQ1. For dual SPI protocol, the command code is input on DQ[1:0], and output on DQ[1:0]. For quad SPI protocol, the command code is input on DQ[3:0], and is output on DQ[3:0]. The operation is terminated by driving S# HIGH at any time during data output.

The nonvolatile configuration register can be read continuously. After all 16 bits of the register have been read, a 0 is output. All reserved fields output a value of 1.

READ VOLATILE or ENHANCED VOLATILE CONFIGURATION REGISTER Command

To execute a READ VOLATILE CONFIGURATION REGISTER command or a READ ENHANCED VOLATILE CONFIGURATION REGISTER command, S# is driven LOW. For extended SPI protocol, the command code is input on DQ0, and output on DQ1. For dual SPI protocol, the command code is input on DQ[1:0], and output on DQ[1:0]. For quad SPI protocol, the command code is input on DQ[3:0], and is output on DQ[3:0]. The operation is terminated by driving S# HIGH at any time during data output.

When the register is read continuously, the same byte is output repeatedly.

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READ EXTENDED ADDRESS REGISTER Command

To initiate a READ EXTENDED ADDRESS REGISTER command, S# is driven LOW. For extended SPI protocol, the command code is input on DQ0, and output on DQ1. For dual SPI protocol, the command code is input on DQ[1:0], and output on DQ[1:0]. For quad SPI protocol, the command code is input on DQ[3:0], and is output on DQ[3:0]. The operation is terminated by driving S# HIGH at any time during data output.

When the register is read continuously, the same byte is output repeatedly.

WRITE STATUS REGISTER Command

To issue a WRITE STATUS REGISTER command, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. For extended SPI protocol, the command code is input on DQ0, followed by the data bytes. For dual SPI protocol, the command code is input on DQ[1:0], followed by the data bytes. For quad SPI protocol, the command code is input on DQ[3:0], followed by the data bytes. When S# is driven HIGH, the operation, which is self-timed, is initiated; its duration is ^{t}W.

This command is used to write new values to status register bits 7:2, enabling software data protection. The status register can also be combined with the W#/V_{PP} signal to provide hardware data protection. The WRITE STATUS REGISTER command has no effect on status register bits 1:0.

When the operation is in progress, the program or erase controller bit of the flag status register is set to 0. To obtain the operation status, the flag status register must be polled four times, with S# toggled twice in between commands. When the operation completes, the program or erase controller bit is cleared to 1. The end of operation can be detected when the flag status register outputs the program or erase controller bit to 1 each of the four times. When the maximum time is achieved (see AC Characteristics and Operating Conditions), polling the flag status register four times is not required.

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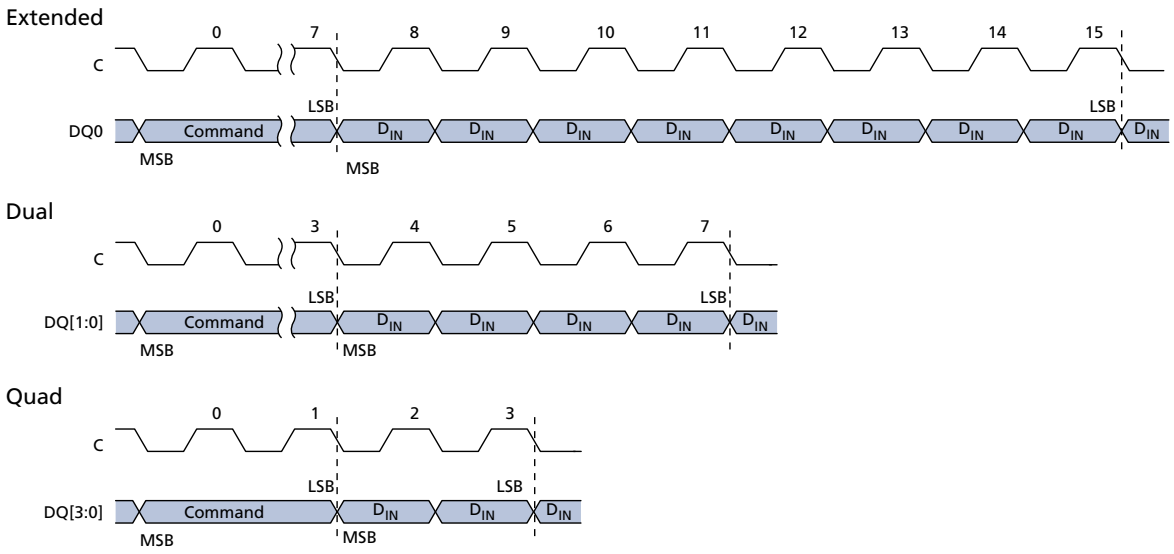
Figure 10: WRITE REGISTER Command



Notes:
1. Supports all WRITE REGISTER commands except WRITE LOCK REGISTER.
2. A WRITE NONVOLATILE CONFIGURATION REGISTER operation requires data being sent starting from least significant byte. For this command, the data in consists of two bytes.

WRITE NONVOLATILE CONFIGURATION REGISTER Command

To execute the WRITE NONVOLATILE CONFIGURATION REGISTER command, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. S# is driven LOW and held LOW until the 16th bit of the last data byte has been latched in, after which it must be driven HIGH. For extended SPI protocol, the command code is input on DQ0, followed by two data bytes. For dual SPI protocol, the command code is input on DQ[1:0], followed by the data bytes. For quad SPI protocol, the command code is input on DQ[3:0], followed by the data bytes. When S# is driven HIGH, the operation, which is self-timed, is initiated; its duration is ^{t}WNVCR.

When the operation is in progress, the program or erase controller bit of the flag status register is set to 0. To obtain the operation status, the flag status register must be polled four times, with S# toggled twice in between commands. When the operation completes, the program or erase controller bit is cleared to 1. The end of operation can be detected when the flag status register outputs the program or erase controller bit to 1 each of the four times. When the maximum time is achieved (see AC Characteristics and Operating Conditions), polling the flag status register four times is not required.

WRITE VOLATILE or ENHANCED VOLATILE CONFIGURATION REGISTER Command

To execute a WRITE VOLATILE CONFIGURATION REGISTER command or a WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. For extended SPI protocol, the command code is input on DQ0,

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followed by the data bytes. For dual SPI protocol, the command code is input on DQ[1:0], followed by the data bytes. For quad SPI protocol, the command code is input on DQ[3:0], followed by the data bytes.

Because register bits are volatile, change to the bits is immediate. After the data is latched in, S# must be driven HIGH. Reserved bits are not affected by this command.

WRITE EXTENDED ADDRESS REGISTER Command

To initiate a WRITE EXTENDED ADDRESS REGISTER command, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. The command code is input on DQ0, followed by the data bytes. For dual SPI protocol, the command code is input on DQ[1:0], followed by the data bytes. For quad SPI protocol, the command code is input on DQ[3:0], followed by the data bytes.

Because register bits are volatile, change to the bits is immediate. After the data is latched in, S# must be driven HIGH. Reserved bits are not affected by this command.

READ LOCK REGISTER Command

To execute the READ LOCK REGISTER command, S# is driven LOW. For extended SPI protocol, the command code is input on DQ0, followed by address bytes that point to a location in the sector. For dual SPI protocol, the command code is input on DQ[1:0]. For quad SPI protocol, the command code is input on DQ[3:0]. Each address bit is latched in during the rising edge of the clock. For extended SPI protocol, data is shifted out on DQ1 at a maximum frequency ^{f}C during the falling edge of the clock. For dual SPI protocol, data is shifted out on DQ[1:0], and for qual SPI protocol, data is shifted out on DQ[3:0]. The operation is terminated by driving S# HIGH at any time during data output.

When the register is read continuously, the same byte is output repeatedly. Any READ LOCK REGISTER command that is executed while an ERASE, PROGRAM, or WRITE cycle is in progress is rejected with no affect on the cycle in progress.

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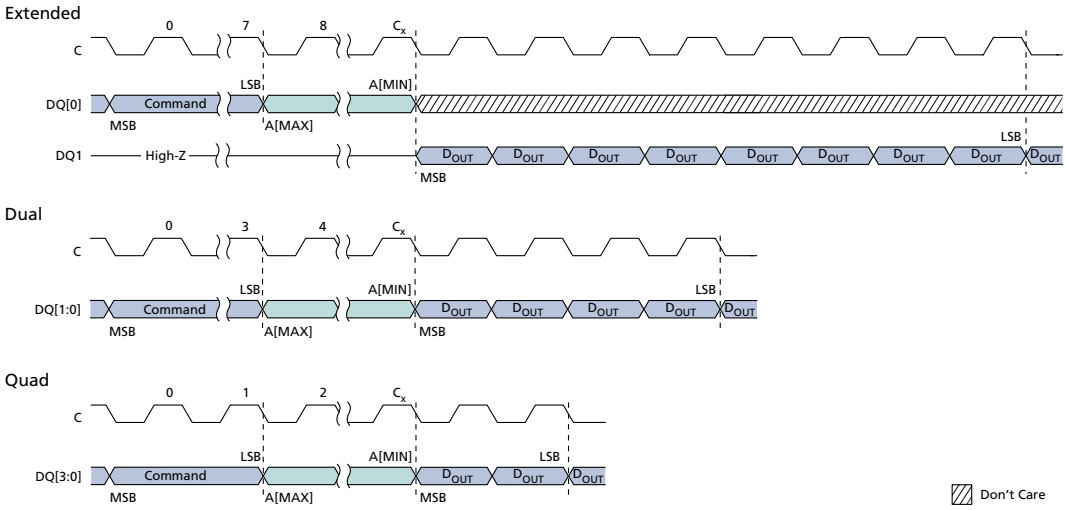
Table 19: Lock Register

Note 1 applies to entire table

Bit	Name	Settings	Description
7:2	Reserved	0	Bit values are 0.
1	Write lock down	0 = Cleared (Default) 1 = Set	Volatile bit: the device always powers-up with this bit cleared, which means sector lock down and sector write lock bits can be set. When this bit set, neither of the lock register bits can be written to until the next power cycle.
0	Sector write lock	0 = Cleared (Default) 1 = Set	Volatile bit: the device always powers-up with this bit cleared, which means that PROGRAM and ERASE operations in this sector can be executed and sector content modified. When this bit is set, PROGRAM and ERASE operations in this sector will not be executed.

Note: 1. Sector lock register bits 1:0 are written to by the WRITE LOCK REGISTER command. The command will not execute unless the sector lock down bit is cleared.

Figure 11: READ LOCK REGISTER Command



Note: 1. For extended SPI protocol, C_x = 7 + (A[MAX] + 1).

For dual SPI protocol, C_x = 3 + ((A[MAX] + 1)/2).

For quad SPI protocol, C_x = 1 + ((A[MAX] + 1)/4).

WRITE LOCK REGISTER Command

To initiate the WRITE LOCK REGISTER command, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. The command code is input on DQn, followed by address bytes that point to a

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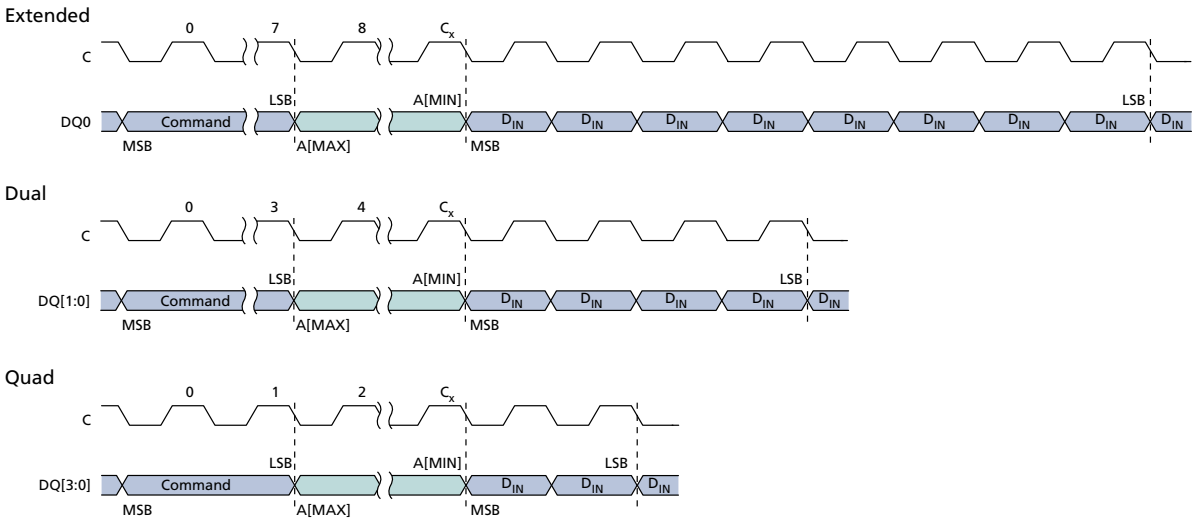
location in the sector, and then one data byte that contains the desired settings for lock register bits 0 and 1.

When execution is complete, the write enable latch bit is cleared within ^{t}SHSL2 and no error bits are set. Because lock register bits are volatile, change to the bits is immediate. WRITE LOCK REGISTER can be executed when an ERASE SUSPEND operation is in effect. After the data is latched in, S# must be driven HIGH.

Figure 12: WRITE LOCK REGISTER Command



Note: 1. For extended SPI protocol, C_x = 7 + (A[MAX] + 1).

For dual SPI protocol, C_x = 3 + ((A[MAX] + 1)/2).

For quad SPI protocol, C_x = 1 + ((A[MAX] + 1)/4).

CLEAR FLAG STATUS REGISTER Command

To execute the CLEAR FLAG STATUS REGISTER command and clear the error bits (erase, program, and protection), S# is driven LOW. For extended SPI protocol, the command code is input on DQ0. For dual SPI protocol, the command code is input on DQ[1:0]. For quad SPI protocol, the command code is input on DQ[3:0]. The operation is terminated by driving S# HIGH at any time.

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READ IDENTIFICATION Operations

READ ID and MULTIPLE I/O READ ID Commands

To execute the READ ID or MULTIPLE I/O READ ID commands, S# is driven LOW and the command code is input on DQ*n*. The device outputs the information shown in the tables below. If an ERASE or PROGRAM cycle is in progress when the command is executed, the command is not decoded and the command cycle in progress is not affected. When S# is driven HIGH, the device goes to standby. The operation is terminated by driving S# HIGH at any time during data output.

Table 20: Data/Address Lines for READ ID and MULTIPLE I/O READ ID Commands

Command Name	Data In	Data Out	Unique ID is Output	Extended	Dual	Quad
READ ID	DQ0	DQ0	Yes	Yes	No	No
MULTIPLE I/O READ ID	DQ[3:0]	DQ[1:0]	No	No	Yes	Yes

Note: 1. *Yes* in the protocol columns indicates that the command is supported and has the same functionality and command sequence as other commands marked *Yes*.

Table 21: Read ID Data Out

Size (Bytes)	Name	Content Value	Assigned by
1	**Manufacturer ID**	20h	JEDEC
2	**Device ID**		
	Memory Type	BAh	Manufacturer
	Memory Capacity	21h (1Gb)	
17	**Unique ID**		
	1 Byte: Length of data to follow	10h	Factory
	2 Bytes: Extended device ID and device configuration information	ID and information such as uniform architecture, and HOLD or RESET functionality	
	14 Bytes: Customized factory data	Optional	

Note: 1. The 17 bytes of information in the unique ID is read by the READ ID command, but cannot be read by the MULTIPLE I/O READ ID command.

Table 22: Extended Device ID, First Byte

Bit 7	Bit 6	Bit 5[1]	Bit 4[2]	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	1 = Alternate BP scheme 0 = Standard BP scheme	Volatile configuration register bit setting: 0 = Micron XIP 1 = Basic XIP	HOLD#/RESET#: 0 = HOLD 1 = RESET	Addressing: 0 = by byte	Architecture: 00 = Uniform	

Notes: 1. For alternate BP scheme information, contact the factory.
2. For more information, contact the factory.

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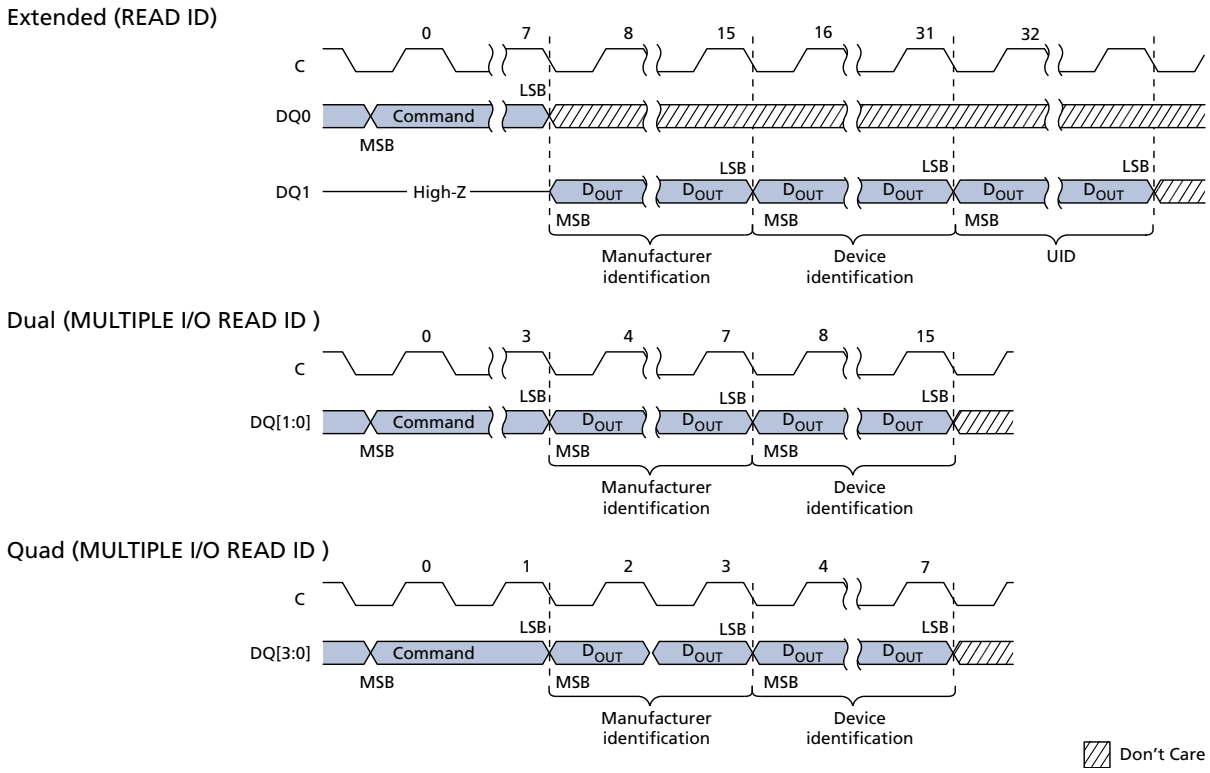
Figure 13: READ ID and MULTIPLE I/O Read ID Commands



Note: 1. The READ ID command is represented by the extended SPI protocol timing shown first. The MULTIPLE I/O READ ID command is represented by the dual and quad SPI protocols are shown below extended SPI protocol.

READ SERIAL FLASH DISCOVERY PARAMETER Command

To execute READ SERIAL FLASH DISCOVERY PARAMETER command, S# is driven LOW. The command code is input on DQ0, followed by three address bytes and eight dummy clock cycles (address is always 3 bytes, even if the device is configured to work in 4-byte address mode). The device outputs the information starting from the specified address. When the 2048-byte boundary is reached, the data output wraps to address 0 of the serial Flash discovery parameter table. The operation is terminated by driving S# HIGH at any time during data output.

The operation always executes in continuous mode so the read burst wrap setting in the volatile configuration register does not apply.

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Table 23: Serial Flash Discovery Parameter Data Structure

Compliant with JEDEC standard JC-42.4 1775.03

Description		Address (Byte Mode)	Address (Bit)	Data
Serial Flash discoverable parameters signature		00h	7:0	53h
		01h	15:08	46h
		02h	23:16	44h
		03h	31:24	50h
Serial Flash discoverable parameters	Minor revision	04h	7:0	00h
	Major revision	05h	15:8	01h
Number of parameter headers		06h	7:0	00h
Reserved		07h	15:8	FFh
Parameter ID (0) JEDEC-defined parameter table		08h	7:0	00h
Parameter	Minor revision	09h	15:8	00h
	Major revision	0Ah	23:16	01h
Parameter length (DW)		0Bh	31:24	09h
Parameter table pointer		0Ch	7:0	30h
		0Dh	15:8	00h
		0Eh	23:16	00h
Reserved		0Fh	31:24	FFh

Table 24: Parameter ID

Description	Byte Address	Bits	512Mb Data
Minimum block/sector erase sizes	30h	1:0	01b
Write granularity		2	1
WRITE ENABLE command required for writing to volatile status registers		3	0
WRITE ENABLE command selected for writing to volatile status registers		4	0
Reserved		7:5	111b
4KB ERASE command	31h	7:0	20h

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Table 24: Parameter ID (Continued)

Description	Byte Address	Bits	512Mb Data
Supports DUAL OUTPUT FAST READ operation (single input address, dual output)	32h	0	1
Number of address bytes used (3-byte or 4-byte) for array READ, WRITE, and ERASE commands		2:1	01b
Supports double transfer rate clocking		3	1
Supports DUAL INPUT/OUTPUT FAST READ operation (dual input address, dual output)		4	1
Supports QUAD INPUT/OUTPUT FAST READ operation (quad input address, quad output)		5	1
Supports QUAD OUTPUT FAST READ operation (single input address, quad output)		6	1
Reserved		7	1
Reserved	33h	7:0	FFh
Flash size (bits)	34h	7:0	FFh
	35h	7:0	FFh
	36h	7:0	FFh
	37h	7:0	3Fh
Number of dummy clock cycles required before valid output from QUAD INPUT/OUTPUT FAST READ operation	38h	4:0	01001b
Number of XIP confirmation bits for QUAD INPUT/OUTPUT FAST READ operation		7:5	001b
Command code for QUAD INPUT/OUTPUT FAST READ operation	39h	7:0	EBh
Number of dummy clock cycles required before valid output from QUAD OUTPUT FAST READ operation	3Ah	4:0	00111b
Number of XIP confirmation bits for QUAD OUTPUT FAST READ operation		7:5	001b
Command code for QUAD OUTPUT FAST READ operation	3Bh	7:0	6Bh
Number of dummy clock cycles required before valid output from DUAL OUTPUT FAST READ operation	3Ch	4:0	00111b
Number of XIP confirmation bits for DUAL OUTPUT FAST READ operation		7:5	001b
Command code for DUAL OUTPUT FAST READ operation	3Dh	7:0	3Bh
Number of dummy clock cycles required before valid output from DUAL INPUT/OUTPUT FAST READ operation	3Eh	4:0	00111b
Number of XIP confirmation bits for DUAL INPUT/OUTPUT FAST READ		7:5	001b
Command code for DUAL INPUT/OUTPUT FAST READ operation	3Fh	7:0	BBh

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Table 24: Parameter ID (Continued)

Description	Byte Address	Bits	512Mb Data
Supports FAST READ operation in dual SPI protocol	40h	0	1
Reserved		3:1	111b
Supports FAST READ operation in quad SPI protocol		4	1
Reserved		7:5	111b
Reserved	43:41h	FFFFFFh	FFFFFFh
Reserved	45:44h	FFFFh	FFFFh
Number of dummy clock cycles required before valid output from FAST READ operation in dual SPI protocol	46h	4:0	00111b
Number of XIP confirmation bits for FAST READ operation in dual SPI protocol		7:5	001b
Command code for FAST READ operation in dual SPI protocol	47h	7:0	BBh
Reserved	49:48h	FFFFh	FFFFh
Number of dummy clock cycles required before valid output from FAST READ operation in quad SPI protocol	4Ah	4:0	01001b
Number of XIP confirmation bits for FAST READ operation in quad SPI protocol		7:5	001b
Command code for FAST READ operation in quad SPI protocol	4Bh	7:0	EBh
Sector type 1 size (4k)	4Ch	7:0	0Ch
Sector type 1 command code (4k)	4Dh	7:0	20h
Sector type 2 size (64KB)	4Eh	7:0	10h
Sector type 2 command code 64KB)	4Fh	7:0	D8h
Sector type 3 size (not present)	50h	7:0	00h
Sector type 3 size (not present)	51h	7:0	00h
Sector type 4 size (not present)	52h	7:0	00h
Sector type 4 size (not present)	53h	7:0	00h

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READ MEMORY Operations

The device supports default reading and writing to an A[MAX:MIN] of A[23:0] (3-byte address).

Reading and writing to an A[MAX:MIN] of A[31:0] (4-byte address) is also supported. Selection of the 3-byte or 4-byte address range can be enabled in two ways: through the nonvolatile configuration register or through the ENABLE 4-BYTE ADDRESS MODE/ EXIT 4-BYTE ADDRESS MODE commands. Further details for these settings and commands are in the respective register and command sections of the data sheet.

After any READ command is executed, the device will output data from the selected address in the die. After a die boundary is reached, the device will start reading again from the beginning of the same 256Mb die.

A complete device reading is completed by executing READ four times.

3-Byte Address

To execute READ MEMORY commands, S# is driven LOW. The command code is input on DQ*n*, followed by input on DQ*n* of three address bytes. Each address bit is latched in during the rising edge of the clock. The addressed byte can be at any location, and the address automatically increments to the next address after each byte of data is shifted out; therefore, a die can be read with a single command. The operation is terminated by driving S# HIGH at any time during data output.

Table 25: Command/Address/Data Lines for READ MEMORY Commands

Note 1 applies to entire table

	Command Name					
	READ	FAST READ	DUAL OUTPUT FAST READ	DUAL INPUT/OUTPUT FAST READ	QUAD OUTPUT FAST READ	QUAD INPUT/OUTPUT FAST READ
STR Mode	**03**	**0B**	**3B**	**BB**	**6B**	**EB**
DTR Mode	**–**	**0D**	**3D**	**BD**	**6D**	**ED**
Extended SPI Protocol						
Supported	Yes	Yes	Yes	Yes	Yes	Yes
Command Input	DQ0	DQ0	DQ0	DQ0	DQ0	DQ0
Address Input	DQ0	DQ0	DQ0	DQ[1:0]	DQ0	DQ[3:0]
Data Output	DQ1	DQ1	DQ[1:0]	DQ[1:0]	DQ[3:0]	DQ[3:0]
Dual SPI Protocol						
Supported	No	Yes	Yes	Yes	No	No
Command Input	–	DQ[1:0]	DQ[1:0]	DQ[1:0]	–	–
Address Input	–	DQ[1:0]	DQ[1:0]	DQ[1:0]	–	–
Data Output	–	DQ[1:0]	DQ[1:0]	DQ[1:0]	–	–
Quad SPI Protocol						
Supported	No	Yes	No	No	Yes	Yes
Command Input	–	DQ[3:0]	–	–	DQ[3:0]	DQ[3:0]
Address Input	–	DQ[3:0]	–	–	DQ[3:0]	DQ[3:0]

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Table 25: Command/Address/Data Lines for READ MEMORY Commands (Continued)

Note 1 applies to entire table

	Command Name					
	READ	FAST READ	DUAL OUTPUT FAST READ	DUAL INPUT/OUTPUT FAST READ	QUAD OUTPUT FAST READ	QUAD INPUT/OUTPUT FAST READ
STR Mode	**03**	**0B**	**3B**	**BB**	**6B**	**EB**
DTR Mode	**–**	**0D**	**3D**	**BD**	**6D**	**ED**
Data Output	–	DQ[3:0]	–	–	DQ[3:0]	DQ[3:0]

Notes:
1. *Yes* in the "Supported' row for each protocol indicates that the command in that column is supported; when supported, a command's functionality is identical for the entire column regardless of the protocol. For example, a FAST READ functions the same for all three protocols even though its data is input/output differently depending on the protocol.
2. FAST READ is similar to READ, but requires dummy clock cycles following the address bytes and can operate at a higher frequency (f_C).

4-Byte Address

To execute 4-byte READ MEMORY commands, S# is driven LOW. The command code is input on DQ*n*, followed by input on DQ*n* of four address bytes. Each address bit is latched in during the rising edge of the clock. The addressed byte can be at any location, and the address automatically increments to the next address after each byte of data is shifted out; therefore, a die can be read with a single command. The operation is terminated by driving S# HIGH at any time during data output.

Table 26: Command/Address/Data Lines for READ MEMORY Commands – 4-Byte Address

Notes 1 and 2 apply to entire table

	Command Name (4-Byte Address)					
	READ	FAST READ	DUAL OUTPUT FAST READ	DUAL INPUT/OUTPUT FAST READ	QUAD OUTPUT FAST READ	QUAD INPUT/OUTPUT FAST READ
STR Mode	**03/13**	**0B/0C**	**3B/3C**	**BB/BC**	**6B/6C**	**EB/EC**
DTR Mode	**–**	**0D**	**3D**	**BD**	**6D**	**ED**
Extended SPI Protocol						
Supported	Yes	Yes	Yes	Yes	Yes	Yes
Command Input	DQ0	DQ0	DQ0	DQ0	DQ0	DQ0
Address Input	DQ0	DQ0	DQ0	DQ[1:0]	DQ0	DQ[3:0]
Data Output	DQ1	DQ1	DQ[1:0]	DQ[1:0]	DQ[3:0]	DQ[3:0]
Dual SPI Protocol						
Supported	No	Yes	Yes	Yes	No	No
Command Input	–	DQ[1:0]	DQ[1:0]	DQ[1:0]	–	–
Address Input	–	DQ[1:0]	DQ[1:0]	DQ[1:0]	–	–
Data Output	–	DQ[1:0]	DQ[1:0]	DQ[1:0]	–	–

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Table 26: Command/Address/Data Lines for READ MEMORY Commands – 4-Byte Address (Continued)

Notes 1 and 2 apply to entire table

	Command Name (4-Byte Address)					
	READ	FAST READ	DUAL OUTPUT FAST READ	DUAL INPUT/OUTPUT FAST READ	QUAD OUTPUT FAST READ	QUAD INPUT/OUTPUT FAST READ
STR Mode	**03/13**	**0B/0C**	**3B/3C**	**BB/BC**	**6B/6C**	**EB/EC**
DTR Mode	**–**	**0D**	**3D**	**BD**	**6D**	**ED**
Quad SPI Protocol						
Supported	No	Yes	No	No	Yes	Yes
Command Input	–	DQ[3:0]	–	–	DQ[3:0]	DQ[3:0]
Address Input	–	DQ[3:0]	–	–	DQ[3:0]	DQ[3:0]
Data Output	–	DQ[3:0]	–	–	DQ[3:0]	DQ[3:0]

Notes:
1. *Yes* in the "Supported' row for each protocol indicates that the command in that column is supported; when supported, a command's functionality is identical for the entire column regardless of the protocol. For example, a FAST READ functions the same for all three protocols even though its data is input/output differently depending on the protocol.
2. Command codes 13, 0C, 3C, BC, 6C, and EC do not need to be set up in the addressing mode; they will work directly in 4-byte addressing mode.
3. A 4-BYTE FAST READ command is similar to 4-BYTE READ operation, but requires dummy clock cycles following the address bytes and can operate at a higher frequency (^{f}C).

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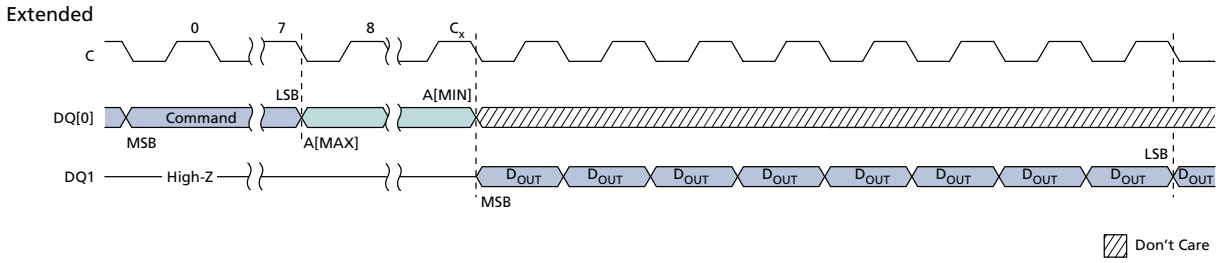
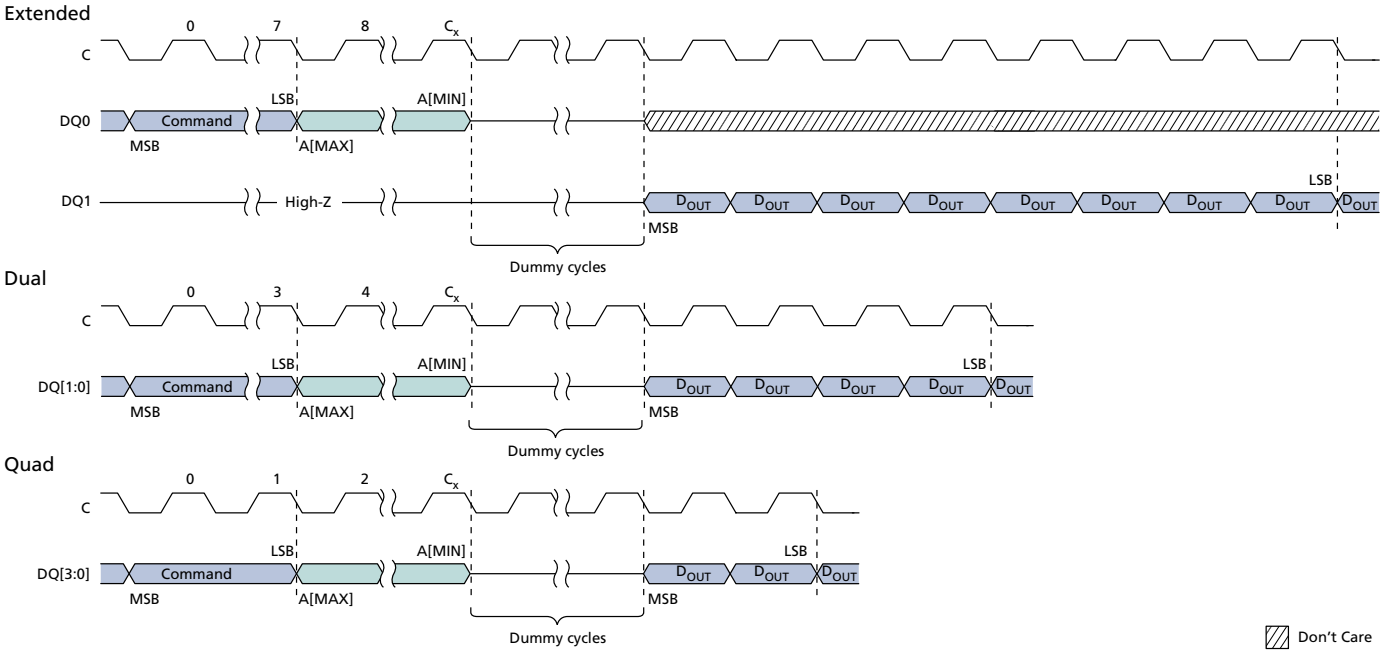
Figure 14: READ Command



Note: 1. $C_x = 7 + (A[MAX] + 1)$.

READ MEMORY Operations Timing – Single Transfer Rate

Figure 15: FAST READ Command



Note: 1. For extended protocol, $C_x = 7 + (A[MAX] + 1)$.
For dual protocol, $C_x = 3 + (A[MAX] + 1)/2$.
For quad protocol, $C_x = 1 + (A[MAX] + 1)/4$.

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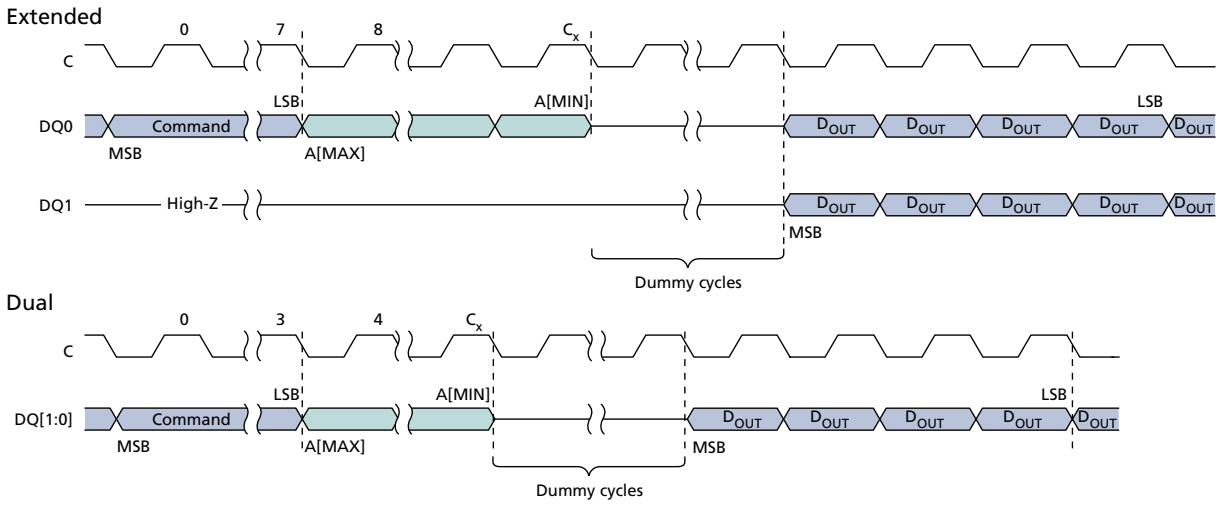
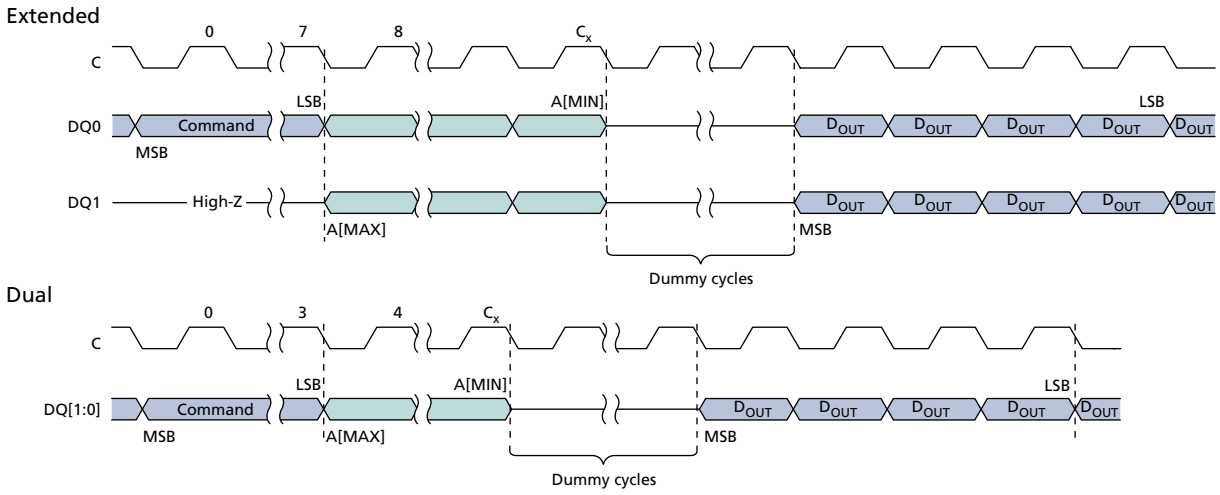
Figure 16: DUAL OUTPUT FAST READ Command



Notes:
1. C_x = 7 + (A[MAX] + 1).
2. Shown here is the DUAL OUTPUT FAST READ timing for the extended SPI protocol. The dual timing shown for the FAST READ command is the equivalent of the DUAL OUTPUT FAST READ timing for the dual SPI protocol.

Figure 17: DUAL INPUT/OUTPUT FAST READ Command



Notes:
1. C_x = 7 + (A[MAX] + 1)/2.
2. Shown here is the DUAL INPUT/OUTPUT FAST READ timing for the extended SPI protocol. The dual timing shown for the FAST READ command is the equivalent of the DUAL INPUT/OUTPUT FAST READ timing for the dual SPI protocol.

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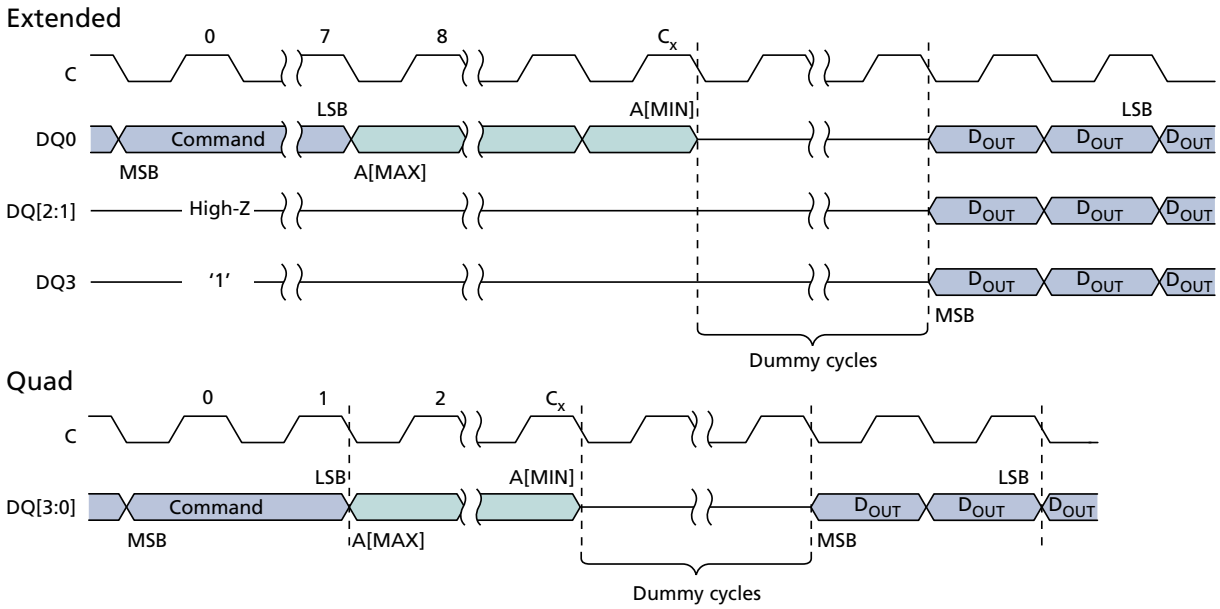
Figure 18: QUAD OUTPUT FAST READ Command



Notes:
1. C_x = 7 + (A[MAX] + 1).
2. Shown here is the QUAD OUTPUT FAST READ timing for the extended SPI protocol. The quad timing shown for the FAST READ command is the equivalent of the QUAD OUTPUT FAST READ timing for the quad SPI protocol.

Figure 19: QUAD INPUT/OUTPUT FAST READ Command

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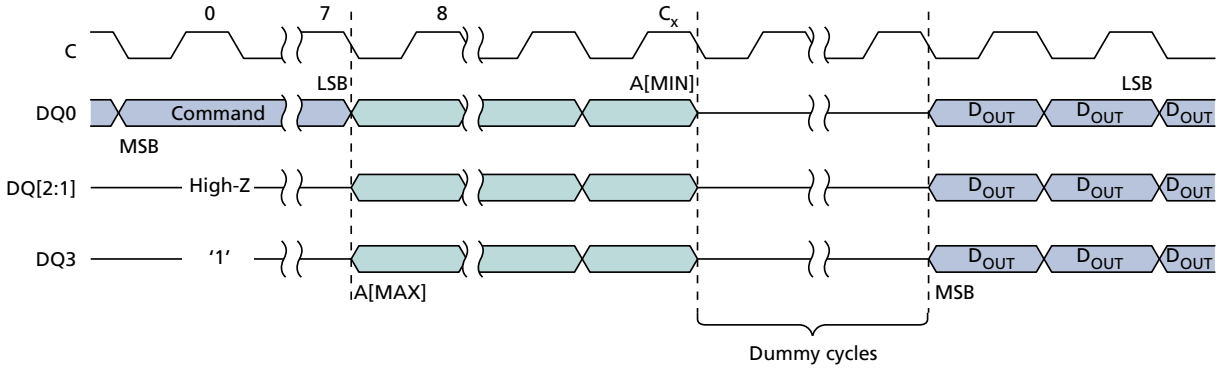
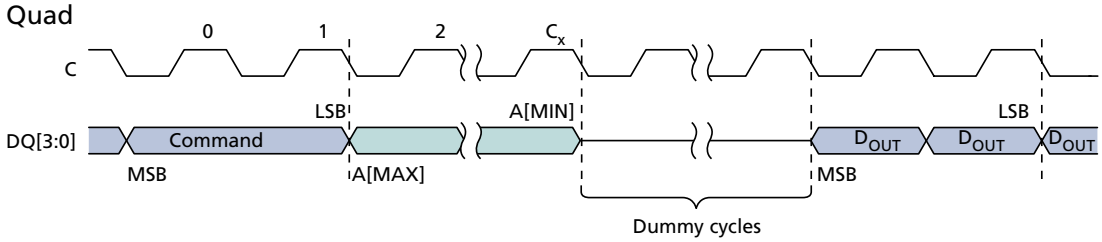
Extended



Quad



Notes:
1. C_x = 7 + (A[MAX] + 1)/4.
2. Shown here is the QUAD INPUT/OUTPUT FAST READ timing for the extended SPI protocol. The quad timing shown for the FAST READ command is the equivalent of the QUAD INPUT/OUTPUT FAST READ timing for the quad SPI protocol.

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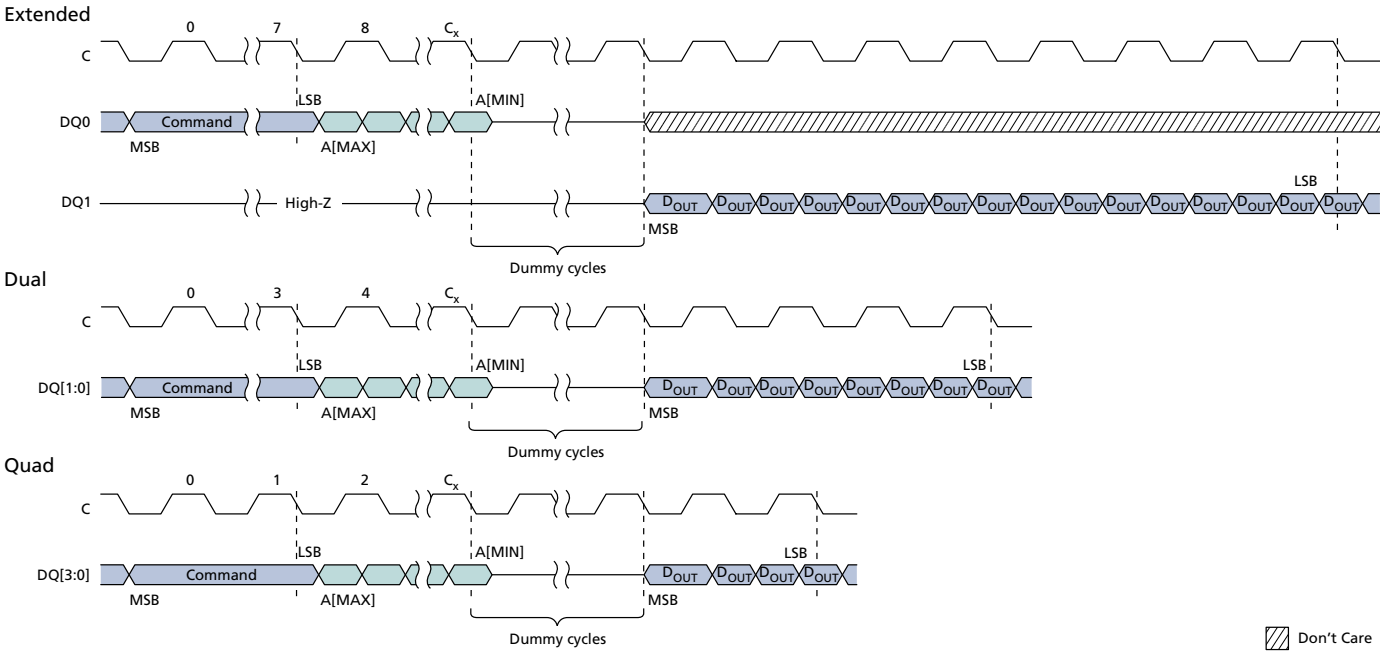
READ MEMORY Operations Timing – Double Transfer Rate

Figure 20: FAST READ Command – DTR



Note: 1. For extended protocol, $C_x = 7 + (A[MAX] + 1)/2$.

For dual protocol, $C_x = 3 + (A[MAX] + 1)/4$.

For quad protocol, $C_x = 1 + (A[MAX] + 1)/8$.

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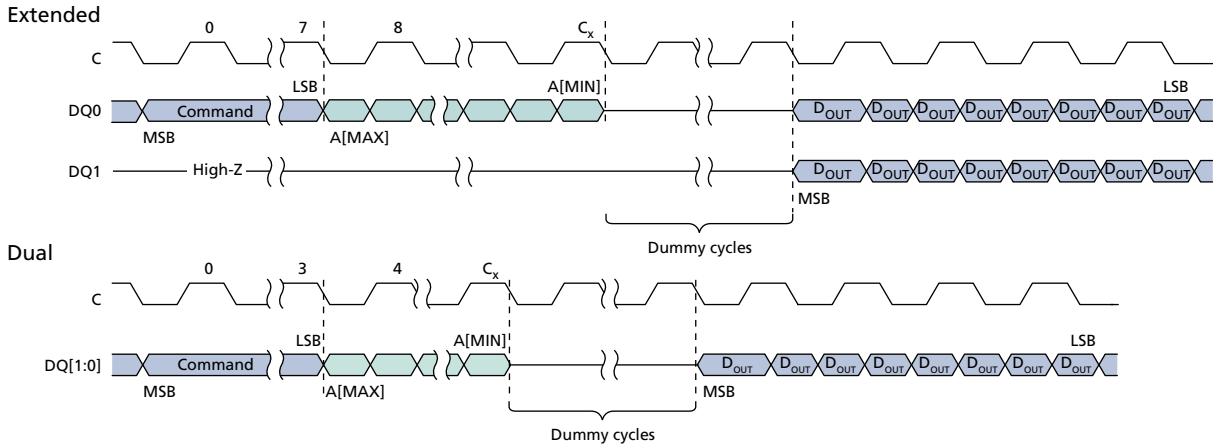
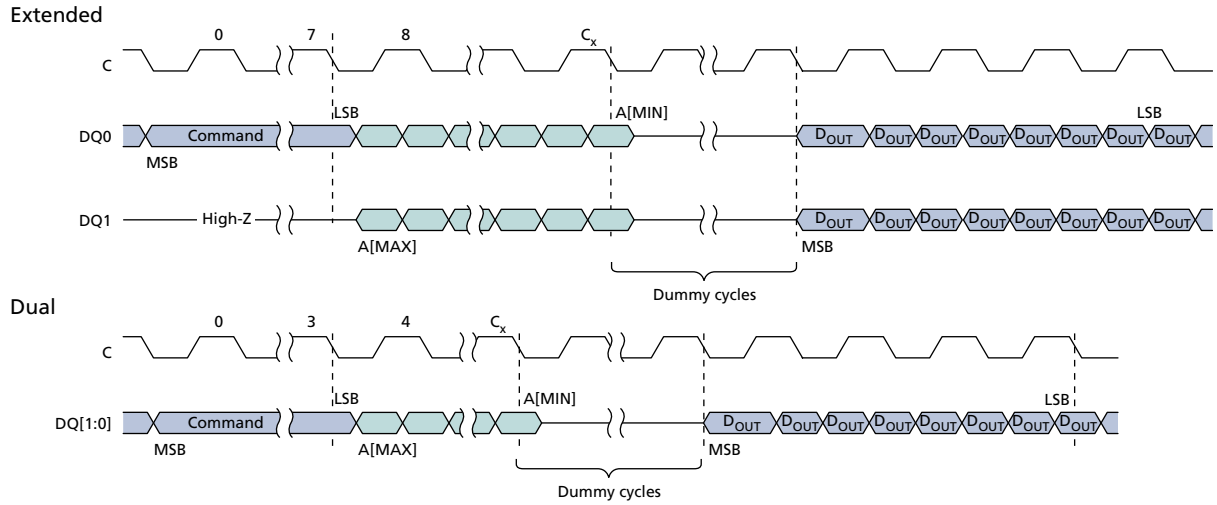
Figure 21: DUAL OUTPUT FAST READ Command – DTR



Notes:
1. $C_x = 7 + (A[MAX] + 1)/2$.
2. Shown here is the DUAL OUTPUT FAST READ timing for the extended SPI protocol. The dual timing shown for the FAST READ command is the equivalent of the DUAL OUTPUT FAST READ timing for the dual SPI protocol.

Figure 22: DUAL INPUT/OUTPUT FAST READ Command – DTR



Notes:
1. $C_x = 7 + (A[MAX] + 1)/4$.
2. Shown here is the DUAL INPUT/OUTPUT FAST READ timing for the extended SPI protocol. The dual timing shown for the FAST READ command is the equivalent of the DUAL INPUT/OUTPUT FAST READ timing for the dual SPI protocol.

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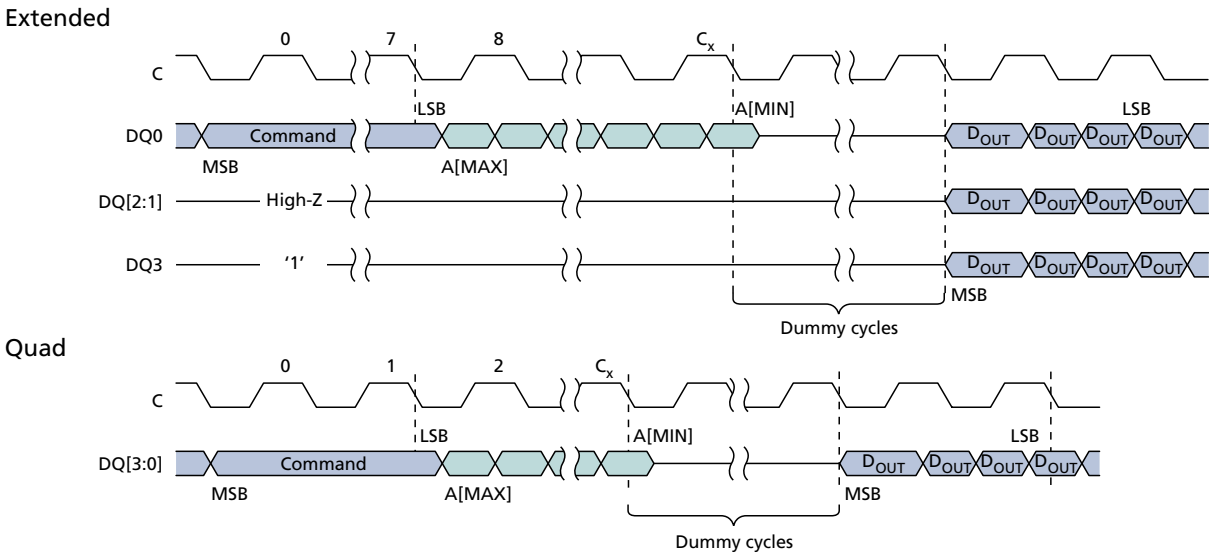
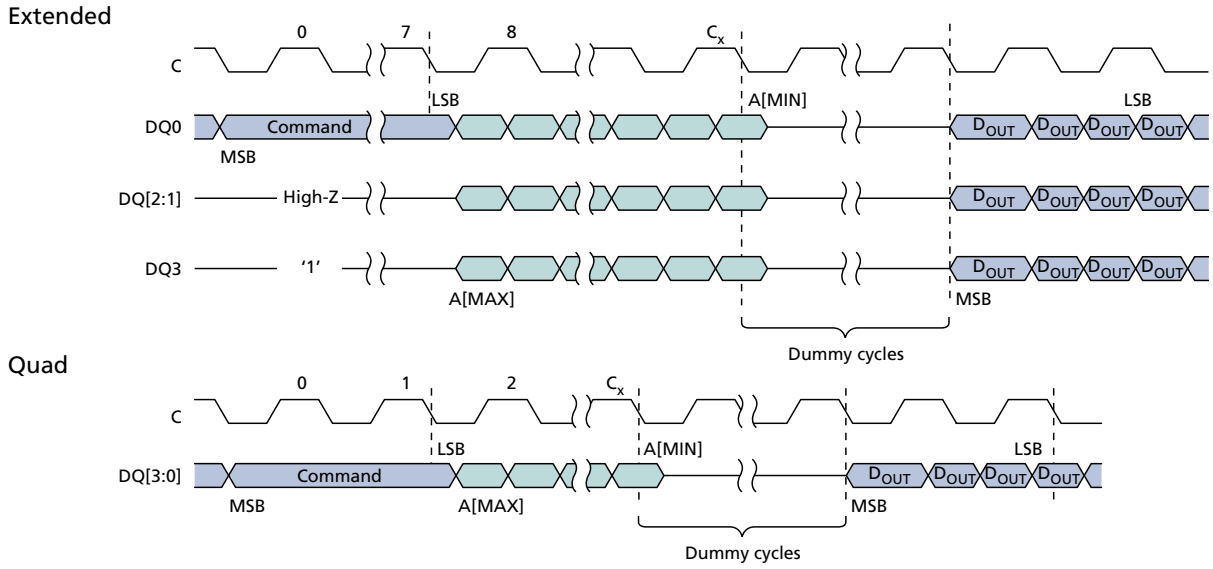
Figure 23: QUAD OUTPUT FAST READ Command – DTR



Notes: 1. C_x = 7 + (A[MAX] + 1)/2.
2. Shown here is the QUAD OUTPUT FAST READ timing for the extended SPI protocol. The quad timing shown for the FAST READ command is the equivalent of the QUAD OUTPUT FAST READ timing for the quad SPI protocol.

Figure 24: QUAD INPUT/OUTPUT FAST READ Command – DTR



Notes: 1. C_x = 7 + (A[MAX] + 1)/8.

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2. Shown here is the QUAD INPUT/OUTPUT FAST READ timing for the extended SPI protocol. The quad timing shown for the FAST READ command is the equivalent of the QUAD INPUT/OUTPUT FAST READ timing for the quad SPI protocol.

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PROGRAM Operations

PROGRAM commands are initiated by first executing the WRITE ENABLE command to set the write enable latch bit to 1. S# is then driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. The command code is input on DQ0, followed by input on DQ[n] of address bytes and at least one data byte. Each address bit is latched in during the rising edge of the clock. When S# is driven HIGH, the operation, which is self-timed, is initiated; its duration is ^{t}PP.

If the bits of the least significant address, which is the starting address, are not all zero, all data transmitted beyond the end of the current page is programmed from the starting address of the same page. If the number of bytes sent to the device exceed the maximum page size, previously latched data is discarded and only the last maximum page-size number of data bytes are guaranteed to be programmed correctly within the same page. If the number of bytes sent to the device is less than the maximum page size, they are correctly programmed at the specified addresses without any effect on the other bytes of the same page.

When the operation is in progress, the program or erase controller bit of the flag status register is set to 0. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. The operation is considered complete after bit 7 of the flag status register outputs 1 with at least one byte output. When the operation completes, the program or erase controller bit is cleared to 1.

If the operation times out, the write enable latch bit is reset and the program fail bit is set to 1. If S# is not driven HIGH, the command is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. When a command is applied to a protected sector, the command is not executed, the write enable latch bit remains set to 1, and flag status register bits 1 and 4 are set.

Note that the flag status register must be polled even if operation times out.

Table 27: Data/Address Lines for PROGRAM Commands

Note 1 applies to entire table

Command Name	Data In	Address In	Extended	Dual	Quad
PAGE PROGRAM	DQ0	DQ0	Yes	Yes	Yes
DUAL INPUT FAST PROGRAM	DQ[1:0]	DQ0	Yes	Yes	No
EXTENDED DUAL INPUT FAST PROGRAM	DQ[1:0]	DQ[1:0]	Yes	Yes	No
QUAD INPUT FAST PROGRAM	DQ[3:0]	DQ0	Yes	No	Yes
EXTENDED QUAD INPUT FAST PROGRAM	DQ[3:0]	DQ[3:0]	Yes	No	Yes

Note: 1. *Yes* in the protocol columns indicates that the command is supported and has the same functionality and command sequence as other commands marked *Yes*.

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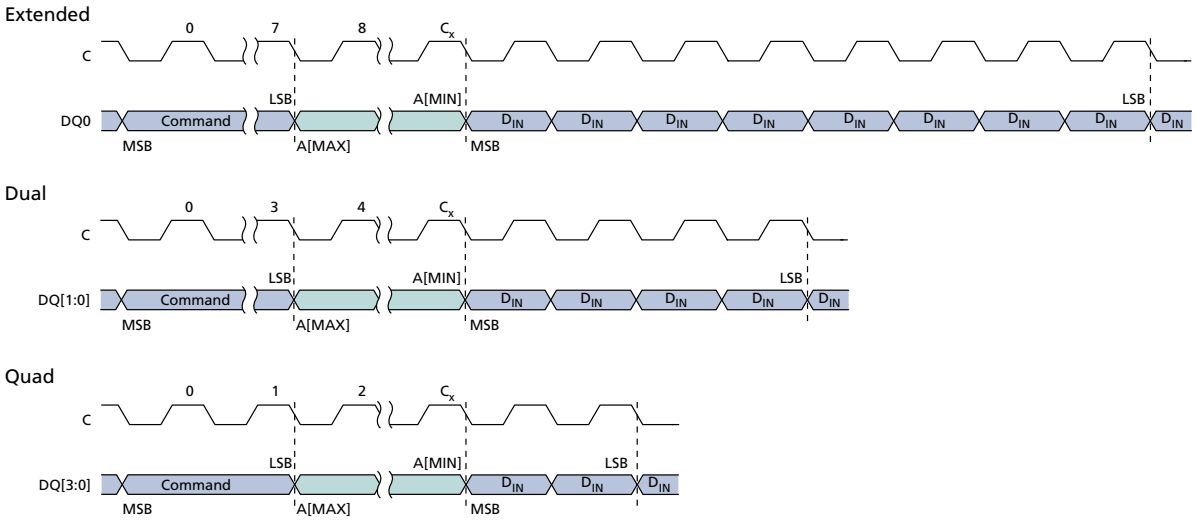
Figure 25: PAGE PROGRAM Command



Note: 1. For extended SPI protocol, C_x = 7 + (A[MAX] + 1).
For dual SPI protocol, C_x = 3 + (A[MAX] + 1)/2.
For quad SPI protocol, C_x = 1 + (A[MAX] + 1)/4.

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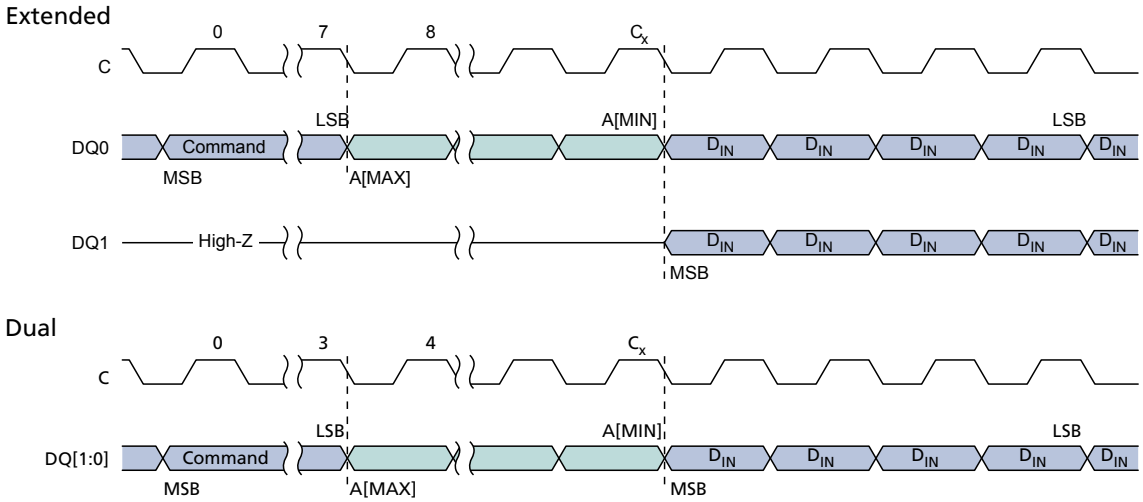
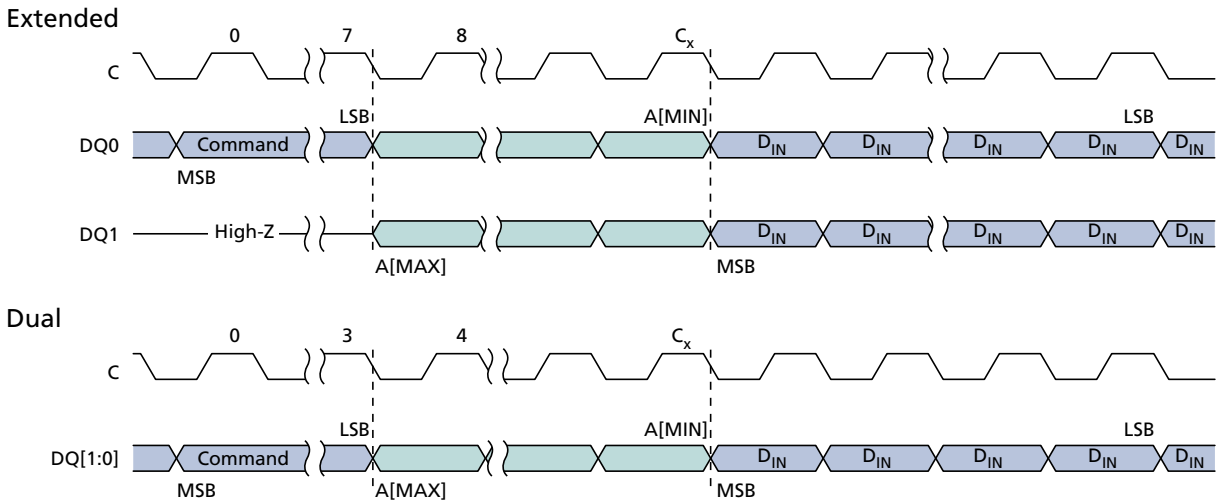
Figure 26: DUAL INPUT FAST PROGRAM Command



Note: 1. For extended SPI protocol, C_x = 7 + (A[MAX] + 1).
For dual SPI protocol, C_x = 3 + (A[MAX] + 1)/2.

Figure 27: EXTENDED DUAL INPUT FAST PROGRAM Command



Note: 1. For extended SPI protocol, C_x = 7 + (A[MAX] + 1)/2.
For dual SPI protocol, C_x = 3 + (A[MAX] + 1)/2.

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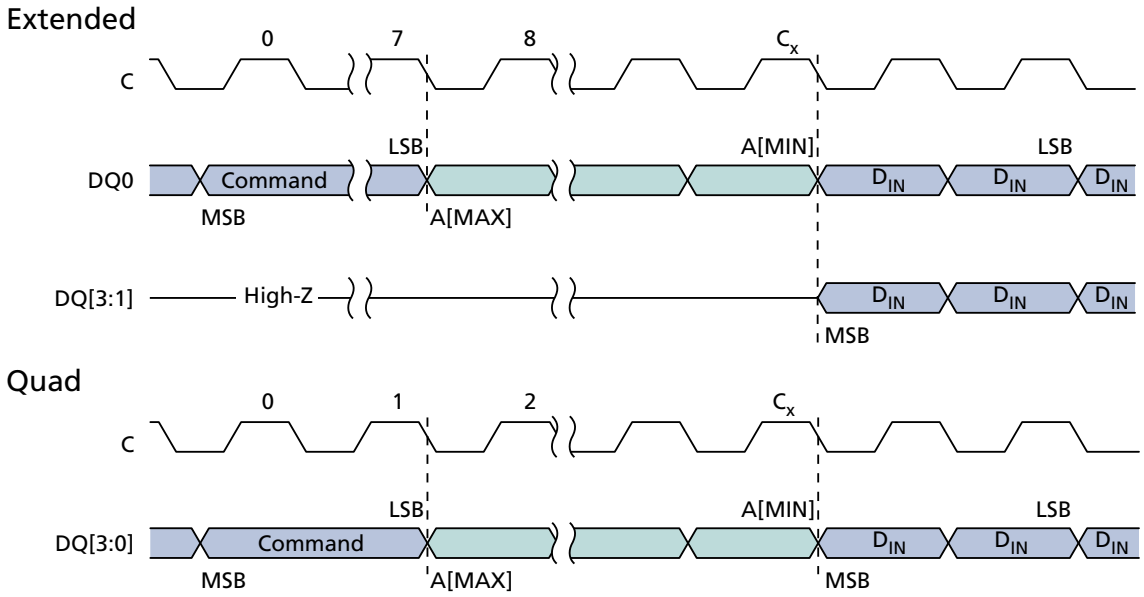
Figure 28: QUAD INPUT FAST PROGRAM Command



Note: 1. For extended SPI protocol, C_x = 7 + (A[MAX] + 1)/4.
For quad SPI protocol, C_x = 1 + (A[MAX] + 1)/4.

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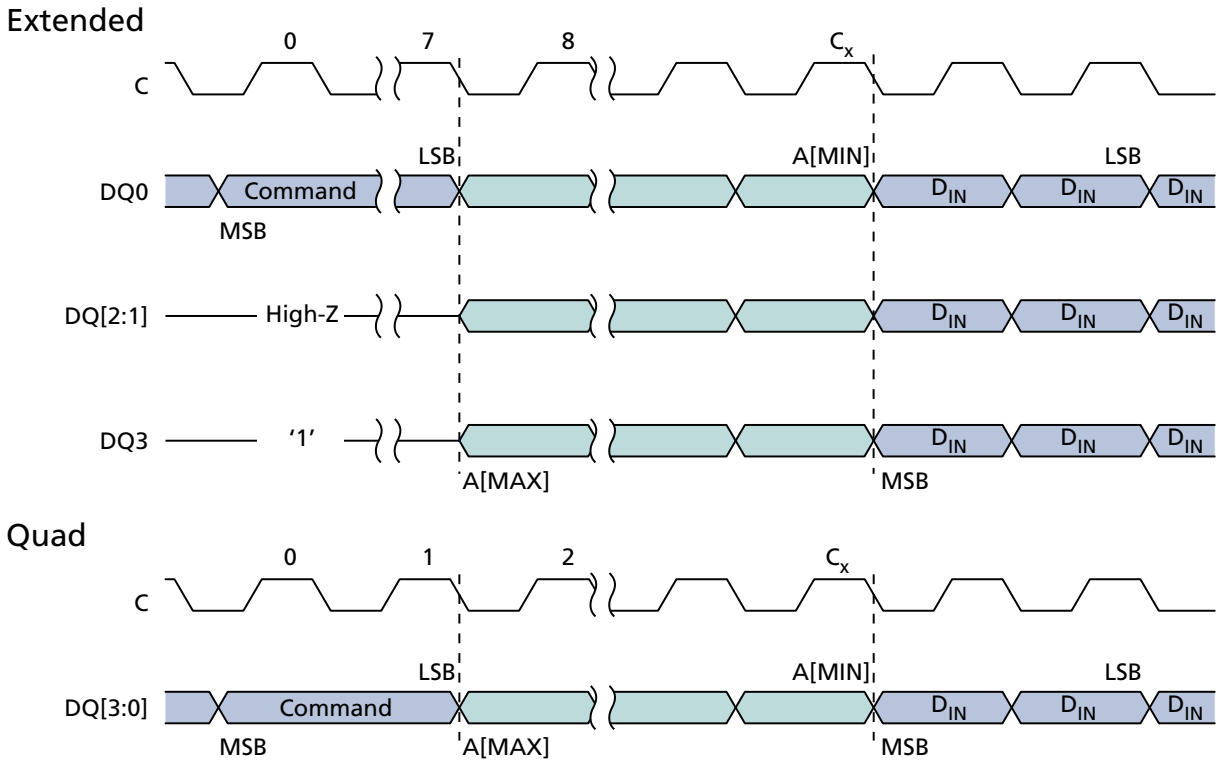
Figure 29: EXTENDED QUAD INPUT FAST PROGRAM Command



Note: 1. For extended SPI protocol, $C_x = 7 + (A[MAX] + 1)/4$.

For quad SPI protocol, $C_x = 1 + (A[MAX] + 1)/4$.

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WRITE Operations

WRITE ENABLE Command

The WRITE ENABLE operation sets the write enable latch bit. To execute a WRITE ENABLE command, S# is driven LOW and held LOW until the eighth bit of the command code has been latched in, after which it must be driven HIGH. The command code is input on DQ0 for extended SPI protocol, on DQ[1:0] for dual SPI protocol, and on DQ[3:0] for quad SPI protocol.

The write enable latch bit must be set before every PROGRAM, ERASE, WRITE, ENTER 4-BYTE ADDRESS MODE, and EXIT 4-BYTE ADDRESS MODE command. If S# is not driven HIGH after the command code has been latched in, the command is not executed, flag status register error bits are not set, and the write enable latch remains cleared to its default setting of 0.

WRITE DISABLE Command

The WRITE DISABLE operation clears the write enable latch bit. To execute a WRITE DISABLE command, S# is driven LOW and held LOW until the eighth bit of the command code has been latched in, after which it must be driven HIGH. The command code is input on DQ0 for extended SPI protocol, on DQ[1:0] for dual SPI protocol, and on DQ[3:0] for quad SPI protocol.

If S# is not driven HIGH after the command code has been latched in, the command is not executed, flag status register error bits are not set, and the write enable latch remains set to 1.

Note: In case of a protection error, write disable will not clear the write enable latch. In this situation, a CLEAR FLAG STATUS REGISTER command must be issued to clear both flags.

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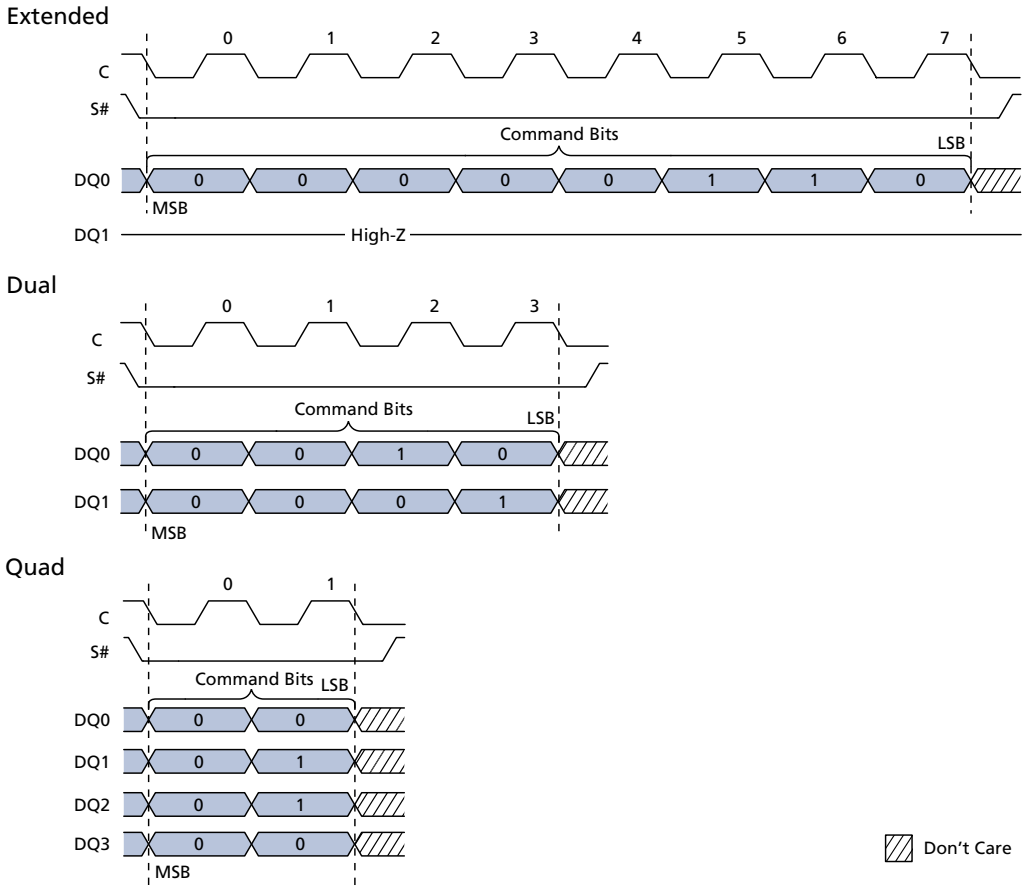
Figure 30: WRITE ENABLE and WRITE DISABLE Command Sequence



Note: 1. Shown here is the WRITE ENABLE command code, which is 06h or 0000 0110 binary. The WRITE DISABLE command sequence is identical, except the WRITE DISABLE command code is 04h or 0000 0100 binary.

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ERASE Operations

When the operation is in progress, the program or erase controller bit of the flag status register is set to 0. The flag status register must be polled for the operation status. When the operation completes, that bit is cleared to 1.

Note that the flag status register must be polled even if operation times out.

SUBSECTOR ERASE Command

To execute the SUBSECTOR ERASE command (and set the selected subsector bits to FFh), the WRITE ENABLE command must be issued to set the write enable latch bit to 1. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. The command code is input on DQ0, followed by address bytes; any address within the subsector is valid. Each address bit is latched in during the rising edge of the clock. When S# is driven HIGH, the operation, which is self-timed, is initiated; its duration is ^{t}SSE. The operation can be suspended and resumed by the PROGRAM/ERASE SUSPEND and PROGRAM/ERASE RESUME commands, respectively.

If the write enable latch bit is not set, the device ignores the SUBSECTOR ERASE command and no error bits are set to indicate operation failure.

When the operation is in progress, the program or erase controller bit is set to 0. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. The operation is considered complete once bit 7 of the flag status register outputs 1 with at least one byte output. When the operation completes, the program or erase controller bit is cleared to 1.

If the operation times out, the write enable latch bit is reset and the erase error bit is set to 1. If S# is not driven HIGH, the command is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. When a command is applied to a protected subsector, the command is not executed. Instead, the write enable latch bit remains set to 1, and flag status register bits 1 and 5 are set.

SECTOR ERASE Command

To execute the SECTOR ERASE command (and set selected sector bits to FFh), the WRITE ENABLE command must be issued to set the write enable latch bit to 1. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. The command code is input on DQ0, followed by address bytes; any address within the sector is valid. Each address bit is latched in during the rising edge of the clock. When S# is driven HIGH, the operation, which is self-timed, is initiated; its duration is ^{t}SE. The operation can be suspended and resumed by the PROGRAM/ERASE SUSPEND and PROGRAM/ERASE RESUME commands, respectively.

If the write enable latch bit is not set, the device ignores the SECTOR ERASE command and no error bits are set to indicate operation failure.

When the operation is in progress, the program or erase controller bit is set to 0. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. The operation is considered complete once bit 7 of the flag status register outputs 1 with at least one

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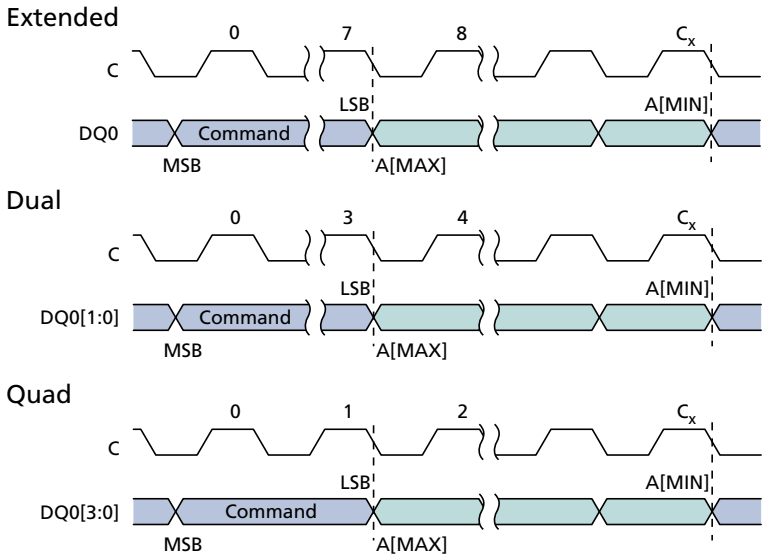
byte output. When the operation completes, the program or erase controller bit is cleared to 1.

If the operation times out, the write enable latch bit is reset and erase error bit is set to 1. If S# is not driven HIGH, the command is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. When a command is applied to a protected sector, the command is not executed. Instead, the write enable latch bit remains set to 1, and flag status register bits 1 and 5 are set.

Figure 31: SUBSECTOR and SECTOR ERASE Command



Note: 1. For extended SPI protocol, C_x = 7 + (A[MAX] + 1).

For dual SPI protocol, C_x = 3 + (A[MAX] + 1)/2.

For quad SPI protocol, C_x = 1 + (A[MAX] + 1)/4.

DIE ERASE Command

To initiate the DIE ERASE command, the WRITE ENABLE command must be issued to set the write enable latch bit to 1. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. The command code is input on DQ0, followed by address bytes; any address within the single 256Mb die is valid. Each address bit is latched in during the rising edge of the clock. When S# is driven HIGH, the operation, which is self-timed, is initiated; its duration is ^{t}DSE.

If the write enable latch bit is not set, the device ignores the DIE ERASE command and no error bits are set to indicate operation failure.

When the operation is in progress, the program or erase controller bit is set to 0. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. The operation is considered complete once bit 7 of the flag status register outputs 1 with at least one

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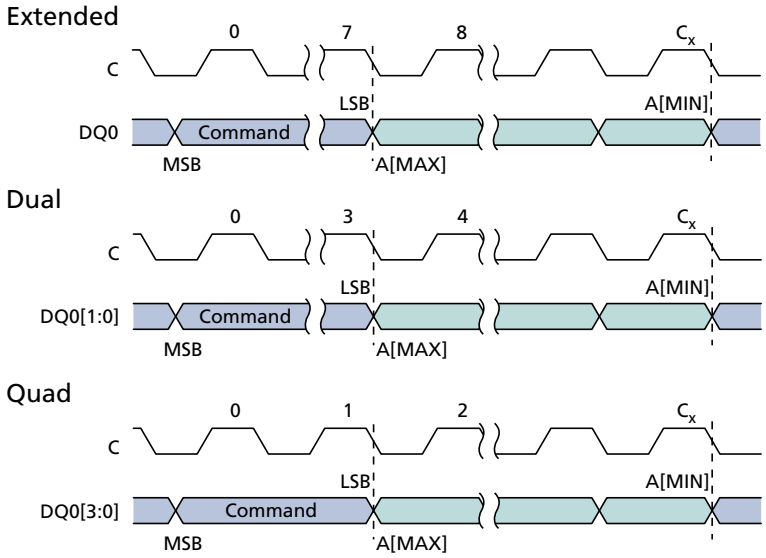
byte output. When the operation completes, the program or erase controller bit is cleared to 1.

The command is not executed if any sector is locked. Instead, the write enable latch bit remains set to 1, and flag status register bits 1 and 5 are set.

Figure 32: DIE ERASE Command



Note: 1. For extended SPI protocol, C_x = 7 + (A[MAX] + 1).

For dual SPI protocol, C_x = 3 + (A[MAX] + 1)/2.

For quad SPI protocol, C_x = 1 + (A[MAX] + 1)/4.

PROGRAM/ERASE SUSPEND Command

To initiate the PROGRAM/ERASE SUSPEND command, S# is driven LOW. The command code is input on DQ0. The operation is terminated by the PROGRAM/ERASE RESUME command.

PROGRAM/ERASE SUSPEND command enables the memory controller to interrupt and suspend an array PROGRAM or ERASE operation within the program/erase latency.

If a SUSPEND command is issued during a PROGRAM operation, then the flag status register bit 2 is set to 1. After erase/program latency time, the flag status register bit 7 is also set to 1, but the device is considered in suspended state once bit 7 of the flag status register outputs 1 with at least one byte output. In the suspended state, the device is waiting for any operation. (See the Operations Allowed/Disallowed During Device States table.)

If a SUSPEND command is issued during an ERASE operation, then the flag status register bit 6 is set to 1. After erase/program latency time, the flag status register bit 7 is also set to 1, but the device is considered in suspended state once bit 7 of the flag status register outputs 1 with at least one byte output. In the suspended state, the device is waiting for any operation. (See the Operations Allowed/Disallowed During Device States table.)

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If the time remaining to complete the operation is less than the suspend latency, the device completes the operation and clears the flag status register bits 2 or 6, as applicable. Because the suspend state is volatile, if there is a power cycle, the suspend state information is lost and the flag status register powers up as 80h.

During an ERASE SUSPEND operation, a PROGRAM or READ operation is possible in any sector except the one in a suspended state. Reading from a sector that is in a suspended state will output indeterminate data. The device ignores a PROGRAM command to a sector that is in an erase suspend state; it also sets the flag status register bit 4 to 1, program failure/protection error, and leaves the write enable latch bit unchanged. The commands allowed during an erase suspend state are shown in the Operations Allowed/Disallowed During Device States table. When the ERASE resumes, it does not check the new lock status of the WRITE LOCK REGISTER command.

During a PROGRAM SUSPEND operation, a READ operation is possible in any page except the one in a suspended state. Reading from a page that is in a suspended state will output indeterminate data. The commands allowed during a program suspend state include the WRITE VOLATILE CONFIGURATION REGISTER command and the WRITE ENHANCED VOLATILE CONFIGURATION REGISTER command.

It is possible to nest a PROGRAM/ERASE SUSPEND operation inside a PROGRAM/ERASE SUSPEND operation just once. Issue an ERASE command and suspend it. Then issue a PROGRAM command and suspend it also. With the two operations suspended, the next PROGRAM/ERASE RESUME command resumes the latter operation, and a second PROGRAM/ERASE RESUME command resumes the former (or first) operation.

Table 28: Suspend Parameters

Parameter	Condition	Typ	Max	Units	Notes
Erase to suspend	Sector erase or erase resume to erase suspend	700	–	µs	1
Program to suspend	Program resume to program suspend	5	–	µs	1
Subsector erase to suspend	Subsector erase or subsector erase resume to erase suspend	50	–	µs	1
Suspend latency	Program	7	–	µs	2
Suspend latency	Subsector erase	15	–	µs	2
Suspend latency	Erase	15	–	µs	3

Notes:
1. Timing is not internally controlled.
2. Any READ command accepted.
3. Any command except the following are accepted: SECTOR, SUBSECTOR, or DIE ERASE; WRITE STATUS REGISTER; WRITE NONVOLATILE CONFIGURATION REGISTER; and PROGRAM OTP.

Table 29: Operations Allowed/Disallowed During Device States

Note 1 applies to entire table

Operation	Standby State	Program or Erase State	Subsector Erase Suspend or Program Suspend State	Erase Suspend State	Notes
READ	Yes	No	Yes	Yes	2
PROGRAM	Yes	No	No	Yes/No	3
ERASE	Yes	No	No	No	4

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Table 29: Operations Allowed/Disallowed During Device States (Continued)

Note 1 applies to entire table

Operation	Standby State	Program or Erase State	Subsector Erase Suspend or Program Suspend State	Erase Suspend State	Notes
WRITE	Yes	No	No	No	5
WRITE	Yes	No	Yes	Yes	6
READ	Yes	Yes	Yes	Yes	7
SUSPEND	No	Yes	No	No	8

Notes:
1. The device can be in only one state at a time. Depending on the state of the device, some operations are allowed (Yes) and others are not (No). For example, when the device is in the standby state, all operations except SUSPEND are allowed in any sector. For all device states except the erase suspend state, if an operation is allowed or disallowed in one sector, it is allowed or disallowed in all other sectors. In the erase suspend state, a PROGRAM operation is allowed in any sector except the one in which an ERASE operation has been suspended.
2. All READ operations except READ STATUS REGISTER and READ FLAG REGISTER. When issued to a sector or subsector that is simultaneously in an erase suspend state, the READ operation is accepted, but the data output is not guaranteed until the erase has completed.
3. All PROGRAM operations except PROGRAM OTP. In the erase suspend state, a PROGRAM operation is allowed in any sector (Yes) except the sector (No) in which an ERASE operation has been suspended.
4. Applies to the SECTOR ERASE or SUBSECTOR ERASE operation.
5. Applies to the following operations: WRITE STATUS REGISTER, WRITE NONVOLATILE CONFIGURATION REGISTER, PROGRAM OTP, and DIE ERASE.
6. Applies to the WRITE VOLATILE CONFIGURATION REGISTER, WRITE ENHANCED VOLATILE CONFIGURATION REGISTER, WRITE ENABLE, WRITE DISABLE, CLEAR FLAG STATUS REGISTER, WRITE EXTENDED ADDRESS REGISTER, ENTER 4-BYTE EXTENDED ADDRESS REGISTER, EXIT 4-BYTE EXTENDED ADDRESS REGISTER, or WRITE LOCK REGISTER operation.
7. Applies to the READ STATUS REGISTER or READ FLAG STATUS REGISTER operation.
8. Applies to the PROGRAM SUSPEND or ERASE SUSPEND operation.

PROGRAM/ERASE RESUME Command

To initiate the PROGRAM/ERASE RESUME command, S# is driven LOW. The command code is input on DQ0. The operation is terminated by driving S# HIGH.

When this command is executed, the status register write in progress bit is set to 1, and the flag status register program erase controller bit is set to 0. This command is ignored if the device is not in a suspended state.

When the operation is in progress, the program or erase controller bit of the flag status register is set to 0. The flag status register must be polled for the operation status. When the operation completes, that bit is cleared to 1. Note that the flag status register must be polled even if operation times out.

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RESET Operations

Table 30: Reset Command Set

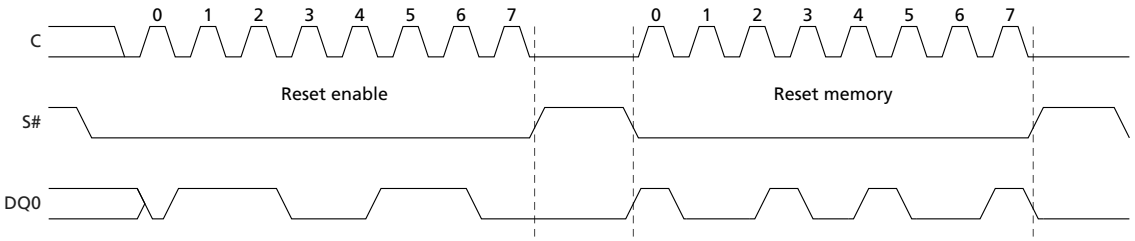
Command	Command Code (Binary)	Command Code (Hex)	Address Bytes
RESET ENABLE	0110 0110	66	0
RESET MEMORY	1001 1001	99	0

RESET ENABLE and RESET MEMORY Command

To reset the device, the RESET ENABLE command must be followed by the RESET MEMORY command. To execute each command, S# is driven LOW. The command code is input on DQ0. A minimum de-selection time of ^{t}SHSL2 must come between the RESET ENABLE and RESET MEMORY commands or a reset is not guaranteed. When these two commands are executed and S# is driven HIGH, the device enters a power-on reset condition. A time of ^{t}SHSL3 is required before the device can be re-selected by driving S# LOW. It is recommended that the device exit XIP mode before executing these two commands to initiate a reset.

If a reset is initiated while a WRITE, PROGRAM, or ERASE operation is in progress or suspended, the operation is aborted and data may be corrupted.

Figure 33: RESET ENABLE and RESET MEMORY Command



Note: 1. The number of lines and rate for transmission varies with extended, dual, or quad SPI.

RESET Conditions

All volatile lock bits, the volatile configuration register, the enhanced volatile configuration register, and the extended address register are reset to the power-on reset default condition. The power-on reset condition depends on settings in the nonvolatile configuration register.

Reset is effective once bit 7 of the flag status register outputs 1 with at least one byte output. A RESET ENABLE command is not accepted in the cases of WRITE STATUS REGISTER and WRITE NONVOLATILE CONFIGURATION REGISTER operations.

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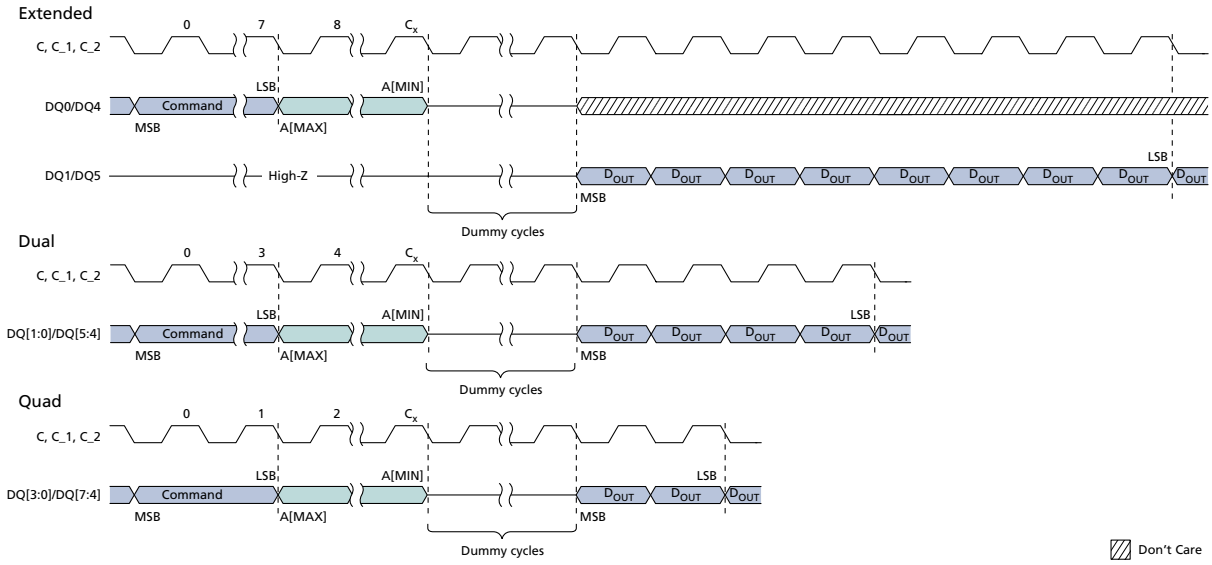
ONE-TIME PROGRAMMABLE Operations

READ OTP ARRAY Command

To initiate a READ OTP ARRAY command, S# is driven LOW. The command code is input on DQ0/DQ4, followed by address bytes and dummy clock cycles. Each address bit is latched in during the rising edge of C. Data is shifted out on DQ1/DQ5, beginning from the specified address and at a maximum frequency of ^{f}C (MAX) on the falling edge of the clock. The address increments automatically to the next address after each byte of data is shifted out. There is no rollover mechanism; therefore, if read continuously, after location 0x40, the device continues to output data at location 0x40. The operation is terminated by driving S# HIGH at any time during data output.

Figure 34: READ OTP Command



Note: 1. For extended SPI protocol, C_x = 7 + (A[MAX] + 1).

For dual SPI protocol, C_x = 3 + (A[MAX] + 1)/2.

For quad SPI protocol, C_x = 1 + (A[MAX] + 1)/4.

PROGRAM OTP ARRAY Command

To initiate the PROGRAM OTP ARRAY command, the WRITE ENABLE command must be issued to set the write enable latch bit to 1; otherwise, the PROGRAM OTP ARRAY command is ignored and flag status register bits are not set. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. The command code is input on DQ0/DQ4, followed by address bytes and at least one data byte. Each address bit is latched in during the rising edge of the clock. When S# is driven HIGH, the operation, which is self-timed, is initiated; its duration is $^{t}POTP$. There is no rollover mechanism; therefore, after a maximum of 65 bytes are latched in the subsequent bytes are discarded.

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PROGRAM OTP ARRAY programs, at most, 64 bytes to the OTP memory area and one OTP control byte. When the operation is in progress, the write in progress bit is set to 1. The write enable latch bit is cleared to 0, whether the operation is successful or not, and the status register and flag status register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0.

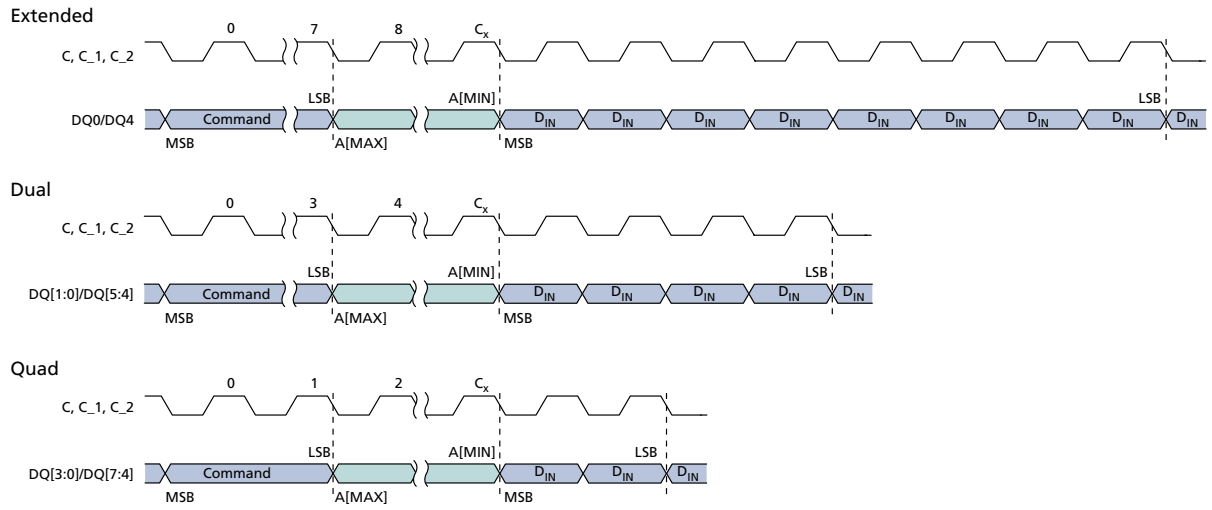
If the operation times out, the write enable latch bit is reset and the program fail bit is set to 1. If S# is not driven HIGH, the command is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. The operation is considered complete once bit 7 of the flag status register outputs 1 with at least one byte output.

The OTP control byte (byte 64) is used to permanently lock the OTP memory array.

Table 31: OTP Control Byte (Byte 64)

Bit	Name	Settings	Description
0	OTP control byte	0 = Locked 1 = Unlocked (Default)	Used to permanently lock the 64-byte OTP array. When bit 0 = 1, the 64-byte OTP array can be programmed. When bit 0 = 0, the 64-byte OTP array is read only. Once bit 0 has been programmed to 0, it can no longer be changed to 1. Program OTP array is ignored, the write enable latch bit remains set, and flag status register bits 1 and 4 are set.

Figure 35: PROGRAM OTP Command



Note: 1. For extended SPI protocol, C_x = 7 + (A[MAX] + 1).
For dual SPI protocol, C_x = 3 + (A[MAX] + 1)/2.
For quad SPI protocol, C_x = 1 + (A[MAX] + 1)/4.

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ADDRESS MODE Operations – Enter and Exit 4-Byte Address Mode

ENTER or EXIT 4-BYTE ADDRESS MODE Command

Both ENTER 4-BYTE ADDRESS MODE and EXIT 4-BYTE ADDRESS MODE commands share the same requirements.

To enter or exit the 4-byte address mode, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. S# must be driven LOW. The command must be input on DQ*n*. The effect of the command is immediate; after the command has been executed, the write enable latch bit is cleared to 0.

The default address mode is three bytes, and the device returns to the default upon exiting the 4-byte address mode.

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XIP Mode

Execute-in-place (XIP) mode allows the memory to be read by sending an address to the device and then receiving the data on one, two, or four pins in parallel, depending on the customer requirements. XIP mode offers maximum flexibility to the application, saves instruction overhead, and reduces random access time.

Activate or Terminate XIP Using Volatile Configuration Register

Applications that boot in SPI and must switch to XIP use the volatile configuration register. XIP provides faster memory READ operations by requiring only an address to execute, rather than a command code and an address.

To activate XIP requires two steps. First, enable XIP by setting volatile configuration register bit 3 to 0. Next, drive the XIP confirmation bit to 0 during the next FAST READ operation. XIP is then active. Once in XIP, any command that occurs after S# is toggled requires only address bits to execute; a command code is not necessary, and device operations use the SPI protocol that is enabled. XIP is terminated by driving the XIP confirmation bit to 1. The device automatically resets volatile configuration register bit 3 to 1.

Note: For devices with basic XIP, indicated by a part number feature set digit of 2 or 4, it is not necessary to set the volatile configuration register bit 3 to 0 to enable XIP. Instead, it is enabled by setting the XIP confirmation bit to 0 during the first dummy clock cycle after any FAST READ command.

Activate or Terminate XIP Using Nonvolatile Configuration Register

Applications that must boot directly in XIP use the nonvolatile configuration register. To enable a device to power-up in XIP using the nonvolatile configuration register, set nonvolatile configuration register bits [11:9]. Settings vary according to protocol, as explained in the Nonvolatile Configuration Register section. Because the device boots directly in XIP, after the power cycle, no command code is necessary. XIP is terminated by driving the XIP confirmation bit to 1.

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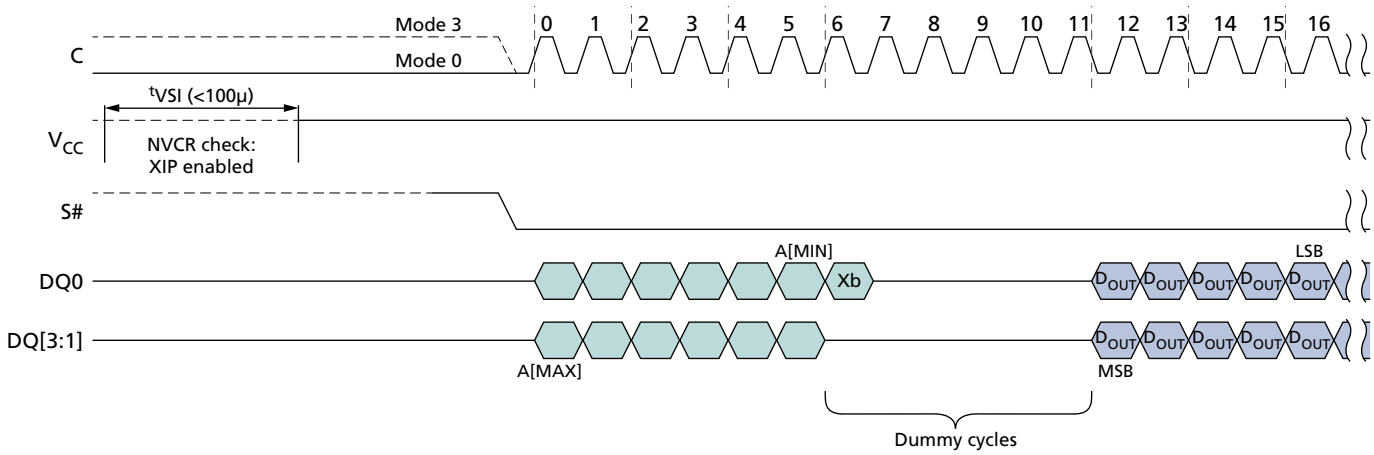
Figure 36: XIP Mode Directly After Power-On



Note: 1. Xb is the XIP confirmation bit and should be set as follows: 0 to keep XIP state; 1 to exit XIP mode and return to standard read mode.

Confirmation Bit Settings Required to Activate or Terminate XIP

The XIP confirmation bit setting activates or terminates XIP after it has been enabled or disabled. This bit is the value on DQ0 during the first dummy clock cycle in the FAST READ operation. In dual I/O XIP mode, the value of DQ1 during the first dummy clock cycle after the addresses is always "Don't Care." In quad I/O XIP mode, the values of DQ3, DQ2, and DQ1 during the first dummy clock cycle after the addresses are always "Don't Care."

Table 32: XIP Confirmation Bit

Bit Value	Description
0	Activates XIP: While this bit is 0, XIP remains activated.
1	Terminates XIP: When this bit is set to 1, XIP is terminated and the device returns to SPI.

Table 33: Effects of Running XIP in Different Protocols

Protocol	Effect
Extended I/O and Dual I/O	In a device with a dedicated part number where RST# is enabled, a LOW pulse on that pin resets XIP and the device to the state it was in previous to the last power-up, as defined by the nonvolatile configuration register.
Dual I/O	Values of DQ1 during the first dummy clock cycle are "Don't Care."

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Table 33: Effects of Running XIP in Different Protocols (Continued)

Protocol	Effect
Quad I/O[1]	Values of DQ[3:1] during the first dummy clock cycle are "Don't Care." In a device with a dedicated part number, it is only possible to reset memory when the device is deselected.

Note: 1. In a device with a dedicated part number where RST# is enabled, a LOW pulse on that pin resets XIP and the device to the state it was in previous to the last power-up, as defined by the nonvolatile configuration register only when the device is deselected.

Terminating XIP After a Controller and Memory Reset

The system controller and the device can become out of synchronization if, during the life of the application, the system controller is reset without the device being reset. In such a case, the controller can reset the memory to power-on reset if the memory has reset functionality. (Reset is available in devices with a dedicated part number.)

- 7 clock cycles within S# LOW (S# becomes HIGH before 8th clock cycle)
- + 9 clock cycles within S# LOW (S# becomes HIGH before 10th clock cycle)
- + 13 clock cycles within S# LOW (S# becomes HIGH before 14th clock cycle)
- + 17 clock cycles within S# LOW (S# becomes HIGH before 18th clock cycle)
- + 25 clock cycles within S# LOW (S# becomes HIGH before 26th clock cycle)
- + 33 clock cycles within S# LOW (S# becomes HIGH before 34th clock cycle)

These sequences cause the controller to set the XIP confirmation bit to 1, thereby terminating XIP. However, it does not reset the device or interrupt PROGRAM/ERASE operations that may be in progress. After terminating XIP, the controller must execute RESET ENABLE and RESET MEMORY to implement a software reset and reset the device.

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Power-Up and Power-Down

Power-Up and Power-Down Requirements

At power-up and power-down, the device must not be selected; that is, S# must follow the voltage applied on V_{CC} until V_{CC} reaches the correct values: $V_{CC,min}$ at power-up and V_{SS} at power-down.

To avoid data corruption and inadvertent WRITE operations during power-up, a power-on reset circuit is included. The logic inside the device is held to RESET while V_{CC} is less than the power-on reset threshold voltage shown here; all operations are disabled, and the device does not respond to any instruction. During a standard power-up phase, the device ignores all commands except READ STATUS REGISTER and READ FLAG STATUS REGISTER. These operations can be used to check the memory internal state. After power-up, the device is in standby power mode; the write enable latch bit is reset; the write in progress bit is reset; and the lock registers are configured as: (write lock bit, lock down bit) = (0,0).

Normal precautions must be taken for supply line decoupling to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} line decoupled by a suitable capacitor (typically 100nF) close to the package pins. At power-down, when V_{CC} drops from the operating voltage to below the power-on-reset threshold voltage shown here, all operations are disabled and the device does not respond to any command.

When the operation is in progress, the program or erase controller bit of the status register is set to 0. To obtain the operation status, the flag status register must be polled once for each die in the device, with S# toggled twice between commands, until each die is ready. When the operation completes, the program or erase controller bit is cleared to 1. The cycle is complete after the flag status register outputs the program or erase controller bit to 1 for each polling operation.

Note: If power-down occurs while a WRITE, PROGRAM, or ERASE cycle is in progress, data corruption may result.

V_{PPH} must be applied only when V_{CC} is stable and in the $V_{CC,min}$ to $V_{CC,max}$ voltage range.

Figure 37: Power-Up Timing

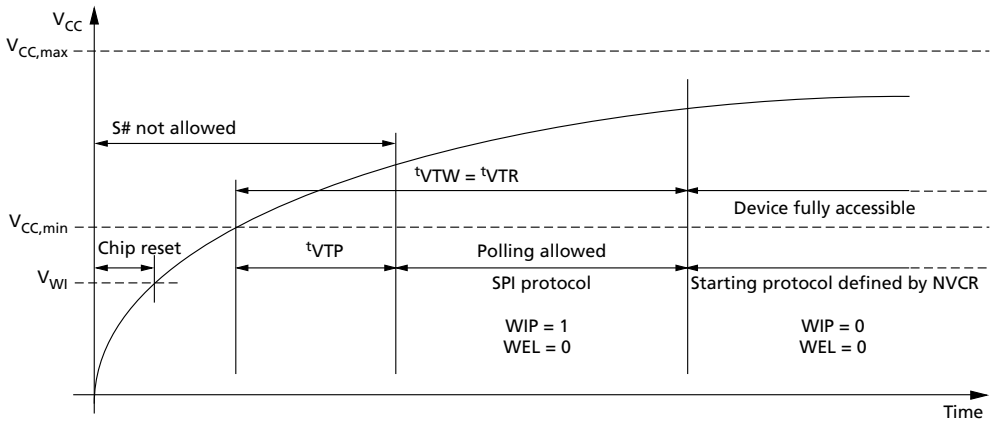

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Table 34: Power-Up Timing and V_{WI} Threshold

Note 1 applies to entire table

Symbol	Parameter	Min	Max	Unit
^{t}VTR	$V_{CC,min}$ to read	–	150	µs
^{t}VTW	$V_{CC,min}$ to device fully accessible	–	150	µs
V_{WI}	Write inhibit voltage	1.5	2.5	V
^{t}VTP	$V_{CC,min}$ to polling allowed	–	100	µs

Note: 1. Parameters listed are characterized only.

Power Loss Recovery Sequence

If a power loss occurs during a WRITE NONVOLATILE CONFIGURATION REGISTER command, after the next power-on, the device might begin in an undetermined state (XIP mode or an unnecessary protocol). If this occurs, until the next power-up, a recovery sequence must reset the device to a fixed state (extended SPI protocol without XIP). After the recovery sequence, the issue should be resolved definitively by running the WRITE NONVOLATILE CONFIGURATION REGISTER command again. The recovery sequence is composed of two parts that must be run in the correct order. During the entire sequence, $^{t}SHSL2$ must be at least 50ns. The first part of the sequence is DQ0 (PAD DATA) and DQ3 (PAD HOLD) equal to 1 for the situations listed below:

- 7 clock cycles within S# LOW (S# becomes HIGH before 8th clock cycle)
- + 9 clock cycles within S# LOW (S# becomes HIGH before 10th clock cycle)
- + 13 clock cycles within S# LOW (S# becomes HIGH before 14th clock cycle)
- + 17 clock cycles within S# LOW (S# becomes HIGH before 18th clock cycle)
- + 25 clock cycles within S# LOW (S# becomes HIGH before 26th clock cycle)
- + 33 clock cycles within S# LOW (S# becomes HIGH before 34th clock cycle)

The second part of the sequence is exiting from dual or quad SPI protocol by using the following FFh sequence: DQ0 and DQ3 equal to 1 for 8 clock cycles within S# LOW; S# becomes HIGH before 9th clock cycle.

After this two-part sequence the extended SPI protocol is active.

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AC Reset Specifications

Table 35: AC RESET Conditions

Note 1 applies to entire table

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reset pulse width	^{t}RLRH[2]		50	–	–	ns
Reset recovery time	^{t}RHSL	Device deselected (S# HIGH) and is in XIP mode	–	–	40	ns
		Device deselected (S# HIGH) and is in standby mode	–	–	40	ns
		Commands are being decoded, any READ operations are in progress or any WRITE operation to volatile registers are in progress	–	–	40	ns
		Any device array PROGRAM/ERASE/SUSPEND/RESUME, PROGRAM OTP, NONVOLATILE SECTOR LOCK, and ERASE NONVOLATILE SECTOR LOCK ARRAY operations are in progress	–	–	30	µs
		While a WRITE STATUS REGISTER operation is in progress	–	^{t}W	–	ms
		While a WRITE NONVOLATILE CONFIGURATION REGISTER operation is in progress	–	^{t}WNVCR	–	ms
		On completion or suspension of a SUBSECTOR ERASE operation	–	^{t}SSE	–	s
Software reset recovery time	^{t}SHSL3	Device deselected (S# HIGH) and is in standby mode	–	–	40	ns
		Any Flash array PROGRAM/ERASE/SUSPEND/RESUME, PROGRAM OTP, NONVOLATILE SECTOR LOCK, and ERASE NONVOLATILE SECTOR LOCK ARRAY operations are in progress	–	–	30	µs
		While WRITE STATUS REGISTER operation is in progress	–	^{t}W	–	ms
		While a WRITE NONVOLATILE CONFIGURATION REGISTER operation is in progress	–	^{t}WNVCR	–	ms
		On completion or suspension of a SUBSECTOR ERASE operation	–	^{t}SSE	–	s
S# deselect to reset valid	^{t}SHRV	Deselect to reset valid in quad output or in QIO-SPI	2	–	–	ns

Notes:
1. Values are guaranteed by characterization; not 100% tested.
2. The device reset is possible but not guaranteed if ^{t}RLRH < 50ns.

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Figure 38: Reset AC Timing During PROGRAM or ERASE Cycle

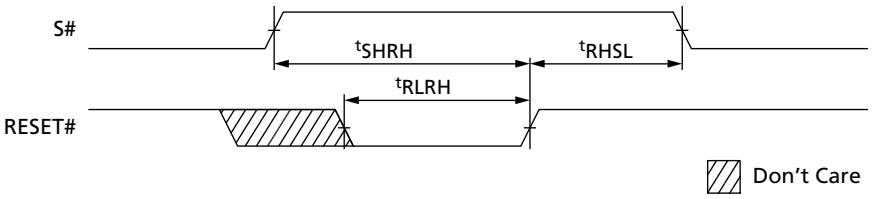

Figure 39: Reset Enable

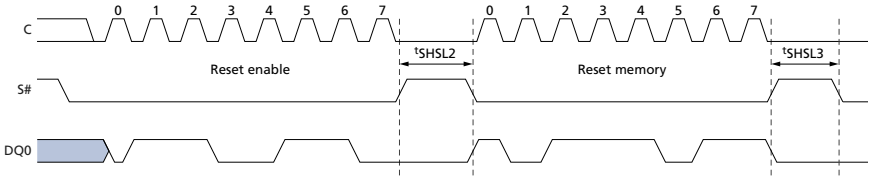

Figure 40: Serial Input Timing

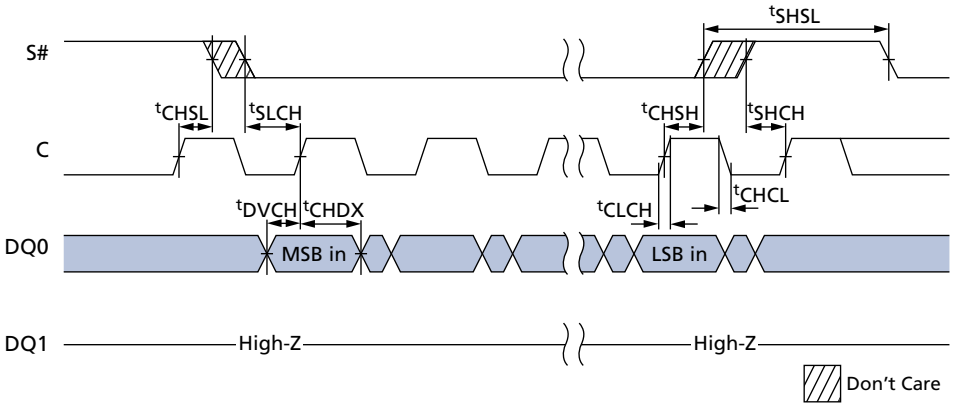

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Figure 41: Hold Timing

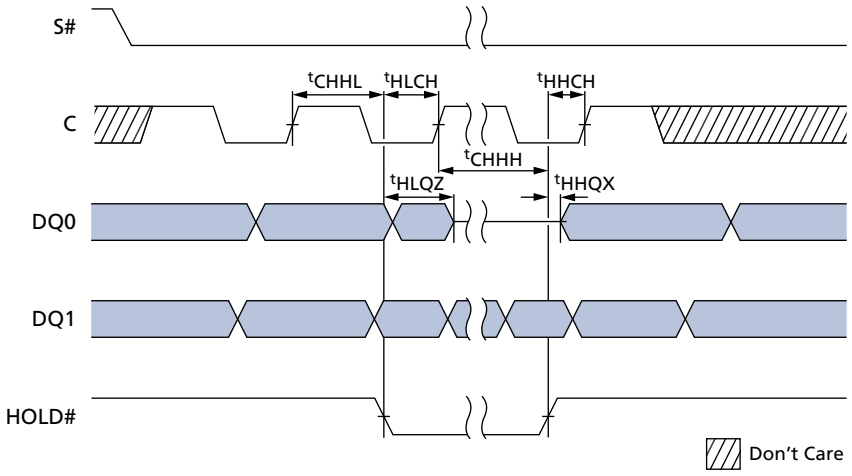

Figure 42: Output Timing

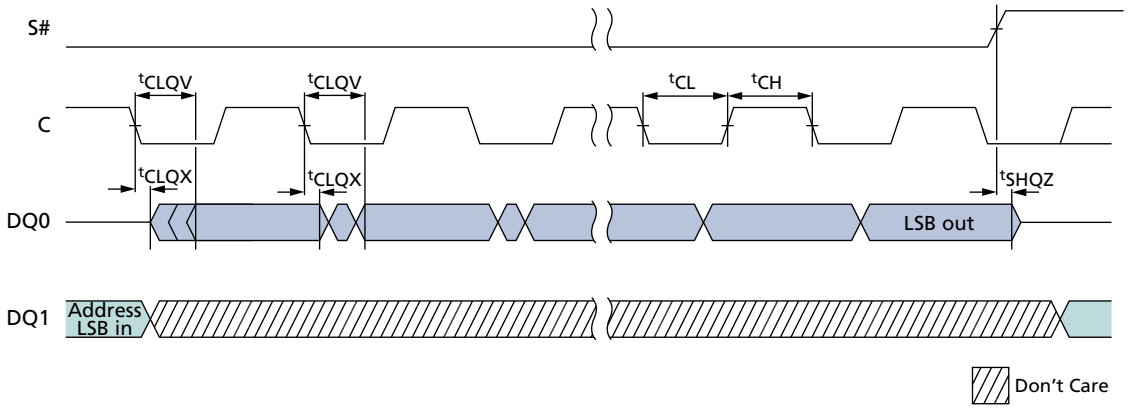

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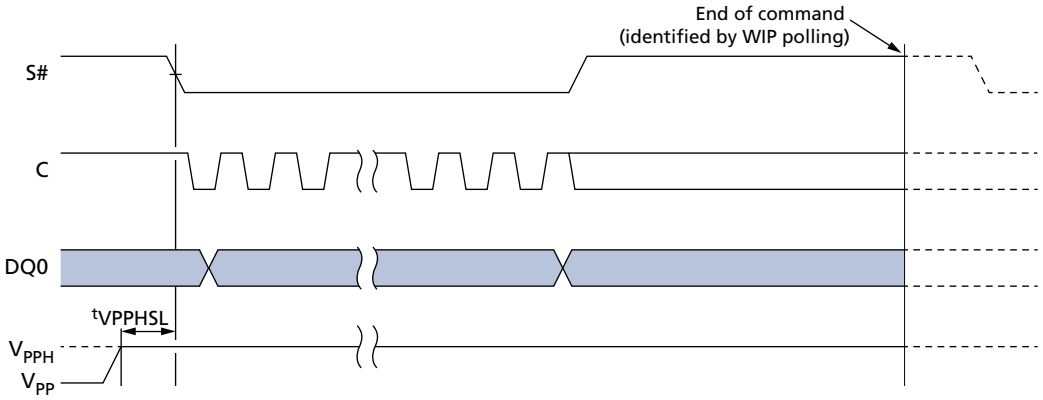
Figure 43: V_{PPH} Timing



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Absolute Ratings and Operating Conditions

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating for extended periods may adversely affect reliability. Stressing the device beyond the absolute maximum ratings may cause permanent damage.

Table 36: Absolute Ratings

Symbol	Parameter	Min	Max	Units	Notes
T_{STG}	Storage temperature	–65	150	°C	
T_{LEAD}	Lead temperature during soldering	–	See note 1	°C	
V_{CC}	Supply voltage	–0.6	4.0	V	
V_{PP}	Fast program/erase voltage	–0.2	10	V	
V_{IO}	Input/output voltage with respect to ground	–0.6	V_{CC} + 0.6	V	3, 4
V_{ESD}	Electrostatic discharge voltage (human body model)	–2000	2000	V	2

Notes:
1. Compliant with JEDEC Standard J-STD-020C (for small-body, Sn-Pb or Pb assembly), RoHS, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. JEDEC Standard JESD22-A114A (C1 = 100pF, R1 = 1500Ω, R2 = 500Ω).
3. During signal transitions, minimum voltage may undershoot to –1V for periods less than 10ns.
4. During signal transitions, maximum voltage may overshoot to V_{CC} + 1V for periods less than 10ns.

Table 37: Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply voltage	2.7	3.6	V
V_{PPH}	Supply voltage on V_{PP}	8.5	9.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 38: Input/Output Capacitance

Note 1 applies to entire table

Symbol	Description	Test Condition	Min	Max	Units
$C_{IN/OUT}$	Input/output capacitance (DQ0/DQ1/DQ2/DQ3)	V_{OUT} = 0V	–	8	pF
C_{IN}	Input capacitance (other pins)	V_{IN} = 0V	–	6	pF

Note:
1. These parameters are sampled only, not 100% tested. T_A = 25°C at 54 MHz.

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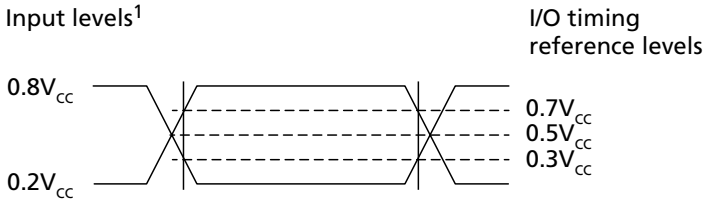
Table 39: AC Timing Input/Output Conditions

Symbol	Description	Min	Max	Units	Notes
C_L	Load capacitance	30	30	pF	1
–	Input rise and fall times	–	5	ns	
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V	2
	Input timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V	
	Output timing reference voltages	$V_{CC}/2$	$V_{CC}/2$	V	

Notes: 1. Output buffers are configurable by user.
2. For quad/dual operations: 0V to V_{CC}.

Figure 44: AC Timing Input/Output Reference Levels



Note: 1. $0.8V_{CC} = V_{CC}$ for dual/quad operations; $0.2V_{CC} = 0V$ for dual/quad operations.

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DC Characteristics and Operating Conditions

Table 40: DC Current Characteristics and Operating Conditions

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input leakage current	I_{LI}		–	±2	µA
Output leakage current	I_{LO}		–	±2	µA
Standby current	I_{CC1}	S = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	200	µA
Operating current (fast-read extended I/O)	I_{CC3}	C = 0.1V_{CC}/0.9V_{CC} at 108 MHz, DQ1 = open	–	15	mA
		C = 0.1V_{CC}/0.9V_{CC} at 54 MHz, DQ1 = open	–	6	mA
Operating current (fast-read dual I/O)		C = 0.1V_{CC}/0.9V_{CC} at 108 MHz	–	18	mA
Operating current (fast-read quad I/O)		C = 0.1V_{CC}/0.9V_{CC} at 108 MHz	–	20	mA
Operating current (program)	I_{CC4}	S# = V_{CC}	–	20	mA
Operating current (write status register)	I_{CC5}	S# = V_{CC}	–	20	mA
Operating current (erase)	I_{CC6}	S# = V_{CC}	–	20	mA

Table 41: DC Voltage Characteristics and Operating Conditions

Parameter	Symbol	Conditions	Min	Max	Unit
Input low voltage	V_{IL}		–0.5	0.3V_{CC}	V
Input high voltage	V_{IH}		0.7V_{CC}	V_{CC} + 0.4	V
Output low voltage	V_{OL}	I_{OL} = 1.6mA	–	0.4	V
Output high voltage	V_{OH}	I_{OH} = –100µA	V_{CC} - 0.2	–	V

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AC Characteristics and Operating Conditions

Table 42: AC Characteristics and Operating Conditions

Parameter		Symbol	Min	Typ[1]	Max	Unit	Notes
Clock frequency for all commands other than READ (SPI-ER, QIO-SPI protocol)		^{f}C	DC	–	108	MHz	
Clock frequency for READ commands		^{f}R	DC	–	54	MHz	
Clock HIGH time		^{t}CH	4	–	–	ns	2
Clock LOW time		^{t}CL	4	–	–	ns	1
Clock rise time (peak-to-peak)		$^{t}CLCH$	0.1	–	–	V/ns	3, 4
Clock fall time (peak-to-peak)		$^{t}CHCL$	0.1	–	–	V/ns	3, 4
S# active setup time (relative to clock)		$^{t}SLCH$	4	–	–	ns	
S# not active hold time (relative to clock)		$^{t}CHSL$	4	–	–	ns	
Data in setup time		$^{t}DVCH$	2	–	–	ns	
Data in hold time		$^{t}CHDX$	3	–	–	ns	
S# active hold time (relative to clock)		$^{t}CHSH$	4	–	–	ns	
S# not active setup time (relative to clock)		$^{t}SHCH$	4	–	–	ns	
S# deselect time after a READ command		$^{t}SHSL1$	20	–	–	ns	
S# deselect time after a nonREAD command		$^{t}SHSL2$	50	–	–	ns	
Output disable time		$^{t}SHQZ$	–	–	8	ns	3
Clock LOW to output valid under 30pF	STR	$^{t}CLQV$	–	–	8	ns	
	DTR		–	–	9	ns	
Clock LOW to output valid under 10pF	STR		–	–	6	ns	
	DTR		–	–	7	ns	
Output hold time (clock LOW)		$^{t}CLQX$	1	–	–	ns	
Output hold time (clock HIGH)		$^{t}CHQX$	1	–	–	ns	
HOLD command setup time (relative to clock)		$^{t}HLCH$	4	–	–	ns	
HOLD command hold time (relative to clock)		$^{t}CHHH$	4	–	–	ns	
HOLD command setup time (relative to clock)		$^{t}HHCH$	4	–	–	ns	
HOLD command hold time (relative to clock)		$^{t}CHHL$	4	–	–	ns	
HOLD command to output Low-Z		$^{t}HHQX$	–	–	8	ns	3
HOLD command to output High-Z		$^{t}HLQZ$	–	–	8	ns	3
Write protect setup time		$^{t}WHSL$	20	–	–	ns	5
Write protect hold time		$^{t}SHWL$	100	–	–	ns	5
Enhanced V_{PPH} HIGH to S# LOW for extended and dual I/O page program		$^{t}VPPHSL$	200	–	–	ns	6
WRITE STATUS REGISTER cycle time		^{t}W	–	1.3	8	ms	
Write NONVOLATILE CONFIGURATION REGISTER cycle time		$^{t}WNVCR$	–	0.2	3	s	
CLEAR FLAG STATUS REGISTER cycle time		$^{t}CFSR$	–	40	–	ns	

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Table 42: AC Characteristics and Operating Conditions (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Notes
WRITE VOLATILE CONFIGURATION REGISTER cycle time	tWVCR	–	40	–	ns	
WRITE VOLATILE ENHANCED CONFIGURATION REGISTER cycle time	tWRVECR	–	40	–	ns	
WRITE EXTENDED ADDRESS REGISTER cycle time	tWREAR	–	40	–	ns	
PAGE PROGRAM cycle time (256 bytes)	tPP	–	0.5	5	ms	7
PAGE PROGRAM cycle time (*n* bytes)		–	int(n/8) × 0.015[8]	5	ms	7
PAGE PROGRAM cycle time, $V_{PP} = V_{PPH}$ (256 bytes)		–	0.4	5	ms	7
PROGRAM OTP cycle time (64 bytes)		–	0.2	–	ms	7
Subsector ERASE cycle time	tSSE	–	0.25	0.8	s	
Sector ERASE cycle time	tSE	–	0.7	3	s	
Sector ERASE cycle time (with $V_{PP} = V_{PPH}$)		–	0.6	3	s	
DIE ERASE cycle time	tBE	–	240	480	s	
DIE ERASE cycle time (with $V_{PP} = V_{PPH}$)		–	200	480	s	

Notes:
1. Typical values given for T_A = 25 °C.
2. tCH + tCL must add up to 1/fC.
3. Value guaranteed by characterization; not 100% tested.
4. Expressed as a slew-rate.
5. Only applicable as a constraint for a WRITE STATUS REGISTER command when STATUS REGISTER WRITE is set to 1.
6. V_{PPH} should be kept at a valid level until the PROGRAM or ERASE operation has completed and its result (success or failure) is known.
7. When using the PAGE PROGRAM command to program consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes (1 < n < 256).
8. int(A) corresponds to the upper integer part of A. For example int(12/8) = 2, int(32/8) = 4 int(15.3) =16.

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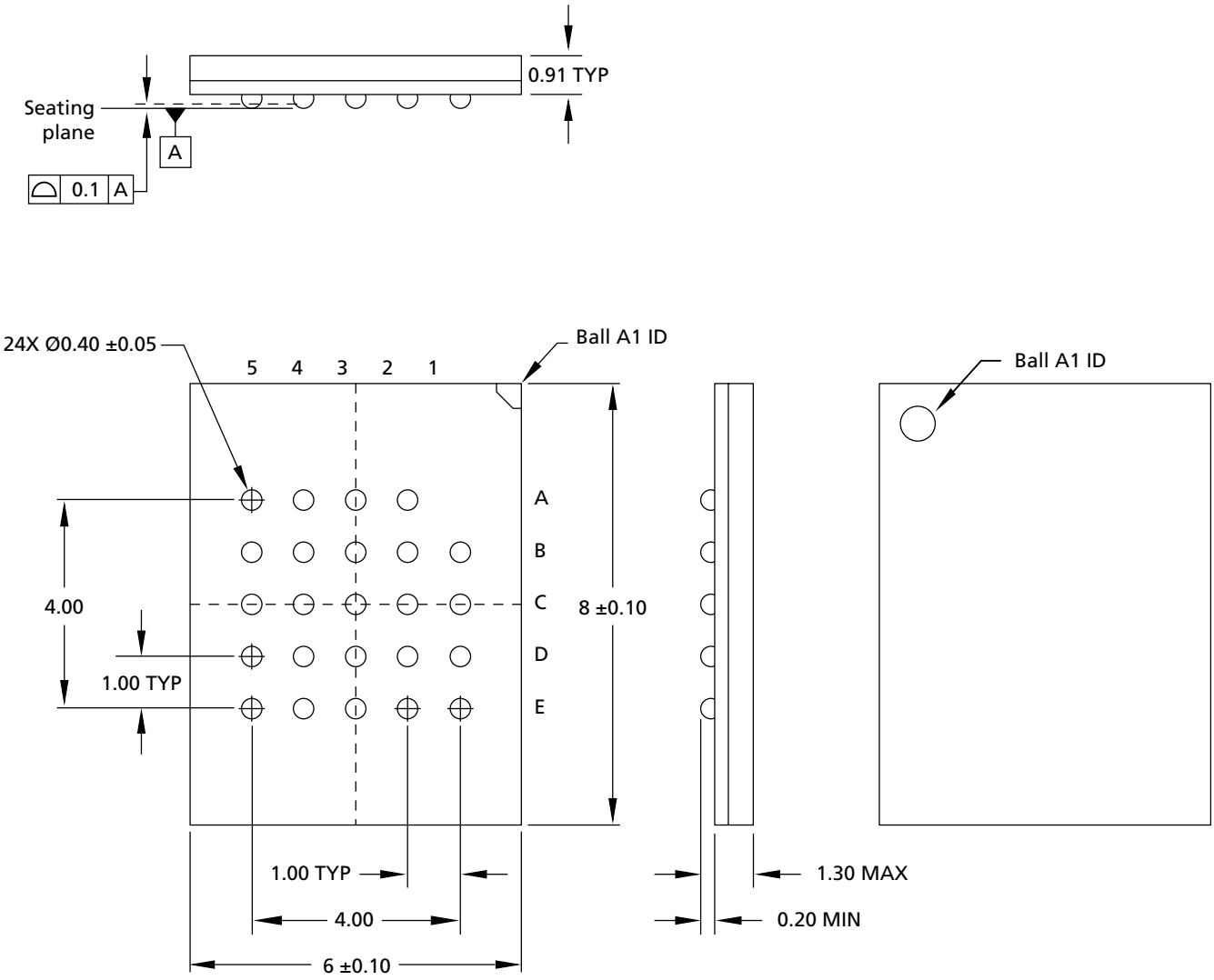
Package Dimensions

Figure 45: L-PBGA-24b05/6mm x 8mm



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

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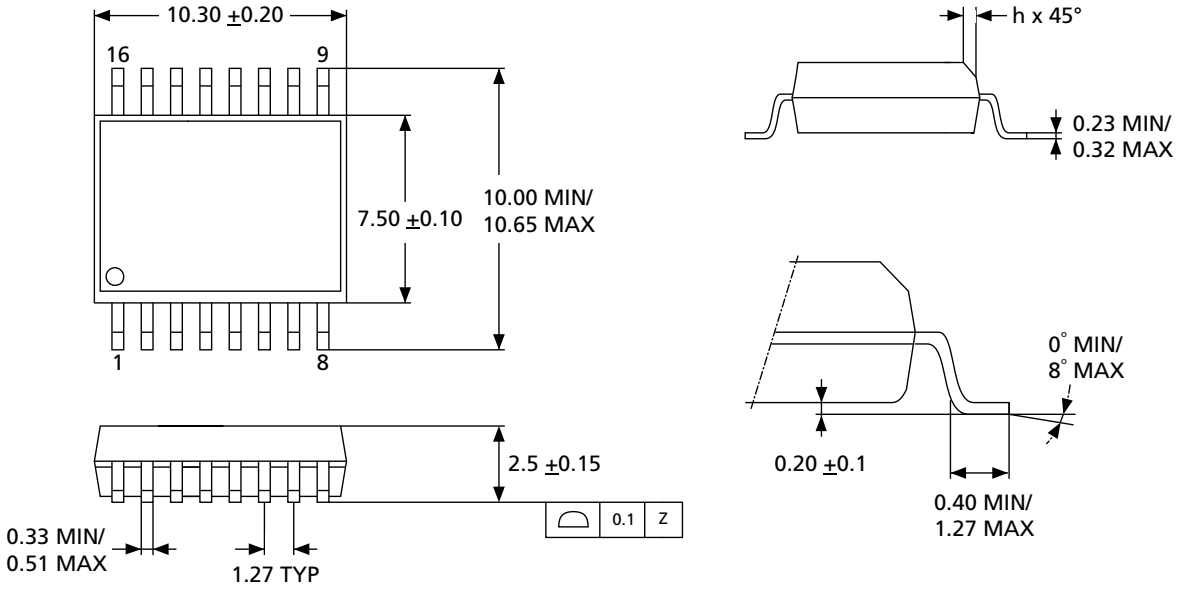
Figure 46: SOP2-16/300 mils



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

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Part Number Ordering Information

Micron Serial NOR Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at micron.com. To compare features and specifications by device type, visit micron.com/products. Contact the factory for devices not found.

For more information on how to identify products and top-side marking by the process identification letter, refer to technical note TN-12-24, "Serial Flash Memory Device Marking for the M25P, M25PE, M25PX, and N25Q Product Families."

Table 43: Part Number Information

Part Number Category	Category Details	Notes
Device type	N25Q = Serial NOR Flash memory, Multiple Input/Output (Single, Dual, Quad I/O), XIP	
Density	00A = 1Gb	
Technology	A = 65nm	
Feature set	1 = Byte addressability; HOLD pin; Micron XIP	1
	2 = Byte addressability; HOLD pin; Basic XIP	1
	3 = Byte addressability; RST# pin; Micron XIP	1
	4 = Byte addressability; RST# pin; Basic XIP	1
	7 = Byte addressability; HOLD pin; Micron XIP	2
Operating voltage	3 = V_{CC} = 2.7 to 3.6V	
Block structure	G = Uniform (64KB and 4KB) , easy transparent stack	
Package (RoHS-compliant)	12 = L-PBGA-24b05/6mm x 8mm SF = SOP2-16/300mils	3
Temperature and test flow	4 = IT: –40°C to 85°C; Device tested with standard test flow A = Automotive temperature range, –40 to 125°C; Device tested with high reliability certified test flow H = IT: –40°C to 85°C; Device tested with high reliability certified test flow	
Security features	0 = Default	4
Shipping material	E = Tray F = Tape and reel G = Tube	

Notes:
1. Enter 4-byte address mode and exit 4-byte address mode supported.
2. 4-byte addressing mode is the default at power-up. Enter and exit 4-byte addressing mode are not supported.
3. See the table below for additional information.
4. Additional secure options are available upon customer request.

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Table 44: Package Details

Micron SPI and JEDEC Package Name	Shortened Package Name	Package Description	M25P M45PE Symbol	N25Q Symbol	M25P M45PE Package Names	Alternate Package Name
L-PBGA-24b05/ 6mm x 8mm	LBGA 24	Thin, plastic-ball grid array, 24-ball, 6mm x 8mm	–	12	LBGA24 6 x 8mm	L-PBGA-24b05/6x8
SOP2-16/300 mil	SO16W	Small-outline integrated circuit, 16-pin, wide (300 mil)	MF	SF	SO16W, SO16 wide 300 mil body width	SOIC-16/300 mil, SOP 16L 300 mil

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Revision History

Rev. N – 02/18

- Added Important Notes and Warnings section for further clarification aligning to industry standards

Rev. M – 03/14

- In Command Set table, updated value for Quad I/O FAST READ – DTR from 3Dh to 6Dh

Rev. L – 01/14

- Corrected RESET ENABLE and RESET MEMORY command timing diagram

Rev. K – 09/13

- Replaced TBGA package information with LPBGA package information

Rev. J – 07/13

- Removed part numbers from ENTER or EXIT 4-BYTE ADDRESS MODE Command
- Removed ENTER or EXIT QUAD Command
- Revised Extended Address Register Bit Definitions table

Rev. I – 02/13

- Updated the READ ID Operation figure in READ ID Operations
- Updated ERASE Operations
- Added link to part number chart in Part Number Ordering Information
- Updated part numbers in Features

Rev. H – 11/12

- Typo fix in Command Set table in Command Definitions – Dual I/O FAST READ - DTR from DBh to BDh

Rev. G – 11/12

- Updated Upper and Lower Memory Array Segments figure in Nonvolatile and Volatile Registers

Rev. F – 06/12

- Added SOP2-16/300 mils package information
- Updated part number in Features
- Typo fix in Supported Clock Frequencies - DTR table in Nonvolatile and Volatile Registers
- Updated ^{t}SSE specification in AC Reset Conditions table

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Rev. E – 02/12

- To Production status

Rev. D – 01/12

- Updated AC Reset Specifications to include power-down values

Rev. C – 11/11

- Updated Supported Clock Frequencies – STR in Nonvolatile and Volatile Registers

Rev. B – 11/11

- Corrected address description from [A24:A25] to A[26:24] in Upper and Lower Memory Array Segments figure; corrected bit 1:0, A24 in Description corrected to A[26:24] of Extended Address Register Bit Definitions table in Nonvolatile and Volatile Registers

Rev. A – 08/11

- Initial release

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