

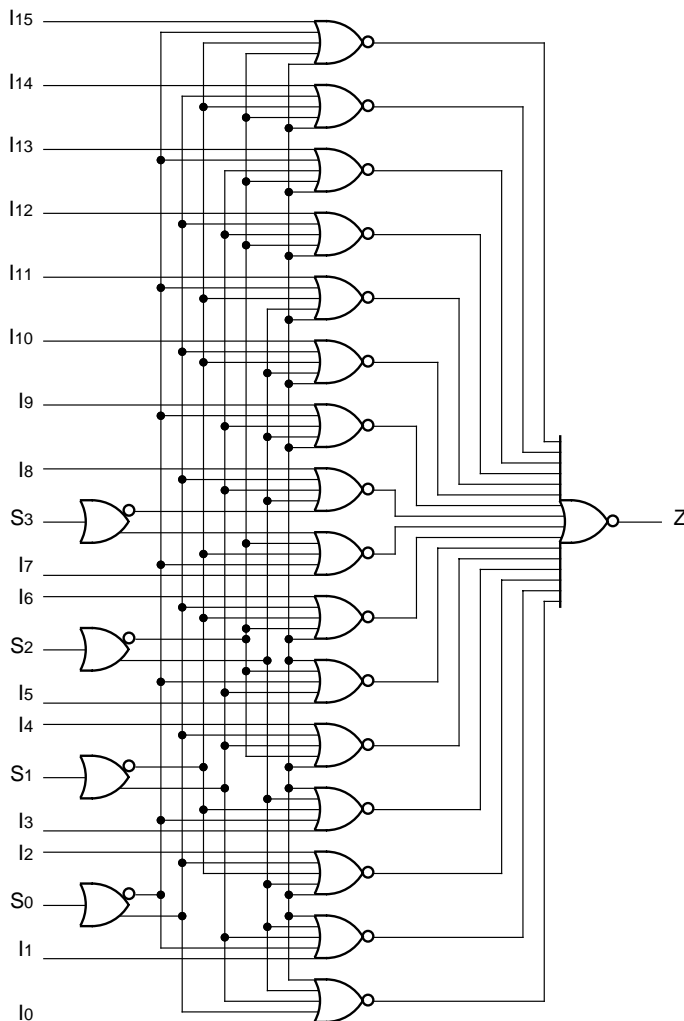
### FEATURES

- Max. propagation delay of 1300ps
- IEE min. of -63mA
- Industry standard 100K ECL levels
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 70% faster than Fairchild
- 40% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

### DESCRIPTION

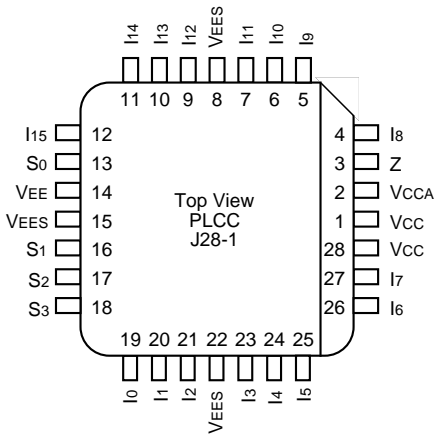
The SY100S364 is a 16-input multiplexer designed for use in high-performance ECL systems. The four Data Select inputs (S<sub>0</sub>, S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub>) determine the bit from the 16 inputs (I<sub>n</sub>) that will be passed on to the output as shown in the Truth Table. The output data polarity is the same as the input. The inputs on the device have 75KΩ pull-down resistors.

### BLOCK DIAGRAM

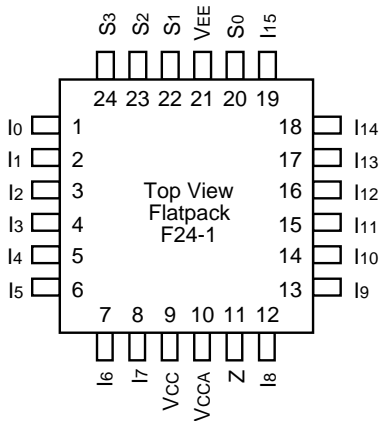


**PACKAGE/ORDERING INFORMATION**

**Ordering Information**



**28-Pin PLCC (J28-1)**



**24-Pin Cerpack (F24-1)**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S364FC	F24-1	Commercial	SY100S364FC	Sn-Pb
SY100S364FCTR <sup>(1)</sup>	F24-1	Commercial	SY100S364FC	Sn-Pb
SY100S364JC	J28-1	Commercial	SY100S364JC	Sn-Pb
SY100S364JCTR <sup>(1)</sup>	J28-1	Commercial	SY100S364JC	Sn-Pb
SY100S364JZ <sup>(2)</sup>	J28-1	Commercial	SY100S364JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S364JZTR <sup>(1, 2)</sup>	J28-1	Commercial	SY100S364JZ with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

**PIN NAMES**

Pin	Function
I0 – I15	Data Inputs
S0 – S3	Select Inputs
Z	Data Output
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

**TRUTH TABLE<sup>(1)</sup>**

Select Inputs				Output
S0	S1	S2	S3	Z
L	L	L	L	I0
H	L	L	L	I1
L	H	L	L	I2
H	H	L	L	I3
L	L	H	L	I4
H	L	H	L	I5
L	H	H	L	I6
H	H	H	L	I7
L	L	L	H	I8
H	L	L	H	I9
L	H	L	H	I10
H	H	L	H	I11
L	L	H	H	I12
H	L	H	H	I13
L	H	H	H	I14
H	H	H	H	I15

**NOTE:**  
 1. H = HIGH Voltage Level  
 L = LOW Voltage Level

**DC ELECTRICAL CHARACTERISTICS**

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I <sub>IH</sub>	Input HIGH Current I <sub>n</sub> S0, S1 S2, S3	—	—	200	μA	V <sub>IN</sub> = V <sub>IH</sub> (Max.)
I <sub>EE</sub>	Power Supply Current	-63	-45	-30	mA	Inputs Open

**AC ELECTRICAL CHARACTERISTICS**

**CERPACK**

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I0 – I15 to Output	400	1400	400	1400	400	1400	ps	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S0, S1 to Output	400	1900	400	1900	400	1900	ps	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S2, S3 to Output	400	1700	400	1700	400	1700	ps	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

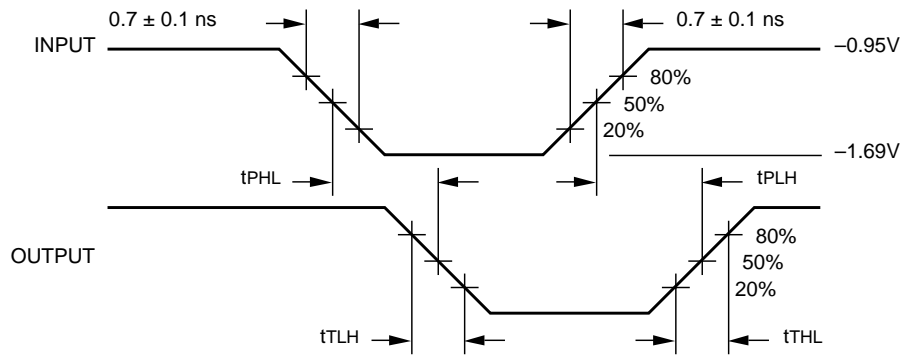
**AC ELECTRICAL CHARACTERISTICS**

**PLCC**

V<sub>EE</sub> = -4.2V to -5.5V unless otherwise specified; V<sub>CC</sub> = V<sub>CCA</sub> = GND

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I <sub>0</sub> – I <sub>15</sub> to Output	400	1300	400	1300	400	1300	ps	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>0</sub> , S <sub>1</sub> to Output	400	1800	400	1800	400	1800	ps	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>2</sub> , S <sub>3</sub> to Output	400	1600	400	1600	400	1600	ps	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

**TIMING DIAGRAM**

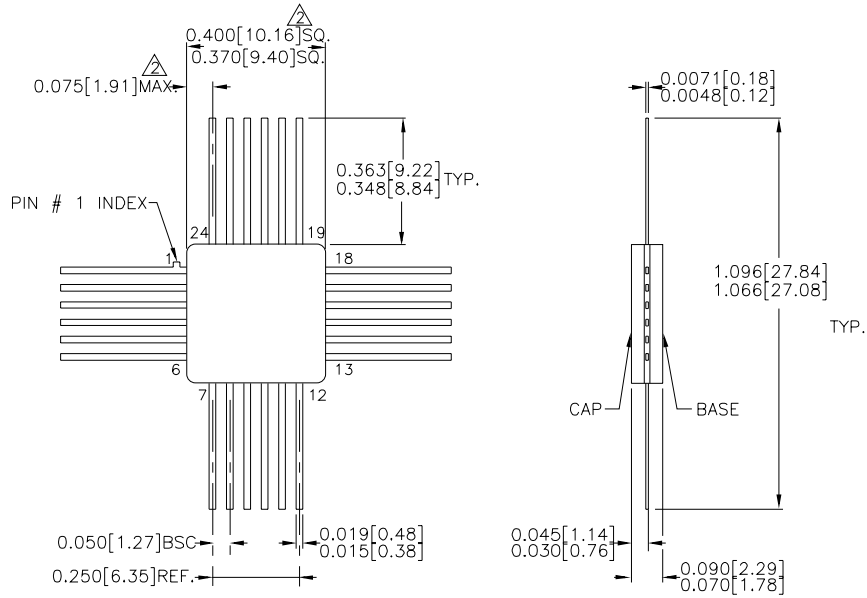


**Propagation Delay and Transition Times**

**Note:**

V<sub>EE</sub> = -4.2V to -5.5V unless otherwise specified; V<sub>CC</sub> = V<sub>CCA</sub> = GND

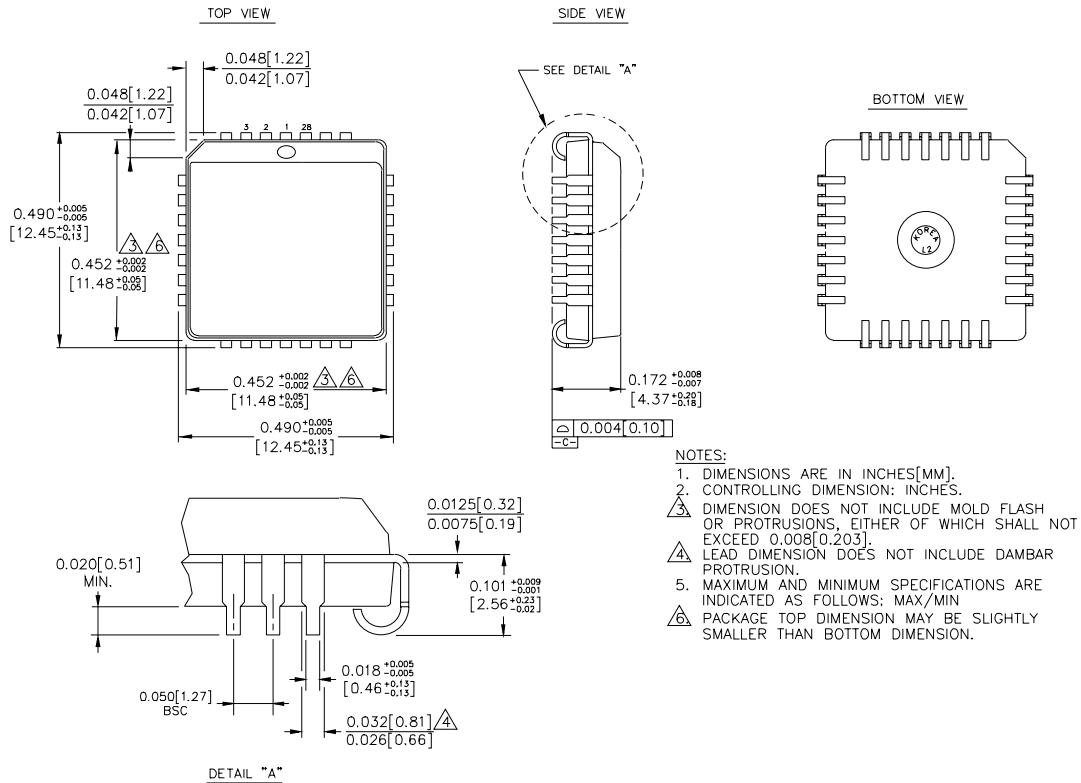
**24-PIN CERPACK (F24-1)**



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
  2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
  3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

**28-PIN PLCC (J28-1)**



Rev. 03

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