THE DATASHEET OF

MX7537JCWG+

19-2249; Rev 1; 7/95

MAXIM

CMOS Parallel Loading Dual 12-Bit Multiplying D/A Converters

General Description

The Maxim MX7537/MX7547 contain two 12-bit current-output multiplying digital-to-analog converters (DAC) in a single package. Input level shifters, data registers and control logic make microprocessor interfacing straightforward. Operation is from a single +12V to +15V power supply maintaining TTL, 74HC and 5V CMOS logic compatibility.

The MX7547 accepts $\overline{CSA}$, $\overline{CSB}$, $\overline{WR}$ control signals and 12 data inputs for DAC selection and full parallel data loading. The MX7537 receives data in 2 bytes, using a right justified 8+4 format. A0, A1, $\overline{CS}$, $\overline{WR}$ and $\overline{UPD}$ signals provide full control for DAC selection and data loading.

Each of the DACs in the MX7537/MX7547 provides 4-quadrant multiplication capabilities and separate reference input and feedback resistor pins. The MX7537 additionally makes available separate AGND pins for applications where each DAC is biased at a different voltage. Since both DACs are on a single monolithic chip, matching and temperature tracking between them is excellent. Gain error is specified at less than ±1 LSB, and 12-bit linearity and monotonicity are guaranteed over the full operating temperature ranges.

Maxim's MX7537 and MX7547 are available in narrow 24-lead 0.3" DIP and Wide SO, as well as, 28-pin-lead PLCC packages.

Applications

Automatic Test Equipment

Audio Gain Control

Motion Control Systems

Synchro Applications

Process Control

Digitally Controlled Filters

Features

- ◆ Two 12-Bit DACs in One Package
- ◆ 0.5% DAC-to-DAC Matching
- ◆ Narrow 0.3" DIP, Wide SO, and PLCC Packages
- ◆ 4-Quadrant Multiplication
- ◆ Low INL and DNL (±1/2 LSB max)
- ◆ Gain Accuracy to ±1 LSB max
- ◆ Low Gain Tempco (±5ppm/°C max)
- ◆ Operates with Single +12V to +15V Supply
- ◆ Fast Microprocessor Interface

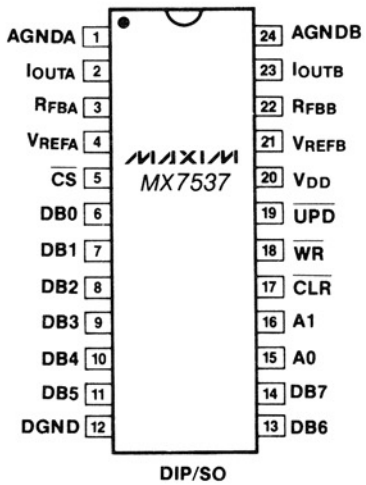
Ordering Information

PART	TEMP. RANGE	PACKAGE	GAIN ERROR
MX7537JN	0°C to +70°C	24 Plastic DIP	±6 LSB
MX7537KN	0°C to +70°C	24 Plastic DIP	±3 LSB
MX7537LN	0°C to +70°C	24 Plastic DIP	±1 LSB
MX7537JCWG	0°C to +70°C	24 Wide SO	±6 LSB
MX7537KCWG	0°C to +70°C	24 Wide SO	±3 LSB
MX7537LCWG	0°C to +70°C	24 Wide SO	±1 LSB
MX7537JP	0°C to +70°C	28 PLCC	±6 LSB
MX7537KP	0°C to +70°C	28 PLCC	±3 LSB
MX7537LP	0°C to +70°C	28 PLCC	±1 LSB
MX7537J/D	0°C to +70°C	Dice	±6 LSB
MX7537AQ	-25°C to +85°C	24 CERDIP	±6 LSB
MX7537BQ	-25°C to +85°C	24 CERDIP	±3 LSB
MX7537CQ	-25°C to +85°C	24 CERDIP	±1 LSB

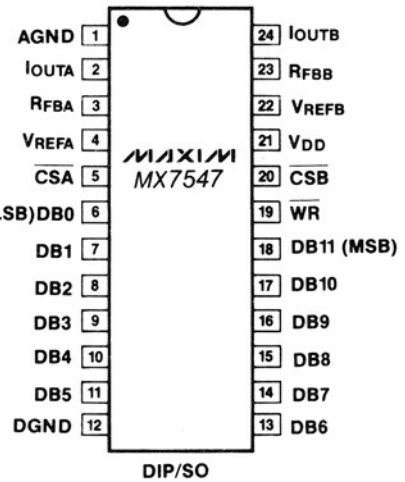
(Ordering Information continued on page 15.)

Pin Configurations

Top View



DIP/SO



DIP/SO

See page 5 for Plastic Chip Carrier Configurations.

CMOS Parallel Loading Dual 12-Bit Multiplying D/A Converters

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V, +17V
V_{REFA}, V_{REFB} to AGND ..... ±25V
V_{RFBA}, V_{RFBB} to AGND ..... ±25V
Digital Input Voltage to DGND ..... -0.3V, V_{DD}+0.3V
I_{OUTA}, I_{OUTB} Voltage to DGND ..... -0.3V, V_{DD}+0.3V
AGND to DGND ..... -0.3V, V_{DD}+0.3V
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C ..... 6mW/°C

Operating Temperature Range
MX7537J/K/L, MX7547J/K/L ..... 0°C to +70°C
MX7537A/B/C, MX7547A/B/C ..... -25°C to +85°C
MX7537JE/KE/LE, MX7547JE/KE/LE .... -40°C to +85°C
MX7537S/T/Q, MX7547S/T/Q ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +12V to +15V, ±10%, V_{REFA} = V_{REFB} = +10V, V_{AGND} = V_{DGND} = V_{IOUTA} = V_{IOUTB} = 0V, output amplifiers are MAX400s, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE								
Resolution	N				12			Bits
Relative Accuracy	INL			MX75X7J/A/Q MX75X7K/L/B/C/T/U			±1 ±½	LSB
Differential Nonlinearity	DNL	All grades guaranteed monotonic over temperature.					±1	LSB
Gain Error	FSE	Measured using R_{FBA}, R_{FBB}. Both DAC registers loaded with all 1s.		MX75X7L/C MX75X7U MX75X7K/B/T MX75X7J/A/S			±1 ±2 ±3 ±6	LSB
Gain Tempco ΔGain/ΔTemperature (Note 1)	TCFS					±1	±5	ppm/°C
I_{OUTA}, I_{OUTB} Leakage Current	ILKG	DAC register loaded with all 0s.	All	T_A = +25°C			±10	nA
			MX75X7J/K/L/A/B/C MX75X7S/T/U	T_A = T_{MIN} to T_{MAX} T_A = T_{MIN} to T_{MAX}			±150 ±250	
REFERENCE INPUT								
V_{REFA}, V_{REFB} Input Resistance	R_{REF}				9	14	20	kΩ
V_{REFA}, V_{REFB} Input Resistance Match	ΔR_{REF}			MX75X7L/C/U MX75X7J/K/A/B/S/T		±0.5 ±0.5	±1 ±3	% %
DIGITAL INPUTS								
Input High Voltage	V_{IH}				2.4			V
Input Low Voltage	V_{IL}						0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}		T_A = +25°C T_A = T_{MIN} to T_{MAX}			±1 ±10	μA
Input Capacitance (Note 1)	C_{IN}						10	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +12V to +15V, ±10%, V_{REFA} = V_{REFB} = +10V, V_{AGND} = V_{DGND} = V_{IOUTA} = V_{IOUTB} = 0V, output amplifiers are MAX400s, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
POWER SUPPLY								
Supply Voltage	V_{DD}	Operating Range.			10.8		16.5	V
		Functional with degraded specifications.				5.0		
Supply Current	I_{DD}						2	mA
DYNAMIC PERFORMANCE (Note 2)								
Current Settling Time	t_S	To ±½ LSB. I_{OUT} load is 100Ω ‖ 13pF. DAC output measured from rising edge of $\overline{WR}$.		T_A = +25°C		0.8	1.5	µs
Digital-to-Analog Glitch Impulse		Measured with V_{REFA} = V_{REFB} = 0V. I_{OUT} load is 100Ω ‖ 13pF. DAC registers alternately loaded with all 1s and all 0s.				7		nV-s
AC Feedthrough	FTE	DAC registers loaded with all 0s.	V_{REFA} = 20Vp-p 10kHz sine wave, V_{REFB} = 0V	V_{REFA} to I_{OUTA}			-70	dB
			V_{REFB}=20Vp-p 10kHz sine wave, V_{REFA} = 0V	V_{REFB} to I_{OUTB}			-70	
Power Supply Rejection $\Delta Gain/\Delta V_{DD}$	PSR	ΔV_{DD} = V_{DD} max - V_{DD} min.					±0.001	%/%
Output Capacitance (I_{OUTA}, I_{OUTB})	C_{OUT}	DAC A, DAC B loaded with all 0s. DAC A, DAC B loaded with all 1s.					70 140	pF
Channel-to-Channel Isolation		V_{REFA} = 20Vp-p 10kHz sine wave, V_{REFB} = 0V		V_{REFA} to I_{OUTB}		-84		dB
		V_{REFB} = 20Vp-p 10kHz sine wave, V_{REFA} = 0V		V_{REFB} to I_{OUTA}		-84		
Digital Crosstalk		Measured for digital inputs changed from all 0s to all 1s. I_{OUTA}, I_{OUTB} load is 100Ω ‖ 13pF.				7		nV-s
Total Harmonic Distortion		V_{IN} = 6V_{RMS}, 1kHz. Both DACs loaded with all 1s.				-82		dB
Output Noise Voltage Density (10Hz to 100kHz)		Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}.				25		nV//Hz

Note 1: Guaranteed by design.
Note 2: These characteristics are for design guidance only and are not subject to test.

CMOS Parallel Loading Dual 12-Bit Multiplying D/A Converters

TIMING CHARACTERISTICS—AD7537

(V_{DD} = +10.8V to +16.5V. See Figure 2 for timing diagram.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Address Valid to Write Setup Time	t_1	All	T_A = +25°C	20			ns
		MX7537J/K/L/A/B/C	$T_A = T_{MIN}$ to T_{MAX}	20			
		MX7537S/T/U	$T_A = T_{MIN}$ to T_{MAX}	30			
Address Valid to Write Hold Time	t_2	All	T_A = +25°C	20			ns
		MX7537J/K/L/A/B/C	$T_A = T_{MIN}$ to T_{MAX}	20			
		MX7537S/T/U	$T_A = T_{MIN}$ to T_{MAX}	25			
Data Setup Time	t_3	All	T_A = +25°C	60			ns
			$T_A = T_{MIN}$ to T_{MAX}	80			
Data Hold Time	t_4			25			ns
Chip Select or Update to Write Setup Time	t_5			0			ns
Chip Select or Update to Write Hold Time	t_6			0			ns
Write Pulse Width	t_7	All	T_A = +25°C	80			ns
		MX7537J/K/L/A/B/C	$T_A = T_{MIN}$ to T_{MAX}	80			
		MX7537S/T/U	$T_A = T_{MIN}$ to T_{MAX}	100			
Clear Pulse Width	t_8	All	T_A = +25°C	80			ns
		MX7537J/K/L/A/B/C	$T_A = T_{MIN}$ to T_{MAX}	80			
		MX7537S/T/U	$T_A = T_{MIN}$ to T_{MAX}	100			

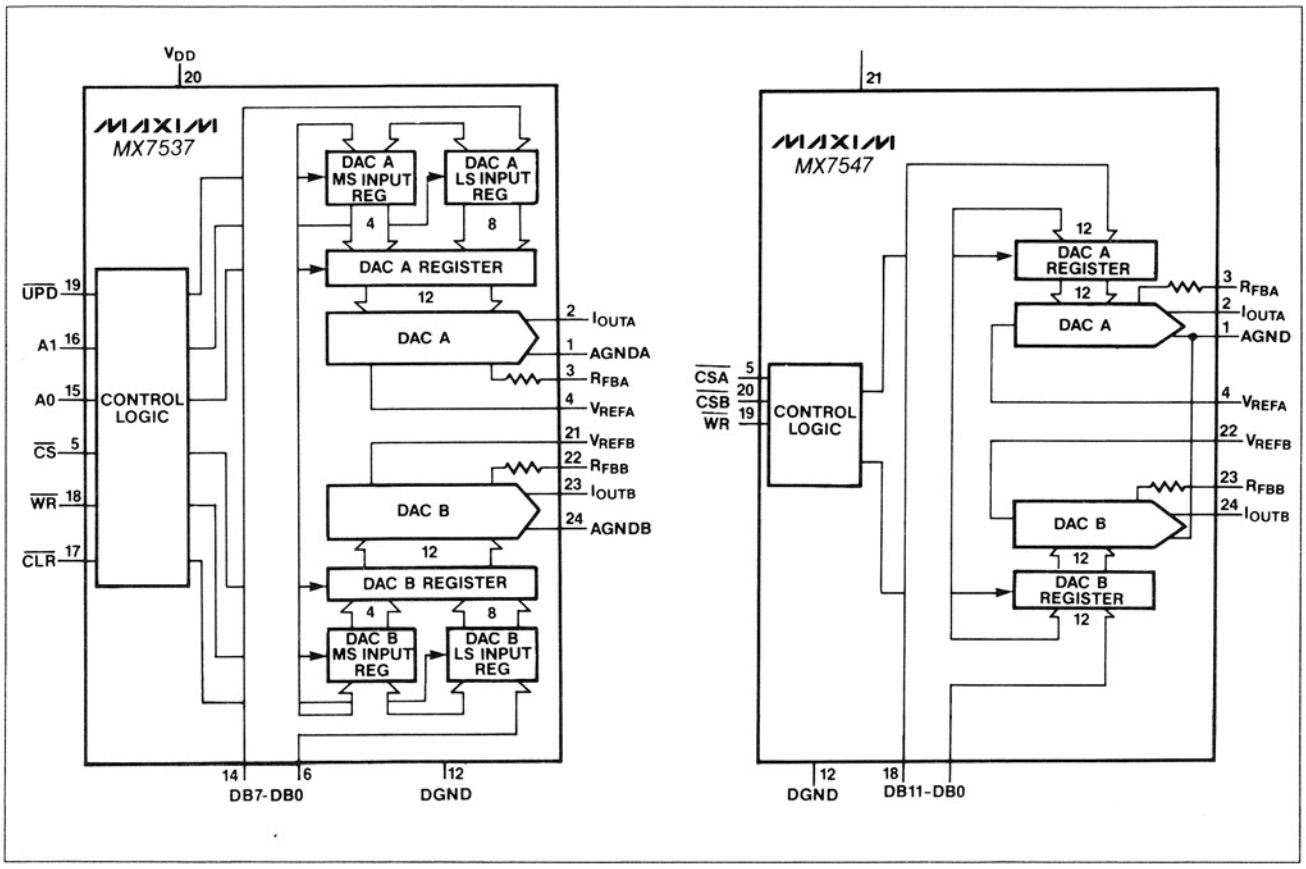
TIMING CHARACTERISTICS—AD7547

(V_{DD} = +10.8V to +16.5V. See Figure 3 for timing diagram.)

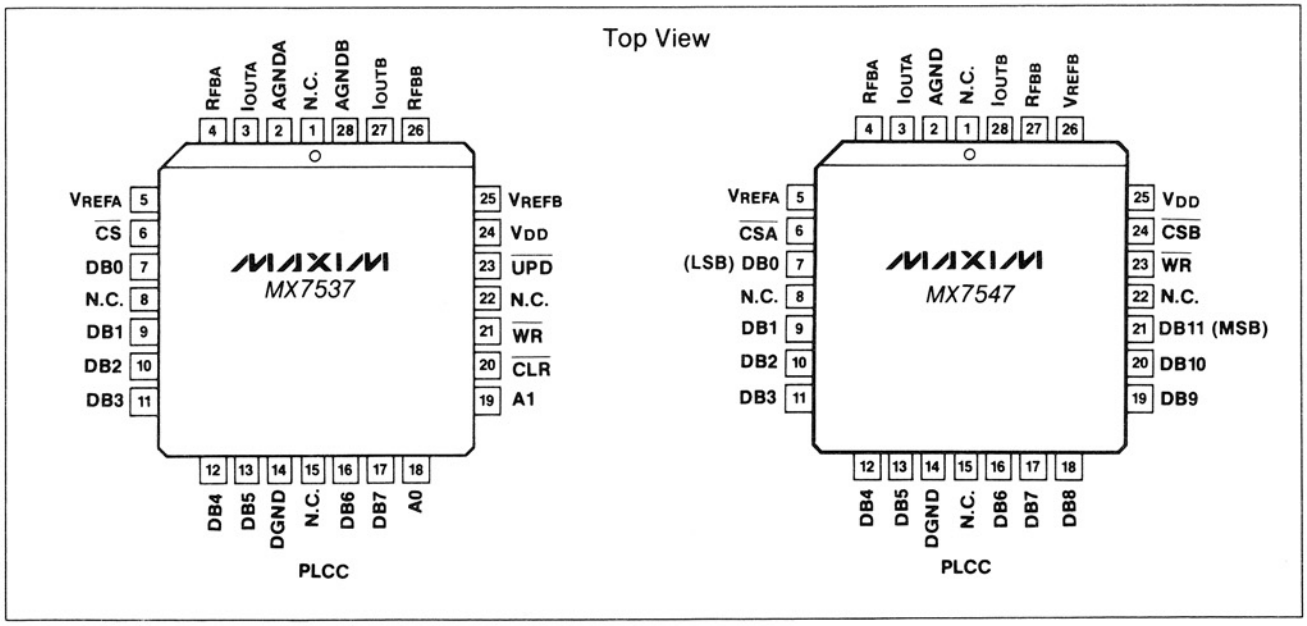
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Data Setup Time	t_1	All	T_A= +25°C	60			ns
		MX7547J/K/L/A/B/C	$T_A = T_{MIN}$ to T_{MAX}	60			
		MX7547S/T/U	$T_A = T_{MIN}$ to T_{MAX}	80			
Data Hold Time	t_2			25			ns
Chip Select to Write Setup Time	t_3	All	T_A = +25°C	80			ns
		MX7547J/K/L/A/B/C	$T_A = T_{MIN}$ to T_{MAX}	80			
		MX7547S/T/U	$T_A = T_{MIN}$ to T_{MAX}	100			
Chip Select to Write Hold Time	t_4			0			ns
Write Pulse Width	t_5	All	T_A = +25°C	80			ns
		MX7547J/K/L/A/B/C	$T_A = T_{MIN}$ to T_{MAX}	80			
		MX7547S/T/U	$T_A = T_{MIN}$ to T_{MAX}	100			

CMOS Parallel Loading Dual 12-Bit Multiplying D/A Converters

Functional Diagrams



Pin Configurations (continued)



CMOS Parallel Loading Dual 12-Bit Multiplying D/A Converters

Pin Descriptions

MX7537		
PIN	**NAME**	**FUNCTION**
1	AGNDA	Analog ground for DAC A
2	I_{OUTA}	Current output for DAC A
3	R_{FBA}	Feedback resistor for DAC A
4	V_{REFA}	Reference input for DAC A
5	$\overline{CS}$	Chip select input. Active low.
6-14	DB0-DB7	Data inputs
12	DGND	Digital ground
15	A0	Address input
16	A1	Address input
17	$\overline{CLR}$	Clear input. Active low. Clears all registers.
18	$\overline{WR}$	Write input. Active low.
19	$\overline{UPD}$	Update input. Active low. Updates DAC registers from input registers.
20	V_{DD}	Power supply input. +12V to +15V with ±10% tolerance.
21	V_{REFB}	Reference input for DAC B
22	R_{FBB}	Feedback resistor for DAC B
23	I_{OUTB}	Current output for DAC B
24	AGNDB	Analog ground for DAC B

MX7547		
PIN	**NAME**	**FUNCTION**
1	AGND	Analog ground
2	I_{OUTA}	Current output for DAC A
3	R_{FBA}	Feedback resistor for DAC A
4	V_{REFA}	Reference input for DAC A
5	$\overline{CSA}$	Chip select input for DAC A. Active low.
6-18	DB0-DB11	Data inputs. DB0(LSB) to DB11(MSB).
12	DGND	Digital ground
19	$\overline{WR}$	Write input. Active low.
20	$\overline{CSB}$	Chip select input for DAC B. Active low.
21	V_{DD}	Power supply input. +12V to +15V with ±10% tolerance.
22	V_{REFB}	Reference input for DAC B
23	R_{FBB}	Feedback resistor for DAC B
24	I_{OUTB}	Current output for DAC B

Table 1. MX7537 Truth Table

$\overline{CLR}$	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A1	A0	FUNCTION
1	1	1	X	X	X	No Data Transfer
1	1	X	1	X	X	No Data Transfer
0	X	X	X	X	X	All Registers Cleared
1	1	0	0	0	0	DAC A LS Input Register Loaded with DB7-DB0.
1	1	0	0	0	1	DAC A MS Input Register Loaded with DB3-DB0.
1	1	0	0	1	0	DAC B LS Input Register Loaded with DB7-DB0.
1	1	0	0	1	1	DAC B MS Input Register Loaded with DB3-DB0.
1	0	1	0	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers. Input Registers Not Changed.
1	0	0	0	X	X	DAC A, DAC B Registers are Transparent. Input Registers Loaded as Shown Above.

Note: X = Don't Care

Table 2. MX7547 Truth Table

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
⎍	⎍	0	A Rising Edge on $\overline{CSA}$ or $\overline{CSB}$ Transfers Data to the Respective DAC.
0	1	⎍	DAC A Register Loaded from Data Bus.
1	0	⎍	DAC B Register Loaded from Data Bus.
0	0	⎍	DAC A and DAC B Registers Loaded from Data Bus.

Notes:
1. X = Don't care.
2. $\overline{WR}$ Input is edge-triggered.

CMOS Parallel Loading Dual 12-Bit Multiplying D/A Converters

Detailed Description

D/A Converter

The basic MX7537/MX7547 circuit includes two identical DACs with laser trimmed, thin-film resistor (R-2R) arrays and NMOS current switches, as shown in Figure 1. Binary weighted currents switch to either I_{OUT} or GND depending on the status of each input data bit. Although the currents at I_{OUT} and GND depend on the digital input code, the sum of the two output currents are always equal to the input current at V_{REF}.

Either current output can be converted to a voltage by adding an external output amplifier (Figures 4, 5). The V_{REF} input accepts a wide range of signals, including fixed and time varying voltage or current inputs. If a current source is used for the reference input, a low tempco external resistor should be used for R_{FB} to minimize gain variation with temperature.

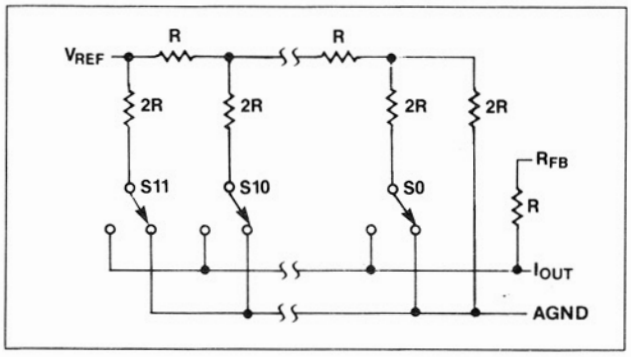


Figure 1. Simplified Circuit Diagram for DAC

The internal feedback resistor, R_{FB}, is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This results in excellent supply rejection and gain temperature coefficient.

The I_{OUT} pin output capacitance, C_{OUT}, is code dependent and is typically 40pF with all switches connected to GND and 100pF with all switches to I_{OUT}.

Digital Circuit

The input buffer inverters of the MX7537/MX7547 act as level shifters converting TTL levels into CMOS logic levels. Logic inputs are TTL, 74HC, and +5V CMOS compatible (0.8V and 2.4V) at V_{DD} = +12V to +15V. DAC supply current can be reduced below specified levels by keeping digital input voltages as close to the logic supply and ground as possible (as with CMOS logic levels). All logic inputs are designed to withstand ESD voltages of over 5,000V.

MX7537 Interface

Figure 2 shows the timing diagram for the MX7537. A1 and A0 select the most-significant (MS) or the least-significant (LS) input registers for DAC A or DAC B (Table 1). When loading the MS register, DB3 is the MSB of the 12-bit data input. Similarly, when the LS register is loaded, DB0 is the LSB. Data is loaded into the DAC when $\overline{CS}$ and $\overline{WR}$ both go low. $\overline{CLR}$ and $\overline{UPD}$ must be kept high while the data is loaded. When $\overline{CLR}$ is low, all registers are cleared without regard to the state of other control signals. When $\overline{UPD}$ and $\overline{WR}$ are low, the DAC registers are updated simultaneously from the input registers. When $\overline{UPD}$, $\overline{CS}$ and $\overline{WR}$ are low, the DAC registers are transparent and load the

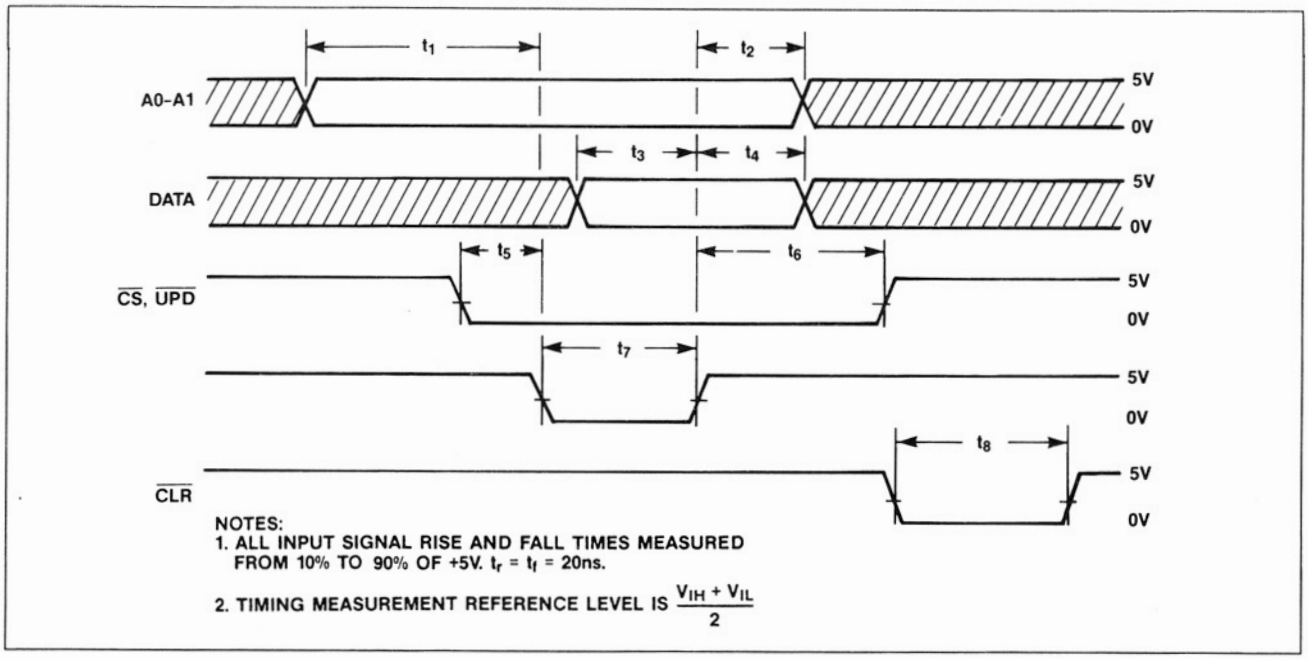


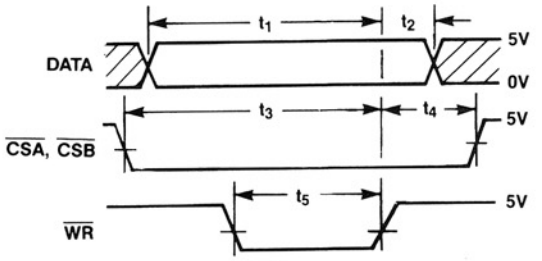
Figure 2. Timing Diagram for MX7537

CMOS Parallel Loading Dual 12-Bit Multiplying D/A Converters

data inputs immediately, as selected by the address inputs. Figure 17 shows the control logic equivalent circuit for the MX7537.

MX7547 Interface

Figure 3 shows the timing diagram for the MX7547. Data is loaded into the DAC A register on the rising edge of $\overline{WR}$ while $\overline{CSA}$ is low. Similarly, DAC B register is loaded on the rising edge of $\overline{WR}$ while $\overline{CSB}$ is low (Table 2).



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 3. Timing Diagram for MX7547

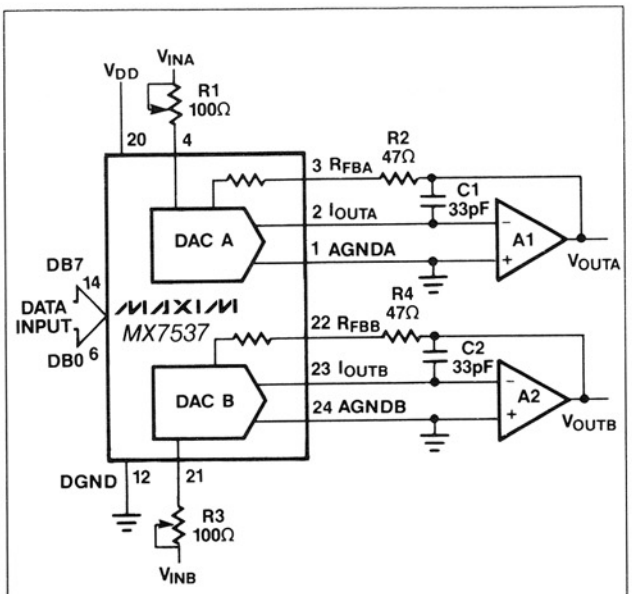
Circuit Configurations

Unipolar Operation

Basic applications of the MX7537/MX7547 are shown in Figure 4. These circuits are used for unipolar operation or 2-quadrant multiplication. The code table for this mode is given in Table 3. Note that the polarity of the output is the inverse of the reference voltage, V_{IN}.

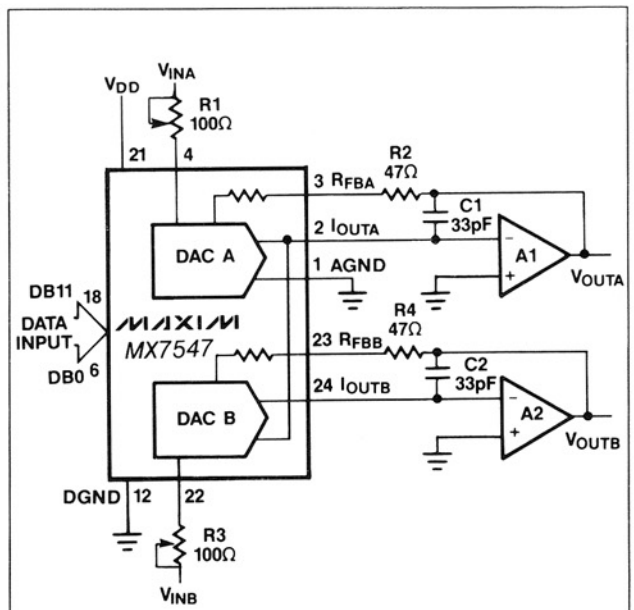
Table 3. Binary Code for Unipolar Circuit

BINARY NUMBER MSB LSB	V_{OUTA} or V_{OUTB}
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V



NOTES:
1. CONTROL CIRCUITRY OMITTED FOR CLARITY
2. A1, A2 ARE MAX400, TLC272 OR AD644

Figure 4A. MX7537 Unipolar Binary Operation



NOTES:
1. CONTROL CIRCUITRY OMITTED FOR CLARITY
2. A1, A2 ARE MAX400, TLC272 OR AD644

Figure 4B. MX7547 Unipolar Binary Operation

To adjust the circuits of Figure 4, correct the zero error, if necessary, by loading the appropriate DAC with all 0's code and adjusting the amplifier offset so that V_{OUT} = 0V. Next, correct the full scale error by loading the DAC with all 1s and adjust resistors R1 (or R3) so that $V_{OUT} = -V_{IN}(4095/4096)$.

In many applications, gain adjustment is not necessary if the untrimmed gain accuracy of the DAC is sufficient, or if the gain is trimmed at the voltage reference source. In these cases, resistors R1, R2, R3 and R4 can be omitted. When trimming is used and the DAC is operated over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used for these resistors.

The capacitors C1 and C2 provide phase compensation and reduce overshoot and ringing when fast amplifiers are used at the output of the DAC. Single or dual op amps can be used in this application.

Bipolar Operation

Figure 5 shows the MX7537/MX7547 operating in the bipolar, or 4-quadrant multiplying mode. These circuits require an additional amplifier and three matched resistors (R3, R4 and R5) for each DAC. The resistors must be of the same material (preferably metal film or wire-wound) for best temperature tracking characteristics (<15ppm/°C), and should match to 0.01% for 12-bit performance. Output code is offset binary and is listed in Table 4. In multiplying applications, the MSB determines output polarity while the lower eleven bits control amplitude. The MSB can be inverted in software using an exclusive-OR instruction to make the MX7537/MX7547 work with 2's complement coding. Table 5 shows the code relationships to output voltage for 2's complement operation.

Table 4. Offset Binary Code for Bipolar Circuit

BINARY NUMBER MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right) = -V_{IN}$

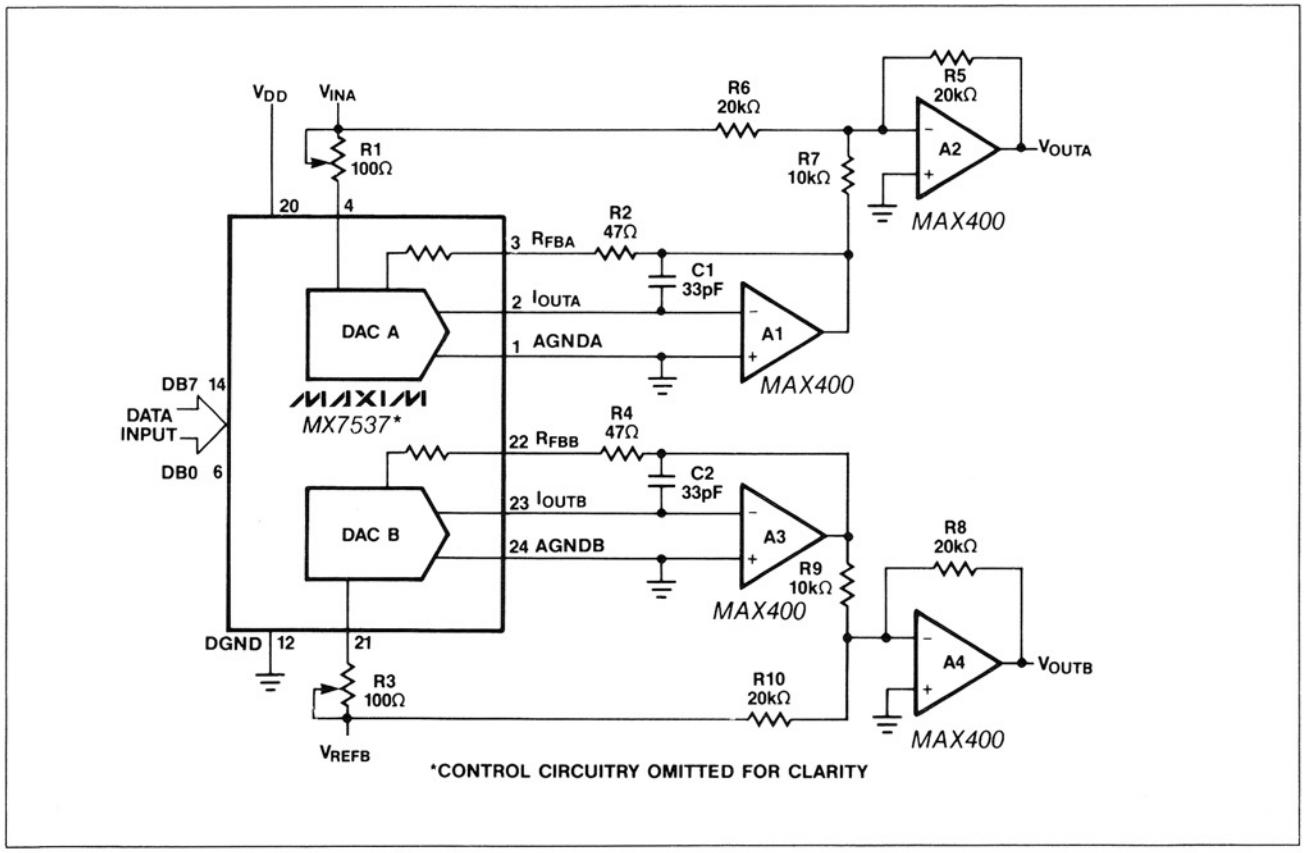


Figure 5A. MX7537 Bipolar Operation (Offset Binary Coding)

CMOS Parallel Loading Dual 12-Bit Multiplying D/A Converters

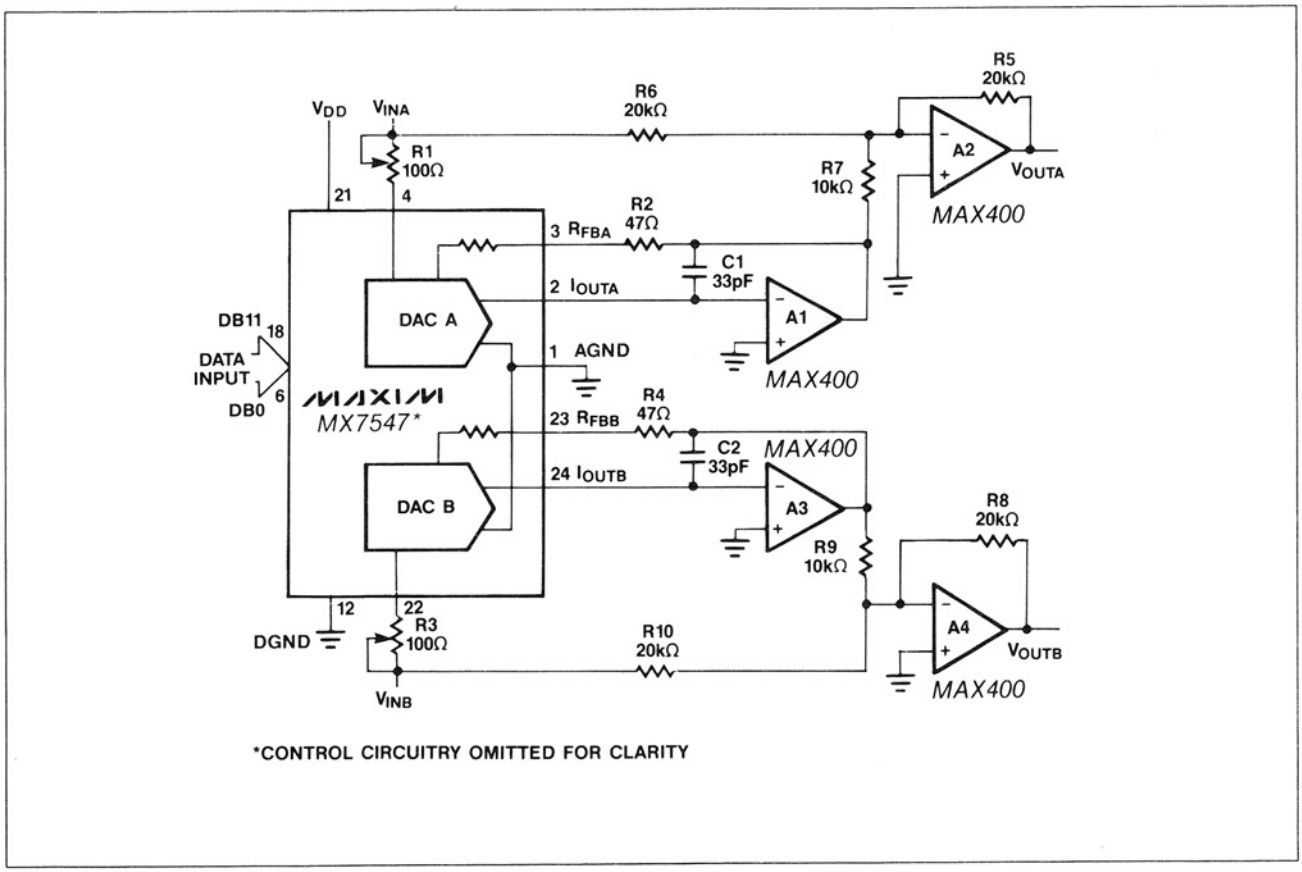


Figure 5B. MX7547 Bipolar Operation (Offset Binary Coding)

Table 5. 2's Complement Code Table

DIGITAL INPUT MSB		LSB	ANALOG OUTPUT
0111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
0000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	0
1111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

To adjust the bipolar circuit, load the DAC with a code of 1000 0000 0000 and trim R1 (or R3) for V_{OUT} = 0V. With R1 and R2 (or R3 and R4) omitted, an alternative zero trim is to adjust the ratios of R5 and R6 (or R8 and R10) for V_{OUT} = 0V. Full scale can be trimmed by loading the DAC with all 0s or all 1s and adjusting the amplitude of V_{REF}, or varying R5 (or R8) until the desired positive or negative output is obtained. In many applications, gain adjustment will not be necessary, especially when using parts with ±1LSB guaranteed maximum gain error. If R1, R2 (or R3, R4) are omitted, then ratio matched 0.01% resistors must be used at R5, R6 and R7 (R8, R9 and R10) for gain error performance to the data sheet specifications. In any case, if the DAC is operated over a wide temperature range, then low tempco (<300ppm/°C) resistors of the same material will provide best performance.

Single Supply Applications

The MX7537/MX7547 can be conveniently used in single supply operation with AGND biased at any voltage between DGND and V_{DD}. Figure 6 shows an MX7547 application which outputs +5V to +10V by biasing AGND at +5V with respect to DGND. The transfer function for each channel is:

$$V_{OUT} = +5V\ (1 + R_{FB}/R_{EQ})$$

where $R_{EQ} = \infty$ and V_{OUT} = +5V with all 0s loaded into the DAC, and $R_{EQ} = R_{FB}$ and V_{OUT} = +10V with all 1s in the DAC.

CMOS Parallel Loading Dual 12-Bit Multiplying D/A Converters

The MX7537 provides separate AGND pins for DAC A and DAC B which allow the two DACs to be biased at different voltages. In Figure 7, DAC A is connected as a programmable attenuator with AGNDA at DGND. DAC B has a +5V bias at AGNDB, resulting in an output range of +5V to +10V for DAC B.

Figure 8 shows a voltage output DAC connection, where I_{OUT} is connected to the reference voltage source (V_{IN}) and AGND is tied to DGND. This is known as "voltage mode" operation. The DAC output now appears at the V_{REF} pin which has a constant output impedance equal to the reference input resistance (typically 11kΩ). R_{FB} is not used in this mode.

Two advantages of the voltage mode operation are single supply operation and that a negative reference is not required for a positive output. Limitations are that the reference input (I_{OUT}) must be positive and less than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal NMOS switches result in degraded integral (INL) and differential nonlinearity (DNL). For optimum performance, V_{IN} must stay between 0V and 2.5V, and a buffer amplifier should be used at the DAC outputs and the inputs. Figure 9 shows how the differential linearity is affected by increasing V_{IN}.

The unipolar and bipolar circuits in Figures 4 and 5 can all be converted to voltage output mode.

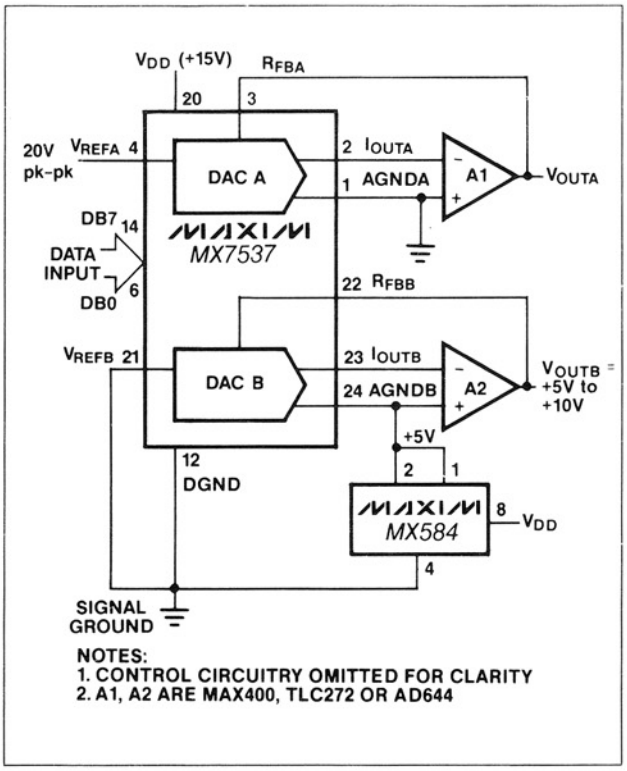


Figure 7. MX7537 DACs Used in Different Modes

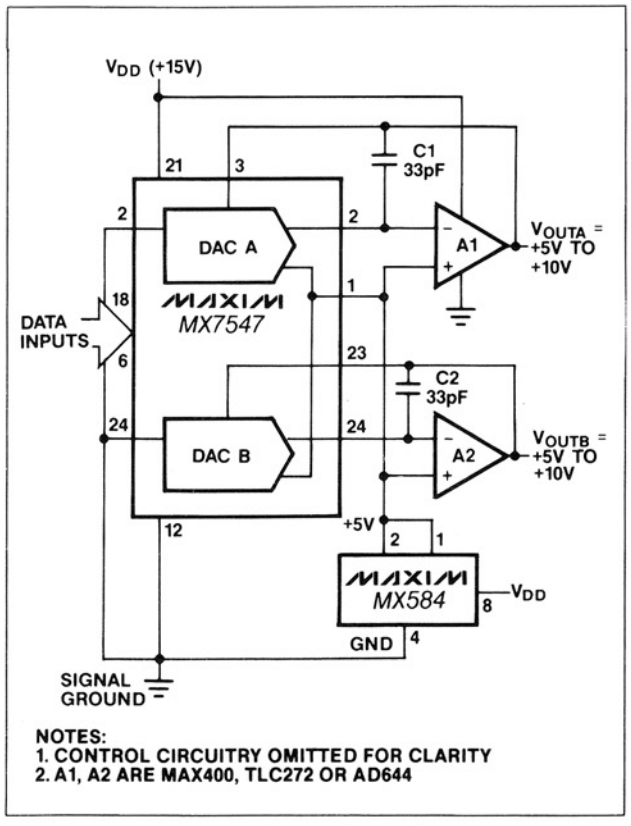


Figure 6. MX7547 Single Supply Operation

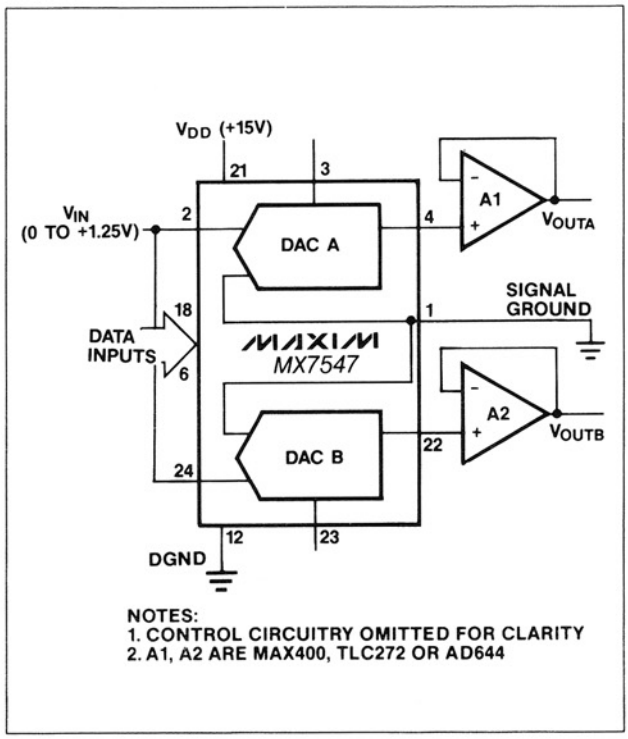


Figure 8. MX7547 Operated in Single Supply, Voltage Switching Mode

CMOS Parallel Loading Dual 12-Bit Multiplying D/A Converters

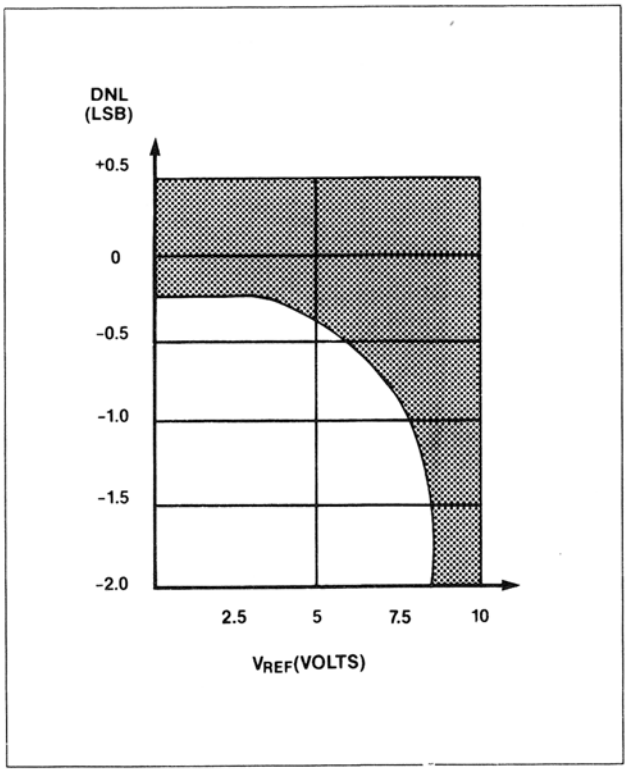


Figure 9. Differential Nonlinearity vs. Reference Voltage for Circuit of Figure 8. V_{DD} = 15V. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occurs for L, C and U Grades.

Microprocessor Interface

MX7537

The MX7537 2-byte interface simplifies the connection to 8-bit microprocessors (μP). Figures 10 and 11 show interface connections to the MC6809 and MC68008. Figure 12 shows how multiple MX7537s can be used in a μP system by tying all the UPD lines together and controlling these with a single address decoder output. Although this application uses a Z80, any other 8-bit μP can be as easily used.

MX7547

The 12-bit parallel interface circuit of the MX7547 simplifies the interface to 16-bit μPs. Figures 13 and 14 show 8086 and 68000 interfaces. Possibility of loading invalid data to the DAC is avoided, since the rising edge of the $\overline{WR}$ signal is used to load the data into the DAC.

Application Information

Output Amplifier Offset

For best linearity, I_{OUT} and AGND should be terminated at exactly 0V. In most applications I_{OUT} is connected to the summing junction of an inverting op amp. The input offset voltage of the amplifier can degrade the linearity of the DAC by causing I_{OUT} to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}\ (1 + R_{FB}/R_O)$$

where V_{OS} is the op amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 11kΩ to 33kΩ. The error voltage range is then typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will, therefore, degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is V_{OS} should be no more than 1/10LSB.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error. I_B should, therefore, be much less than the DAC output current for 1LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier noninverting input is grounded through a "bias current compensation resistor." This resistor adds to the offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} pin to I_{OUT}. This normally is a function of board layout and lead-to-lead package capacitance. Noise signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between the digital input, V_{REF}, and I_{OUT} pins. Suggested PC board layouts that minimize the parasitic signal feedthrough from V_{REFA} and V_{REFB} to the DAC outputs in multiplying applications are shown in Figures 15 and 16.

Compensation

A compensation capacitor, C1 (C2), may be required when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance, C_{OUT}, and the internal feedback resistor, R_{FB}. Its value depends on the type of op amp used but typically ranges from 10pF to 33pF. Too small a value causes output ringing while excess capacitance over-damps the output. The size of C1 (C2) can be minimized and the output voltage settling time improved by keeping the circuit board trace and stray capacitance at I_{OUT} as low as possible.

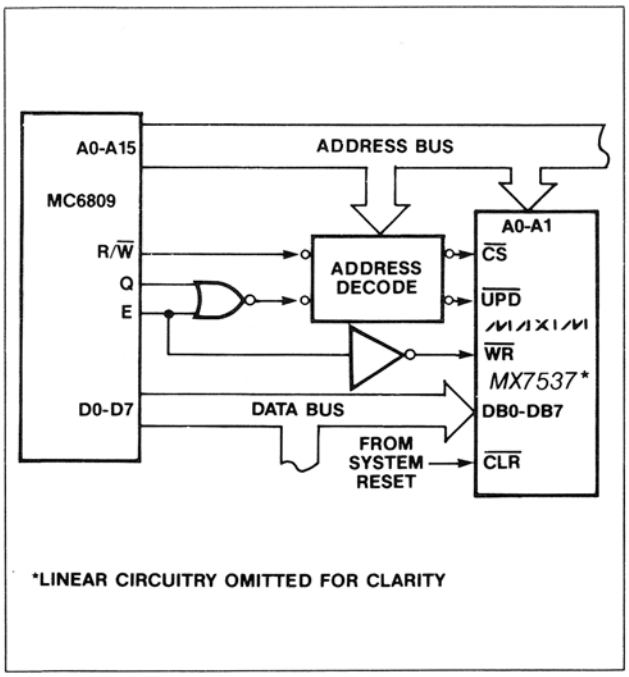


Figure 10. MX7537 — MC6809 Interface

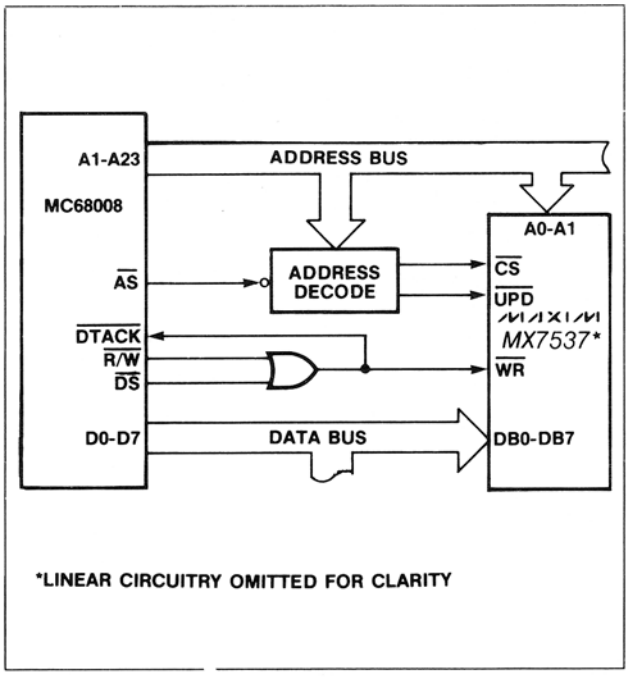


Figure 11. MX7537 — MC68008 Interface

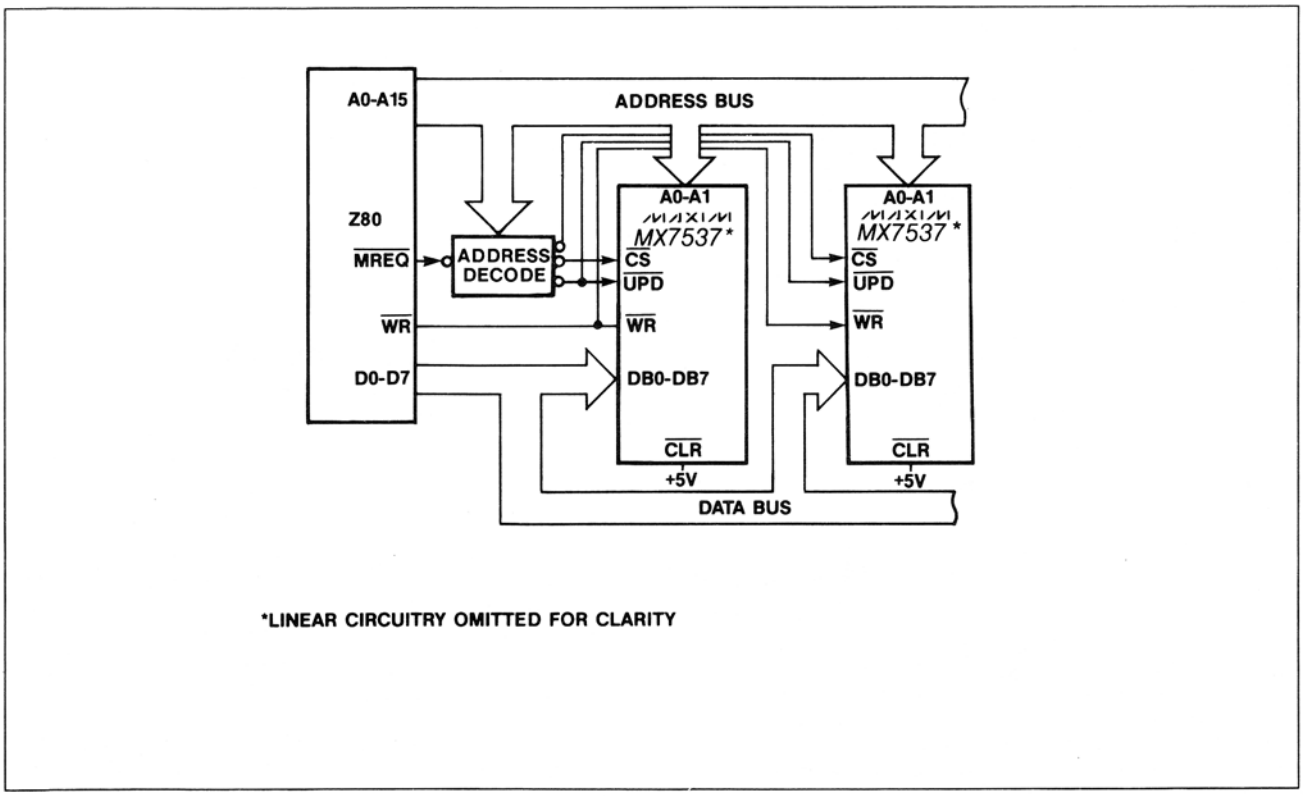


Figure 12. Expanded MX7537 System

CMOS Parallel Loading Dual 12-Bit Multiplying D/A Converters

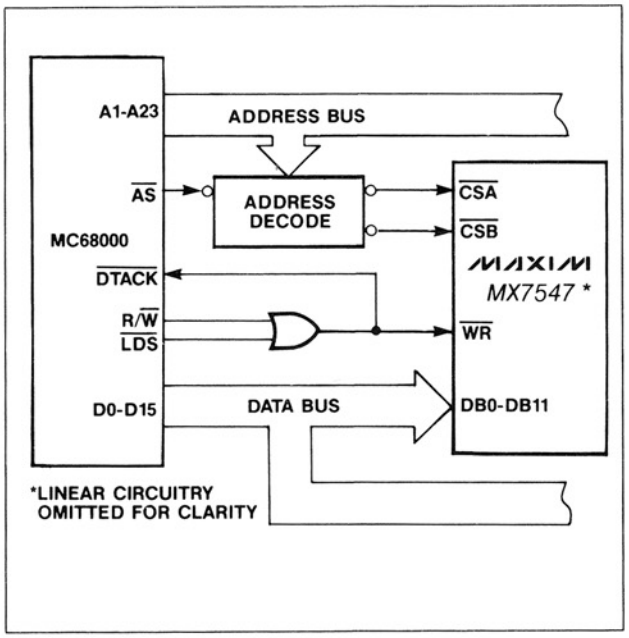


Figure 13. MX7547 — MC68000 Interface

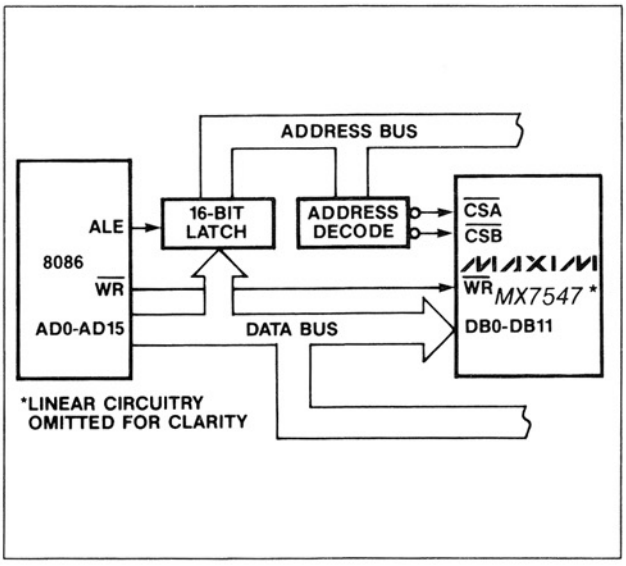


Figure 14. MX7547 — 8086 Interface

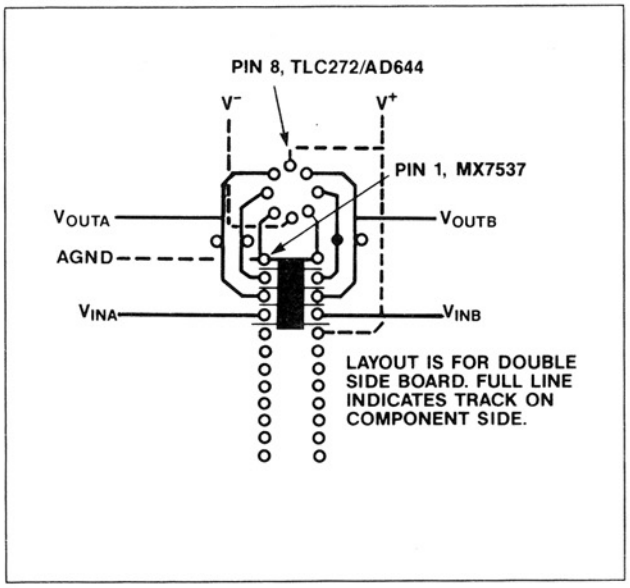


Figure 15. Suggested Layout for MX7537 Circuit of Figure 4A

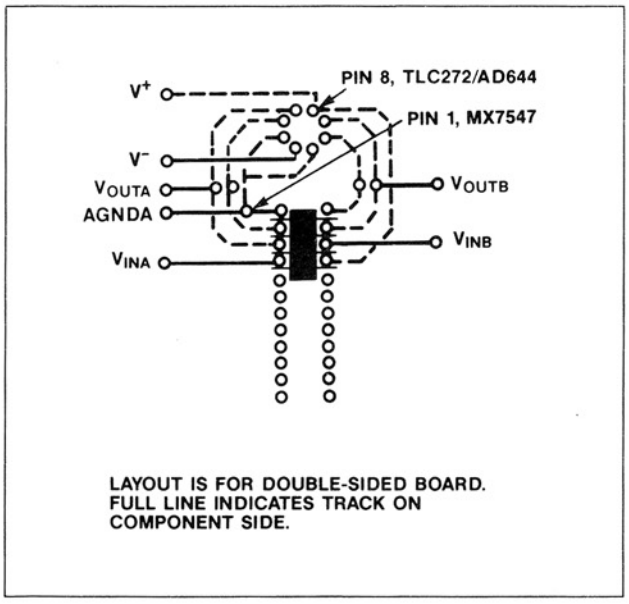


Figure 16. Suggested Layout for MX7547 Circuit of Figure 4B

Grounding and Bypassing

Since I_{OUT} and the noninverting input of the output amplifier are sensitive to offset voltages, nodes that are to be grounded should be connected directly to a "single point" ground through a separate, low resistance (less than 0.2Ω) connection. The current at I_{OUT} and AGND varies with input code, creating a code dependent error if these terminals are connected to ground (or a "virtual ground") through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic capacitor, should be connected across V_{DD} and DGND as close to the device pins as possible.

The MX7537/MX7547 have high impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or DGND when not used. It is good practice to connect active inputs to V_{DD} or DGND through high valued resistors (1MΩ) to prevent static charge accumulation if the pins are left floating, such as when a circuit card is left unconnected.

CMOS Parallel Loading Dual 12-Bit Multiplying D/A Converters

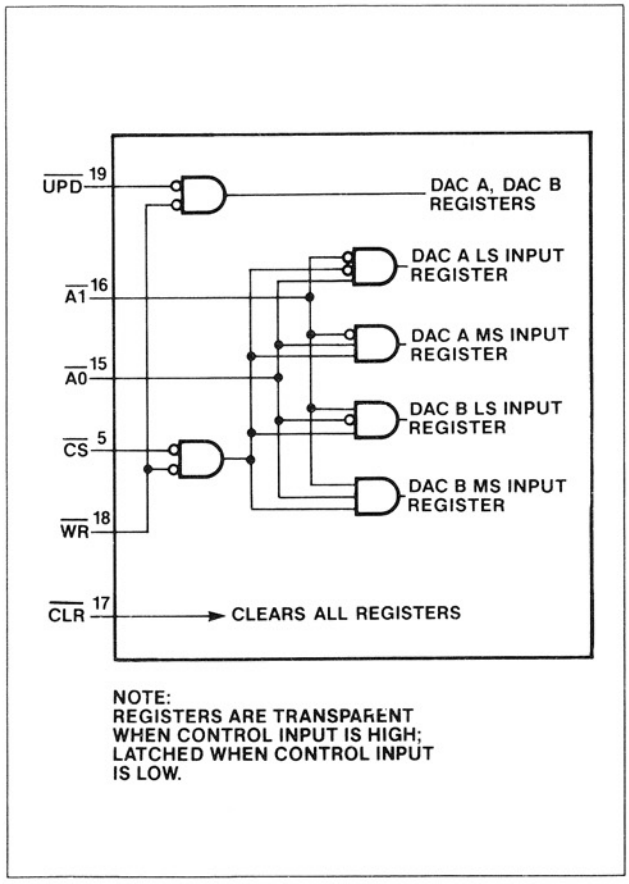


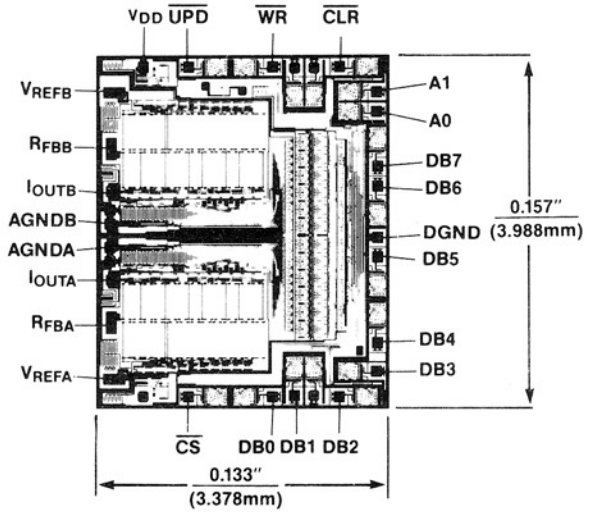
Figure 17. MX7537 Control Logic Equivalent Circuit

Ordering Information (continued)

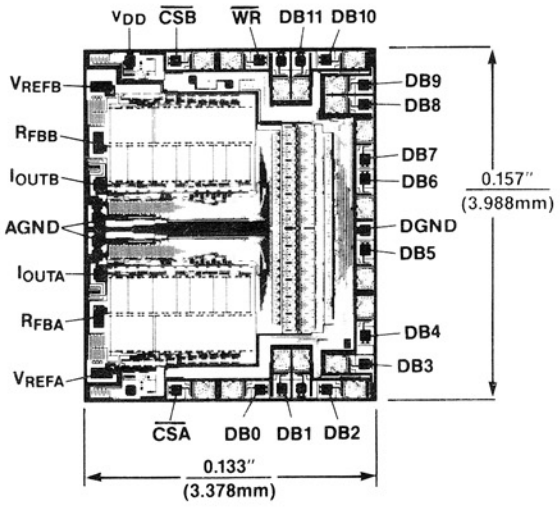
PART	TEMP. RANGE	PACKAGE	GAIN ERROR
MX7537JEWG	-40°C to +85°C	24 Wide SO	±6 LSB
MX7537KEWG	-40°C to +85°C	24 Wide SO	±3 LSB
MX7537LEWG	-40°C to +85°C	24 Wide SO	±1 LSB
MX7537SQ	-55°C to +125°C	24 CERDIP	±6 LSB
MX7537TQ	-55°C to +125°C	24 CERDIP	±3 LSB
MX7537UQ	-55°C to +125°C	24 CERDIP	±2 LSB
MX7547JN	0°C to +70°C	24 Plastic DIP	±6 LSB
MX7547KN	0°C to +70°C	24 Plastic DIP	±3 LSB
MX7547LN	0°C to +70°C	24 Plastic DIP	±1 LSB
MX7547JCWG	0°C to +70°C	24 Wide SO	±6 LSB
MX7547KCWG	0°C to +70°C	24 Wide SO	±3 LSB
MX7547LCWG	0°C to +70°C	24 Wide SO	±1 LSB
MX7547JP	0°C to +70°C	28 PLCC	±6 LSB
MX7547KP	0°C to +70°C	28 PLCC	±3 LSB
MX7547LP	0°C to +70°C	28 PLCC	±1 LSB
MX7547J/D	0°C to +70°C	Dice	±6 LSB
MX7547AQ	-25°C to +85°C	24 CERDIP	±6 LSB
MX7547BQ	-25°C to +85°C	24 CERDIP	±3 LSB
MX7547CQ	-25°C to +85°C	24 CERDIP	±1 LSB
MX7547JEWG	-40°C to +85°C	24 Wide SO	±6 LSB
MX7547KEWG	-40°C to +85°C	24 Wide SO	±3 LSB
MX7547LEWG	-40°C to +85°C	24 Wide SO	±1 LSB
MX7547SQ	-55°C to +125°C	24 CERDIP	±6 LSB
MX7547TQ	-55°C to +125°C	24 CERDIP	±3 LSB
MX7547UQ	-55°C to +125°C	24 CERDIP	±2 LSB

Chip Topographies

MX7537



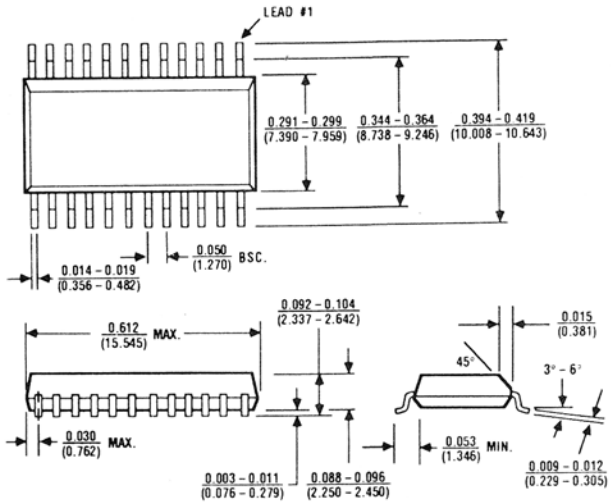
MX7547



CMOS Parallel Loading Dual 12-Bit Multiplying D/A Converters

Package Information

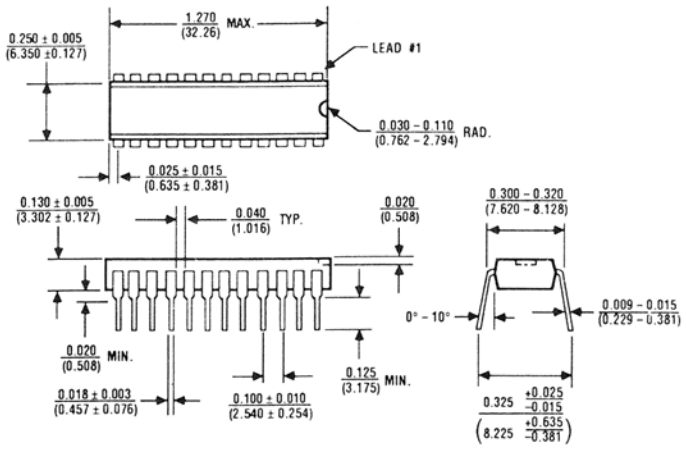
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



24 Lead Small Outline, Wide (WG)

θ_{JA} = 85°C/W

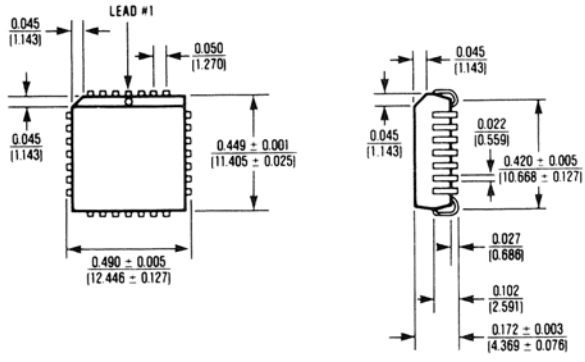
θ_{JC} = 45° C/W



24 Lead Plastic Narrow DIP (NG)

θ_{JA} = 120°C/W

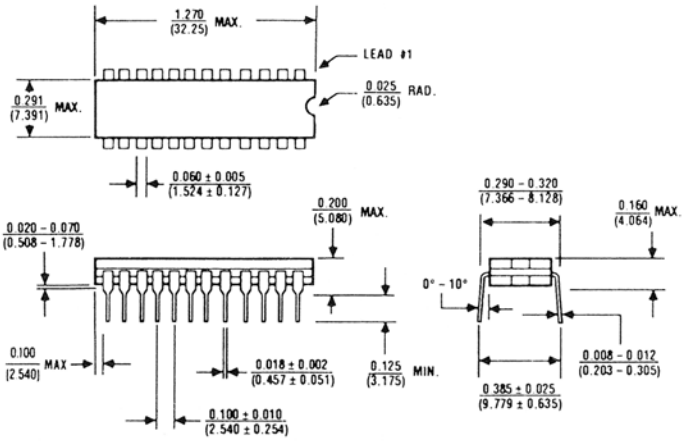
θ_{JC} = 60°C/W



28 Lead Plastic Chip Carrier (Quad Pak) (QI)

θ_{JA} = 100°C/W

θ_{JC} = 45°C/W



24 Lead Narrow CERDIP (RG)

θ_{JA} = 80°C/W

θ_{JC} = 40°C/W

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MX7537JCWG+ on WIN SOURCE
- Maxim Integrated Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management