WINSOURCE ELECTRONICS

THE DATASHEET OF

TXB0106IPWRQ1

TXB0106-Q1 6-Bit Bidirectional Voltage-Level Translator With Auto-Direction Sensing and ±10-kV ESD Protection

1 Features

- Qualified for Automotive Applications
- 1.2 V to 3.6 V on A Port and 1.65 to 5.5 V on B Port ($V_{CCA} \le V_{CCB}$)
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
- OE Input Circuit Referenced to V_{CCA}
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds AEC-Q100
  - A Port
    - 2000-V Human-Body Model
    - 1500-V Charged-Device Model
  - B Port
    - ±10-kV Human-Body Model
    - 1500-V Charged-Device Model

2 Applications

- Heating and Cooling
- Telematics
- Radar

3 Description

This 6-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes. V_{CCA} should not exceed V_{CCB}.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

The TXB0106-Q1 device is designed so that the OE input circuit is supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TXB0106-Q1	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Operating Circuit

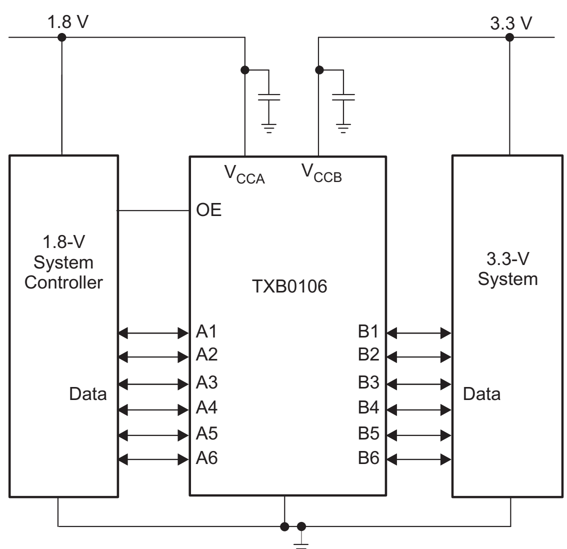


Table of Contents

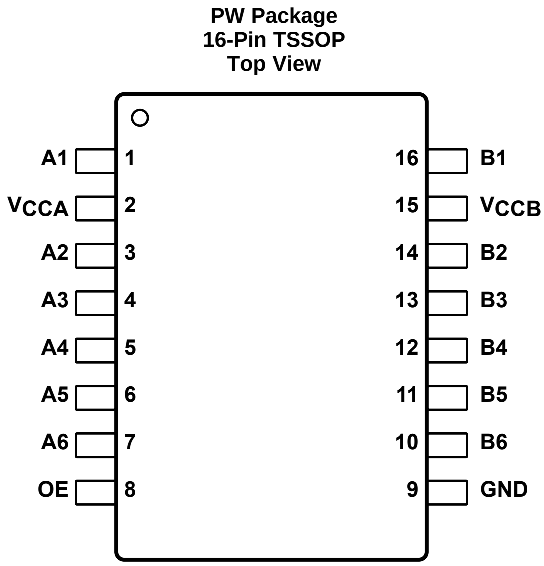
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2009) to Revision A — **Page**

- Added *Applications* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section... 1
- Changed the entry in the TYPE column from "—" to "I" for V_{CCA} and V_{CCB} ... 3
- Added row for junction temperature to *Absolute Maximum Ratings* ... 4
- Added parameter descriptons to *Electrical Characteristics* table ... 5
- Added "-Q1" to the device name throughout the document... 12
- Changed I to I_{CC} in *Output Load Considerations*... 15
- Changed TXS01xx series to TXS family in *Pullup or Pulldown Resistors on I/O Lines* ... 16
- Changed TXS010X to TXS in *Application Information* ... 17
- Clarified wording of sentences and added references to two application reports... 18

5 Pin Configuration and Functions



Pin Functions

NAME	NO.	I/O	DESCRIPTION
A1	1	I/O	Input/output 1. Referenced to V_{CCA}.
A2	3	I/O	Input/output 2. Referenced to V_{CCA}.
A3	4	I/O	Input/output 3. Referenced to V_{CCA}.
A4	5	I/O	Input/output 4. Referenced to V_{CCA}.
A5	6	I/O	Input/output 5. Referenced to V_{CCA}.
A6	7	I/O	Input/output 6. Referenced to V_{CCA}.
B1	16	I/O	Input/output 1. Referenced to V_{CCB}.
B2	14	I/O	Input/output 2. Referenced to V_{CCB}.
B3	13	I/O	Input/output 3. Referenced to V_{CCB}.
B4	12	I/O	Input/output 4. Referenced to V_{CCB}.
B5	11	I/O	Input/output 5. Referenced to V_{CCB}.
B6	10	I/O	Input/output 6. Referenced to V_{CCB}.
GND	9	—	Ground
OE	8	I	Output enable. Pull OE low to place all outputs in the high-impedance state. Referenced to V_{CCA}.
V_{CCA}	2	I	A-port supply voltage. 1.2 V ≤ V_{CCA}≤ 3.6 V, V_{CCA}≤ V_{CCB}.
V_{CCB}	15	I	B-port supply voltage. 1.65 V ≤ V_{CCB} ≤ 5.5 V.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	4.6	V
V_{CCB}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2) (3)	A inputs	–0.5	V_{CCA} + 0.5	V
		B inputs	–0.5	V_{CCB} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The values of V_{CCA} and V_{CCB} are provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions(1) (2)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCI} × 0.65(3)	V_{CCI}	V
		OE			V_{CCA} × 0.65	5.5	
V_{IL}	Low-level input voltage	Data inputs	1.2 V to 5.5 V	1.65 V to 5.5 V	0	V_{CCI} × 0.35(3)	V
		OE	1.2 V to 3.6 V		0	V_{CCA} × 0.35	
Δt/Δv	Input transition rise or fall rate	A-port inputs	1.2 V to 3.6 V	1.65 V to 5.5 V		40	ns/V
		B-port inputs	1.2 V to 3.6 V	1.65 V to 3.6 V		40	
				4.5 V to 5.5 V		30	
T_A	Operating ambient temperature				–40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, that is, both at V_{CCI} or both at GND.
(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.
(3) V_{CCI} is the supply voltage associated with the input port.

6.4 Thermal Information

THERMAL METRIC(1)		TXB0106-Q1 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics(1) (2)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C MIN	TYP	MAX	–40°C to 85°C MIN	MAX	UNIT
V_{OHA}		Output high voltage, A port	I_{OH} = –20 µA	1.2 V			1.1				V
				1.4 V to 3.6 V					V_{CCA} – 0.4		
V_{OLA}		Output low voltage, A port	I_{OL} = 20 µA	1.2 V			0.9				V
				1.4 V to 3.6 V						0.4	
V_{OHB}		Output high voltage, B port	I_{OH} = –20 µA		1.65 V to 5.5 V				V_{CCB} – 0.4		V
V_{OLB}		Output low voltage, B port	I_{OL} = 20 µA		1.65 V to 5.5 V					0.4	V
$I_{lkg(I)}$	OE	Input leakage current		1.2 V to 3.6 V	1.65 V to 5.5 V			±1		±2	µA
$I_{lkg(off)}$	A port	Off-state leakage current		0 V	0 V to 5.5 V			±1		±2	µA
	B port			0 V to 3.6 V	0 V			±1		±2	
I_{OZ}	A or B port	High-impedance output current	OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V			±1		±2	µA
I_{CCA}		V_{CCA} supply current	$V_I = V_{CCI}$ or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		0.06				µA
				1.4 V to 3.6 V						9	
				3.6 V	0 V					2	
				0 V	5.5 V					2	
I_{CCB}		V_{CCB} supply current	$V_I = V_{CCI}$ or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		3.4				µA
				1.4 V to 3.6 V						9	
				3.6 V	0 V					–2	
				0 V	5.5 V					2	
$I_{CCA} + I_{CCB}$		Combined supply current	$V_I = V_{CCI}$ or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		3.5				µA
				1.4 V to 3.6 V						18	
I_{CCZA}		High-impedance V_{CCA} supply current	$V_I = V_{CCI}$ or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		0.05				µA
				1.4 V to 3.6 V						5	
I_{CCZB}		High-impedance V_{CCB} supply current	$V_I = V_{CCI}$ or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		3.3				µA
				1.4 V to 3.6 V						5	
C_I	OE	Input capacitance		1.2 V to 3.6 V	1.65 V to 5.5 V		5			5.5	pF

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.

Electrical Characteristics[1] [2] (continued)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
C_{io}	A port		1.2 V to 3.6 V	1.65 V to 5.5 V		5			6.5	pF
	B port					8			10	

6.6 Timing Requirements – V_{CCA} = 1.2 V, T_A = 25°C

			V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
	Data rate		20	20	20	20	Mbps
t_w	Pulse duration	Data inputs	50	50	50	50	ns

6.7 Timing Requirements – V_{CCA} = 1.5 V ± 0.1 V

over recommended operating ambient temperature range (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			50		50		50		50	Mbps
t_w	Pulse duration	Data inputs	20		20		20		20		ns

6.8 Timing Requirements – V_{CCA} = 1.8 V ± 0.15 V

over recommended operating ambient temperature range (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			52		60		60		60	Mbps
t_w	Pulse duration	Data inputs	19		17		17		17		ns

6.9 Timing Requirements – V_{CCA} = 2.5 V ± 0.2 V

over recommended operating ambient temperature range (unless otherwise noted)

			V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			70		100		100	Mbps
t_w	Pulse duration	Data inputs	14		10		10		ns

6.10 Timing Requirements – V_{CCA} = 3.3 V ± 0.3 V

over recommended operating ambient temperature range (unless otherwise noted)

			V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
	Data rate			100		100	Mbps
t_w	Pulse duration	Data inputs	10		10		ns

6.11 Switching Characteristics – V_{CCA} = 1.2 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
t_{pd}	A	B	9.5	7.9	7.6	8.5	ns
	B	A	9.2	8.8	8.4	8	
t_{en}	OE	A	1	1	1	1	µs
		B	1	1	1	1	
t_{dis} (1)	OE	A	20	17	17	18	ns
		B	20	16	15	15	
t_{rA}, t_{fA}	A-port rise and fall times		4.1	4.4	4.1	3.9	ns
t_{rB}, t_{fB}	B-port rise and fall times		5	5	5.1	5.1	ns
$t_{SK(O)}$	Channel-to-channel skew		2.4	1.7	1.9	7	ns
Max. data rate			20	20	20	20	Mbps

(1) Test procedure uses a 25-MHz sine wave on the input.

6.12 Switching Characteristics – V_{CCA} = 1.5 V ± 0.1 V

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.4	13.5	1.2	10.5	1.1	10.5	0.8	10.1	ns
	B	A	0.9	15.2	0.7	13.8	0.4	13.8	0.3	13.7	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis} (1)	OE	A	6.6	33	6.4	25.3	6.1	23.1	5.9	24.6	ns
		B	6.6	35.6	5.8	25.6	5.5	22.1	5.6	20.6	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	6.5	0.8	6.3	0.8	6.3	0.8	6.3	ns
t_{rB}, t_{fB}	B-port rise and fall times		1	7.3	0.7	4.9	0.7	4.6	0.6	4.6	ns
$t_{SK(O)}$	Channel-to-channel skew			2.6		1.9		1.6		1.3	ns
Max data rate			50		50		50		50		Mbps

(1) Test procedure uses a 25-MHz sine wave on the input.

6.13 Switching Characteristics – V_{CCA} = 1.8 V ± 0.15 V

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	12	1.4	7.7	1.3	6.8	1.2	6.5	ns
	B	A	1.5	13.5	1.2	10	0.8	8.2	0.5	8	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis} (1)	OE	A	5.9	26.7	5.6	21.6	5.4	18.9	4.8	18.7	ns
		B	6.1	33.9	5.2	23.7	5	19.9	5	17.6	
t_{rA}, t_{fA}	A-port rise and fall times		0.7	5.1	0.7	5	1	5	0.7	5	ns
t_{rB}, t_{fB}	B-port rise and fall times		1	7.3	0.7	5	0.7	3.9	0.6	3.8	ns
$t_{SK(O)}$	Channel-to-channel skew			0.8		0.7		0.6		0.6	ns
Max data rate			52		60		60		60		Mbps

(1) Test procedure uses a 25-MHz sine wave on the input.

6.14 Switching Characteristics – V_{CCA} = 2.5 V ± 0.2 V

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.1	6.7	1	5.7	0.9	5	ns
	B	A	1	8.5	0.6	7	0.3	7	
t_{en}	OE	A		1		1		1	µs
		B		1		1		1	
t_{dis} (1)	OE	A	5	16.9	4.9	15	4.5	13.8	ns
		B	4.8	21.8	4.5	17.9	4.4	15.2	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	3.6	0.6	3.6	0.5	3.5	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.6	4.9	0.7	3.9	0.6	3.2	ns
$t_{SK(O)}$	Channel-to-channel skew			0.4		0.3		0.3	ns
Max data rate			70		100		100		Mbps

(1) Test procedure uses a 25-MHz sine wave on the input.

6.15 Switching Characteristics – V_{CCA} = 3.3 V ± 0.3 V

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	B	0.9	5.5	0.8	4.5	ns
	B	A	0.5	6.5	0.2	6	
t_{en}	OE	A		1		1	µs
		B		1		1	
t_{dis} (1)	OE	A	4.5	13.9	4.1	12.4	ns
		B	4.1	17.3	4	14.4	
t_{rA}, t_{fA}	A-port rise and fall times		0.5	3	0.5	3	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.7	3.9	0.6	3.2	ns
$t_{SK(O)}$	Channel-to-channel skew			0.4		0.3	ns
Max data rate			100		100		Mbps

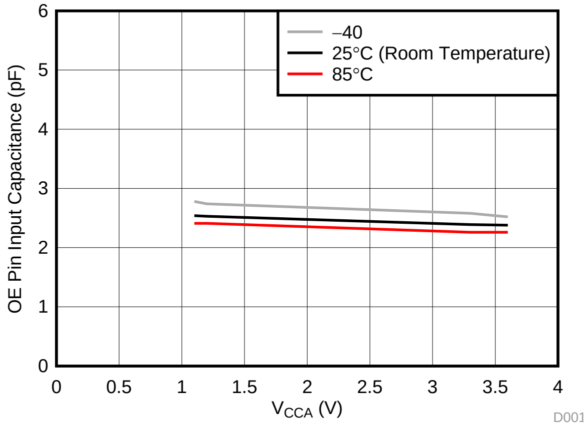
(1) Test procedure uses a 25-MHz sine wave on the input.

6.16 Operating Characteristics

T_A = 25°C

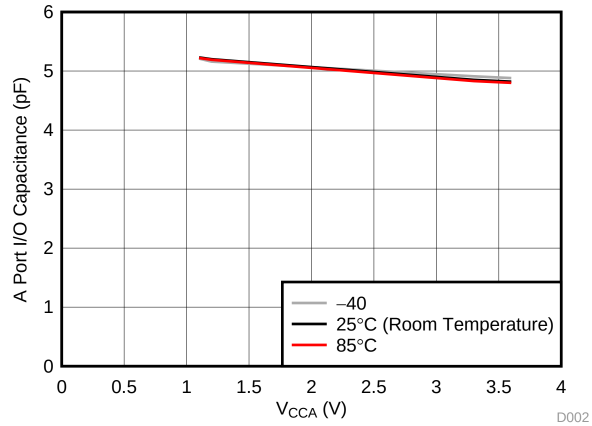
PARAMETER		TEST CONDITIONS	V_{CCA} 1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V	UNIT
			V_{CCB} 5 V	1.8 V	1.8 V	1.8 V	2.5 V	5 V	3.3 V to 5 V	
			TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = V_{CCA} (outputs enabled)	9	8	7	7	7	7	8	pF
	B-port input, A-port output		12	11	11	11	11	11	11	
C_{pdB}	A-port input, B-port output		35	26	27	27	27	27	28	pF
	B-port input, A-port output		26	19	18	18	18	20	21	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = GND (outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C_{pdB}	A-port input, B-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	pF
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	

6.17 Typical Characteristics



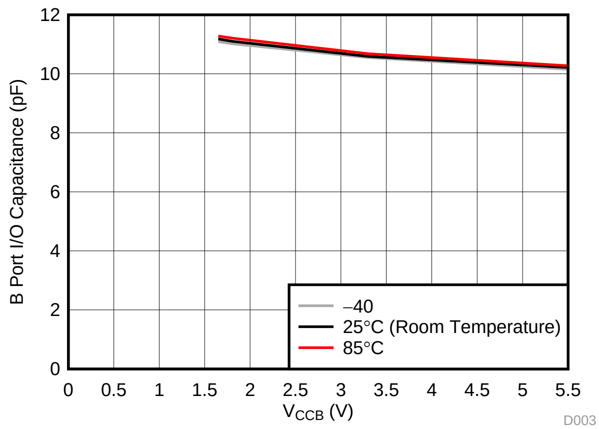
V_{CCB}= 3.3 V

Figure 1. Input capacitance for OE pin (C_I) vs Power Supply (V_{CCA})



V_{CCB}= 3.3 V

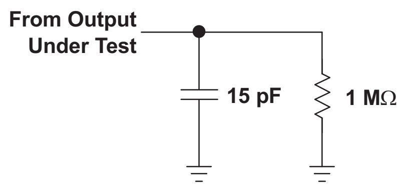
Figure 2. Capacitance for A port I/O pins (C_{iO}) vs Power Supply (V_{CCA})



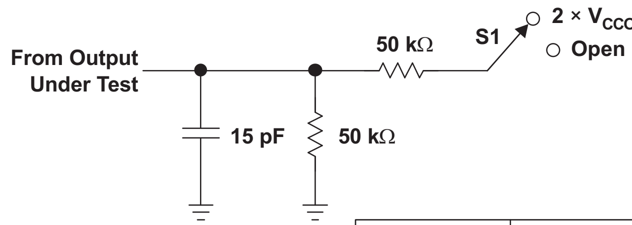
V_{CCA}= 1.8 V

Figure 3. Capacitance for B port I/O pins (C_{iO}) vs Power Supply (V_{CCB})

7 Parameter Measurement Information

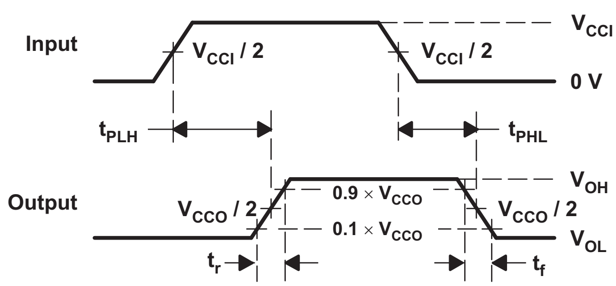


LOAD CIRCUIT FOR MAX. DATA RATE, PULSE DURATION, PROPAGATION DELAY, AND OUTPUT RISE AND FALL TIME MEASUREMENT



LOAD CIRCUIT FOR ENABLE OR DISABLE TIME MEASUREMENT

TEST	S1
t_{PZL} or t_{PLZ}	2 × V_{CCO}
t_{PHZ} or t_{PZH}	Open



VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS FOR PULSE DURATION

A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. V_{CCI} is the V_{CC} associated with the input port.
F. V_{CCO} is the V_{CC} associated with the output port.
G. All parameters and waveforms are not applicable to all devices.

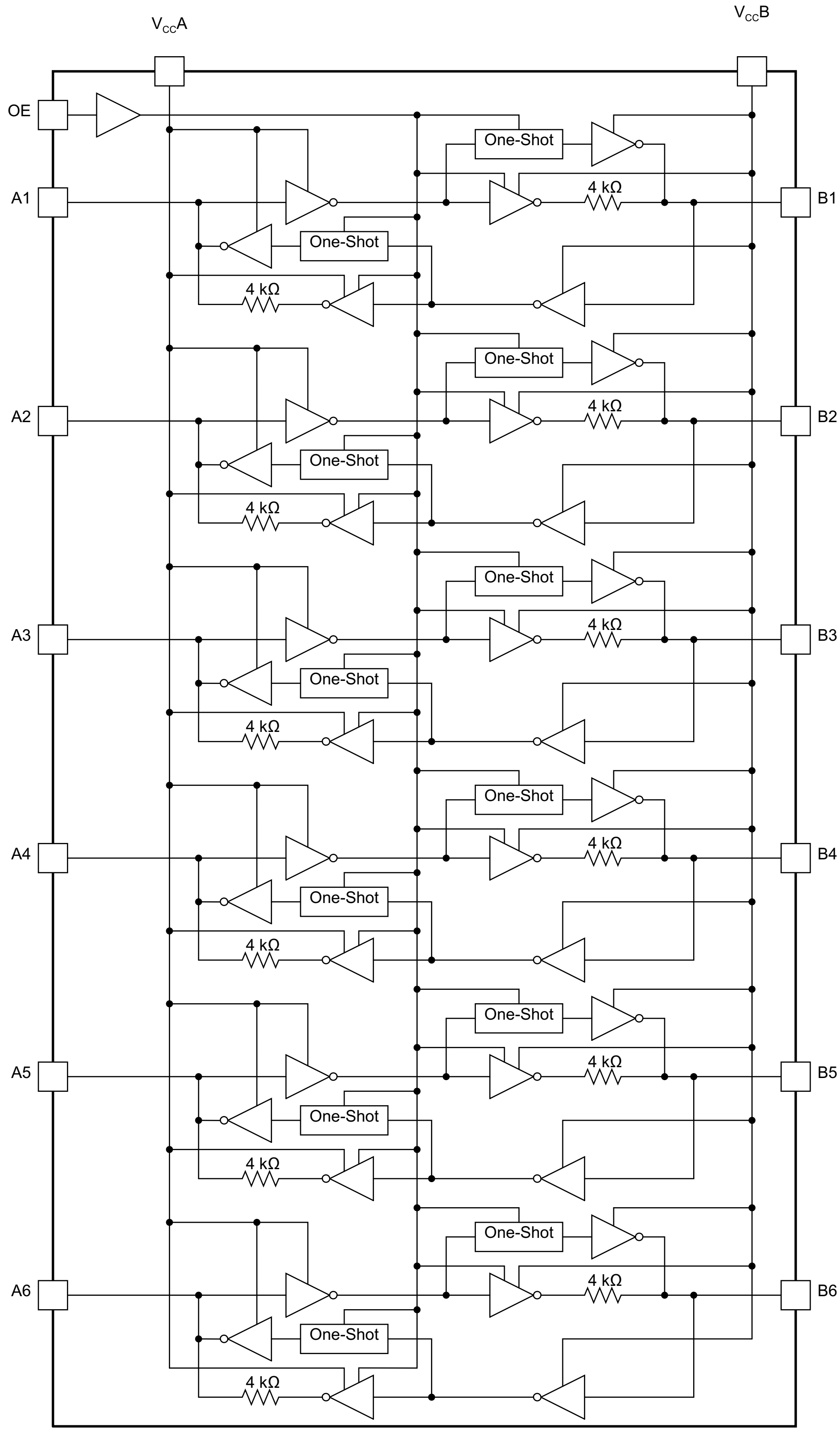
Figure 4. Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TXB0106-Q1 device is a 6-bit, directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. For open-drain signal translation, see TI's TXS family of products.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Architecture

The TXB0106-Q1 architecture (see Figure 5) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0106-Q1 device can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing in the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at V_{CCO} = 1.2 V to 1.8 V, 50 Ω at V_{CCO} = 1.8 V to 3.3 V, and 40 Ω at V_{CCO} = 3.3 V to 5 V.

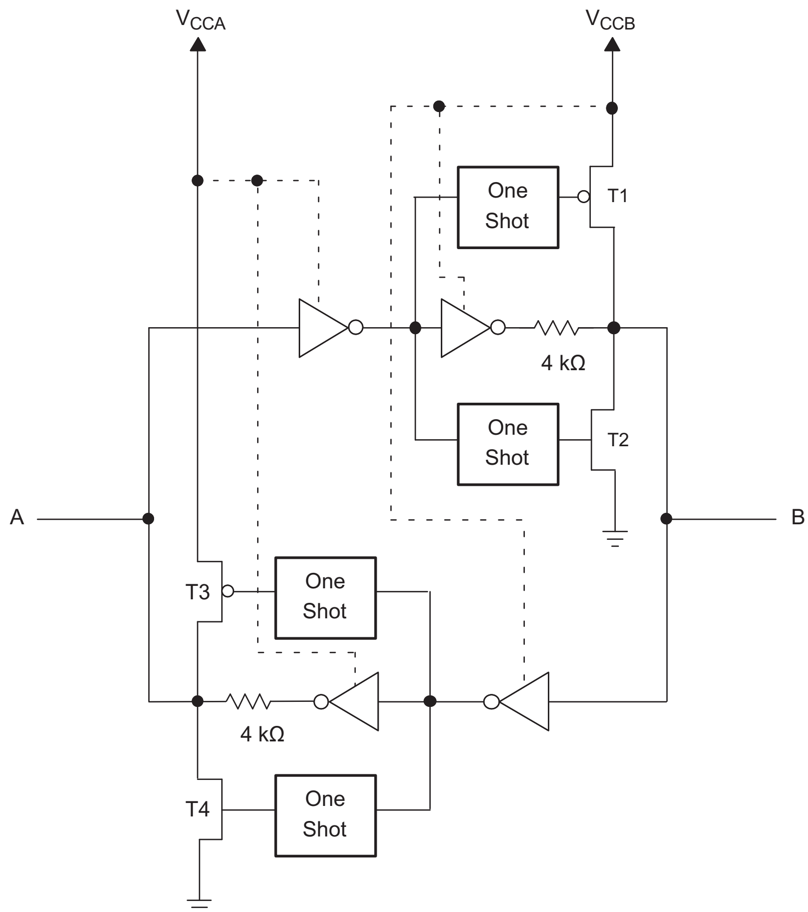
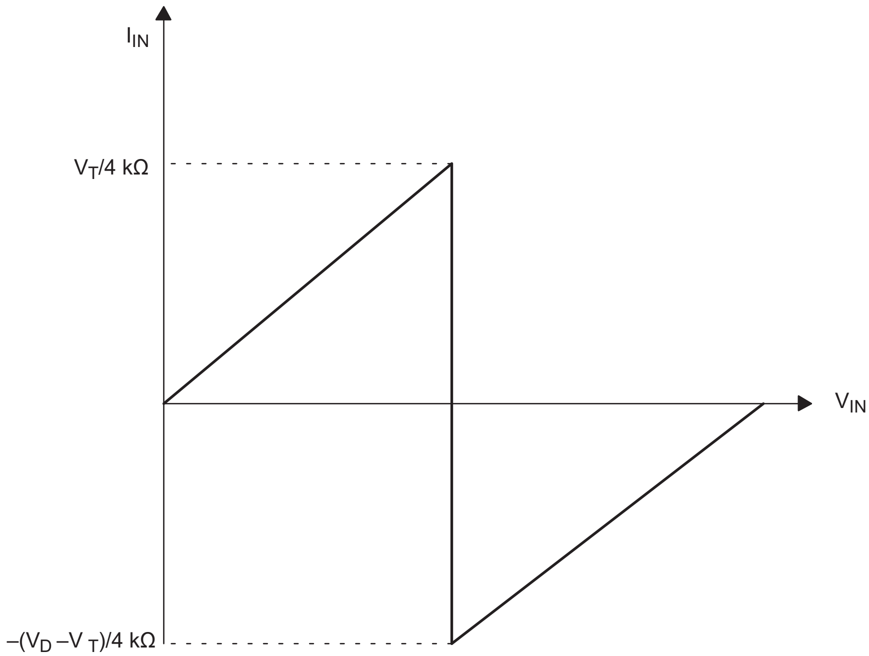


Figure 5. Architecture of the TXB0106-Q1 I/O Cell

8.3.2 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0106-Q1 device are shown in Figure 6. For proper operation, the device driving the data I/Os of the TXB0106-Q1 device must have drive strength of at least ±2 mA.

Feature Description (continued)



A. V_T is the input threshold voltage of the TXB0106-Q1 device (typically V_{CCI} / 2).

B. V_D is the supply voltage of the external driver.

Figure 6. Typical I_{IN} vs V_{IN} Curve

8.3.3 Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0106-Q1 device has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B}$ = 0 V).

8.3.4 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper one-shot (O.S.) triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the O.S. duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the O.S. duration. With very heavy capacitive loads, the O.S. can time out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXB0106-Q1 output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

8.3.5 Enable and Disable

The TXB0106-Q1 device has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the O.S. circuitry to become operational after OE is taken high.

Feature Description (continued)

8.3.6 Pullup or Pulldown Resistors on I/O Lines

The TXB0106-Q1 device is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0106-Q1 device have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 kΩ to ensure that they do not contend with the output drivers of the TXB0106-Q1 device.

For the same reason, the TXB0106-Q1 device should not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from TI's TXS family of level translators.

8.4 Device Functional Modes

The TXB0106-Q1 device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high-impedance state. Setting the OE input to high will enable the device.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TXB0106-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. For open-drain signal translation, see TI's TXS products. Any external pulldown or pullup resistors are recommended to be larger than 50 kΩ.

9.2 Typical Application

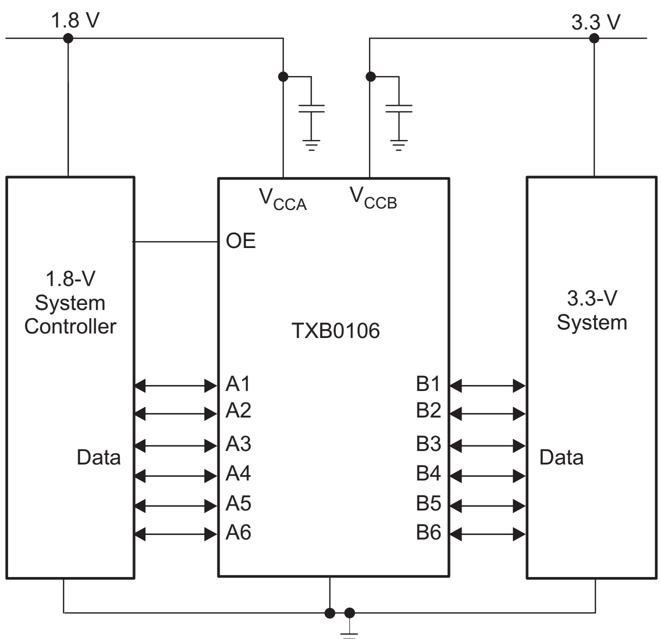


Figure 7. Typical Operating Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1. And make sure that $V_{CCA} \le V_{CCB}$.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.65 V to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXB0106-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.

- Output voltage range
  - Use the supply voltage of the device that the TXB0106-Q1 device is driving to determine the output voltage range.
  - Avoid the use of external pullup or pulldown resistors, if possible. If not possible, it is recommended the value should be larger than 50 kΩ.
- An external pulldown or pullup resistor decreases the output V_{OH} and V_{OL}. Use the following equations to estimate the V_{OH} and V_{OL} as a result of an external pulldown and pullup resistor. See *Effects of External Pullup and Pulldown Resistors on TXS and TXB Devices* and *Factors Affecting VOL for TXS and LSF Auto-bidirectional Translation Devices*.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4.5\ k\Omega)$$
$$V_{OL} = V_{CCx} \times 4.5\ k\Omega / (R_{PU} + 4.5\ k\Omega)$$

Where
- V_{CCx} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pulldown resistor
- R_{PU} is the value of the external pullup resistor
- 4.5 kΩ accounts for the tolerance of the serial 4-kΩ resistor in the I/O line.

9.2.3 Application Curve

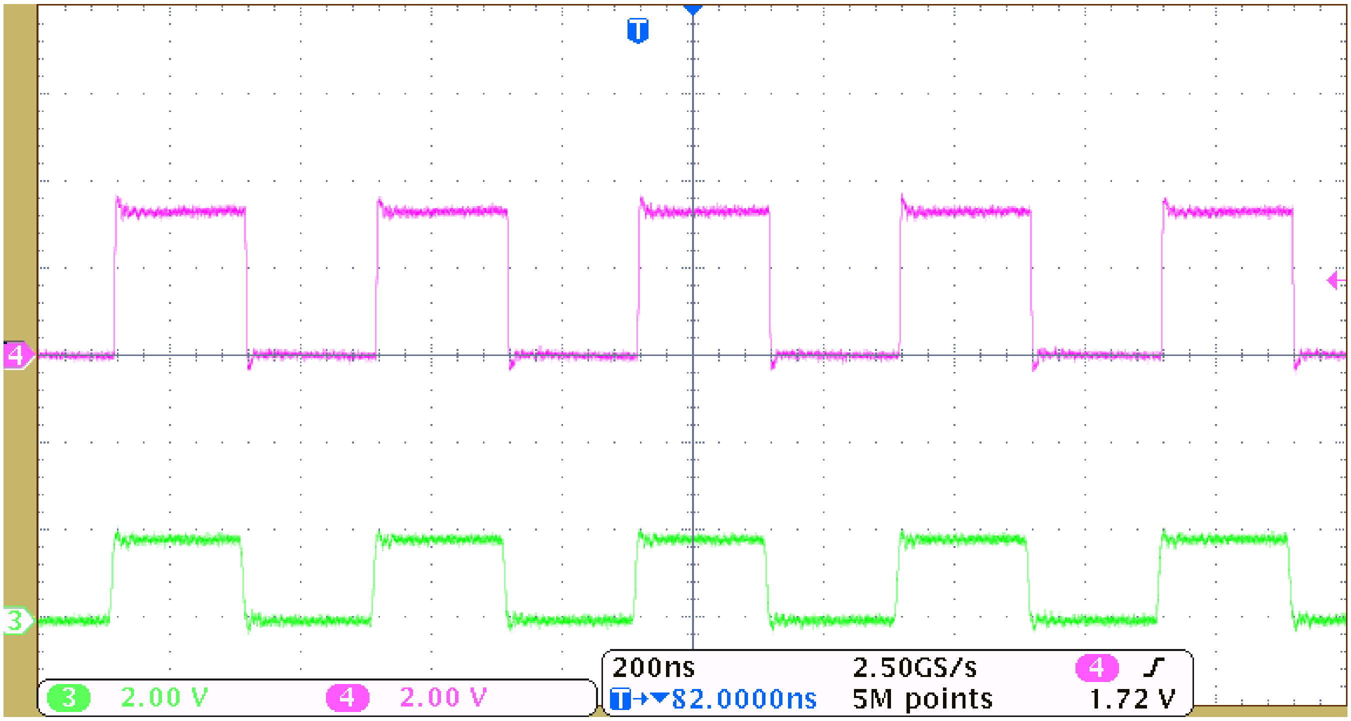


Figure 8. Level Translation of a 2.5-MHz Signal

10 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0106-Q1 device has circuitry that disables all output ports when either V_{CC} is switched off (V_{CCA} or V_{CCB}= 0 V). The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA}, and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

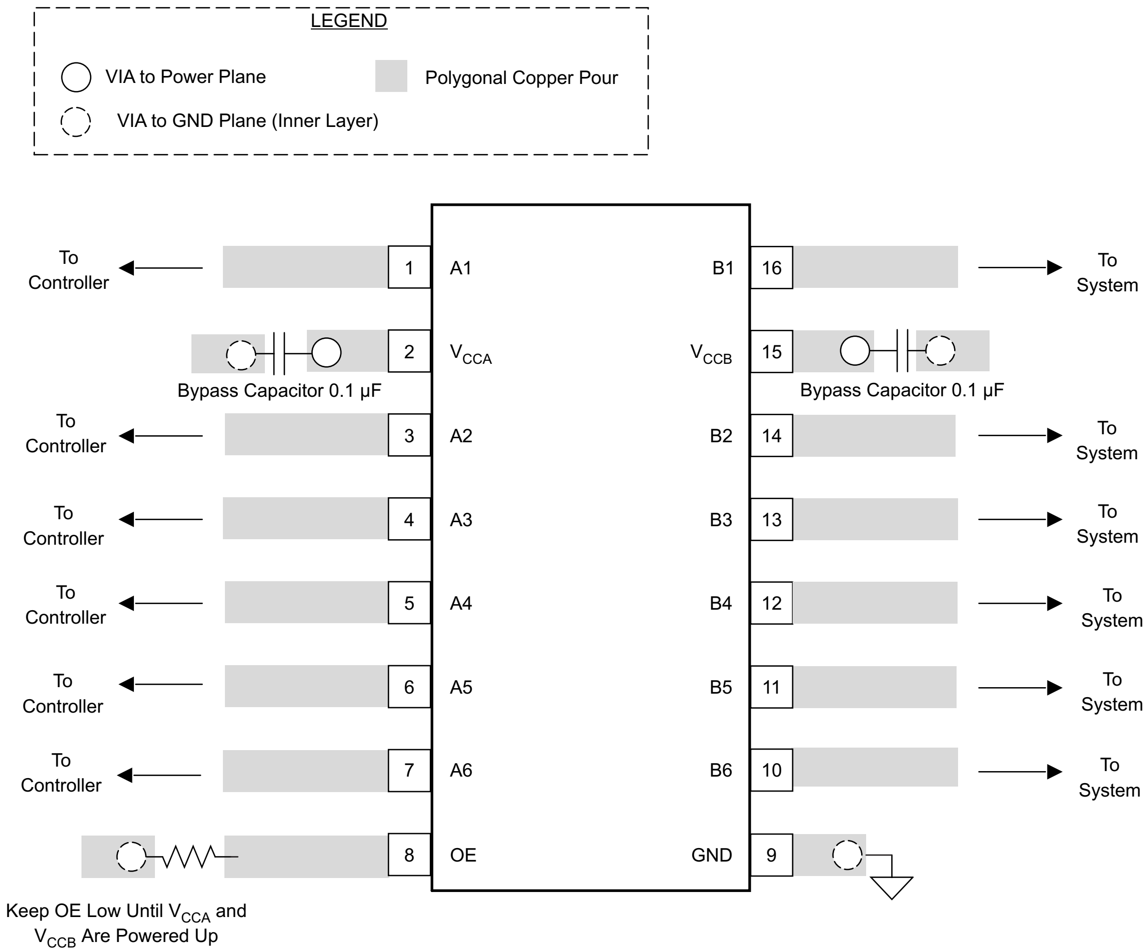
11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended.

- Bypass capacitors should be used on power supplies, and should be placed as close as possible to the V_{CCA} and V_{CCB} pins and the GND pin
- Short trace-lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the O.S. duration, approximately 10 ns, ensuring that any reflection encounters low impedance at the source driver.

11.2 Layout Example



12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0106IPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YE06Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXB0106-Q1 :

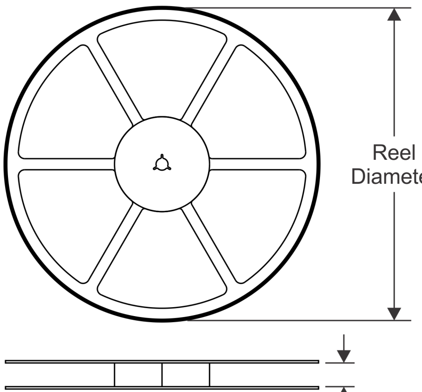
- Catalog: TXB0106

NOTE: Qualified Version Definitions:

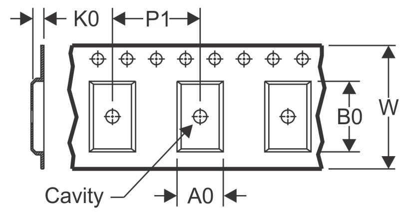
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

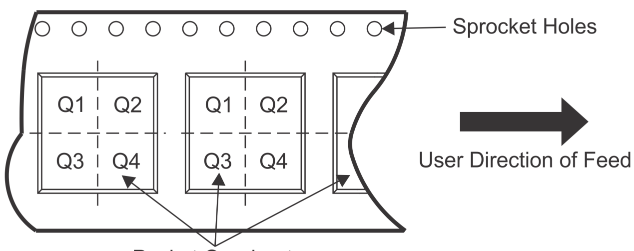


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

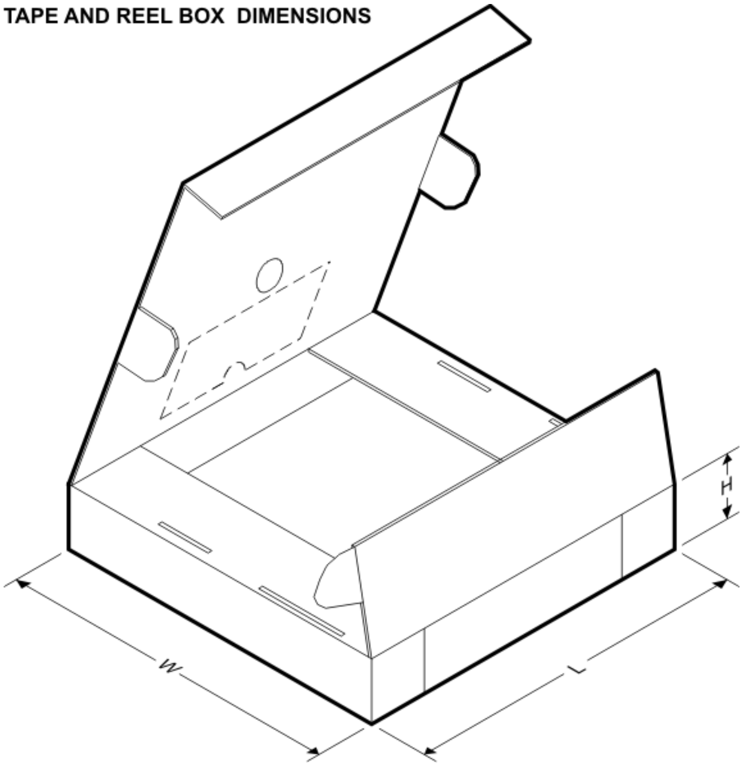
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

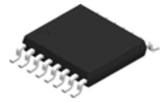
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0106IPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

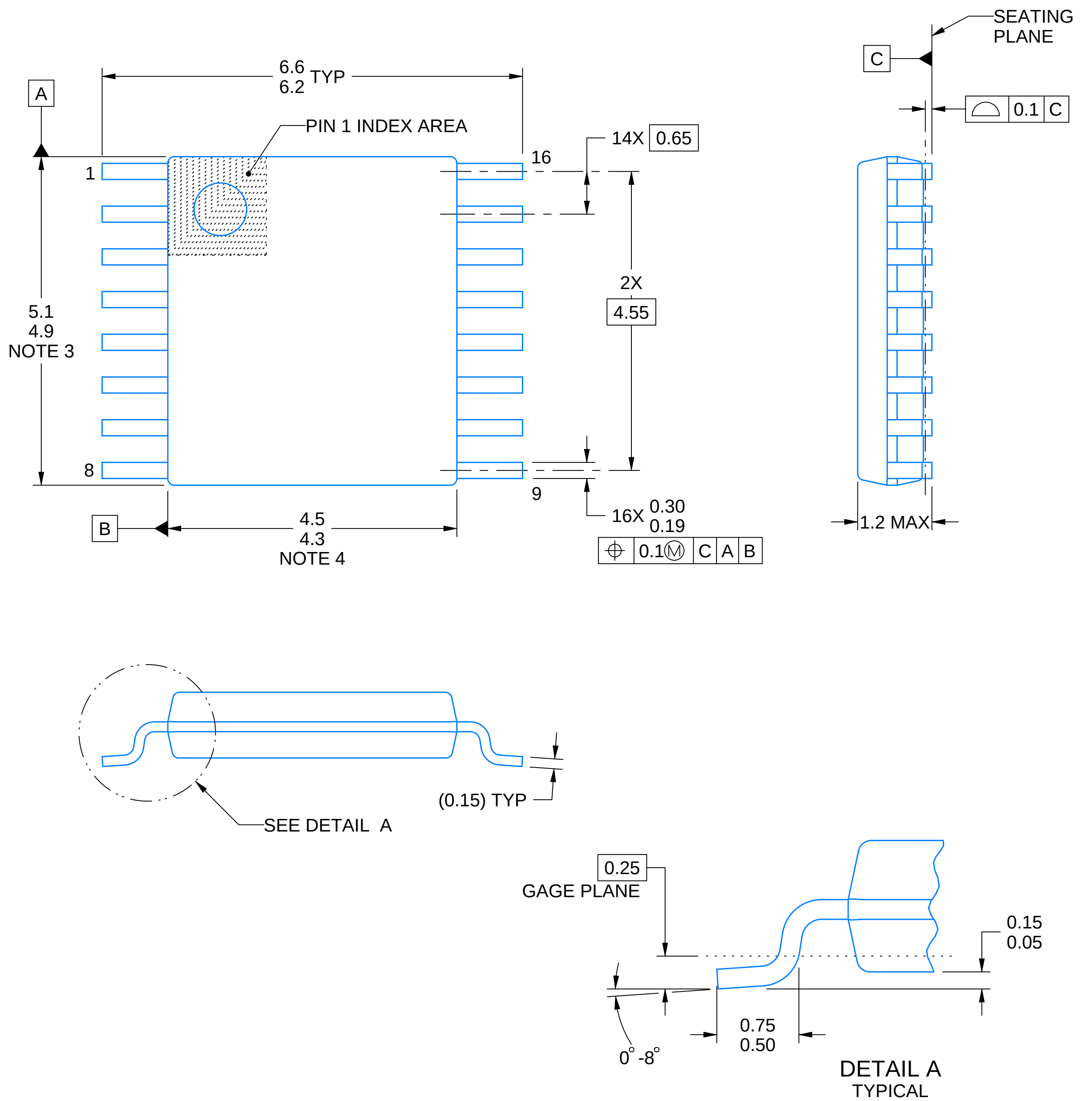
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0106IPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

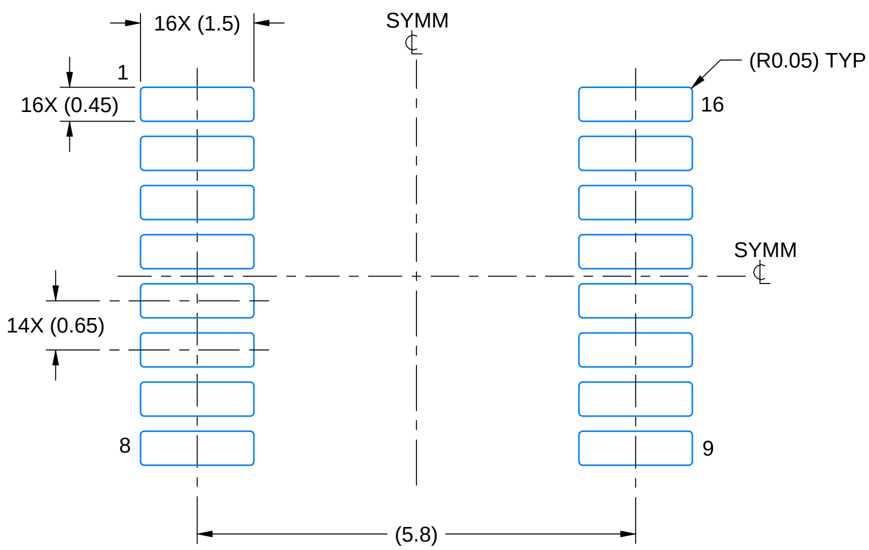
SMALL OUTLINE PACKAGE



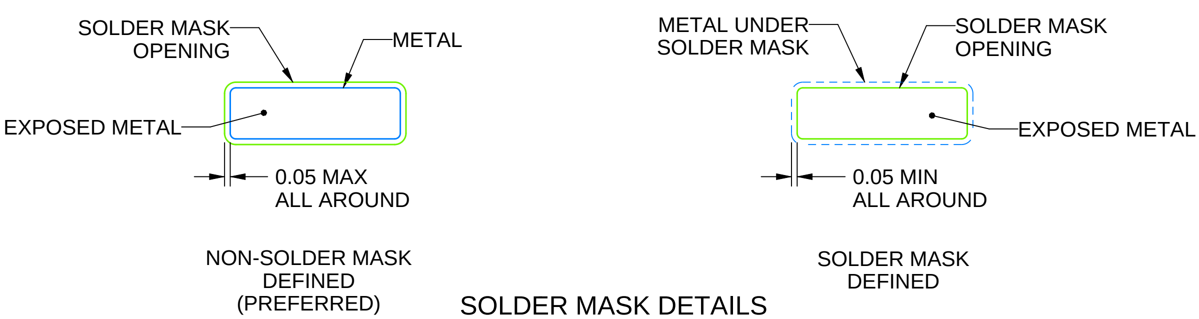
4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

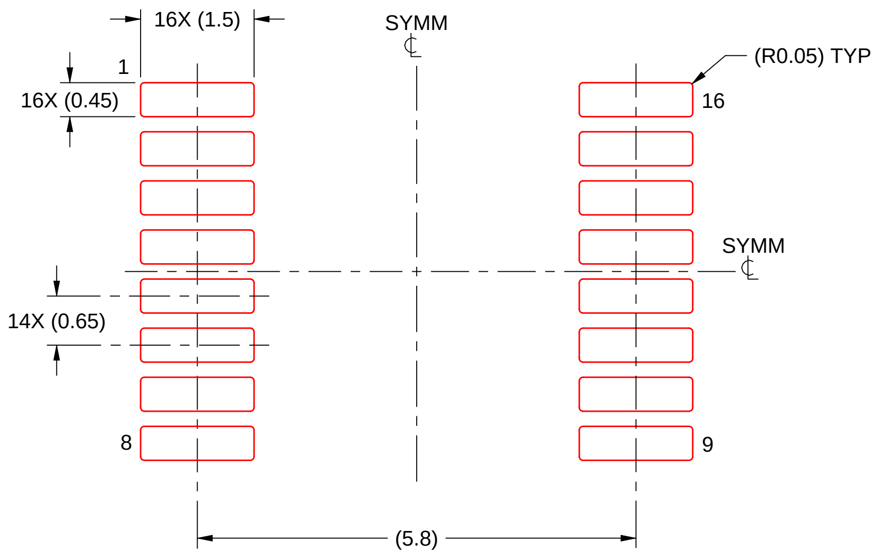


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265