



**THE DATASHEET OF
SN74LVC2G66QDCURQ1**

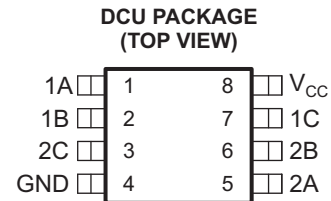


DUAL BILATERAL ANALOG SWITCH

Check for Samples: [SN74LVC2G66-Q1](#)

FEATURES

- Qualified for Automotive Applications
 - AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H2
 - Device CDM ESD Classification Level C3B
 - 1.65-V to 5.5-V V_{CC} Operation
 - Inputs Accept Voltages to 5.5 V
 - High On-Off Output Voltage Ratio
 - High Degree of Linearity
 - High Speed, Typically 0.5 ns
- ($V_{CC} = 3\text{ V}$, $C_L = 50\text{ pF}$)
 - Rail-to-Rail Input/Output
 - Low On-State Resistance, Typically #6 Ω ($V_{CC} = 4.5\text{ V}$)



DESCRIPTION

The design of this dual bilateral analog switch is for 1.65-V to 5.5-V V_{CC} operation. The SN74LVC2G66-Q1 can handle both analog and digital signals. The device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction. Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

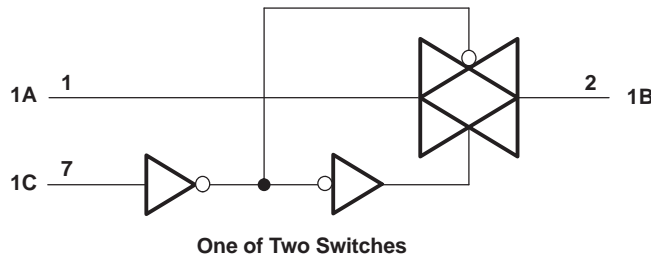
| T _A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽²⁾ |
|----------------|------------------------|--------------|-----------------------|---------------------------------|
| -40°C to 125°C | VSSOP – DCU | Reel of 3000 | SN74LVC2G66QDCURQ1 | CAY_ |

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) DCU: The actual top-side marking has one additional character that designates the assembly/test site.

**FUNCTION TABLE
(EACH SECTION)**

| CONTROL INPUT (C) | SWITCH |
|-------------------|--------|
| L | Off |
| H | On |

LOGIC DIAGRAM, EACH SWITCH (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|--|--|-----------------------|------|
| V _{CC} | Supply voltage range ⁽²⁾ | -0.5 | 6.5 | V |
| V _I | Input voltage range ^{(2) (3)} | -0.5 | 6.5 | V |
| V _O | Switch I/O voltage range ^{(2) (3) (4)} | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Control input clamp current | V _I < 0 | -50 | mA |
| I _{I/O} | I/O port diode current | V _{I/O} < 0 or V _{I/O} > V _{CC} | -50 | mA |
| I _T | On-state switch current | V _{I/O} = 0 to V _{CC} | ±50 | mA |
| | Continuous current through V _{CC} or GND | | ±100 | mA |
| T _{stg} | Storage temperature range | -65 | 150 | °C |
| ESD ratings | Human-Body Model (HBM) AEC-Q100 Classification Level H2 | | 2 | kV |
| | Charged-Device Model (CDM) AEC-Q100 Classification Level C3B | | 750 | V |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) Exceeding the input and output negative-voltage ratings is permitted when in observance of the input and output clamp-current ratings.
- (4) This limit on this value is limited 5.5 V maximum.

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | SN74LVC2G66-Q1 | UNIT |
|-------------------------------|---|----------------|------|
| | | DCU | |
| | | 8 PINS | |
| θ_{JA} | Junction-to-ambient thermal resistance ⁽²⁾ | 204.4 | °C/W |
| θ_{JcTop} | Junction-to-case (top) thermal resistance ⁽³⁾ | 77 | °C/W |
| θ_{JB} | Junction-to-board thermal resistance ⁽⁴⁾ | 83.2 | °C/W |
| ψ_{JT} | Junction-to-top characterization parameter ⁽⁵⁾ | 7.1 | °C/W |
| ψ_{JB} | Junction-to-board characterization parameter ⁽⁶⁾ | 82.7 | °C/W |
| θ_{JcBot} | Junction-to-case (bottom) thermal resistance ⁽⁷⁾ | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|---|---|----------------------|------|
| V_{CC} | Supply voltage | 1.65 | 5.5 | V |
| $V_{I/O}$ | I/O port voltage | 0 | V_{CC} | V |
| V_{IH} | High-level input voltage, control input | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $V_{CC} \times 0.65$ | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $V_{CC} \times 0.7$ | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | $V_{CC} \times 0.7$ | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $V_{CC} \times 0.7$ | |
| V_{IL} | Low-level input voltage, control input | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $V_{CC} \times 0.35$ | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $V_{CC} \times 0.3$ | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | $V_{CC} \times 0.3$ | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $V_{CC} \times 0.3$ | |
| V_I | Control input voltage | 0 | 5.5 | V |
| $\Delta t/\Delta v$ | Input transition rise/fall time | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | 20 | ns/V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 20 | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | 10 | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 10 | |
| T_A | Operating free-air temperature | -40 | 125 | °C |

- (1) Hold all unused inputs of the device at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---|--|------------------------|--------|--------------------|---------------------|------|
| r _{on} On-state switch resistance | V _I = V _{CC} or GND, V _C = V _{IH} (see Figure 1 and Figure 2) | I _S = 4 mA | 1.65 V | 12.5 | 35 | Ω |
| | | I _S = 8 mA | 2.3 V | 9 | 30 | |
| | | I _S = 24 mA | 3 V | 7.5 | 20 | |
| | | I _S = 32 mA | 4.5 V | 6 | 15 | |
| r _{on(p)} Peak on-state resistance | V _I = V _{CC} to GND, V _C = V _{IH} (see Figure 1 and Figure 2) | I _S = 4 mA | 1.65 V | 85 | 120 ⁽¹⁾ | Ω |
| | | I _S = 8 mA | 2.3 V | 22 | 30 ⁽¹⁾ | |
| | | I _S = 24 mA | 3 V | 12 | 25 | |
| | | I _S = 32 mA | 4.5 V | 7.5 | 20 | |
| Δr _{on} Difference of on-state resistance between switches | V _I = V _{CC} to GND, V _C = V _{IH} (see Figure 1 and Figure 2) | I _S = 4 mA | 1.65 V | | 10 | Ω |
| | | I _S = 8 mA | 2.3 V | | 8 | |
| | | I _S = 24 mA | 3 V | | 6 | |
| | | I _S = 32 mA | 4.5 V | | 5 | |
| I _{S(off)} Off-state switch leakage current | V _I = V _{CC} and V _O = GND or V _I = GND and V _O = V _{CC} , V _C = V _{IL} (see Figure 3) | 5.5 V | | ±2 | ±0.1 ⁽¹⁾ | μA |
| I _{S(on)} On-state switch leakage current | V _I = V _{CC} or GND, V _C = V _{IH} , V _O = Open (see Figure 4) | 5.5 V | | ±2 | ±0.1 ⁽¹⁾ | μA |
| I _I Control input current | V _C = V _{CC} or GND | 5.5 V | | ±1 | ±0.1 ⁽¹⁾ | μA |
| I _{CC} Supply current | V _C = V _{CC} or GND | 5.5 V | | 15 | 1 ⁽¹⁾ | μA |
| ΔI _{CC} Supply-current change | V _C = V _{CC} – 0.6 V | 5.5 V | | | 500 | μA |
| C _{ic} Control input capacitance | | 5 V | | 3.5 | | pF |
| C _{io(off)} Switch input/output capacitance | | 5 V | | 6 | | pF |
| C _{io(on)} Switch input/output capacitance | | 5 V | | 14 | | pF |

(1) T_A = 25°C

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | UNIT |
|---------------------------------|--------------|-------------|----------------------------------|------|---------------------------------|-----|---------------------------------|-----|-------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{en} ⁽¹⁾ | C | A or B | 2.3 | 12 | 1.6 | 7.5 | 1.5 | 6.4 | 1.3 | 5.9 | ns |
| t _{dis} ⁽²⁾ | C | A or B | 2.2 | 12.5 | 1.2 | 7.9 | 2 | 9.2 | 1.1 | 8.3 | ns |

(1) t_{PZL} and t_{PZH} are the same as t_{en}.

(2) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

ANALOG SWITCH CHARACTERISTICS

 $T_A = 25^\circ\text{C}$

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|---|--------------|-------------|---|-----------------|-------|------|
| Frequency response (switch on) | A or B | B or A | $C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = \text{sine wave}$ (see Figure 6) | 1.65 V | 35 | MHz |
| | | | | 2.3 V | 120 | |
| | | | | 3 V | 175 | |
| | | | | 4.5 V | 195 | |
| | | | $C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f_{in} = \text{sine wave}$ (see Figure 6) | 1.65 V | >300 | |
| | | | | 2.3 V | >300 | |
| | | | | 3 V | >300 | |
| | | | | 4.5 V | >300 | |
| Crosstalk ⁽¹⁾ (between switches) | A or B | B or A | $C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 7) | 1.65 V | -58 | dB |
| | | | | 2.3 V | -58 | |
| | | | | 3 V | -58 | |
| | | | | 4.5 V | -58 | |
| | | | $C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 7) | 1.65 V | -42 | |
| | | | | 2.3 V | -42 | |
| | | | | 3 V | -42 | |
| | | | | 4.5 V | -42 | |
| Crosstalk (control input to signal output) | C | A or B | $C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (square wave) (see Figure 8) | 1.65 V | 35 | mV |
| | | | | 2.3 V | 50 | |
| | | | | 3 V | 70 | |
| | | | | 4.5 V | 100 | |
| Feedthrough attenuation (switch off) | A or B | B or A | $C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 9) | 1.65 V | -58 | dB |
| | | | | 2.3 V | -58 | |
| | | | | 3 V | -58 | |
| | | | | 4.5 V | -58 | |
| | | | $C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 9) | 1.65 V | -42 | |
| | | | | 2.3 V | -42 | |
| | | | | 3 V | -42 | |
| | | | | 4.5 V | -42 | |
| Sine-wave distortion | A or B | B or A | $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $f_{in} = 1\text{ kHz}$ (sine wave) (see Figure 10) | 1.65 V | 0.1 | % |
| | | | | 2.3 V | 0.025 | |
| | | | | 3 V | 0.015 | |
| | | | | 4.5 V | 0.01 | |
| | | | $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $f_{in} = 10\text{ kHz}$ (sine wave) (see Figure 10) | 1.65 V | 0.15 | |
| | | | | 2.3 V | 0.025 | |
| | | | | 3 V | 0.015 | |
| | | | | 4.5 V | 0.01 | |

 (1) Adjust f_{in} voltage to obtain 0 dBm at input.

OPERATING CHARACTERISTICS

 $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | V _{CC} = 5 V | UNIT |
|---|-----------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
| | | TYP | TYP | TYP | TYP | |
| C _{pd} Power-dissipation capacitance | f = 10 MHz | 8 | 9 | 9.5 | 11 | pF |

PARAMETER MEASUREMENT INFORMATION

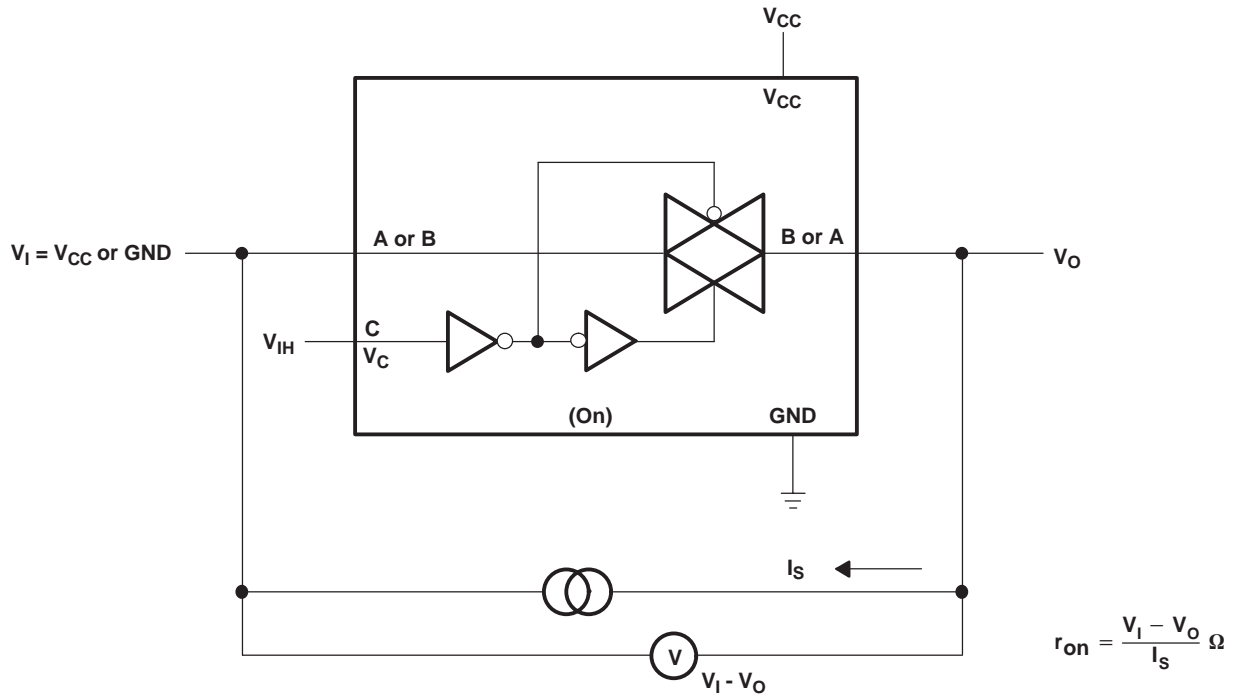


Figure 1. On-State Resistance Test Circuit

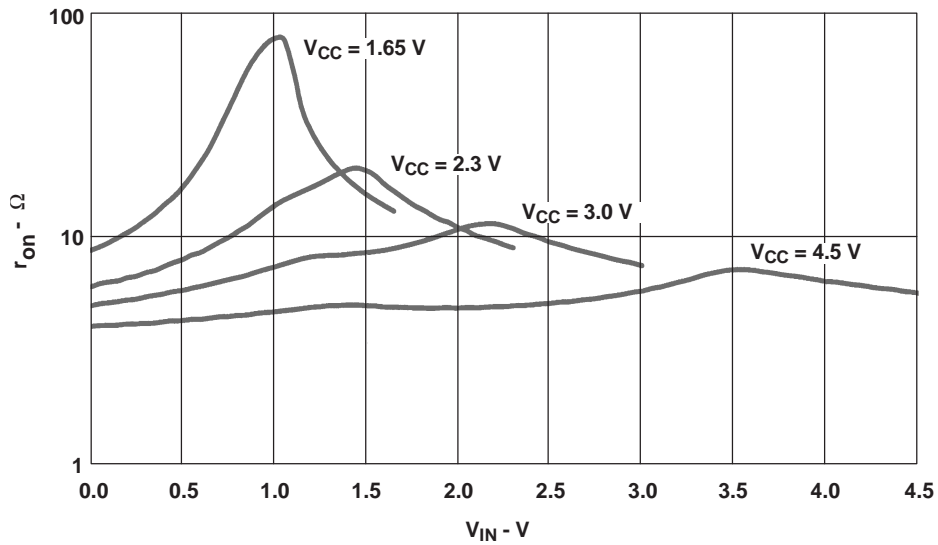


Figure 2. Typical r_{on} as a Function of Input Voltage (V_I) for $V_I = 0$ to V_{CC}

PARAMETER MEASUREMENT INFORMATION (continued)

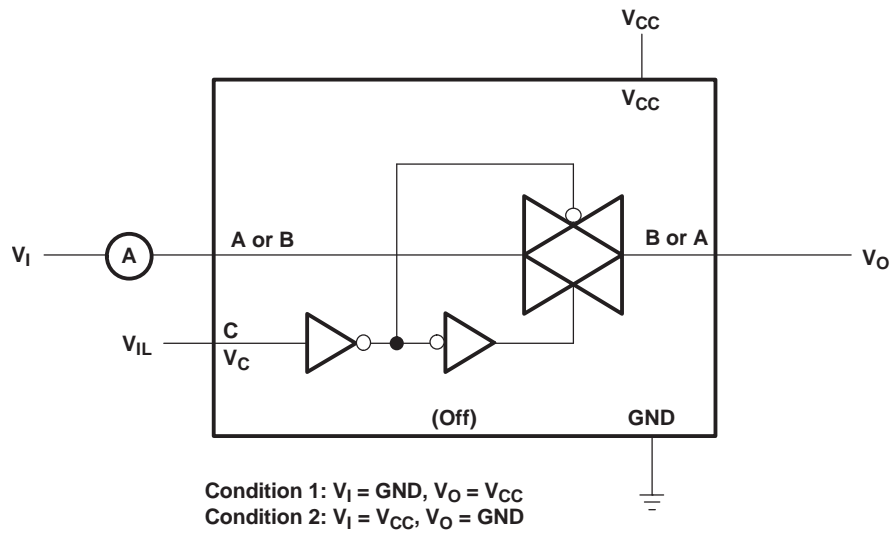


Figure 3. Off-State Switch Leakage-Current Test Circuit

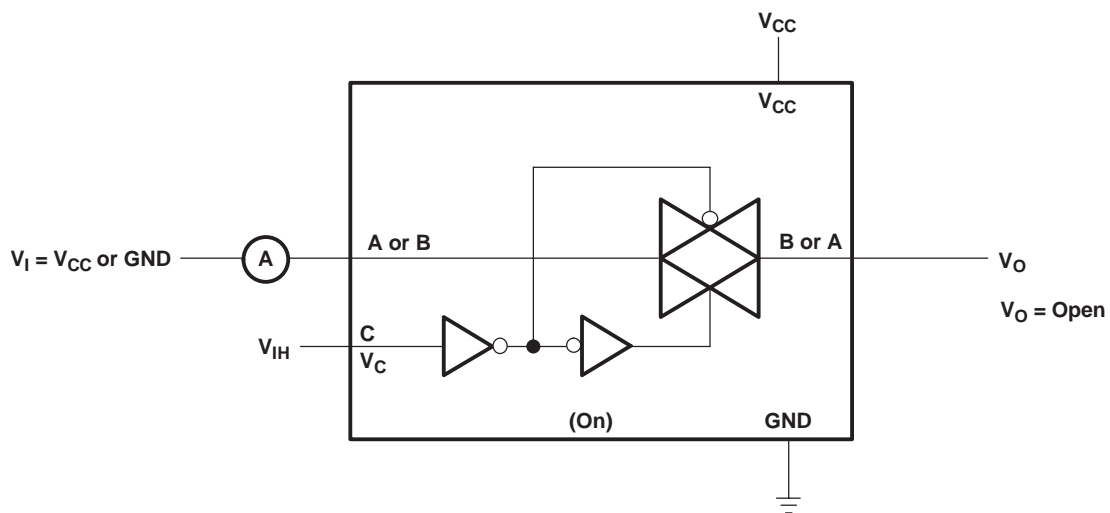
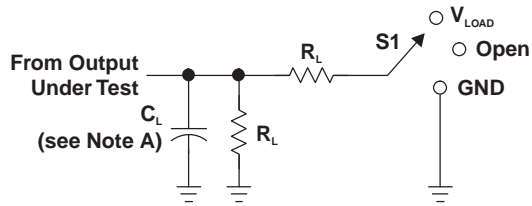


Figure 4. On-State Leakage-Current Test Circuit

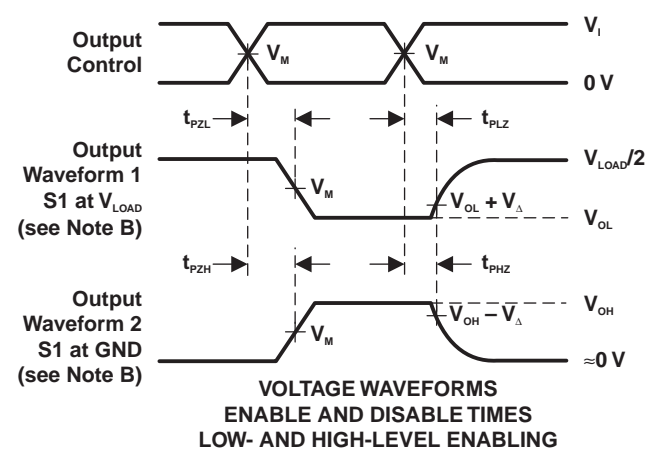
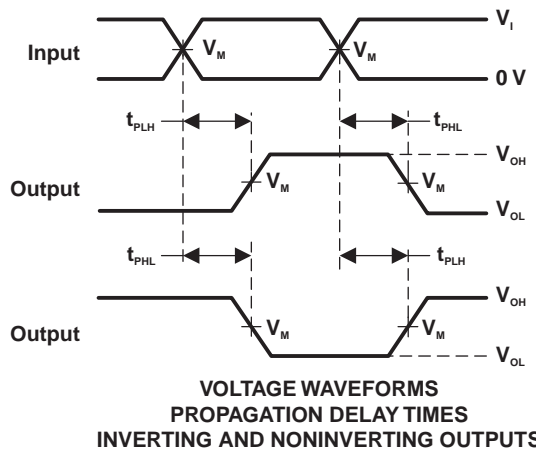
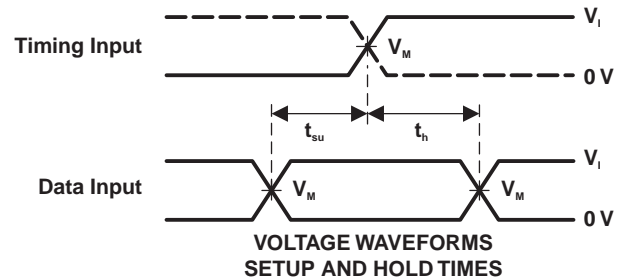
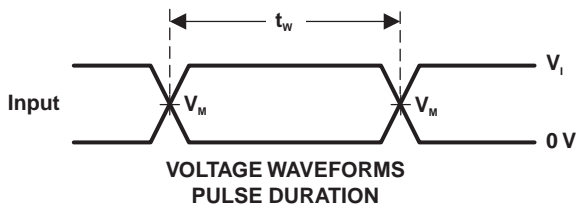
PARAMETER MEASUREMENT INFORMATION (continued)



LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_i | t_f/t_r | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators have the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

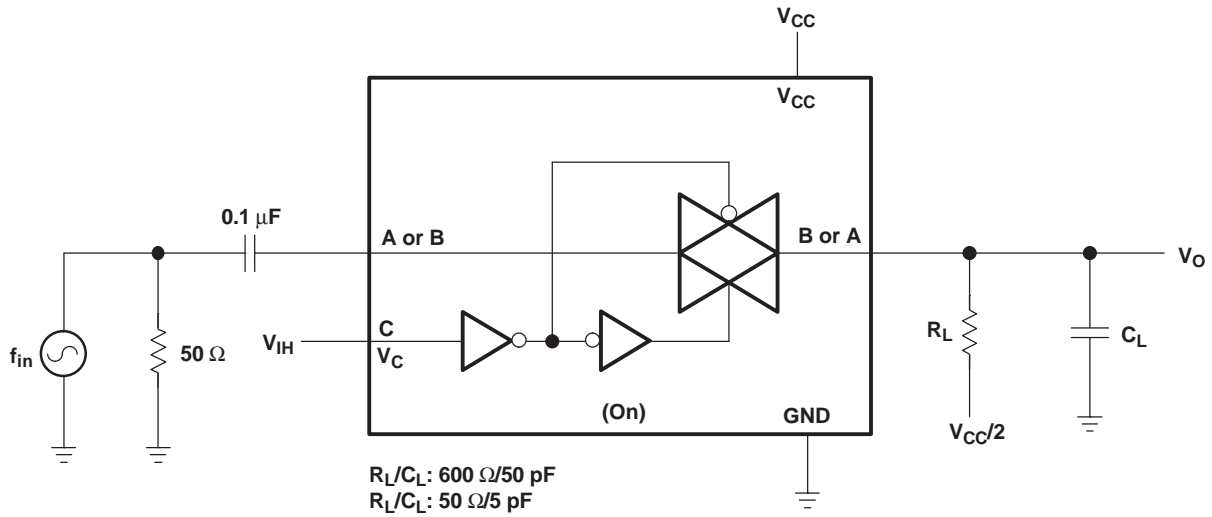


Figure 6. Frequency Response (Switch On)

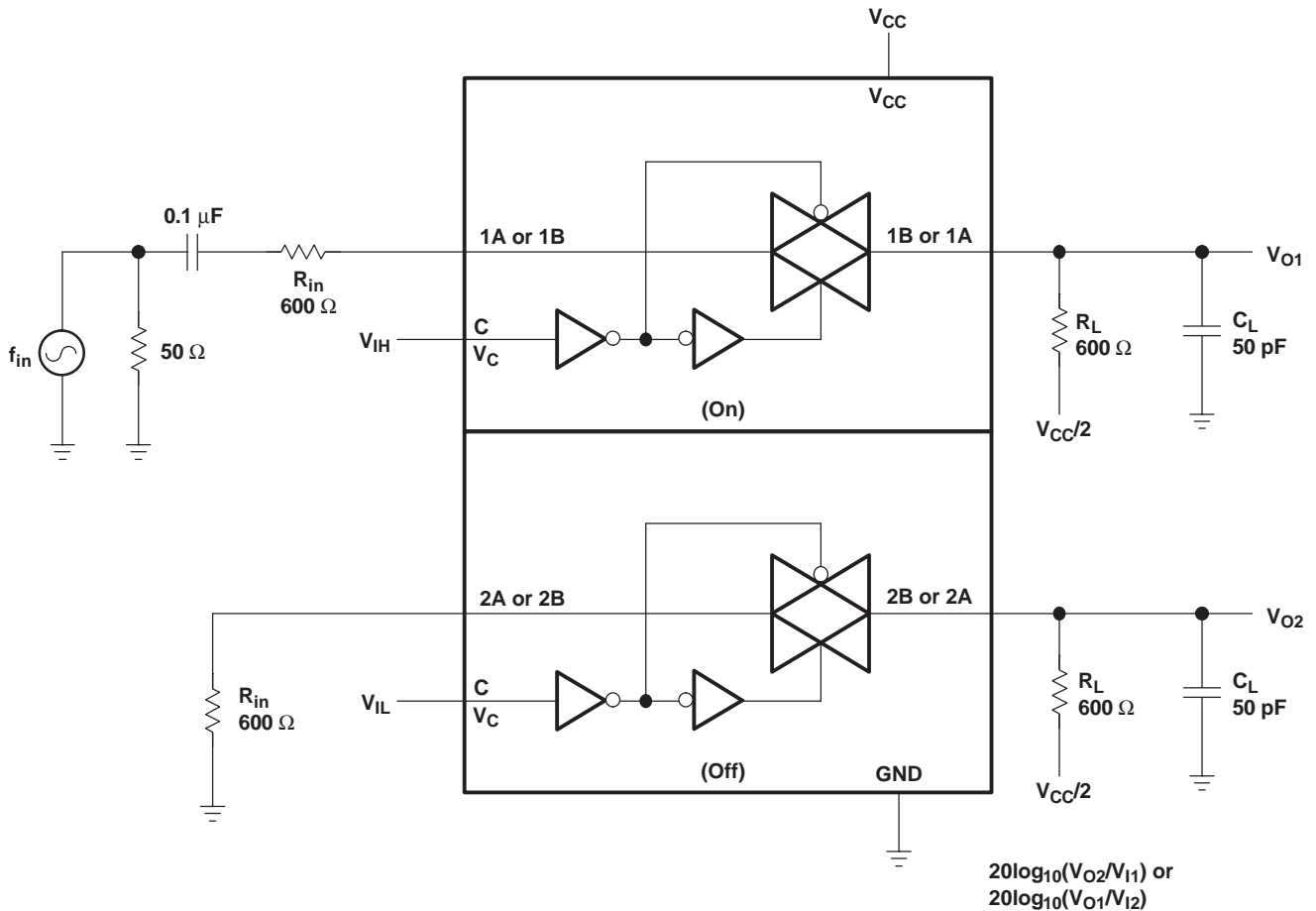


Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION (continued)

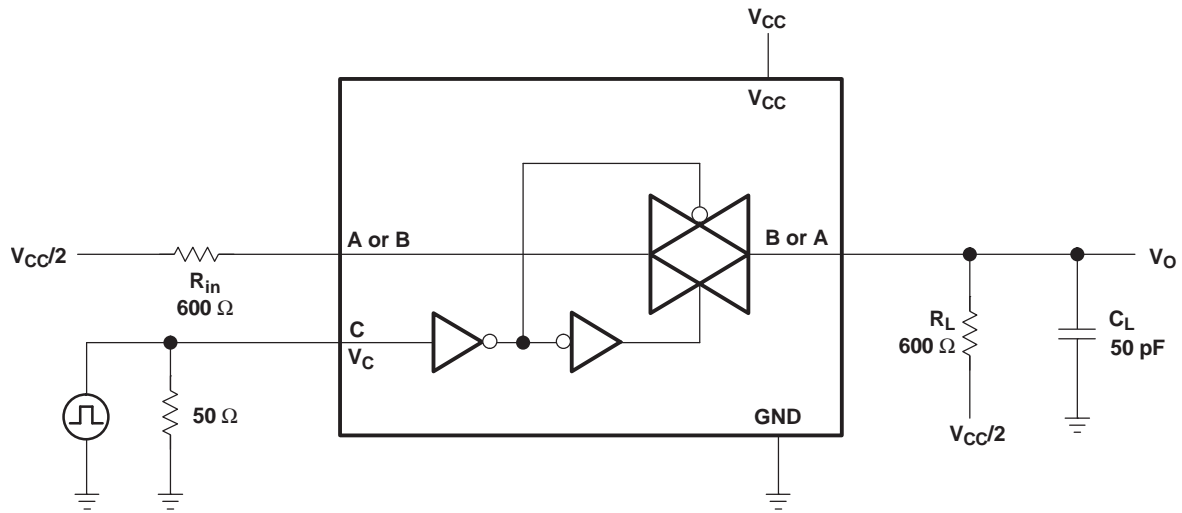


Figure 8. Crosstalk (Control Input, Switch Output)

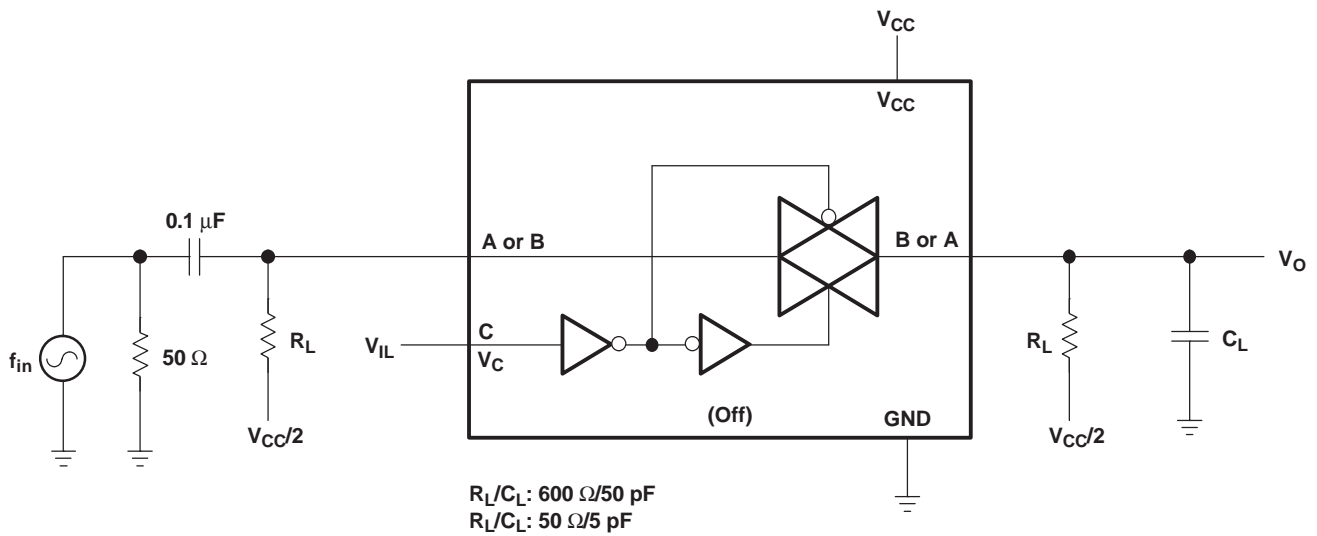


Figure 9. Feedthrough (Switch Off)

PARAMETER MEASUREMENT INFORMATION (continued)

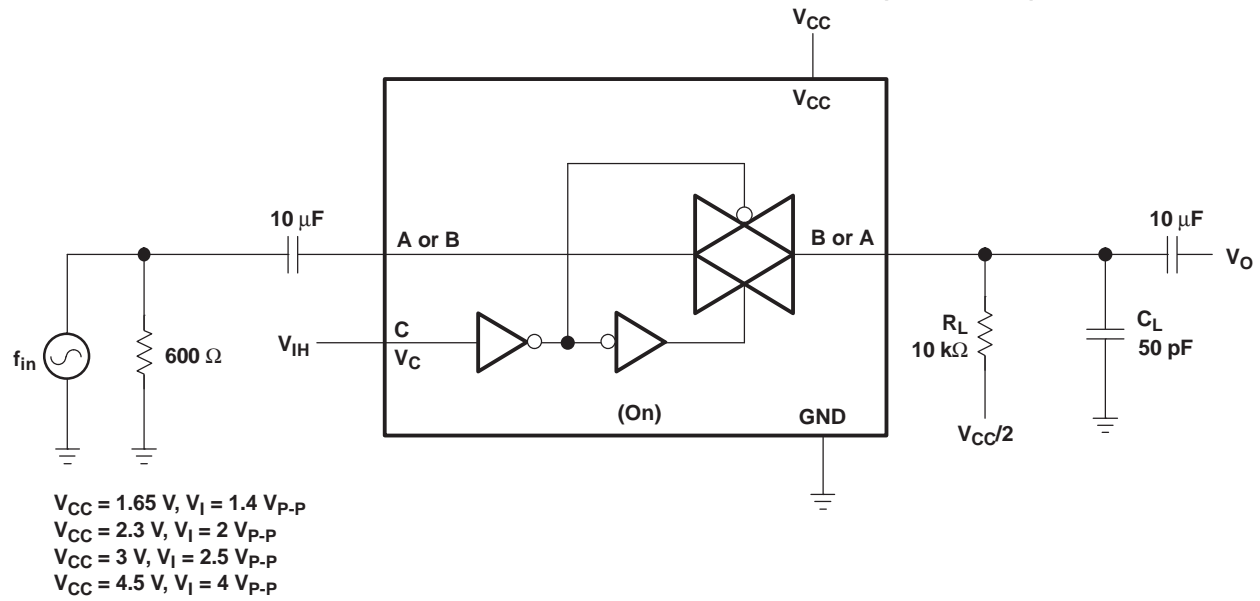


Figure 10. Sine-Wave Distortion

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| SN74LVC2G66QDCURQ1 | ACTIVE | VSSOP | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAYR | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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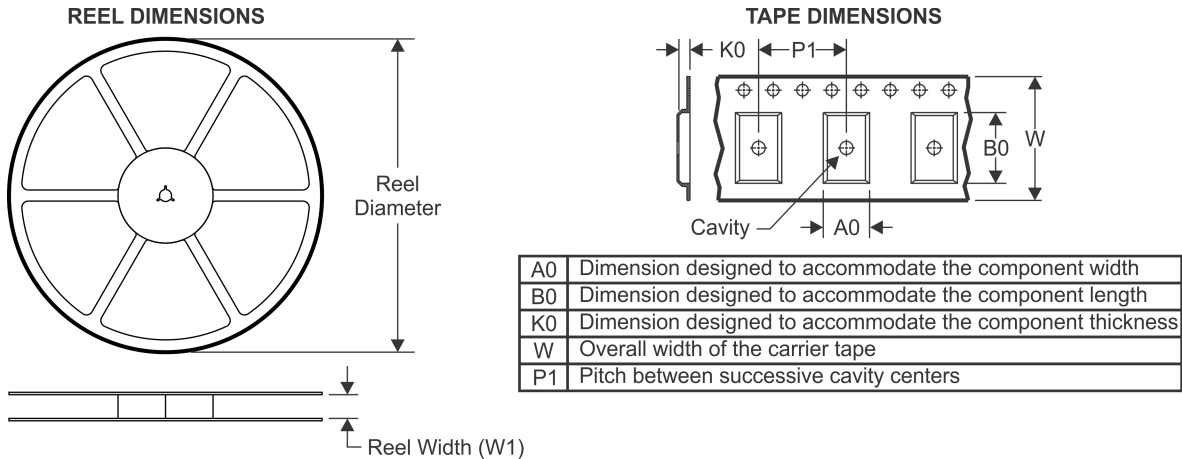
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OTHER QUALIFIED VERSIONS OF SN74LVC2G66-Q1 :

- Catalog: [SN74LVC2G66](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC2G66QDCURQ1 | VSSOP | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS

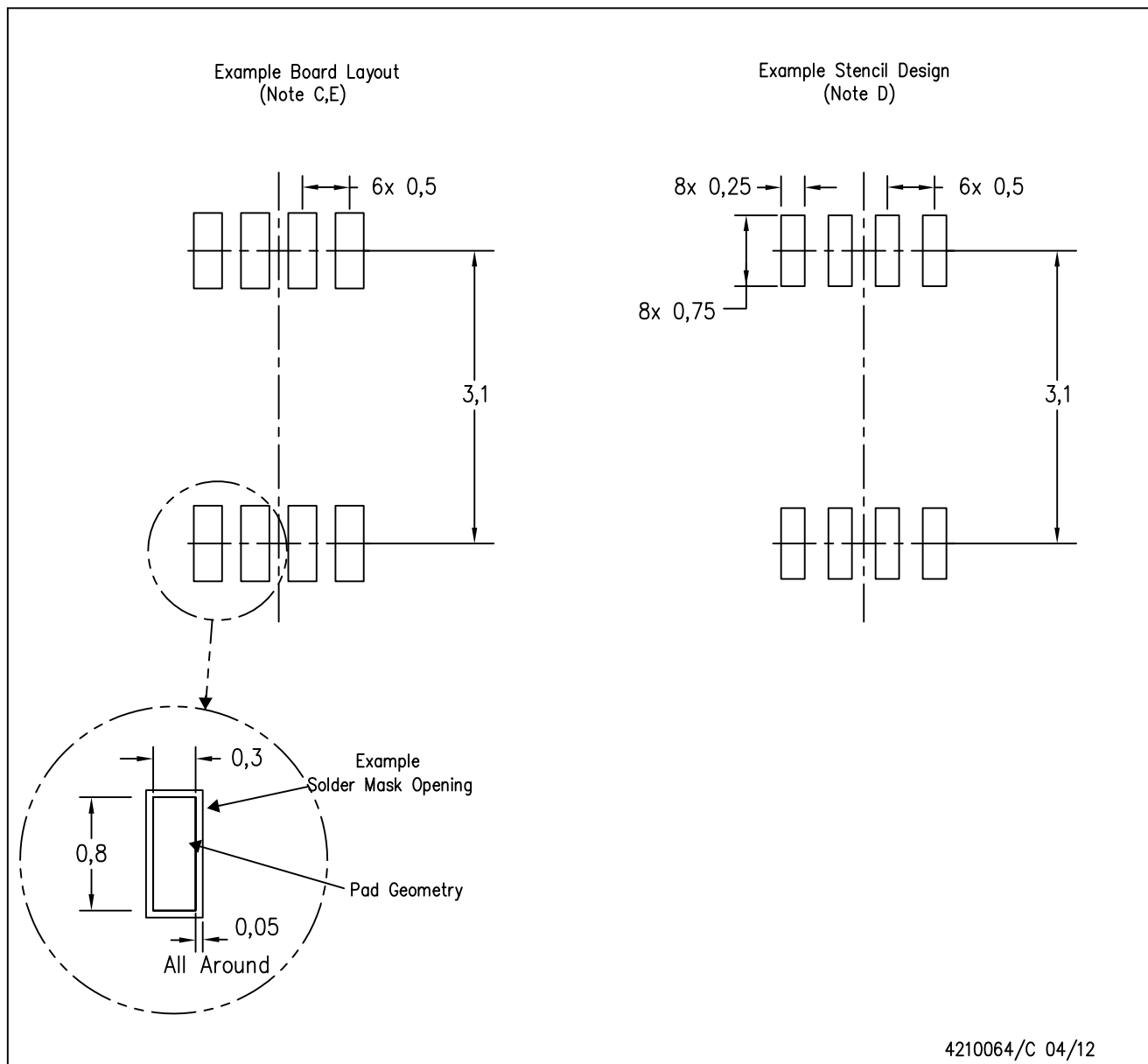


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC2G66QDCURQ1 | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



4210064/C 04/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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