



# THE DATASHEET OF AD7699BCPZ

### FEATURES

- 16-bit resolution with no missing codes
- 8-channel multiplexer with choice of inputs
  - Unipolar single-ended
  - Differential (GND sense)
  - Pseudo bipolar
- Throughput: 500 kSPS
- INL:  $\pm 0.5$  LSB typical,  $\pm 1.5$  LSB maximum ( $\pm 23$  ppm or FSR)
- Dynamic range: 93.3 dB
- SINAD: 91.5 dB at 20 kHz
- THD:  $-97$  dB at 20 kHz
- Analog input range: 0 V to  $V_{REF}$  with  $V_{REF}$  up to VDD
- Multiple reference types
  - Internal 4.096 V
  - External buffered (up to 4.096 V)
  - External (up to VDD)
- Internal temperature sensor
- Channel sequencer, selectable 1-pole filter, busy indicator
- No pipeline delay, SAR architecture
- Single-supply 5 V operation with
  - 1.8 V to 5 V logic interface
- Serial interface compatible with SPI, MICROWIRE, QSPI, and DSP
- Power dissipation
  - 26 mW at 500 kSPS
  - 5.2  $\mu$ W at 100 SPS
- Standby current: 50 nA
- 20-lead 4 mm  $\times$  4 mm LFCSP package
- 20-lead 2.4 mm  $\times$  2.4 mm WLCSP package

### APPLICATIONS

- Battery-powered equipment
- Medical instruments: ECG/EKG
- Mobile communications: GPS
- Personal digital assistants
- Power line monitoring
- Data acquisition
- Seismic data acquisition systems
- Instrumentation
- Process control

### FUNCTIONAL BLOCK DIAGRAM

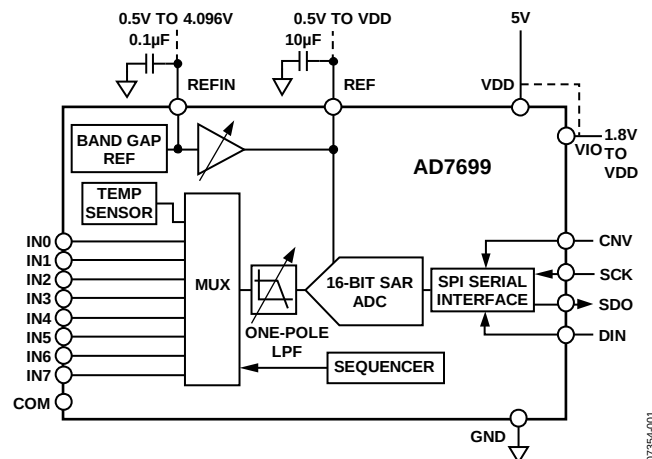


Figure 1.

Table 1. Multichannel 14-/16-Bit PuLSAR® ADC

| Type   | Channels | 250 kSPS               | 500 kSPS               | ADC Driver                |
|--------|----------|------------------------|------------------------|---------------------------|
| 14-Bit | 8        | <a href="#">AD7949</a> |                        | <a href="#">ADA4841-1</a> |
| 16-Bit | 4        | <a href="#">AD7682</a> |                        | <a href="#">ADA4841-1</a> |
| 16-Bit | 8        | <a href="#">AD7689</a> | <a href="#">AD7699</a> | <a href="#">ADA4841-1</a> |

### GENERAL DESCRIPTION

The [AD7699](#) is an 8-channel, 16-bit, charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC) that operates from a single power supply, VDD.

The [AD7699](#) contains all components for use in a multichannel, low power data acquisition system, including a true 16-bit SAR ADC with no missing codes; an 8-channel low crosstalk multiplexer useful for configuring the inputs as single-ended (with or without ground sense), differential, or bipolar; an internal 4.096 V low drift reference and buffer; a temperature sensor; a selectable one-pole filter; and a sequencer that is useful when channels are continuously scanned in order.

The [AD7699](#) uses a simple serial port interface (SPI) for writing to the configuration register and receiving conversion results. The SPI interface uses a separate supply, VIO, which is set to the host logic level. Power dissipation scales with throughput.

The [AD7699](#) is housed in a tiny 20-lead LFCSP and a 20-ball WLCSP with operation specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

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**REVISION HISTORY****7/2018—Rev. F to Rev. G**

|                                               |    |
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**3/2017—Rev. E to Rev. F**

|                                                                           |           |
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| Added CB-20-12 Package.....                                               | Universal |
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**9/2015—Rev. D to Rev. E**

|                                                                                                                                                                                                                                                               |            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| Changed ADSP-BF53x to ADSP-BF531/ADSP-BF532/<br>ADSP-BF533/ADSP-BF535/ADSP-BF536/ADSP-BF537/<br>ADSP-BF538/ADSP-BF539; Changed ADSP-219x to<br>ADSP-2191M/ADSP-2196M, and Changed ADSP-218x to<br>ADSP-2181/ADSP-2183/ADSP-2185/ADSP-2186/<br>ADSP-2189N..... | Throughout |
| Moved General Timing with a Busy Indicator Section and<br>Figure 36 .....                                                                                                                                                                                     | 24         |
| Added Channel Sequencer Section, Examples Section, and<br>Figure 41; Renumbered Sequentially .....                                                                                                                                                            | 27         |

**5/2015—Rev. C to Rev. D**

|                                                                                                                                            |            |
|--------------------------------------------------------------------------------------------------------------------------------------------|------------|
| Changed ADA4841-x to ADA4841-1, ADR43x to ADR430/<br>ADR431/ADR433/ADR434/ADR435, and AD44x to ADR440/<br>ADR441/ADR443/ADR444/ADR445..... | Throughout |
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**9/2011—Rev. 0 to Rev. A**

|                                                                                                                                        |    |
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**10/2008—Revision 0: Initial Version**

## SPECIFICATIONS

VDD = 4.5 V to 5.5 V, VREF = 4.096 to VDD, VIO = 1.8 V to VDD, all specifications TMIN to TMAX, unless otherwise noted.

Table 2.

| Parameter                                            | Test Conditions/Comments                   | Min          | Typ    | Max          | Unit             |
|------------------------------------------------------|--------------------------------------------|--------------|--------|--------------|------------------|
| RESOLUTION                                           |                                            | 16           |        |              | Bits             |
| ANALOG INPUT                                         |                                            |              |        |              |                  |
| Voltage Range                                        | Unipolar mode                              | 0            |        | +VREF        | V                |
|                                                      | Bipolar mode                               | −VREF/2      |        | +VREF/2      | V                |
| Absolute Input Voltage                               | Positive input, unipolar and bipolar modes | −0.1         |        | VREF + 0.1   | V                |
|                                                      | Negative or COM input, unipolar mode       | −0.1         |        | +0.1         | V                |
|                                                      | Negative or COM input, bipolar mode        | VREF/2 − 0.1 | VREF/2 | VREF/2 + 0.1 | V                |
| Analog Input CMRR                                    | fIN = 250 kHz                              |              | 68     |              | dB               |
| Leakage Current at 25°C Input Impedance <sup>1</sup> | Acquisition phase                          |              | 1      |              | nA               |
| THROUGHPUT                                           |                                            |              |        |              |                  |
| Conversion Rate                                      |                                            |              |        |              |                  |
| Full Bandwidth <sup>2</sup>                          |                                            | 0            |        | 500          | kSPS             |
| ¼ Bandwidth <sup>2</sup>                             |                                            | 0            |        | 125          | kSPS             |
| Transient Response                                   | Full-scale step, full bandwidth            |              |        | 400          | ns               |
|                                                      | Full-scale step, ¼ bandwidth               |              |        | 1600         | ns               |
| ACCURACY                                             |                                            |              |        |              |                  |
| No Missing Codes                                     |                                            | 16           |        |              | Bits             |
| Integral Linearity Error                             |                                            |              |        |              |                  |
| LFCSP                                                |                                            | −1.5         | ±0.5   | +1.5         | LSB <sup>3</sup> |
| WLCSP                                                |                                            | −2.5         | ±0.5   | +2.5         | LSB <sup>3</sup> |
| Differential Linearity Error                         |                                            | −1           | ±0.25  | +1.5         | LSB              |
| Transition Noise                                     |                                            |              | 0.5    |              | LSB              |
| Gain Error <sup>4</sup>                              |                                            | −10          | ±1     | +10          | LSB              |
| Gain Error Match                                     |                                            |              |        |              |                  |
| LFCSP                                                |                                            | −3           | ±1     | +3           | LSB              |
| WLCSP                                                |                                            | −5           | ±1     | +5           | LSB              |
| Gain Error Temperature Drift                         |                                            |              | ±0.3   |              | ppm/°C           |
| Offset Error <sup>4</sup>                            |                                            |              |        |              |                  |
| LFCSP                                                |                                            | −10          | ±1     | +10          | LSB              |
| WLCSP                                                |                                            | −12          | ±1     | +12          | LSB              |
| Offset Error Match                                   |                                            |              |        |              |                  |
| LFCSP                                                |                                            | −3           | ±1     | +3           | LSB              |
| WLCSP                                                |                                            | −11          | ±1     | +11          | LSB              |
| Offset Error Temperature Drift                       |                                            |              | ±0.3   |              | ppm/°C           |
| Power Supply Sensitivity                             |                                            |              | ±1.5   |              | LSB              |
| AC Accuracy                                          |                                            |              |        |              |                  |
| Dynamic Range                                        |                                            |              | 93.3   |              | dB <sup>5</sup>  |
| Signal-to-Noise                                      |                                            |              |        |              |                  |
| LFCSP                                                | fIN = 20 kHz, VREF = 5 V                   | 92           | 92.5   |              | dB               |
| WLCSP                                                | fIN = 20 kHz, VREF = 5 V                   | 90           | 92.5   |              | dB               |
| LFCSP                                                | fIN = 20 kHz, VREF = 4.096 V internal REF  | 89.5         | 91.5   |              | dB               |
| WLCSP                                                | fIN = 20 kHz, VREF = 4.096 V internal REF  | 89           | 91.5   |              | dB               |
| SINAD                                                |                                            |              |        |              |                  |
| LFCSP                                                | fIN = 20 kHz, VREF = 5 V                   | 90           | 91.5   |              | dB               |
| WLCSP                                                | fIN = 20 kHz, VREF = 5 V                   | 89           | 91.5   |              | dB               |
|                                                      | fIN = 20 kHz, VREF = 5 V, −60 dB input     |              | 33.5   |              | dB               |
| LFCSP                                                | fIN = 20 kHz, VREF = 4.096 V internal REF  | 89           | 90.5   |              | dB               |
| WLCSP                                                | fIN = 20 kHz, VREF = 4.096 V internal REF  | 88           | 90.5   |              | dB               |

| Parameter                         | Test Conditions/Comments                               | Min       | Typ   | Max        | Unit   |
|-----------------------------------|--------------------------------------------------------|-----------|-------|------------|--------|
| Total Harmonic Distortion         | $f_{IN} = 20 \text{ kHz}$                              |           | −97   |            | dB     |
| Spurious-Free Dynamic Range       | $f_{IN} = 20 \text{ kHz}$                              |           | 112   |            | dB     |
| Channel-to-Channel Crosstalk      | $f_{IN} = 100 \text{ kHz}$ on adjacent channel(s)      |           | −125  |            | dB     |
| SAMPLING DYNAMICS                 |                                                        |           |       |            |        |
| −3 dB Input Bandwidth             | Full bandwidth                                         |           | 14    |            | MHz    |
|                                   | ¼ bandwidth                                            |           | 3.6   |            | MHz    |
| Aperture Delay                    | VDD = 5 V                                              |           | 2.5   |            | ns     |
| INTERNAL REFERENCE                |                                                        |           |       |            |        |
| REF Output Voltage                | At 25°C                                                | 4.086     | 4.096 | 4.106      | V      |
| REFIN Output Voltage <sup>6</sup> | At 25°C                                                |           | 2.3   |            | V      |
| REF Output Current                |                                                        |           | ±300  |            | µA     |
| Temperature Drift                 |                                                        |           | ±10   |            | ppm/°C |
| Line Regulation                   | VDD = 5 V ± 5%                                         |           | ±15   |            | ppm/V  |
| Long-Term Drift                   | 1000 hours                                             |           | 50    |            | ppm    |
| Turn-On Settling Time             | CREF = 10 µF                                           |           | 5     |            | ms     |
| EXTERNAL REFERENCE                |                                                        |           |       |            |        |
| Voltage Range                     | REF input                                              | 0.5       |       | VDD + 0.3  | V      |
|                                   | REFIN input (buffered)                                 | 0.5       |       | VDD − 0.2  | V      |
| Current Drain                     | 500 kSPS, REF = 5 V                                    |           | 100   |            | µA     |
| TEMPERATURE SENSOR                |                                                        |           |       |            |        |
| Output Voltage <sup>7</sup>       | At 25°C                                                |           | 283   |            | mV     |
| Temperature Sensitivity           |                                                        |           | 1     |            | mV/°C  |
| DIGITAL INPUTS                    |                                                        |           |       |            |        |
| Logic Levels                      |                                                        |           |       |            |        |
| V <sub>IL</sub>                   |                                                        | −0.3      |       | +0.3 × VIO | V      |
| V <sub>IH</sub>                   |                                                        | 0.7 × VIO |       | VIO + 0.3  | V      |
| I <sub>IL</sub>                   |                                                        | −1        |       | +1         | µA     |
| I <sub>IH</sub>                   |                                                        | −1        |       | +1         | µA     |
| DIGITAL OUTPUTS                   |                                                        |           |       |            |        |
| Data Format <sup>8</sup>          |                                                        |           |       |            |        |
| Pipeline Delay <sup>9</sup>       |                                                        |           |       |            |        |
| V <sub>OL</sub>                   | I <sub>SINK</sub> = +500 µA                            |           |       | 0.4        | V      |
| V <sub>OH</sub>                   | I <sub>SOURCE</sub> = −500 µA                          | VIO − 0.3 |       |            | V      |
| POWER SUPPLIES                    |                                                        |           |       |            |        |
| VDD                               | Specified performance                                  | 4.5       |       | 5.5        | V      |
| VIO                               | Specified performance                                  | 1.8       |       | VDD + 0.3  | V      |
| Standby Current <sup>10, 11</sup> | VDD and VIO = 5 V, at 25°C                             |           | 50    |            | nA     |
| Power Dissipation                 | VDD = 5 V, 100 kSPS throughput                         |           | 5.2   |            | µW     |
|                                   | VDD = 5 V, 500 kSPS throughput                         |           | 26    | 29         | mW     |
|                                   | VDD = 5 V, 500 kSPS throughput with internal reference |           | 28    | 32         | mW     |
| Energy per Conversion             |                                                        |           | 52    |            | nJ     |
| TEMPERATURE RANGE                 |                                                        |           |       |            |        |
| Specified Performance             | T <sub>MIN</sub> to T <sub>MAX</sub>                   | −40       |       | +85        | °C     |

<sup>1</sup> See the Analog Inputs section.

<sup>2</sup> The bandwidth is set with the configuration register.

<sup>3</sup> LSB means least significant bit. With the 5 V input range, one LSB = 76.3 µV.

<sup>4</sup> See the Terminology section. These specifications include full temperature range variation but not the error contribution from the reference.

<sup>5</sup> All specifications expressed in decibels are referred to a full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

<sup>6</sup> This is the output from the internal band gap.

<sup>7</sup> The output voltage is internal and present on a dedicated multiplexer input.

<sup>8</sup> Unipolar mode: serial 16-bit straight binary.

Bipolar mode: serial 16-bit twos complement.

<sup>9</sup> Conversion results available immediately after completed conversion.

<sup>10</sup> With all digital inputs forced to VIO or GND as required.

<sup>11</sup> During acquisition phase.

## TIMING SPECIFICATIONS

VDD = 4.5 V to 5.5 V, V<sub>REF</sub> = 4.096 to VDD, VIO = 1.8 V to VDD, all specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.

Table 3.

| Parameter <sup>1</sup>                                  | Symbol             | Min                   | Typ | Max   | Unit |
|---------------------------------------------------------|--------------------|-----------------------|-----|-------|------|
| Conversion Time: CNV Rising Edge to Data Available      | t <sub>CONV</sub>  |                       |     |       |      |
| LFCSP                                                   |                    |                       |     | 1.6   | μs   |
| WLCSP                                                   |                    |                       |     | 1.675 | μs   |
| Acquisition Time                                        | t <sub>ACQ</sub>   |                       |     |       |      |
| LFCSP                                                   |                    | 400                   |     |       | ns   |
| WLCSP                                                   |                    | 325                   |     |       | ns   |
| Time Between Conversions <sup>2</sup>                   | t <sub>CYC</sub>   | 2                     |     |       | μs   |
| CNV Pulse Width                                         | t <sub>CNVH</sub>  | 10                    |     |       | ns   |
| Data Write/Read During Conversion                       | t <sub>DATA</sub>  |                       |     | 1.2   | μs   |
| SCK Period                                              | t <sub>SCK</sub>   | t <sub>DSDO</sub> + 2 |     |       | ns   |
| SCK Low Time                                            | t <sub>SCKL</sub>  | 11                    |     |       | ns   |
| SCK High Time                                           | t <sub>SCKH</sub>  | 11                    |     |       | ns   |
| SCK Falling Edge to Data Remains Valid                  | t <sub>HSDO</sub>  | 4                     |     |       | ns   |
| SCK Falling Edge to Data Valid Delay                    | t <sub>DSDO</sub>  |                       |     |       |      |
| VIO Above 4.5 V                                         |                    |                       |     | 16    | ns   |
| VIO Above 3 V                                           |                    |                       |     | 17    | ns   |
| VIO Above 2.7 V                                         |                    |                       |     | 18    | ns   |
| VIO Above 2.3 V                                         |                    |                       |     | 21    | ns   |
| VIO Above 1.8 V                                         |                    |                       |     | 28    | ns   |
| CNV Low to SDO D15 MSB Valid                            | t <sub>EN</sub>    |                       |     |       |      |
| VIO Above 4.5 V                                         |                    |                       |     | 15    | ns   |
| VIO Above 3 V                                           |                    |                       |     | 17    | ns   |
| VIO Above 2.7 V                                         |                    |                       |     | 18    | ns   |
| VIO Above 2.3 V                                         |                    |                       |     | 22    | ns   |
| VIO Above 1.8 V                                         |                    |                       |     | 25    | ns   |
| CNV High or Last SCK Falling Edge to SDO High Impedance | t <sub>DIS</sub>   |                       |     | 32    | ns   |
| CNV Low to SCK Rising Edge                              | t <sub>CLSCK</sub> | 10                    |     |       | ns   |
| Last SCK Falling Edge to CNV Rising Edge Delay          | t <sub>QUIET</sub> | 40                    |     |       | ns   |
| DIN Valid Setup Time from SCK Rising Edge               | t <sub>SDIN</sub>  | 5                     |     |       | ns   |
| DIN Valid Hold Time from SCK Rising Edge                | t <sub>HDIN</sub>  | 5                     |     |       | ns   |

<sup>1</sup> See Figure 2 and Figure 3 for load conditions.

<sup>2</sup> For the WLCSP, a full throughput of 500kSPS can only be achieved using read during conversion or read spanning conversion mode.

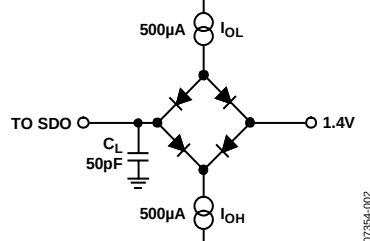
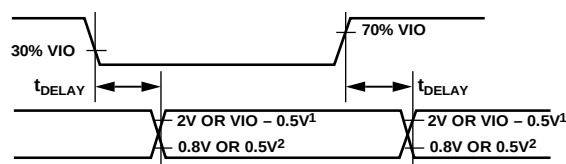


Figure 2. Load Circuit for Digital Interface Timing



<sup>1</sup> 2V IF VIO ABOVE 2.5V, VIO - 0.5V IF VIO BELOW 2.5V.

<sup>2</sup> 0.8V IF VIO ABOVE 2.5V, 0.5V IF VIO BELOW 2.5V.

Figure 3. Voltage Levels for Timing

## ABSOLUTE MAXIMUM RATINGS

Table 4.

| Parameter                                           | Rating                                        |
|-----------------------------------------------------|-----------------------------------------------|
| Analog Inputs<br>INx, <sup>1</sup> COM <sup>1</sup> | GND – 0.3 V to VDD + 0.3 V<br>or VDD ± 130 mA |
| REF, REFIN                                          | GND – 0.3 V to VDD + 0.3 V                    |
| Supply Voltages<br>VDD, VIO to GND                  | –0.3 V to +7 V                                |
| VDD to VIO                                          | ±7 V                                          |
| DIN, CNV, SCK to GND                                | –0.3 V to VIO + 0.3 V                         |
| SDO to GND                                          | –0.3 V to VIO + 0.3 V                         |
| Storage Temperature Range                           | –65°C to +150°C                               |
| Junction Temperature                                | 150°C                                         |
| ESD Ratings                                         |                                               |
| Human Body Model                                    | 1500 V                                        |
| Machine Model                                       | 200 V                                         |
| Field-Induced Charged Device Model                  | 1500 V                                        |

<sup>1</sup> See the Analog Inputs section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 5. Thermal Resistance

| Package Type          | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|-----------------------|---------------|---------------|------|
| CP-20-10 <sup>1</sup> | 47.6          | 4.4           | °C/W |
| CB-20-12 <sup>1</sup> | 46.8          | 0.7           | °C/W |

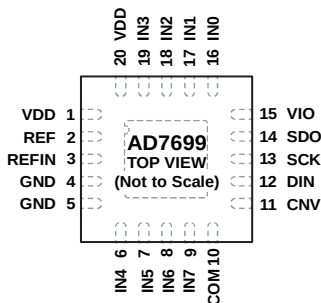
<sup>1</sup> Test Condition 1: thermal impedance simulated values are based upon use of 2S2P JEDEC PCB. See the Ordering Guide.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. THE EXPOSED PAD IS NOT CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SYSTEM GROUND PLANE.

07854-004

Figure 4. 20-Lead LFCSP Pin Configuration

Table 6. 20-Lead LFCSP Pin Function Descriptions

| Pin No.               | Mnemonic                            | Type <sup>1</sup> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----------------------|-------------------------------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 20                 | VDD                                 | P                 | Power Supply. Nominally 4.5 to 5.5 V and must be decoupled with 10 $\mu$ F and 100 nF capacitors.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 2                     | REF                                 | AI/O              | Reference Input/Output. See the Voltage Reference Output/Input section. When the internal reference is enabled, this pin produces 4.096 V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered version of the voltage present on the REFIN pin (VDD – 0.5 V maximum) useful when using low cost, low power references. For improved drift performance, connect a precision reference to REF (0.5 V to VDD). For any reference method, this pin needs decoupling with an external 10 $\mu$ F capacitor connected as close to REF as possible. See the Reference Decoupling section. |
| 3                     | REFIN                               | AI/O              | Internal Reference Output/Reference Buffer Input. See the Voltage Reference Output/Input section. When using the internal reference, the internal unbuffered reference voltage is present and needs decoupling with a 0.1 $\mu$ F capacitor. When using the internal reference buffer, apply a source between 0.5 V and 4.096 V that is buffered to the REF pin as previously described.                                                                                                                                                                                                                                  |
| 4, 5                  | GND                                 | P                 | Power Supply Ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 6 to 9                | IN4 to IN7                          | AI                | Analog Input Channel 4, Analog Input Channel 5, Analog Input Channel 6, and Analog Input Channel 7.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 10                    | COM                                 | AI                | Common Channel Input. All input channels, IN[7:0], can be referenced to a common-mode point of 0 V or $V_{REF}/2$ V.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 11                    | CNV                                 | DI                | Conversion Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held high, the busy indicator is enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 12                    | DIN                                 | DI                | Data Input. This input is used for writing to the 14-bit configuration register. The configuration register can be written to during and after conversion.                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 13                    | SCK                                 | DI                | Serial Data Clock Input. This input clocks out the data on SDO and clock in data on DIN in an MSB first fashion.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 14                    | SDO                                 | DO                | Serial Data Output. The conversion result is output on this pin and synchronized to SCK. In unipolar modes, conversion results are straight binary; in bipolar modes, conversion results are twos complement.                                                                                                                                                                                                                                                                                                                                                                                                             |
| 15                    | VIO                                 | P                 | Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 16 to 19<br>21 (EPAD) | IN0 to IN3<br>Exposed Paddle (EPAD) | AI                | Analog Input Channel 0, Analog Input Channel 1, Analog Input Channel 2, and Analog Input Channel 3. The exposed paddle is not connected internally. For increased reliability of the solder joints, it is recommended that the pad be soldered to the GND plane.                                                                                                                                                                                                                                                                                                                                                          |

<sup>1</sup>AI = analog input, AI/O = analog input/output, DI = digital input, DO = digital output, and P = power.

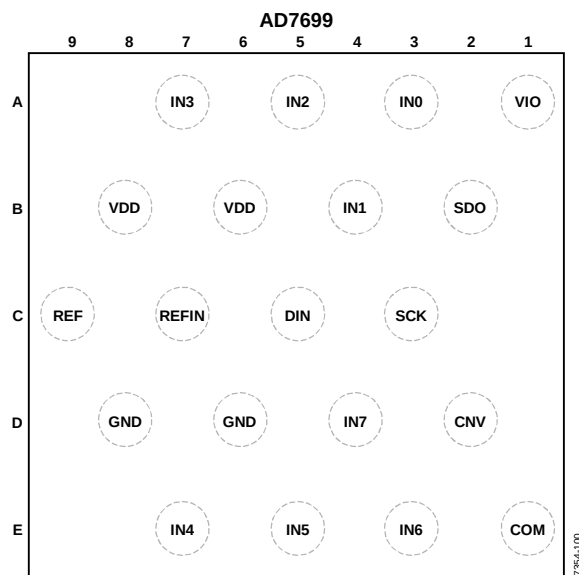


Figure 5. 20-Lead WLCSP Pin Configuration

Table 7. 20-Lead WLCSP Pin Function Descriptions

| Pin No. | Mnemonic | Type <sup>1</sup> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|---------|----------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B6, B8  | VDD      | P                 | Power Supply. Nominally 4.5 V to 5.5 V when using an external reference and decoupled with 10 $\mu$ F and 100 nF capacitors. When using the internal reference for a 2.5 V output, the minimum must be 3.0 V. When using the internal reference for 4.096 V output, the minimum must be 4.6 V.                                                                                                                                                                                                                                                                                                                                                                                    |
| C9      | REF      | AI/O              | Reference Input/Output. See the Voltage Reference Output/Input section. When the internal reference is enabled, this pin produces a selectable system reference of 2.5 V or 4.096 V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered version of the voltage present on the REFIN pin ( $VDD - 0.5$ V, maximum), which is useful when using low cost, low power references. For improved drift performance, connect a precision reference to REF (0.5 V to VDD). For any reference method, this pin needs decoupling with an external 10 $\mu$ F capacitor connected as close to REF as possible. See the Reference Decoupling section. |
| C7      | REFIN    | AI/O              | Internal Reference Output/Reference Buffer Input. See the Voltage Reference Output/Input section. When using the internal reference, the internal unbuffered reference voltage is present and requires decoupling with a 0.1 $\mu$ F capacitor. When using the internal reference buffer, apply a source between 0.5 V and ( $VDD - 0.5$ V) that is buffered to the REF pin, as described in the REF pin description.                                                                                                                                                                                                                                                             |
| D6, D8  | GND      | P                 | Power Supply Ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| A7      | IN3      | AI                | Analog Input Channel 3.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| E5      | IN5      | AI                | Analog Input Channel 5.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| E3      | IN6      | AI                | Analog Input Channel 6.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| D4      | IN7      | AI                | Analog Input Channel 7.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| E1      | COM      | AI                | Common Channel Input. All input channels, IN[7:0], can be referenced to a common-mode point of 0 V or $V_{REF}/2$ V.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| D2      | CNV      | DI                | Conversion Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held low, the busy indicator is enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| C5      | DIN      | DI                | Data Input. Use this input for writing to the 14-bit configuration register. The configuration register can be written to during and after conversion.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| C3      | SCK      | DI                | Serial Data Clock Input. This input clock outs the data on SDO and clock in data on DIN in an MSB first fashion.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| B2      | SDO      | DO                | Serial Data Output. The conversion result is output on this pin, synchronized to SCK. In unipolar modes, conversion results are straight binary. In bipolar modes, conversion results are two's complement.                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| A1      | VIO      | P                 | Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| A3      | IN0      | AI                | Analog Input Channel 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| B4      | IN1      | AI                | Analog Input Channel 1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| A5      | IN2      | AI                | Analog Input Channel 2.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| E7      | IN4      | AI                | Analog Input Channel 4.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

<sup>1</sup> AI means analog input, AI/O means analog input/output, DI means digital input, DO means digital output, P means power, and NC means no internal connection.

## TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 5 V, VREF = 5 V, VIO = VDD, unless otherwise noted.

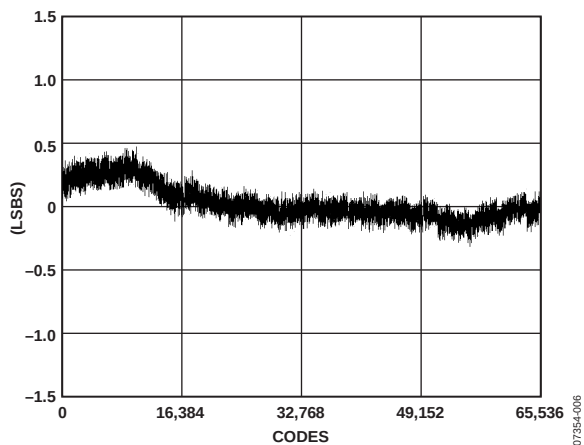


Figure 6. Integral Nonlinearity vs. Code

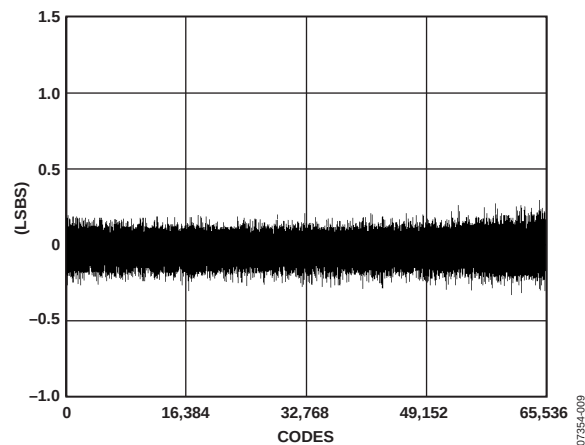


Figure 9. Differential Nonlinearity vs. Code

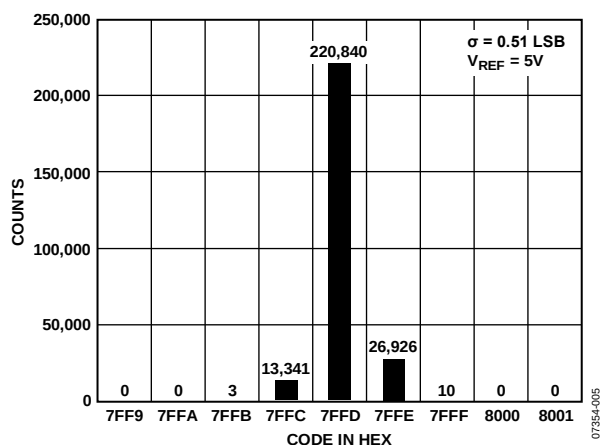


Figure 7. Histogram of a DC Input at Code Center

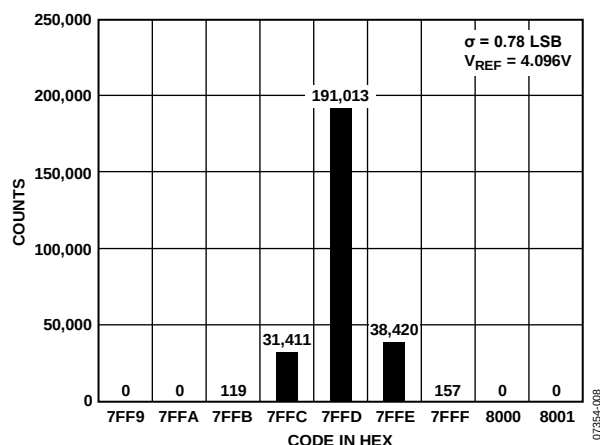


Figure 10. Histogram of a DC Input at Code Center

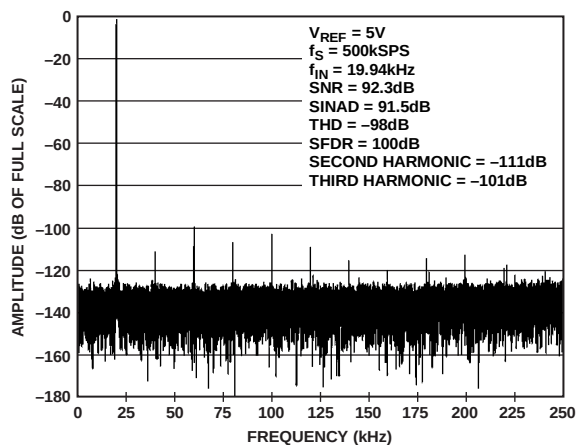


Figure 8. 20 kHz FFT, VREF = 5 V

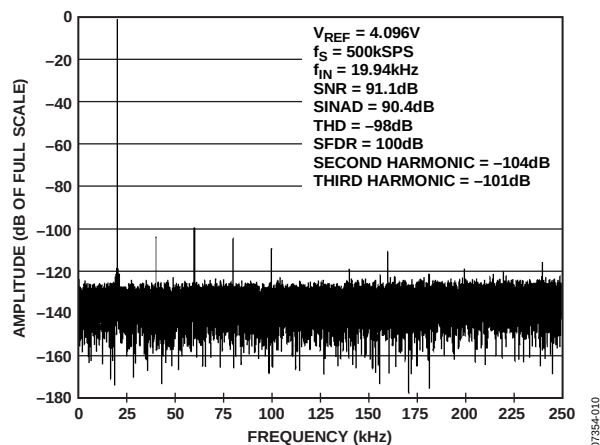


Figure 11. 20 kHz FFT, VREF = 4.096 V

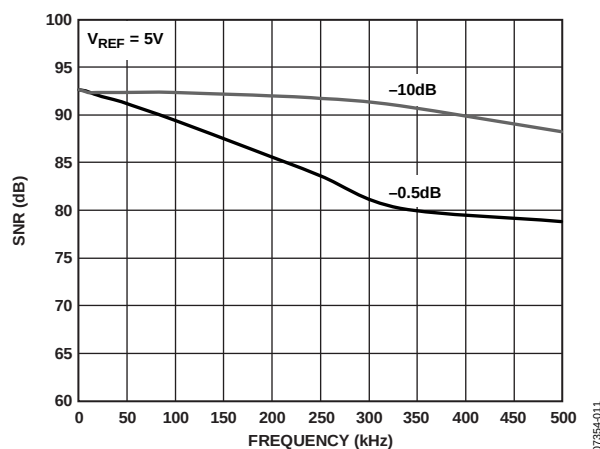


Figure 12. SNR vs. Frequency

07354-011

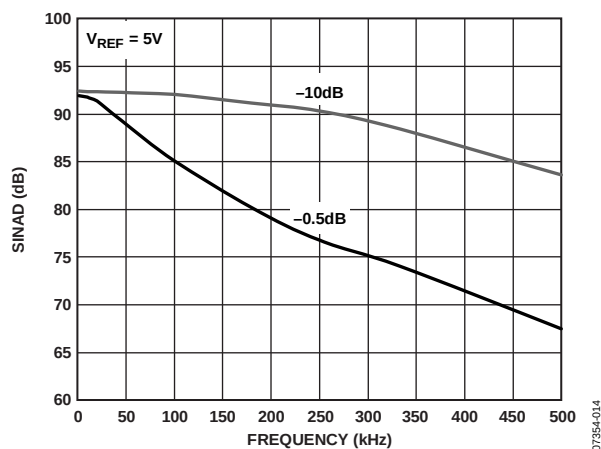


Figure 15. SINAD vs. Frequency

07354-014

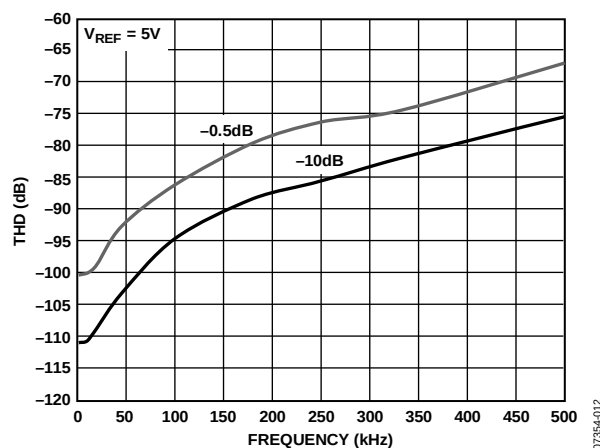


Figure 13. THD vs. Frequency

07354-012

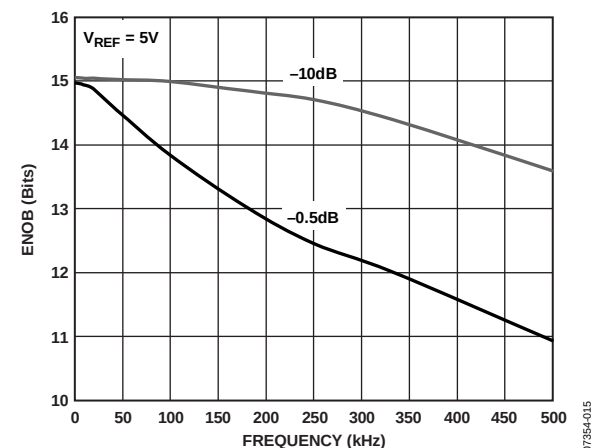


Figure 16. ENOB vs. Frequency

07354-015

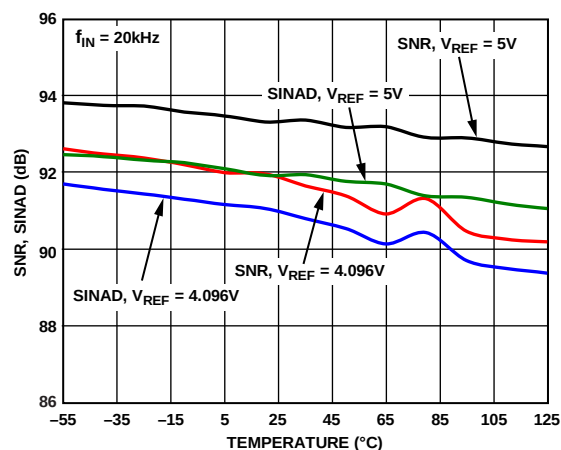


Figure 14. SNR, SINAD vs. Temperature

07354-013

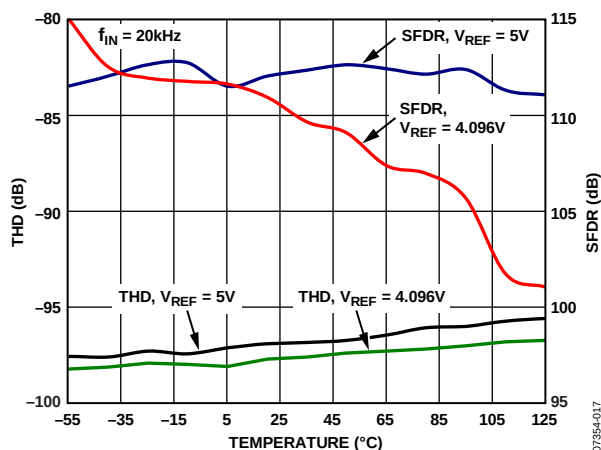


Figure 17. THD, SFDR vs. Temperature

07354-017

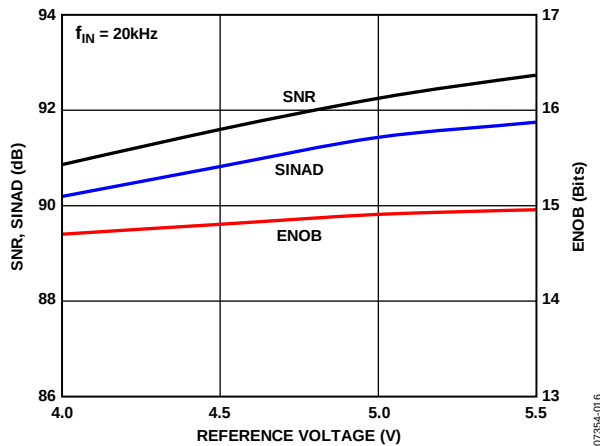


Figure 18. SNR, SINAD, ENOB vs. Reference Voltage

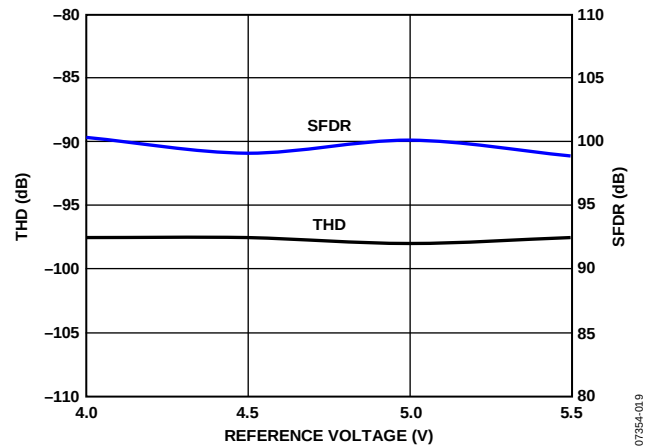


Figure 21. THD, SFDR vs. Reference Voltage

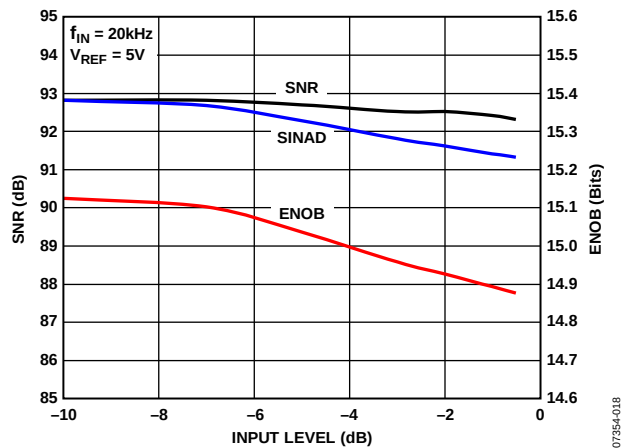


Figure 19. SNR, SINAD, and ENOB vs. Input Level

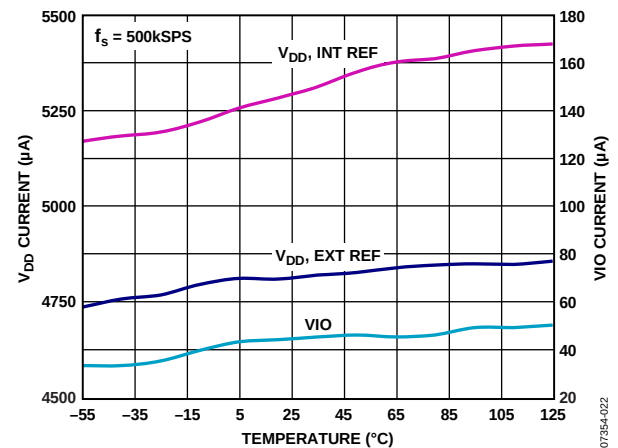


Figure 22. Operating Currents vs. Temperature

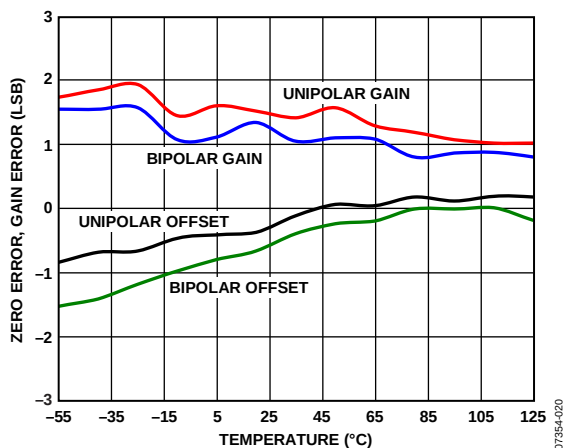


Figure 20. Offset and Gain Errors vs. Temperature, Not Normalized

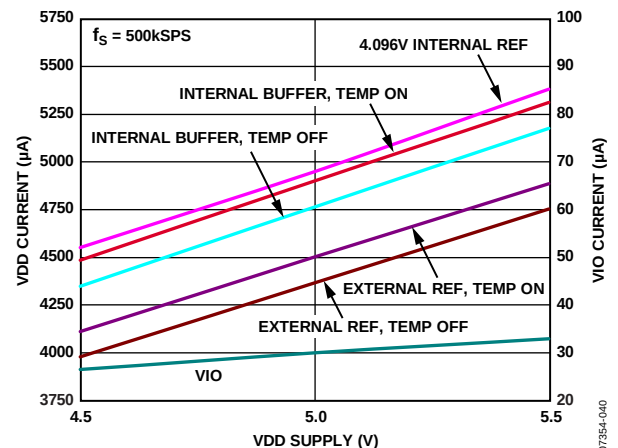


Figure 23. Operating Currents vs. Supply

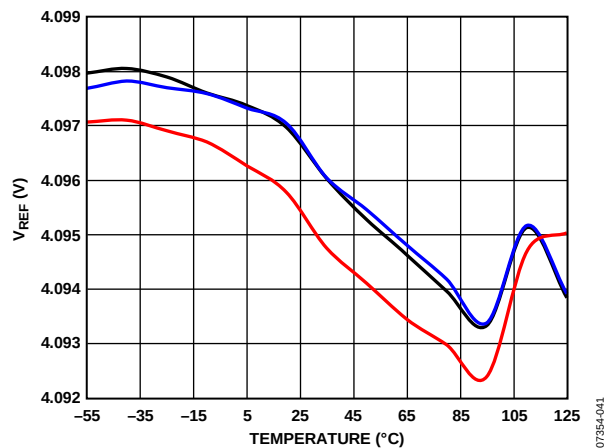


Figure 24. Internal Reference Output Voltage vs. Temperature, Three Devices

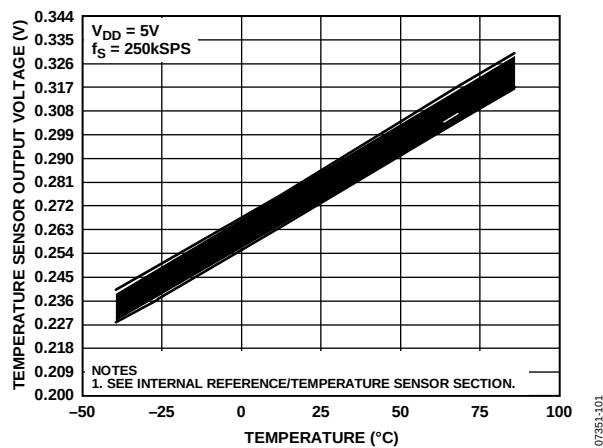
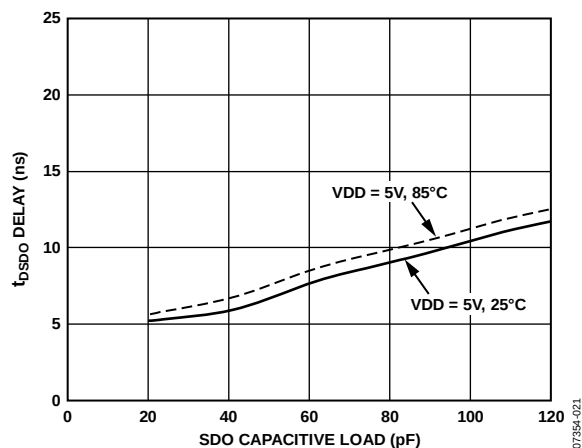


Figure 26. Temperature Sensor Output Voltage vs. Temperature

Figure 25.  $t_{DSO}$  Delay vs. SDO Capacitance Load and Supply

## TERMINOLOGY

### Least Significant Bit (LSB)

The LSB is the smallest increment that can be represented by a converter. For an analog-to-digital converter with N bits of resolution, the LSB expressed in volts is

$$LSB (V) = \frac{V_{REF}}{2^N}$$

### Integral Nonlinearity Error (INL)

INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 28).

### Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

### Offset Error

For unipolar mode, the first transition occurs at a level ½ LSB above analog ground. The unipolar offset error is the deviation of the actual transition from that point. For bipolar mode, the first transition occurs at a level ½ LSB above  $V_{REF}/2$ . The bipolar offset error is the deviation of the actual transition from that point.

### Gain Error

The last transition (from 111 ... 10 to 111 ... 11) occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation in LSB (or percentage of full-scale range) of the actual level of the last transition from the ideal level after the offset error is adjusted out. Closely related is the full-scale error (also in LSB or percentage of full-scale range), which includes the effects of the offset error.

### Aperture Delay

Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and the point at which the input signal is held for a conversion.

### Transient Response

Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

### Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

### Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

### Signal-to-(Noise + Distortion) Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

### Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

### Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

### Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the formula

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

### Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is a measure of the level of crosstalk between any two adjacent channels. It is measured by applying a dc to the channel under test and applying a full-scale, 100 kHz sine wave signal to the adjacent channel(s). The crosstalk is the amount of signal that leaks into the test channel and is expressed in decibels.

### Reference Voltage Temperature Coefficient

Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of devices at the maximum and minimum reference output voltage ( $V_{REF}$ ) measured at  $T_{MIN}$ , T (25°C), and  $T_{MAX}$ . It is expressed in ppm/°C as

$$TCV_{REF}(\text{ppm}/^{\circ}\text{C}) = \frac{V_{REF}(\text{Max}) - V_{REF}(\text{Min})}{V_{REF}(25^{\circ}\text{C}) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:

$V_{REF}(\text{Max})$  = maximum  $V_{REF}$  at  $T_{MIN}$ , T (25°C), or  $T_{MAX}$ .

$V_{REF}(\text{Min})$  = minimum  $V_{REF}$  at  $T_{MIN}$ , T (25°C), or  $T_{MAX}$ .

$V_{REF}(25^{\circ}\text{C})$  =  $V_{REF}$  at 25°C.

$T_{MAX}$  = +85°C.

$T_{MIN}$  = -40°C.

## THEORY OF OPERATION

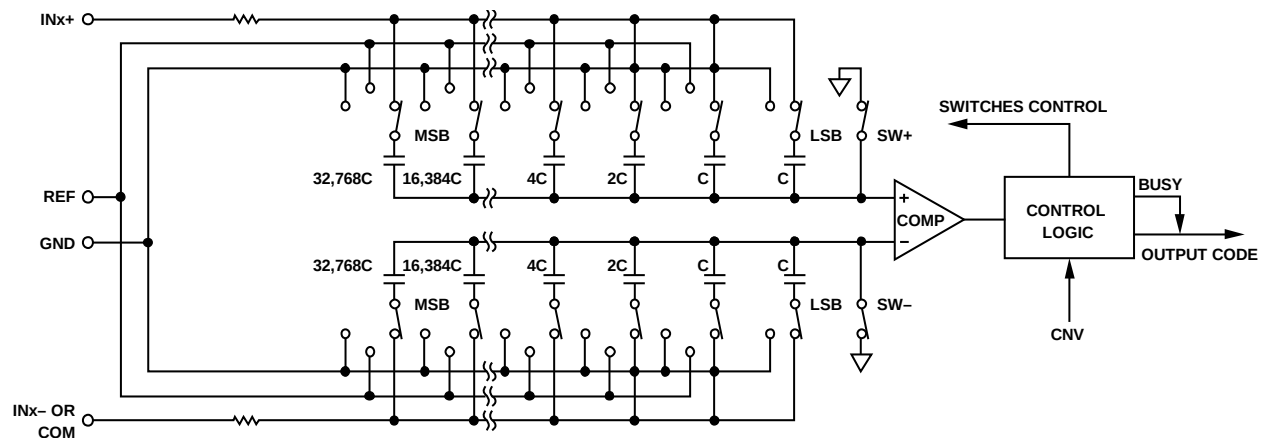


Figure 27. ADC Simplified Schematic

07354-023

### OVERVIEW

The **AD7699** is an 8-channel, 16-bit, charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC). It is capable of converting 500,000 samples per second (500 kSPS) and power down between conversions. For example, when operating with an external reference at 1 kSPS, it consumes 52  $\mu$ W typically, ideal for battery-powered applications.

The **AD7699** contains all of the components for use in a multichannel, low power data acquisition system, including

- 16-bit SAR ADC with no missing codes
- 8-channel, low crosstalk multiplexer
- Internal low drift reference and buffer
- Temperature sensor
- Selectable one-pole filter
- Channel sequencer

These components are configured through an SPI-compatible, 14-bit register. Conversion results, also SPI compatible, can be read after or during conversions with the option for reading back the configuration.

The **AD7699** provides the user with an on-chip track-and-hold and does not exhibit pipeline delay or latency.

The **AD7699** is specified from 4.5 V to 5.5 V and can be interfaced to any 1.8 V to 5 V digital logic family. It is housed in a 20-lead, 4 mm  $\times$  4 mm LFCSP that combines space savings and allows flexible configurations and is also pin-for-pin compatible with the 16-bit **AD7682** and **AD7689**, and the 14-bit **AD7949**.

### CONVERTER OPERATION

The **AD7699** is a successive approximation ADC based on a charge redistribution DAC. Figure 27 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary-weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator input are connected to GND via SW+ and SW-. All independent switches are connected to the analog inputs.

Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the INx+ and INx- (or COM) inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW- are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the INx+ and INx- (or COM) inputs captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary-weighted voltage steps ( $V_{REF}/2$ ,  $V_{REF}/4$ , ...  $V_{REF}/32,768$ ). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the device returns to the acquisition phase, and the control logic generates the ADC output code and a busy signal indicator.

Because the **AD7699** has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

## TRANSFER FUNCTIONS

With the inputs configured for unipolar range (single ended, COM with ground sense, or paired differentially with INx– as ground sense), the data output is straight binary.

With the inputs configured for bipolar range (COM =  $V_{REF}/2$  or paired differentially with INx– =  $V_{REF}/2$ ), the data outputs are twos complement.

The ideal transfer characteristic for the AD7699 is shown in Figure 28 and for both unipolar and bipolar ranges with the internal 4.096 V reference.

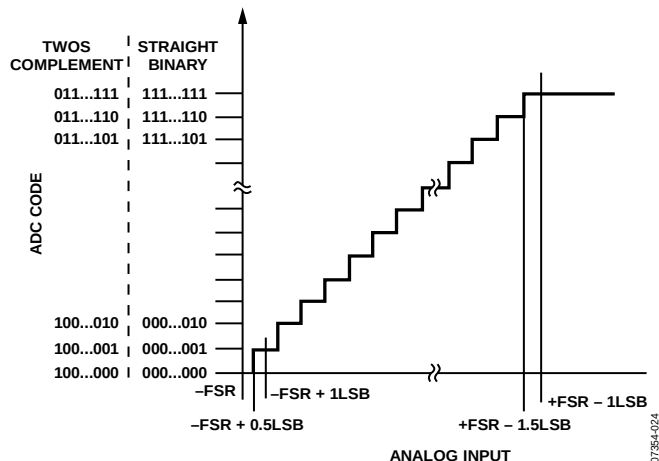


Figure 28. ADC Ideal Transfer Function

Table 8. Output Codes and Ideal Input Voltages

| Description      | Unipolar Analog Input <sup>1</sup><br>$V_{REF} = 4.096 \text{ V}$ | Digital Output Code<br>(Straight Binary Hex) | Bipolar Analog Input <sup>2</sup><br>$V_{REF} = 4.096 \text{ V}$ | Digital Output Code<br>(Twos Complement Hex) |
|------------------|-------------------------------------------------------------------|----------------------------------------------|------------------------------------------------------------------|----------------------------------------------|
| FSR – 1 LSB      | 4.095938 V                                                        | 0xFFFF <sup>3</sup>                          | 2.047938 V                                                       | 0x7FFF <sup>3</sup>                          |
| Midscale + 1 LSB | 2.048063 V                                                        | 0x8001                                       | 62.5 $\mu\text{V}$                                               | 0x0001                                       |
| Midscale         | 2.048 V                                                           | 0x8000                                       | 0 V                                                              | 0x0000                                       |
| Midscale – 1 LSB | 2.047938 V                                                        | 0x7FFF                                       | –62.5 $\mu\text{V}$                                              | 0xFFFF <sup>4</sup>                          |
| –FSR + 1 LSB     | 62.5 $\mu\text{V}$                                                | 0x0001                                       | –2.047938 V                                                      | 0x8001                                       |
| –FSR             | 0 V                                                               | 0x0000 <sup>3</sup>                          | –2.048 V                                                         | 0x8000                                       |

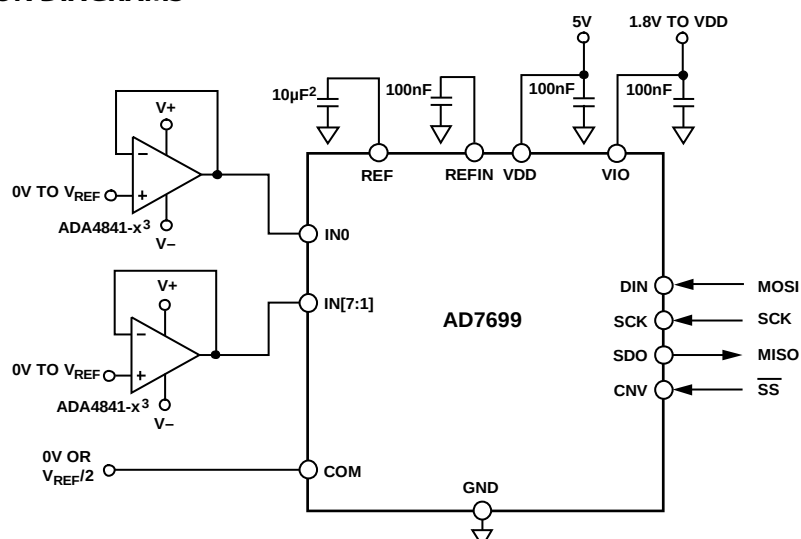
<sup>1</sup> With COM or INx– = 0 V or all INx referenced to GND.

<sup>2</sup> With COM or INx– =  $V_{REF}/2$ .

<sup>3</sup> This is also the code for an overranged analog input ((INx+) – (INx–), or COM, above  $V_{REF} - V_{GND}$ ).

<sup>4</sup> This is also the code for an underranged analog input ((INx+) – (INx–), or COM, below  $V_{GND}$ ).

## TYPICAL CONNECTION DIAGRAMS

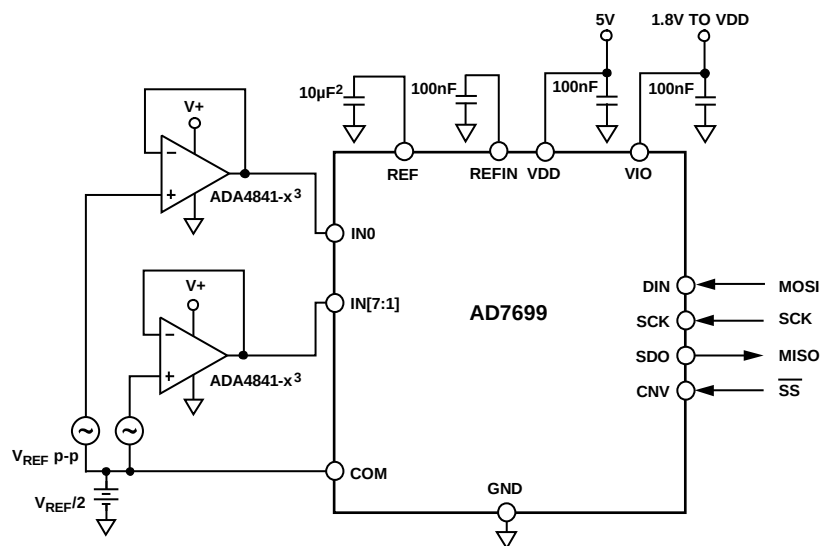


## NOTES

1. INTERNAL REFERENCE SHOWN. SEE THE VOLTAGE REFERENCE OUTPUT/INPUT SECTION FOR REFERENCE SELECTION.
2.  $C_{REF}$  IS USUALLY A  $10\mu\text{F}$  CERAMIC CAPACITOR (X5R).
3. SEE THE DRIVER AMPLIFIER CHOICE SECTION FOR ADDITIONAL RECOMMENDED AMPLIFIERS.
4. SEE THE DIGITAL INTERFACE SECTION FOR CONFIGURING AND READING CONVERSION DATA.

07354-025

Figure 29. Typical Application Diagram with Multiple Supplies



## NOTES

1. INTERNAL REFERENCE SHOWN. SEE THE VOLTAGE REFERENCE OUTPUT/INPUT SECTION FOR REFERENCE SELECTION.
2.  $C_{REF}$  IS USUALLY A  $10\mu\text{F}$  CERAMIC CAPACITOR (X5R).
3. SEE THE DRIVER AMPLIFIER CHOICE SECTION FOR ADDITIONAL RECOMMENDED AMPLIFIERS.
4. SEE THE DIGITAL INTERFACE SECTION FOR CONFIGURING AND READING CONVERSION DATA.

07354-026

Figure 30. Typical Application Diagram Using Bipolar Input

### Unipolar or Bipolar

Figure 29 shows an example of the recommended connection diagram for the AD7699 when multiple supplies are available.

### Bipolar Single Supply

Figure 30 shows an example of a system with a bipolar input using single supplies with the internal reference (optional different VIO supply). This circuit is also useful when the amplifier/signal conditioning circuit is remotely located with some common mode present. Note that for any input configuration, the inputs, INx, are unipolar and always referenced to GND (no negative voltages even in bipolar range).

For this circuit, a rail-to-rail input/output amplifier can be used. However, the offset voltage vs. input common-mode range must be noted and taken into consideration ( $1 \text{ LSB} = 62.5 \mu\text{V}$  with  $V_{\text{REF}} = 4.096 \text{ V}$ ). The conversion results are in twos complement format when using the bipolar input configuration. Refer to the [AN-581 Application Note, Biasing and Decoupling Op Amps in Single Supply Applications](#), at [www.analog.com](http://www.analog.com) for additional details about using single-supply amplifiers.

## ANALOG INPUTS

### Input Structure

Figure 31 shows an equivalent circuit of the input structure of the AD7699. The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN[7:0] and COM. Care must be taken to ensure the analog input signal does not exceed the supply rails by more than 0.3 V because this causes the diodes to become forward-biased and to start conducting current.

These diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions may eventually occur when the input buffer supplies are different from VDD. In such a case, for example, an input buffer with a short circuit, the current limitation can protect the device.

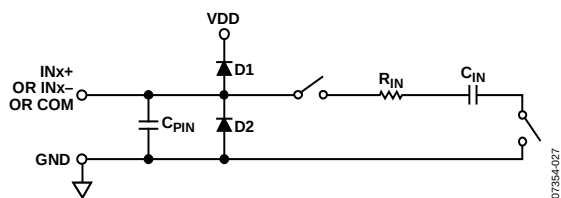


Figure 31. Equivalent Analog Input Circuit

This analog input structure allows the sampling of the true differential signal between INx+ and COM or INx+ and INx-. (COM or INx- =  $\text{GND} \pm 0.1 \text{ V}$  or  $V_{\text{REF}} \pm 0.1 \text{ V}$ ). By using these differential inputs, signals common to both inputs are rejected, as shown in Figure 32.

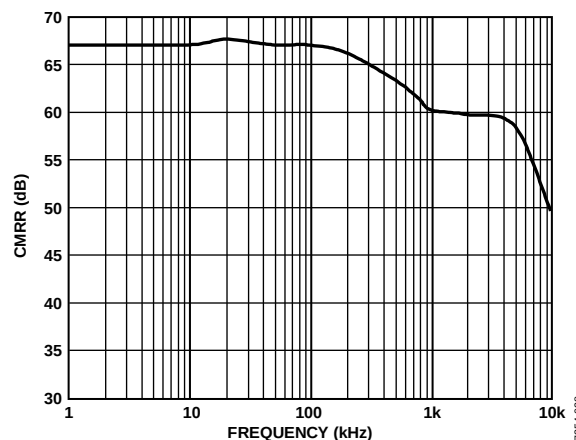


Figure 32. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog inputs can be modeled as a parallel combination of the capacitor,  $C_{\text{PIN}}$ , and the network formed by the series connection of  $R_{\text{IN}}$  and  $C_{\text{IN}}$ .  $C_{\text{PIN}}$  is primarily the pin capacitance.  $R_{\text{IN}}$  is typically  $400 \Omega$  ( $8.8 \text{ k}\Omega$  when the one-pole filter is active) and is a lumped component made up of serial resistors and the on resistance of the switches.  $C_{\text{IN}}$  is typically  $27 \text{ pF}$  and is mainly the ADC sampling capacitor.

### Selectable Low-Pass Filter

During the conversion phase, where the switches are opened, the input impedance is limited to  $C_{\text{PIN}}$ . While the AD7699 is acquiring,  $R_{\text{IN}}$  and  $C_{\text{IN}}$  make a one-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise from the driving circuitry. The low-pass filter can be programmed for the full bandwidth or  $1/4$  of the bandwidth with  $\text{CFG}[6]$ , as shown in Table 10. The converter throughput must also be reduced by  $1/4$  when using the filter. If the maximum throughput is used with the BW set to  $1/4$ , the acquisition time of the converter,  $t_{\text{ACQ}}$ , is violated, resulting in poor THD.

### Input Configurations

Figure 33 shows the different methods for configuring the analog inputs with the configuration register ( $\text{CFG}[12:10]$ ). Refer to the Configuration Register, CFG section for more details.

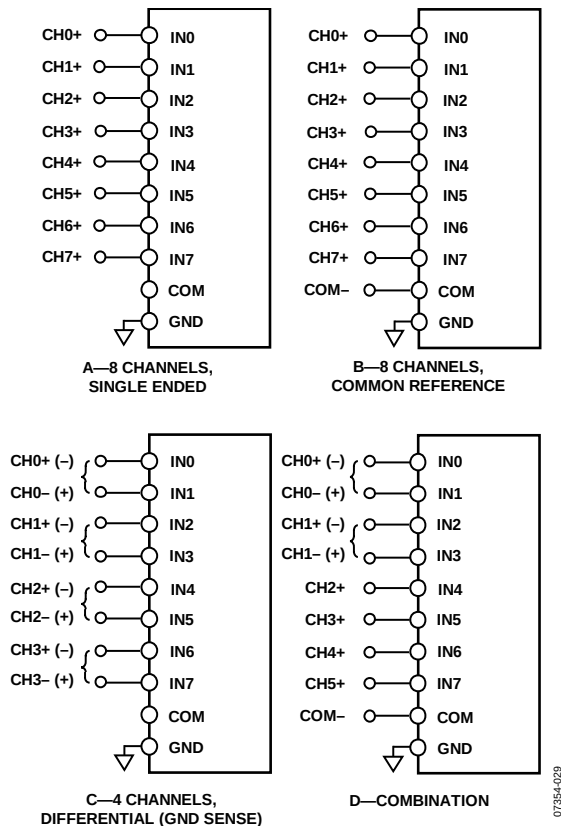


Figure 33. Multiplexed Analog Input Configurations

The AD7699 analog inputs can be configured in either a unipolar single-ended or pseudo differential mode, which means that the positive input pin of the AD7699 can accept signal between 0 V and  $V_{REF}$ , and its negative input (or COM) pin must be always referenced to either a ground or a fixed dc voltage,  $V_{REF}/2$ , as follows:

- Configuration A in Figure 33: single-ended referenced to system ground;  $CFG[12:10] = 111_2$ .
- Configuration B in Figure 33: bipolar differential with a common reference point;  $COM = V_{REF}/2$ ;  $CFG[12:10] = 010_2$ . Unipolar differential with COM connected to a ground sense;  $CFG[12:10] = 110_2$ .
- Configuration C in Figure 33: bipolar differential pairs with  $INx-$  referenced to  $V_{REF}/2$ ;  $CFG[12:10] = 00X_2$ . Unipolar differential pairs with  $INx-$  referenced to a ground sense;  $CFG[12:10] = 10X_2$ . In this configuration, the  $INx+$  is identified by the channel in  $CFG[9:7]$ . For example, for  $IN0 = IN1+$  and  $IN1 = IN1-$ ,  $CFG[9:7] = 000_2$ ; for  $IN1 = IN1+$  and  $IN0 = IN1-$ ,  $CFG[9:7] = 001_2$ .
- Configuration D in Figure 33: inputs configured in any of the above combinations (showing that the AD7699 can be configured dynamically).

### Sequencer

The AD7699 includes a channel sequencer useful for scanning channels in a  $IN0$  to  $IN[7:0]$  fashion. Channels are scanned as singles or pairs, with or without the temperature sensor, after the last channel is sequenced.

The sequencer starts with  $IN0$  and finishes with  $IN[7:0]$  set in  $CFG[9:7]$ . For paired channels, the channels are paired depending on the last channel set in  $CFG[9:7]$ . The channel pairs are always paired as  $IN$  (even) =  $INx+$  and  $IN$  (odd) =  $INx-$  regardless of  $CFG[7]$ .

To enable the sequencer,  $CFG[2:1]$  are written to for initializing the sequencer. After  $CFG[13:0]$  are updated,  $DIN$  must be held low while reading data out (at least for Bit 13), or the  $CFG$  register begins updating again.

While operating in a sequence, the  $CFG$  register can be changed by writing  $01_2$  to  $CFG[2:1]$ . However, if changing  $CFG11$  (paired or single channel) or  $CFG[9:7]$  (last channel in sequence), the sequence reinitializes and converts  $IN0$  (or  $IN1$ ) after  $CFG$  is updated.

### Examples

Bit[13], Bits[6:3], and Bit 0 are configured for the input and sequencer.

As a first example, scan all  $IN[7:0]$  referenced to  $COM = GND$  with the temperature sensor.

| 13  | 12   | 11 | 10 | 9   | 8 | 7 | 6  | 5   | 4 | 3 | 2   | 1 | 0  |
|-----|------|----|----|-----|---|---|----|-----|---|---|-----|---|----|
| CFG | INCC |    |    | INx |   |   | BW | REF |   |   | SEQ |   | RB |
|     | 1    | 1  | 0  | 1   | 1 | 1 |    |     |   |   | 1   | 0 |    |

As a second example, scan three paired channels without the temperature sensor and referenced to  $V_{REF}/2$ .

| 13  | 12   | 11 | 10             | 9   | 8 | 7              | 6  | 5   | 4 | 3 | 2   | 1 | 0  |
|-----|------|----|----------------|-----|---|----------------|----|-----|---|---|-----|---|----|
| CFG | INCC |    |                | INx |   |                | BW | REF |   |   | SEQ |   | RB |
|     | 0    | 0  | X <sup>1</sup> | 1   | 0 | X <sup>1</sup> |    |     |   |   | 1   | 1 |    |

<sup>1</sup> X means don't care.

### Source Resistance

When the source impedance of the driving circuit is low, the AD7699 can be driven directly. Large source impedances significantly affect the ac performance, especially total harmonic distortion (THD). The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

## DRIVER AMPLIFIER CHOICE

Although the AD7699 is easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the AD7699. The AD7699 has a noise much lower than most of the other 16-bit ADCs and, therefore, can be driven by a noisier amplifier to meet a given system noise specification. The noise from the amplifier is filtered by the AD7699 analog input circuit low-pass filter made by  $R_{IN}$  and  $C_{IN}$  or by an external filter, if one is used. Because the typical noise of the AD7699 is 35  $\mu$ V rms (with  $V_{REF} = 5$  V), the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log \left( \frac{35}{\sqrt{35^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}} \right)$$

where:

$f_{-3dB}$  is the input bandwidth in megahertz of the AD7699 (14.7 MHz in full BW or 670 kHz in 1/4 BW) or the cutoff frequency of an input filter, if one is used.

$N$  is the noise gain of the amplifier (for example, 1 in buffer configuration).

$e_N$  is the equivalent input noise voltage of the op amp, in nV/ $\sqrt{\text{Hz}}$ .

- For ac applications, the driver have a THD performance commensurate with the AD7699. Figure 13 shows THD vs. frequency for the AD7699.
- For multichannel, multiplexed applications on each input or input pair, the driver amplifier and the AD7699 analog input circuit must settle a full-scale step onto the capacitor array at a 16-bit level (0.0015%). In amplifier data sheets, settling at 0.1% to 0.01% is more commonly specified. This may differ significantly from the settling time at a 16-bit level and must be verified prior to driver selection.

**Table 9. Recommended Driver Amplifiers**

| Amplifier | Typical Application                                                       |
|-----------|---------------------------------------------------------------------------|
| ADA4805-1 | Low noise, small size, and low power                                      |
| ADA4807-1 | Very low noise and high frequency                                         |
| AD8655    | 5 V single supply, low noise                                              |
| ADA4627-1 | Precision, low noise, and low input bias                                  |
| ADA4522-1 | Precision, zero drift, and EMI enhanced                                   |
| ADA4500-2 | Precision, rail-to-rail input/output, and zero input crossover distortion |

## VOLTAGE REFERENCE OUTPUT/INPUT

The AD7699 allows the choice of a very low temperature drift internal voltage reference, an external reference, or an external buffered reference.

The internal reference of the AD7699 provides excellent performance and can be used in almost all applications. There are five possible choices of voltage reference schemes briefly described in Table 10 with more details in each of the following sections.

### Internal Reference/Temperature Sensor

The internal reference can be set for a 4.096 V output as detailed in Table 10. With the internal reference enabled, the band gap voltage is also present on the REFIN pin, which requires an external 0.1  $\mu$ F capacitor. Because the current output of REFIN is limited, it can be used as a source if followed by a suitable buffer, such as the AD8605.

Enabling the internal reference also enables the internal temperature sensor, which measures the internal temperature of the AD7699 and is thus useful for performing a system calibration. For applications requiring the use of the temperature sensor, the internal reference must be active (internal buffer can be disabled in this case). Note that, when using the temperature sensor, the output is single-ended conversion, straight binary referenced from the AD7699 GND pin. The AD7699 temperature sensor voltage can be thought of as a normal analog input; therefore, the code that represents it is calculated as temperature sensor code = temperature sensor voltage  $\times$  (reference voltage)/(2<sup>16</sup> – 1). Its temperature sensor output voltage is typically 283 mV at 25°C. The internal reference is temperature-compensated to within 10 mV. The reference is trimmed to provide a typical drift of  $\pm 10$  ppm/°C.

### External Reference and Internal Buffer

For improved drift performance, an external reference can be used with the internal buffer. The external reference is connected to REFIN, and the output is produced on the REF pin. An external reference can be used with the internal buffer with or without the temperature sensor enabled. Refer to Table 10 for register details. With the buffer enabled, the gain is unity and is limited to an input/output of 4.096 V.

The internal reference buffer is useful in multiconverter applications because a buffer is typically required in these applications. A low power reference can also be used because the internal buffer provides the necessary performance to drive the SAR architecture of the AD7699.

### External Reference

In any of the five voltage reference schemes, an external reference can be connected directly on the REF pin because the output impedance of REF is  $>5\text{ k}\Omega$ . To reduce power consumption, the reference and buffer can be powered down independently or together for the lowest power consumption. When only using the external reference (and optional reference buffer as shown in Figure 36), an internal buffer is disabled. Refer to Table 10 for register details. For improved drift performance, an external reference such as the [ADR430/ADR431/ADR433/ADR434/ADR435](#) or [ADR440/ADR441/ADR443/ADR444/ADR445](#) is recommended.

### Reference Decoupling

Whether using an internal or external reference, the AD7699 voltage reference output/input, REF, has a dynamic input impedance and are therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins. This decoupling depends on the choice of the voltage reference but usually consists of a low ESR capacitor connected to REF and GND with minimum parasitic inductance. A  $10\text{ }\mu\text{F}$  (X5R, 1206 size) ceramic chip capacitor is appropriate when using the internal reference, the [ADR430/ADR431/ADR433/ADR434/ADR435](#) or [ADR440/ADR441/ADR443/ADR444/ADR445](#) external reference, or a low impedance buffer such as the [AD8031](#) or the [AD8605](#).

The placement of the reference decoupling capacitor is also important to the performance of the AD7699, as explained in the Layout section. Mount the decoupling capacitor on the same side as the ADC at the REF pin with a thick PCB trace. The GND also connects to the reference decoupling capacitor with the shortest distance and to the analog ground plane with several vias.

If desired, smaller reference decoupling capacitor values down to  $2.2\text{ }\mu\text{F}$  can be used with a minimal impact on performance, especially on DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example,  $100\text{ nF}$ ) between the REF and GND pins.

For applications that use multiple AD7699 devices or other PulSAR devices, it is more effective to use the internal reference buffer to buffer the external reference voltage, thus reducing SAR conversion crosstalk.

The voltage reference temperature coefficient (TC) directly impacts full scale; therefore, in applications where full-scale accuracy matters, care must be taken with the TC. For instance, a  $\pm 15\text{ ppm}/^\circ\text{C}$  TC of the reference changes full scale by  $\pm 1\text{ LSB}/^\circ\text{C}$ .

### POWER SUPPLY

The AD7699 uses two power supply pins: an analog and digital core supply (VDD) and a digital input/output interface supply (VIO). VIO allows direct interface with any logic between  $1.8\text{ V}$  and VDD. To reduce the supplies needed, the VIO and VDD pins can be tied together. The AD7699 is independent of power supply sequencing between VIO and VDD. The only restriction is that CNV must be low when powering up the AD7699. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 34.

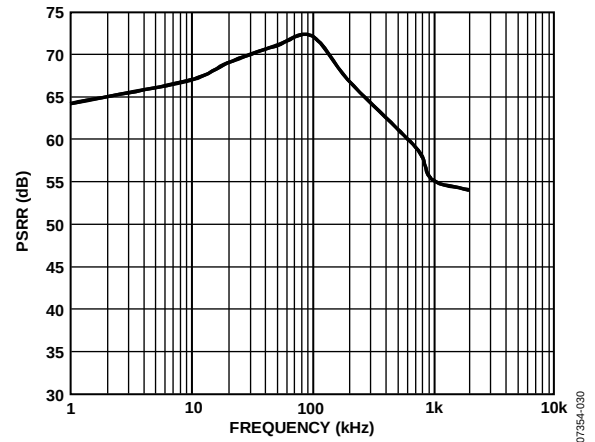


Figure 34. PSRR vs. Frequency

The AD7699 powers down automatically at the end of each conversion phase; therefore, the operating currents and power scale linearly with the sampling rate. This makes the device ideal for low sampling rates (even of a few hertz) and low battery-powered applications.

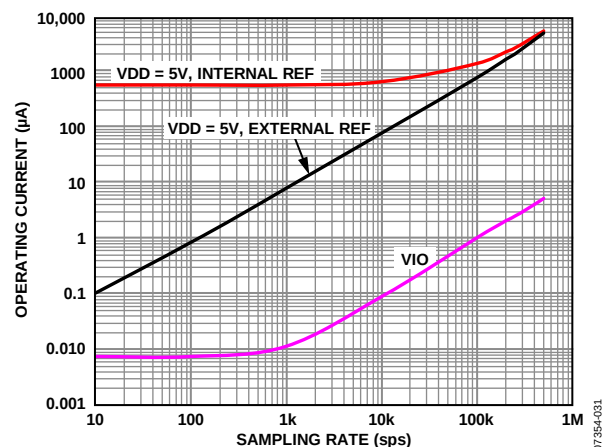


Figure 35. Operating Currents vs. Sampling Rate

### SUPPLYING THE ADC FROM THE REFERENCE

For simplified applications, the [AD7699](#), with its low operating current, can be supplied directly using the reference circuit, as shown in Figure 36. The reference line can be driven by

- The system power supply directly
- A reference voltage with enough current output capability, such as the [ADR430/ADR431/ADR433/ADR434/ADR435](#) or [ADR440/ADR441/ADR443/ADR444/ADR445](#)
- A reference buffer, such as the AD8605, which can also filter the system power supply, as shown in Figure 36

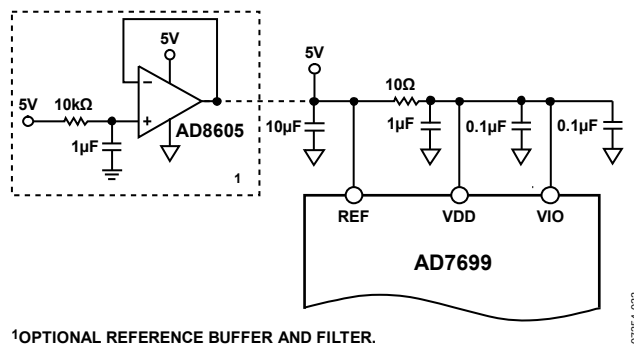


Figure 36. Example of an Application Circuit

## DIGITAL INTERFACE

The AD7699 uses a simple 4-wire interface and is compatible with SPI, MICROWIRE™, QSPI™, digital hosts, and DSPs, for example, Blackfin® ADSP-BF531/ADSP-BF532/ADSP-BF533/ADSP-BF536/ADSP-BF537/ADSP-BF538/ADSP-BF539, SHARC®, ADSP-2191M/ADSP-2196M, and ADSP-2181/ADSP-2183/ADSP-2185/ADSP-2186/ADSP-2189N.

The interface uses the CNV, DIN, SCK, and SDO signals and allows CNV, which initiates the conversion, to be independent of the readback timing. This is useful in low jitter sampling or simultaneous sampling applications.

A 14-bit register, CFG[13:0], configures the ADC for the channel to be converted, the reference selection, and other components, which are detailed in the Configuration Register, CFG section.

When CNV is low, reading/writing can occur during conversion, acquisition, and spanning conversion (acquisition plus conversion), as detailed in the following sections. The CFG word is updated on the first 14 SCK rising edges, and conversion results are output on the first 15 (or 16 if busy mode is selected) SCK falling edges. If the CFG readback is enabled, an additional 14 SCK falling edges are required to output the CFG word associated with the conversion results, with the CFG MSB following the LSB of the conversion result.

A discontinuous SCK is recommended because the device is selected with CNV low, and SCK activity begins to write a new configuration word and clock out data.

Note that in the following sections, the timing diagrams indicate digital activity (SCK, CNV, DIN, SDO) during the conversion. However, due to the possibility of performance degradation, digital activity occurs only prior to the safe data reading/writing time,  $t_{DATA}$ , because the AD7699 provides error correction circuitry that can correct for an incorrect bit during this time. From  $t_{DATA}$  to  $t_{CONV}$ , there is no error correction and conversion results may be corrupted. The user must configure the AD7699 and initiate the busy indicator (if desired) prior to  $t_{DATA}$ . It is also possible to corrupt the sample by having SCK or DIN transitions near the sampling instant. Therefore, it is recommended to keep the digital pins quiet for approximately 30 ns before and 10 ns after the rising edge of CNV, using a discontinuous SCK whenever possible to avoid any potential performance degradation.

For the WLCSP, a full throughput of 500 kSPS can only be achieved using read during conversion or read spanning conversion mode.

### READING/WRITING DURING CONVERSION, FAST HOSTS

When reading/writing during conversion (n), conversion results are for the previous (n – 1) conversion, and writing the CFG is for the next (n + 1) acquisition and conversion.

After the CNV is brought high to initiate conversion, it must be brought low again to allow reading/writing during conversion.

Reading/writing must only occur up to  $t_{DATA}$  and, because this time is limited, the host must use a fast SCK. The SCK frequency required is calculated by

$$f_{SCK} \geq \frac{\text{Number\_SCK\_Edges}}{t_{DATA}}$$

The time between  $t_{DATA}$  and  $t_{CONV}$  is a safe time when digital activity must not occur, or sensitive bit decisions may be corrupt.

### READING/WRITING DURING ACQUISITION, ANY SPEED HOSTS

When reading/writing after conversion, or during acquisition (n), conversion results are for the previous (n – 1) conversion, and writing is for the (n + 1) acquisition.

For the maximum throughput, the only time restriction is that the reading/writing take place during the  $t_{ACQ}$  (min) time. For slow throughputs, the time restriction is dictated by throughput required by the user, and the host is free to run at any speed. Thus for slow hosts, data access must take place during the acquisition phase.

### READING/WRITING SPANNING CONVERSION, ANY SPEED HOST

When reading/writing spanning conversion, the data access starts at the current acquisition (n) and spans into the conversion (n). Conversion results are for the previous (n – 1) conversion, and writing the CFG register is for the next (n + 1) acquisition and conversion.

Similar to reading/writing during conversion, reading/writing only occurs up to  $t_{DATA}$ . For the maximum throughput, the only time restriction is that reading/writing take place during the  $t_{ACQ}$  (min) +  $t_{DATA}$  time.

For slow throughputs, the time restriction is dictated by the user's required throughput, and the host is free to run at any speed. Similar to reading/writing during acquisition, for slow hosts, the data access must take place during the acquisition phase with additional time into the conversion.

Note that data access spanning conversion requires the CNV to be driven high to initiate a new conversion, and data access is not allowed when CNV is high. Thus, the host must perform two bursts of data access when using this method.

### CONFIGURATION REGISTER, CFG

The AD7699 uses a 14-bit configuration register (CFG[13:0]) as detailed in Table 10 for configuring the inputs, the channel to be converted, one-pole filter bandwidth, the reference, and the channel sequencer. The CFG register is latched (MSB first) on DIN with 14 SCK rising edges. CFG update is edge dependent, allowing for asynchronous or synchronous hosts. The register can be written to during conversion, during acquisition, or spanning acquisition/conversion and is updated at the end of conversion,  $t_{CONV}$  (maximum). There is always a one deep delay

when writing the CFG register. Note that at power-up, the CFG register is undefined and two dummy conversions are required to update the register. To preload the CFG register with a factory setting, hold DIN high for two conversions. Thus  $\text{CFG}[13:0] = 0x3FFF$ . This sets the AD7699 for the following:

- IN[7:0] unipolar referenced to GND, sequenced in order
- Full bandwidth for a one-pole filter

- Internal reference/temperature sensor disabled, buffer enabled
- Enables the sequencer
- No readback of the CFG register

Table 10 summarizes the configuration register bit details. See the Theory of Operation section for more details.

| 13  | 12   | 11   | 10   | 9   | 8   | 7   | 6  | 5   | 4   | 3   | 2   | 1   | 0  |
|-----|------|------|------|-----|-----|-----|----|-----|-----|-----|-----|-----|----|
| CFG | INCC | INCC | INCC | INx | INx | INx | BW | REF | REF | REF | SEQ | SEQ | RB |

**Table 10. Configuration Register Description**

| Bit(s)  | Name             | Description                                                                                                                                                                                                                                   |                                                                                                      |                                                          |                                                                                   |
|---------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|----------------------------------------------------------|-----------------------------------------------------------------------------------|
| [13]    | CFG              | Configuration update.<br>0 = Keep current configuration settings.<br>1 = Overwrite contents of register.                                                                                                                                      |                                                                                                      |                                                          |                                                                                   |
| [12:10] | INCC             | Input channel configuration. Selection of pseudobipolar, pseudodifferential, pairs, single-ended, or temperature sensor. Refer to the Input Configurations section.                                                                           |                                                                                                      |                                                          |                                                                                   |
|         |                  | Bit 12                                                                                                                                                                                                                                        | Bit 11                                                                                               | Bit 10                                                   | Function                                                                          |
|         |                  | 0                                                                                                                                                                                                                                             | 0                                                                                                    | X <sup>1</sup>                                           | Bipolar differential pairs; INx– referenced to V <sub>REF</sub> /2 ± 0.1 V.       |
|         |                  | 0                                                                                                                                                                                                                                             | 1                                                                                                    | 0                                                        | Bipolar; INx referenced to COM = V <sub>REF</sub> /2 ± 0.1 V.                     |
|         |                  | 0                                                                                                                                                                                                                                             | 1                                                                                                    | 1                                                        | Temperature sensor.                                                               |
|         |                  | 1                                                                                                                                                                                                                                             | 0                                                                                                    | X <sup>1</sup>                                           | Unipolar differential pairs; INx– referenced to GND ± 0.1 V.                      |
|         |                  | 1                                                                                                                                                                                                                                             | 1                                                                                                    | 0                                                        | Unipolar, IN0 to IN7 referenced to COM = GND ± 0.1 V (GND sense).                 |
|         |                  | 1                                                                                                                                                                                                                                             | 1                                                                                                    | 1                                                        | Unipolar, IN0 to IN7 referenced to GND.                                           |
| [9:7]   | INx              | Input channel selection in binary fashion.                                                                                                                                                                                                    |                                                                                                      |                                                          |                                                                                   |
|         |                  | Bit 9                                                                                                                                                                                                                                         | Bit 8                                                                                                | Bit 7                                                    | Channel                                                                           |
|         |                  | 0                                                                                                                                                                                                                                             | 0                                                                                                    | 0                                                        | IN0                                                                               |
|         |                  | 0                                                                                                                                                                                                                                             | 0                                                                                                    | 1                                                        | IN1                                                                               |
|         |                  | ...                                                                                                                                                                                                                                           | ...                                                                                                  | ...                                                      | ...                                                                               |
|         |                  | 1                                                                                                                                                                                                                                             | 1                                                                                                    | 1                                                        | IN7                                                                               |
| [6]     | BW               | Select bandwidth for low-pass filter. Refer to the Selectable Low-Pass Filter section.<br>0 = ¼ of BW, uses an additional series resistor to further bandwidth limit the noise. Maximum throughput must also be reduced to ¼.<br>1 = Full BW. |                                                                                                      |                                                          |                                                                                   |
| [5:3]   | REF <sup>2</sup> | Reference/buffer selection. Selection of internal, external, and external buffered references, and enabling of the on-chip temperature sensor. Refer to the Voltage Reference Output/Input section.                                           |                                                                                                      |                                                          |                                                                                   |
|         |                  | Bit 5                                                                                                                                                                                                                                         | Bit 4                                                                                                | Bit 3                                                    | Function                                                                          |
|         |                  | 0                                                                                                                                                                                                                                             | 0                                                                                                    | 0                                                        | Do not use.                                                                       |
|         |                  | 0                                                                                                                                                                                                                                             | 0                                                                                                    | 1                                                        | Internal reference and temperature sensor enabled. REF = 4.096 V buffered output. |
|         |                  | 0                                                                                                                                                                                                                                             | 1                                                                                                    | 0                                                        | Use external reference. Temperature sensor enabled. Internal buffer disabled.     |
|         |                  | 0                                                                                                                                                                                                                                             | 1                                                                                                    | 1                                                        | Use external reference. Internal buffer and temperature sensor enabled.           |
|         |                  | 1                                                                                                                                                                                                                                             | 0                                                                                                    | 0                                                        | Do not use.                                                                       |
|         |                  | 1                                                                                                                                                                                                                                             | 0                                                                                                    | 1                                                        | Do not use.                                                                       |
| 1       | 1                | 0                                                                                                                                                                                                                                             | Use external reference. Internal reference, internal buffer and temperature sensor disabled.         |                                                          |                                                                                   |
| 1       | 1                | 1                                                                                                                                                                                                                                             | Use external reference. Internal buffer enabled. Internal reference and temperature sensor disabled. |                                                          |                                                                                   |
| [2:1]   | SEQ              | Channel sequencer. Allows scanning channels in an IN0 to IN[7:0] fashion. Refer to the Sequencer section.                                                                                                                                     |                                                                                                      |                                                          |                                                                                   |
|         |                  | Bit 2                                                                                                                                                                                                                                         | Bit 1                                                                                                | Function                                                 |                                                                                   |
|         |                  | 0                                                                                                                                                                                                                                             | 0                                                                                                    | Disable sequencer.                                       |                                                                                   |
|         |                  | 0                                                                                                                                                                                                                                             | 1                                                                                                    | Update configuration during sequence.                    |                                                                                   |
|         |                  | 1                                                                                                                                                                                                                                             | 0                                                                                                    | Scan IN0 to IN[7:0] (set in CFG[9:7]), then temperature. |                                                                                   |
| 1       | 1                | Scan IN0 to IN[7:0] (set in CFG[9:7]).                                                                                                                                                                                                        |                                                                                                      |                                                          |                                                                                   |
| 0       | RB               | Read back the CFG register.<br>0 = Read back current configuration at end of data.<br>1 = Do not read back contents of configuration.                                                                                                         |                                                                                                      |                                                          |                                                                                   |

<sup>1</sup> X means don't care.

<sup>2</sup> The temperature sensor is always enabled when internal bandgap reference is enabled. See the Voltage Reference Output/Input section.

## GENERAL TIMING WITHOUT A BUSY INDICATOR

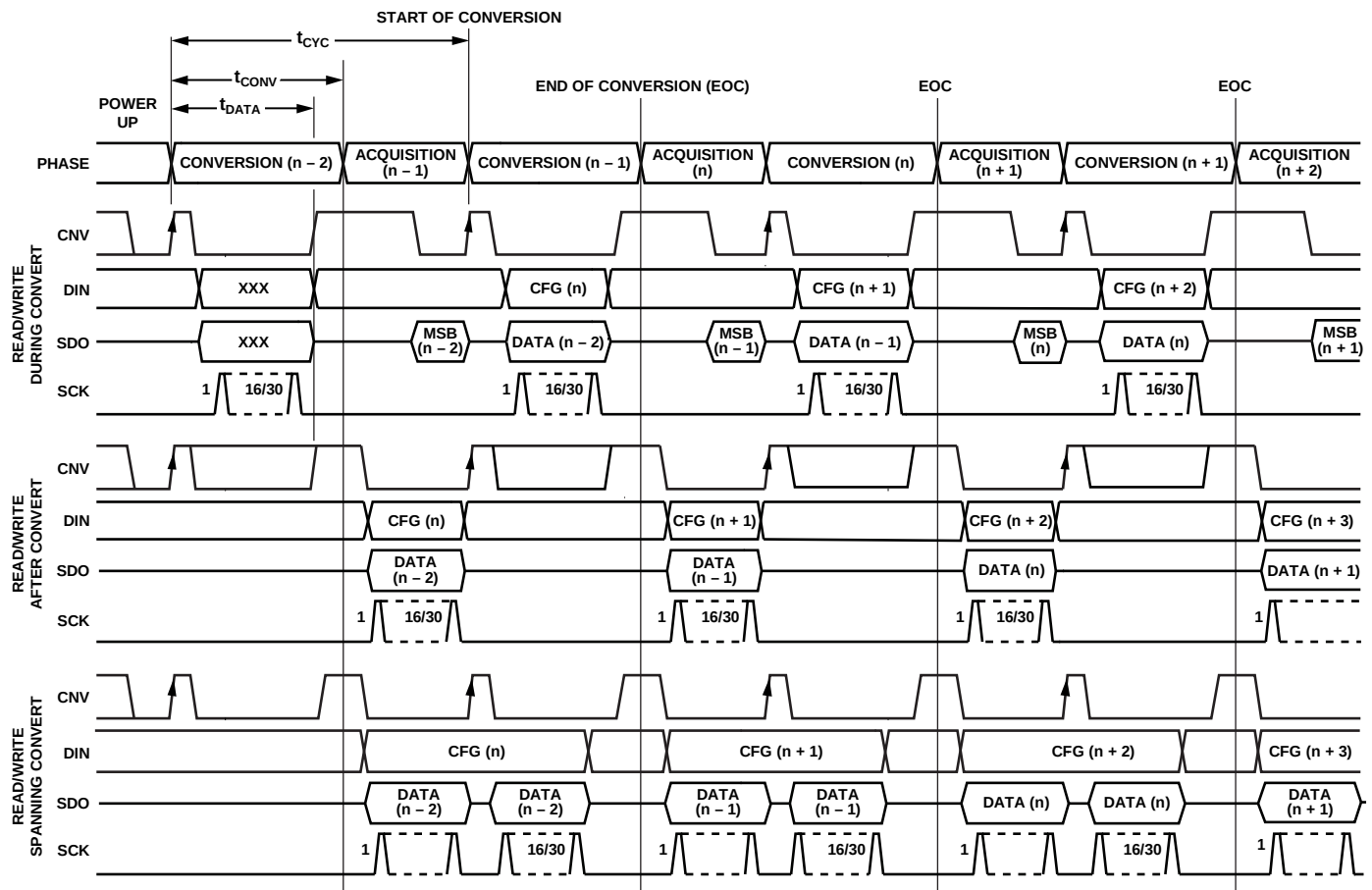
Figure 37 details the timing for all three modes: reading/writing during conversion, after conversion, and spanning conversion. The gating item for both CFG and data readback is at the end of conversion (EOC). At the end of conversions (EOC), if CNV is high, the busy indicator is disabled.

As detailed previously, the data access occurs up to safe data reading/writing time,  $t_{DATA}$ . If the full CFG word was not written to prior to EOC, it is discarded and the current configuration remains. If the conversion result is not read out fully prior to EOC, it is lost as the ADC updates SDO with the MSB of the

current conversion. For detailed timing, refer to Figure 39 and Figure 40, which depict reading/writing spanning conversion with all timing details, including setup, hold, and SCK.

When CNV is brought low after EOC, SDO is driven from high impedance to the MSB. Falling SCK edges clock out bits starting with MSB - 1.

The SCK can idle high or low depending on the clock polarity (CPOL) and clock phase (CPHA) settings if SPI is used. A simple solution is to use CPOL = CPHA = 0 as shown in Figure 37 with SCK idling low.



### NOTES

1. CNV MUST BE HIGH PRIOR TO THE END OF CONVERSION (EOC) TO AVOID THE BUSY INDICATOR. A TOTAL OF 16 SCK FALLING EDGES IS REQUIRED TO RETURN SDO TO HIGH-Z. IF CFG READBACK IS ENABLED, A TOTAL OF 30 SCK FALLING EDGES IS REQUIRED TO RETURN SDO TO HIGH-Z.

Figure 37. General Interface Timing for the AD7699 Without a Busy Indicator

07954-033

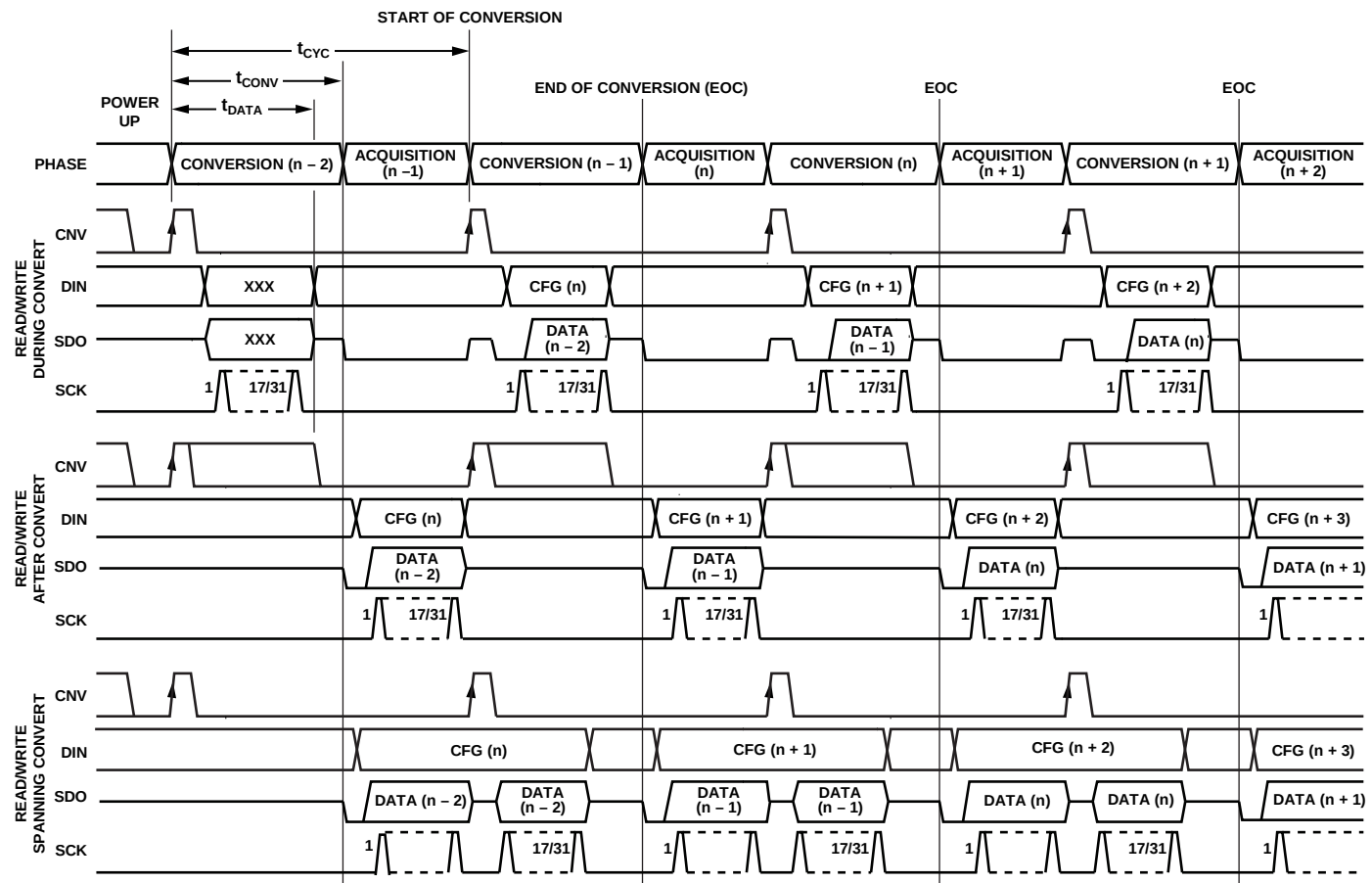
## GENERAL TIMING WITH A BUSY INDICATOR

Figure 38 details the timing for all three modes: reading/writing during conversion, after conversion, and spanning conversion. The gating item for both CFG and data readback is at the end of conversion (EOC). As detailed previously, the data access occurs up to safe data reading/writing time,  $t_{DATA}$ . If the full CFG word is not written to prior to EOC, it is discarded and the current configuration remains.

At the EOC, if CNV is low, the busy indicator is enabled. To generate the busy indicator properly, the host must assert a minimum of 17 SCK falling edges to return SDO to high impedance because the last bit of data on SDO remains active. Unlike the case detailed in the

General Timing Without a Busy Indicator section, if the conversion result is not read out fully prior to EOC, the last bit clocked out remains. If this bit is low, the busy signal indicator cannot be generated because the digital output requires a high impedance, or a bit remaining high, to low transition for the interrupt input of the host. A good example of this occurs when an SPI host sends 16 SCKs because these are usually limited to 8-bit or 16-bit bursts, thus the LSB remains. Because the transition noise of the AD7699 is 4 LSBs peak to peak (or greater), the LSB is low 50% of the time. For this interface, the SPI host must burst 24 SCKs, or a QSPI interface can be used and programmed for 17 SCKs.

The SCK can idle high or low depending on the CPOL and CPHA settings if SPI is used. A simple solution is to use CPOL = CPHA = 1 (not shown) with SCK idling high.



### NOTES

1. CNV MUST BE HIGH PRIOR TO THE END OF CONVERSION (EOC) TO AVOID THE BUSY INDICATOR. A TOTAL OF 17 SCK FALLING EDGES IS REQUIRED TO RETURN SDO TO HIGH-Z. IF CFG READBACK IS ENABLED, A TOTAL OF 31 SCK FALLING EDGES IS REQUIRED TO RETURN SDO TO HIGH-Z.

Figure 38. General Interface Timing for the AD7699 with a Busy Indicator

07354-036

## READ/WRITE SPANNING CONVERSION WITHOUT A BUSY INDICATOR

This mode is used when the AD7699 is connected to any host using an SPI, serial port, or FPGA. The connection diagram is shown in Figure 39, and the corresponding timing is given in Figure 40. For SPI, the host must use  $CPHA = CPOL = 0$ . Reading/writing spanning conversion is shown, which covers all three modes detailed in the Digital Interface section. For this mode, the host must generate the data transfer based on the conversion time. For an interrupt driven transfer, refer to the next section, which uses a busy indicator.

A rising edge on CNV initiates a conversion, forces SDO to high impedance, and ignores data present on DIN. After a conversion is initiated, it continues until completion irrespective of the state of CNV. CNV must be returned high before the safe data transfer time,  $t_{DATA}$ , and then held high beyond the conversion time,  $t_{CONV}$ , to avoid generation of the busy signal indicator.

After the conversion is complete, the AD7699 enters the acquisition phase and powers down. When the host brings CNV low after  $t_{CONV}(\max)$ , the MSB is enabled on SDO. The host also

must enable the MSB of CFG at this time (if necessary) to begin the CFG update. While CNV is low, both a CFG update and a data readback take place. The first 14 SCK rising edges update the CFG, and the first 15 SCK falling edges clock out the conversion results starting with MSB - 1. The restriction for both configuring and reading is that they both must occur before the  $t_{DATA}$  time of the next conversion elapses. All 14 bits of  $CFG[13:0]$  must be written, or they are ignored. If the 16-bit conversion result is not read back before  $t_{DATA}$  elapses, it is lost.

The SDO data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16<sup>th</sup> (or 30<sup>th</sup>) SCK falling edge, or when CNV goes high (whichever occurs first), SDO returns to high impedance.

If CFG readback is enabled, the CFG associated with the conversion result is read back MSB first following the LSB of the conversion result. A total of 30 SCK falling edges is required to return SDO to high impedance if this is enabled.

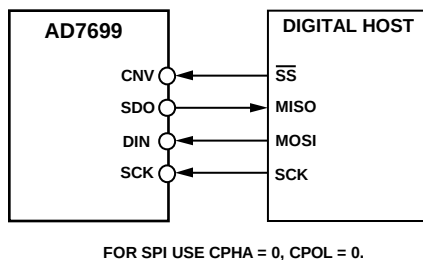


Figure 39. Connection Diagram for the AD7699 Without a Busy Indicator

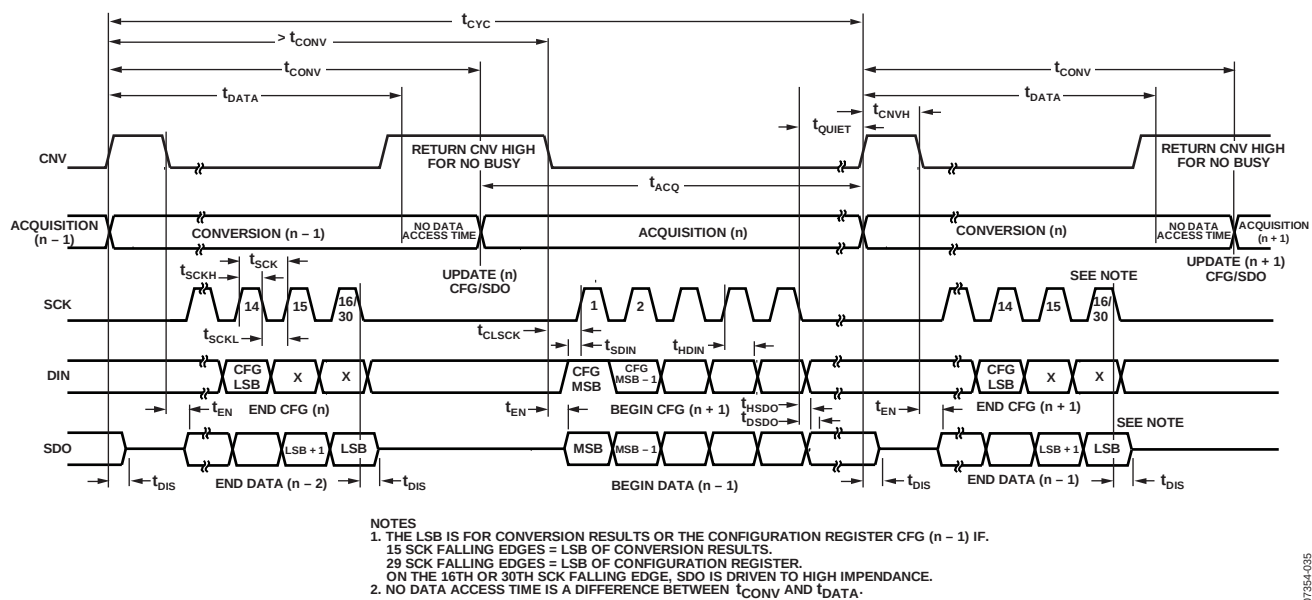


Figure 40. Serial Interface Timing for the AD7699 Without a Busy Indicator

## READ/WRITE SPANNING CONVERSION WITH A BUSY INDICATOR

This mode is used when the AD7699 is connected to any host using an SPI, serial port, or FPGA with an interrupt input. The connection diagram is shown in Figure 41, and the corresponding timing is given in Figure 42. For SPI, the host uses  $CPHA = CPOL = 1$ . Reading/writing spanning conversion is shown, which covers all three modes detailed in the Digital Interface section.

A rising edge on CNV initiates a conversion, forces SDO to high impedance, and ignores data present on DIN. After a conversion is initiated, it continues until completion irrespective of the state of CNV. CNV must be returned low before the safe data transfer time,  $t_{DATA}$ , and then held low beyond the conversion time,  $t_{CONV}$ , to generate the busy signal indicator. When the conversion is complete, SDO transitions from high impedance to low with a pull-up to VIO, which can interrupt the host to begin data transfer.

After the conversion is complete, the AD7699 enters the acquisition phase and power-down. The host must enable the MSB of CFG at this time (if necessary) to begin the CFG

update. While CNV is low, both a CFG update and a data readback take place. The first 14 SCK rising edges update the CFG register, and the first 16 SCK falling edges clock out the conversion results starting with the MSB. The restriction for both configuring and reading is that they both occur before the  $t_{DATA}$  time elapses for the next conversion. All 14 bits of CFG[13:0] must be written or they are ignored. Also, if the 16-bit conversion result is not read back before  $t_{DATA}$  elapses, it is lost.

The SDO data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 17<sup>th</sup> SCK falling edge, SDO returns to high impedance. Note that, if the optional SCK falling edge is not used, the busy feature cannot be detected if the LSB for the conversion is low.

If CFG readback is enabled, the CFG register associated with the conversion result ( $n - 1$ ) is read back MSB first following the LSB of the conversion result. A total of 31 SCK falling edges is required to return SDO to high impedance if this is enabled.

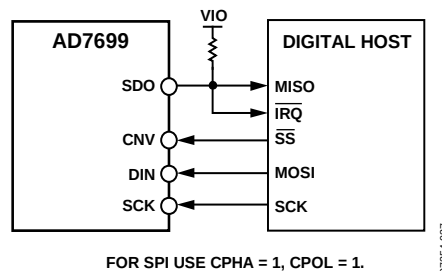


Figure 41. Connection Diagram for the AD7699 with a Busy Indicator

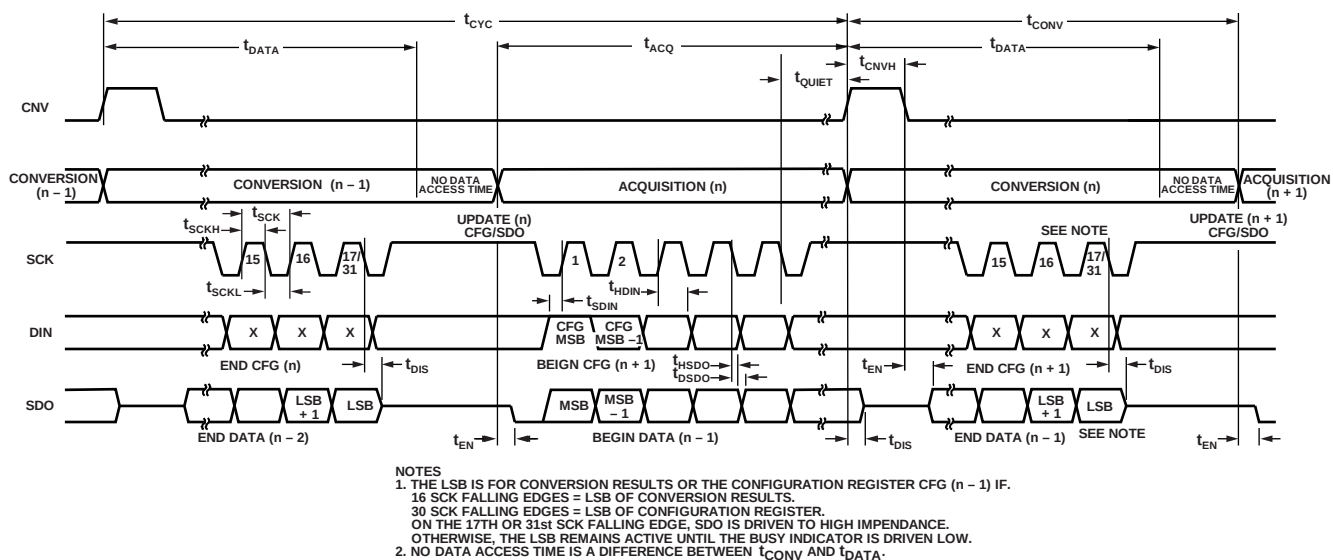


Figure 42. Serial Interface Timing for the AD7699 with a Busy Indicator



## APPLICATION HINTS

### LAYOUT

The printed circuit board that houses the [AD7699](#) must be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the [AD7699](#), with all its analog signals on the left side and all its digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die unless a ground plane under the [AD7699](#) is used as a shield. Fast switching signals, such as CNV or clocks, must not run near analog signal paths. Avoid crossover of digital and analog signals.

At least one ground plane must be used. It can be common or split between the digital and analog sections. In the latter case, join the planes underneath the [AD7699](#).

The [AD7699](#) voltage reference input, REF, has a dynamic input impedance and must be decoupled with minimal parasitic

inductances. This is done by placing the reference decoupling ceramic capacitor close to, ideally right up against, the REF and GND pins and connecting them with wide, low impedance traces.

Finally, decouple the power supplies, VDD and VIO, of the [AD7699](#) with ceramic capacitors, typically 100 nF, placed close to the [AD7699](#) and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

### EVALUATING [AD7699](#) PERFORMANCE

Other recommended layouts for the [AD7699](#) are outlined in the documentation of the evaluation board for the [AD7699](#) ([EVAL-AD76MUXEDZ](#)). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the evaluation controller board, [EVAL-CED1Z](#).

## OUTLINE DIMENSIONS

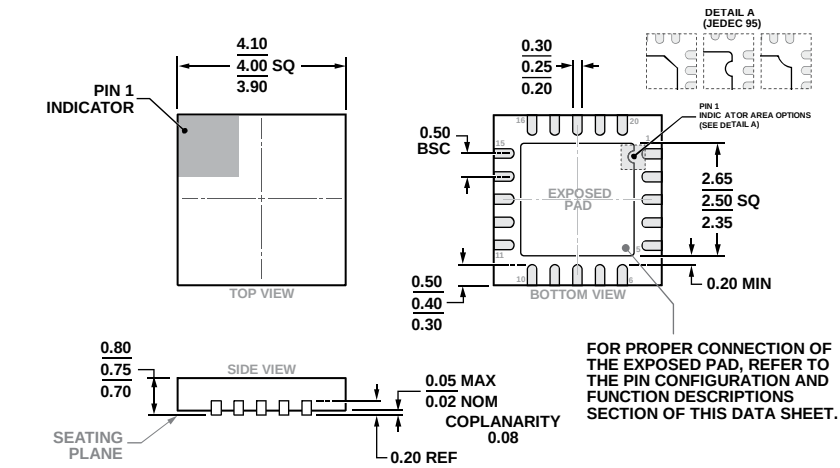


Figure 44. 20-Lead Lead Frame Chip Scale Package [LFCSP]  
4 mm × 4 mm Body and 0.75 mm Package Height  
(CP-20-10)  
Dimensions shown in millimeters

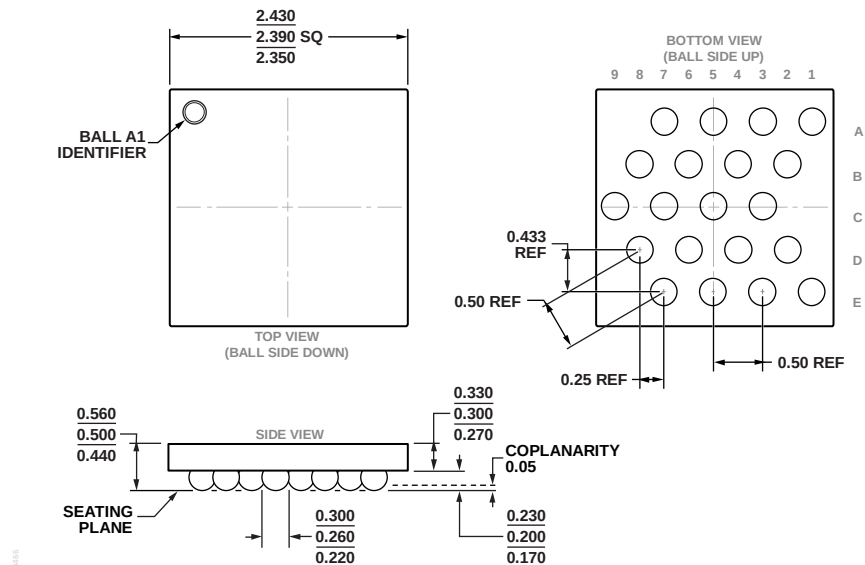


Figure 45. 20-Ball Wafer Level Chip Scale Package [WLCSP]  
(CB-20-12)  
Dimensions shown in millimeters

## ORDERING GUIDE

| Model <sup>1, 2</sup> | Integral Nonlinearity | No Missing Code | Temperature Range | Package Description | Package Option | Ordering Quantity |
|-----------------------|-----------------------|-----------------|-------------------|---------------------|----------------|-------------------|
| AD7699BCPZ            | ±1.5 LSB max          | 16 bits         | −40°C to +85°C    | 20-Lead LFCSP, Tray | CP-20-10       | 490               |
| AD7699BCPZRL7         | ±1.5 LSB max          | 16 bits         | −40°C to +85°C    | 20-Lead LFCSP, Reel | CP-20-10       | 1500              |
| AD7699BCBZ-RL7        | ±2.5 LSB max          | 16 bits         | −40°C to +85°C    | 20-Ball WLCSP       | CB-20-12       | Reel, 1,500       |
| AD7699BCBZ-WP         | ±2.5 LSB max          | 16 bits         | −40°C to +85°C    | 20-Ball WLCSP       | CB-20-12       |                   |
| EVAL-AD7699EDZ        |                       |                 |                   | Evaluation Board    |                |                   |
| EVAL-CED1Z            |                       |                 |                   | Controller Board    |                |                   |

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> The EVAL-CED1Z controller board allows a PC to control and communicate with all Analog Devices evaluation boards with model numbers ending in ED.

**NOTES**

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

⊖ View [AD7699BCPZ](#) on WIN SOURCE

⊖ [Analog Devices Inc.](#) Information

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