MIC2555

USB OTG Transceiver

Features

- Complies with USB-IF USB Standard 2.0 and OTG Supplement Revision 1.0a
- Provides Signaling and Control Logic for SRP and HNP, Enabling USB Dual-Role Device Operation
- Designed for Full-Speed and Low-Speed USB Communications
- I^2C Controller Interface
- Offers Three Modes of Operation:
  - USB
  - UART
  - Audio
- Operates with V_{LOGIC} of 1.6V to 4.5V, Assuring Compatibility with Low Voltage ASICs
- Tri-Level ID Detection for Recognition of USB and non-USB Devices
- Supports USB/Car Kit Audio Interface
- Allows Single-Ended and Differential Logic I/O
- Integrated Charge Pump for V_{BUS} Supply
- On-Chip Pull-Up, Pull-Down Resistors Minimize External Component Count
- Suspend and Power-Down Modes for Power Conservation
- Operates over the Full Industrial Temperature Range: –40°C to +85°C

Applications

- Cellular Telephones
- PDAs
- Digital Still Cameras
- Camcorders
- Data Cradles
- CD and MP3 players
- Printers

General Description

MIC2555 is a USB On-The-Go (OTG) transceiver designed to enable intelligent self-powered devices to communicate on a peer-to-peer basis with other USB and USB OTG enabled devices. Designed to perform as a PHY for USB Serial Interface Engines (SIE), MIC2555 is compatible with a wide variety of stand-alone OTG SIE chips, OTG IP cores (used in ASIC and COT designs), and Application Specific Standard Products (ASSPs).

MIC2555 is fully compliant to USB-IF's *Universal Serial Bus Specification 2.0* and the *On-the-Go Supplement Rev 1.0a*, for low-speed and full-speed operation, and allows dual-role device (DRD) operation via an I^2C-based controller interface. The controller's robust register set permits full control over bus and interface activity for transacting Session Request Protocol (SRP) and Host Negation Protocol (HNP) sequences.

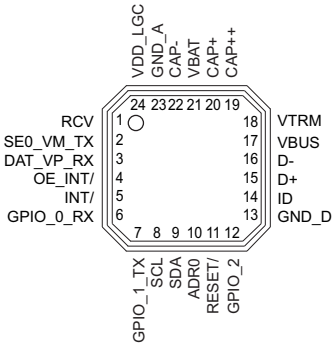
Messaging between Host and Target devices can utilize either USB or UART signaling methods. Additionally, the MIC2555 permits audio signaling on its D+, D–, and ID lines in support of analog car kit applications.

USB communication is complemented with on-chip D+, D– pull-up/pull-down resistors, an integrated charge pump and low dropout voltage regulators to provide stable internal supply voltages and to supply V_{BUS} power when operating as an A-device. Logic input levels spanning 1.6V to 4.5V ensure compatibility with current and future generations of process technology.

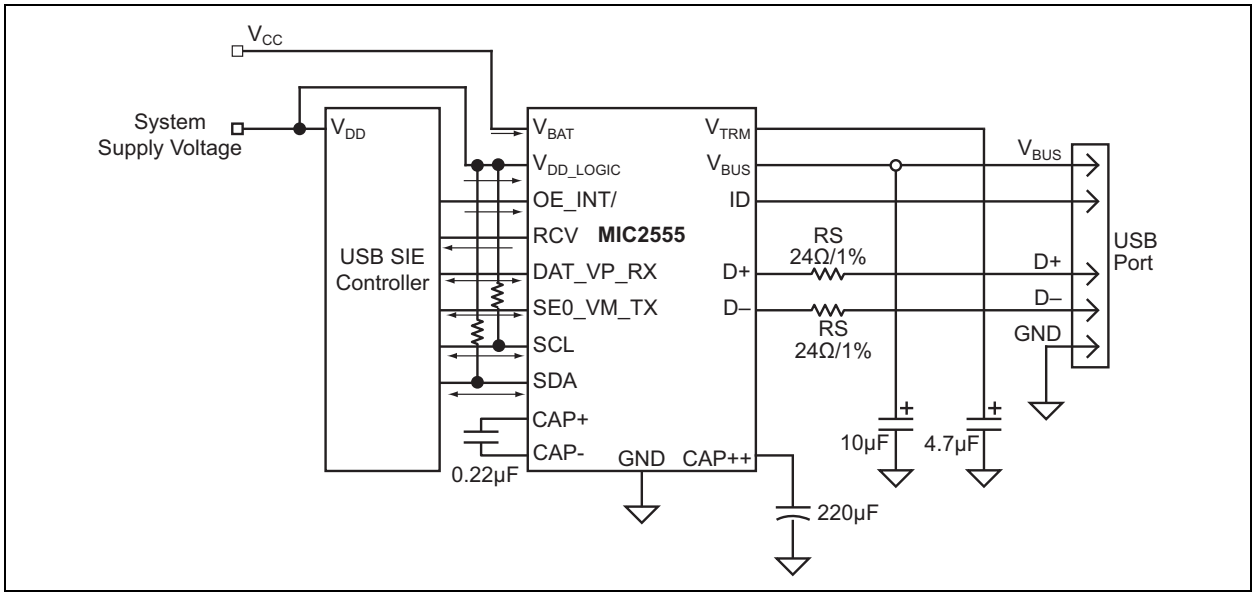
The MIC2555 is offered in a space-saving 4 mm x 4 mm 24-pin QFN package.

Package Type

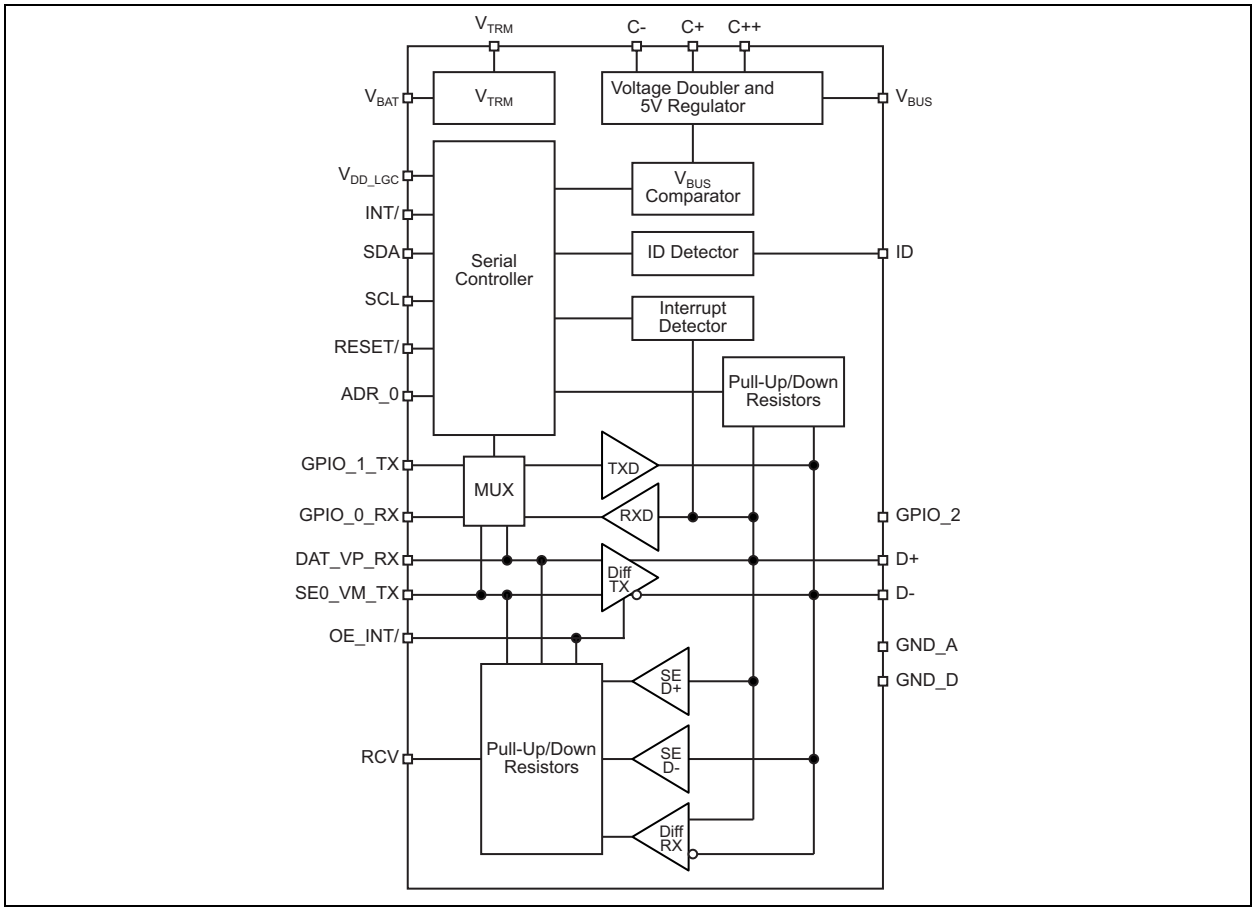
MIC2555
4x4 24-Lead QFN (ML)
(Top View)



Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Power Supply Voltage:
$V_{BAT, GPIO}$ ..... –0.3V to +6.0V
V_{DD_LGC} ..... –0.3V to +6.0V and ≤ V_{BAT}
USB Bus Voltage:
V_{BUS} ..... –0.3V to +6.0V
V_{DD_LGC} ..... –0.3V to +6.0V and ≤ V_{BUS}
Voltage on Any Other Pin ..... –0.3V to +4.5V
Current into/out of Any Pin ..... ±10 mA
ESD Rating, HBM (V_{BUS}, D+, D–, ID) ..... 8 kV
ESD Rating, HBM (All Other Pins) ..... 1.5 kV

Operating Ratings ††

Power Supply Voltage:
V_{BUS} ..... +4.4V to +5.25V
V_{BAT} ..... +3.0V to +4.5V

† Notice: Exceeding the absolute maximum ratings may damage the device.

†† Notice: The device is not guaranteed to function outside its operating ratings.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Test condition is +25°C unless otherwise specified. **Bold** values are valid for –40°C to +85°C, V_{BAT} = 3.6V, V_{DD_LGC} = 3.6V, V_{BUS} = 5.0V, V_{TRM} = 1 µF, C+ = 0.22 µF, C++ = 220 µF, C_{VBUS} = 10 µF. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supplies						
System Supply Voltage	V_{BAT}	**3.0**	—	**4.5**	V	—
Logic Supply Voltage	V_{DD_LGC}	**1.6**	—	**V_{BAT}**	V	—
Termination Voltage (Internal Supply Voltage)	V_{TRM}	**2.8**	3.3	**3.6**	V	I_{TRM} ≤ 2.5 mA, 3.0 < V_{BAT} < 3.6V
System Supply Current	I_{BAT_PD}	—	13	**20**	µA	Power Down mode
	I_{BAT_SUS}	—	140	**250**	µA	Suspend mode
	$I_{BAT\_FS\_I}$	—	2.8	**5.0**	mA	Full Speed, Idle, D+ ≥ 2.8V, D– ≤ 0.3V, I_{VBUS} = 0 mA
	$I_{BAT\_FS\_HC}$	—	17	**40**	mA	Full Speed Transmitting 12 Mb/s, C_{LOAD} ≤ 350 pF on D+, D–, I_{VBUS} = 0 mA
	$I_{BAT\_FS\_LC}$	—	2.5	**6**	mA	Full Speed Transmitting 12 Mb/s, C_L = 50 pF on D+,D-, I_{VBUS} = 0 mA
	$I_{BAT\_LS\_HC}$	—	6.5	**12**	mA	Low Speed Transmitting 1.5 Mb/s, C_L = 350 pF on D+,D-, I_{VBUS} = 0 mA

Note 1: Specification for packaged product only.
2: Parameters are guaranteed by design. They are not production tested.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Test condition is +25°C unless otherwise specified. **Bold** values are valid for –40°C to +85°C, V_{BAT} = 3.6V, V_{DD_LGC} = 3.6V, V_{BUS} = 5.0V, V_{TRM} = 1 µF, C+ = 0.22 µF, C++ = 220 µF, C_{VBUS} = 10 µF. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Current Drawn by System from V_{BUS}	I_{VBUS_S}	—	80	**100**	µA	Suspend mode, OE_INT/ = 1
Current Drawn by System for Core Logic	I_{VDD_LGC}	—	7	**15**	µA	OE_INT/ = 1
Charge Pump and V_{BUS}						
Voltage Output to V_{BUS}	V_{BUS_OUT}	**4.4**	5.0	**5.25**	V	I_{BUS} = 10 mA, V_{BAT} = 3.0V
V_{BUS} Output Current	I_{VBUS}	**10**	27	—	mA	4.4V ≤ V_{BUS} ≤ 5.25V
B Device SRP Pull-Up Resistor on V_{BUS}	R_{VBUS_PU}	**281**	1300	**7500**	Ω	Pull-up voltage = V_{TRM}
B Device SRP Pull-Down Resistor on V_{BUS}	R_{VBUS_PD}	675	2300	**7500**	Ω	Pull-down to GND
V_{BUS} Input Resistance	$R_{A\_BUS\_IN}$	**40**	63	**100**	kΩ	Seen from V_{BUS} pin to GND
'V_{BUS} Valid' Comparator Threshold Voltage	V_{TH_VBUS}	**4.4**	4.5	**4.6**	V	—
'Session Valid' Comparator Threshold Voltage	V_{TH_SV}	**0.8**	1.4	**2.0**	V	—
'Session End' Comparator Threshold Voltage	V_{TH_SE}	**0.2**	0.4	**0.8**	V	—
ID						
Upper Threshold for ID Resistor Sensing	$V_{THH\_R\_ID}$	**2.45**	2.55	**2.65**	V	V_{BAT} = 3.0V
Lower Threshold for ID Resistor Sensing	$V_{THL\_R\_ID}$	**0.35**	0.42	**0.55**	V	V_{BAT} = 3.0V
Pull-Up Resistor Switched to ID for Detecting Non-USB Devices	R_{ID_PU}	70	90	130	kΩ	—
Weak Pull-Up Current Source Driving ID Pin	I_{ID_WPU}	**2**	4	**6**	µA	V_{ID} = 0V
Interrupt Pulse Switch	$R_{ID\_SW\_GND}$	—	1.0	**4.0**	kΩ	V_{ID} ≤ 200 mV
Logic Levels - SDA, SCL, ADR0, OE_INT/, SE0_VM_TX, DAT_VP_RX, RCV, INT/, RESET/ & GPIO						
Low Level Input Voltage	V_{IL}	—	—	**0.3 x V_{DD_LGC}**	V	SDA, SCL
High Level Input Voltage	V_{IH}	**0.7 x V_{DD_LGC}**	—	—	V	
Input Hysteresis	—	**100**	—	—	mV	
Low Level Input Voltage	V_{IL}	—	—	**0.15 x V_{DD_LGC}**	V	ADR0, OE_INT/, SE0_VM_TX, DAT_VP_RX, RCV, INT/, RESET/ & GPIO Applies to USB and UART modes.
High Level Input Voltage	V_{IH}	**0.85 x V_{DD_LGC}**	—	—	V	

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Test condition is +25°C unless otherwise specified. **Bold** values are valid for –40°C to +85°C, V_{BAT} = 3.6V, V_{DD_LGC} = 3.6V, V_{BUS} = 5.0V, V_{TRM} = 1 µF, C+ = 0.22 µF, C++ = 220 µF, C_{VBUS} = 10 µF. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Leakage Current	I_{IN_LGC}	**–5**	—	**5**	µA	1.6V ≤ V_{DD_LGC} ≤ 4.5V
Low Level Output Voltage	V_{OL}	—	.02	**0.1**	V	I_{OL} = 100 µA
High Level Output Voltage	V_{OH}	**0.9 x V_{DD_LGC}**	—	—	V	I_{OH} = 100 µA
Low Level Output Voltage at SDA Pin	V_{OL_SDA}	—	—	**0.3 x V_{DD_LGC}**	V	I_{OL} = 5 mA
High Level Output Voltage at SDA Pin	V_{OH_SDA}	**0.7 x V_{DD_LGC}**	—	—	V	R_{SDA_PU} = 3.0 kΩ
Low Level Output Voltage at GPIO Pins	V_{OL_GPIO}	—	150	**250**	mV	I_{OL} = 10 mA
High Level Output Voltage at GPIO Pins	V_{OH_GPIO}	—	V_{DD_PU} – 0.1V	**V_{DD_PU}**	V	R_{PU} = 3.0 kΩ
GPIO Output Driver Leakage Current	I_{OH_GPIO}	—	1	**30**	µA	V_{DD_PU} = V_{OH_GPIO} = 5V
Transceiver DC Characteristics - D+, D-						
Differential Input Sensitivity	V_{DI}	**0.2**	—	—	V	|(D+) – (D-)|, V_{IN} = 0.8V – 2.5V
Differential Common-Mode Range	V_{CM}	**0.8**	—	**2.5**	V	Includes V_{DI} Range
Single-Ended Receiver Threshold	V_{TH_SE}	**0.8**	1.5	**2.0**	V	—
Receiver Hysteresis	V_{HYS}	—	200	—	mV	D+, D-
Low Level Output Voltage	V_{OL}	—	0.1	**0.3**	V	OE_INT/ = 0, R_L = 1.5 kΩ to 3.6V
High Level Output Voltage	V_{OH}	**2.8**	3.3	**3.6**	V	OE_INT/ = 0, I_{SOURCE} = 1 mA
Transceiver Output Resistance	R_{DRV}	**5**	12	**24**	Ω	D+, D-
Internal Pull-Up Resistor on D+ and D-	R_{PU_D}	**1.425**	2.25	**3.09**	kΩ	Active, V_{TRM} to D+ or D-
		0.900	1.24	**1.575**	kΩ	Idle, V_{TRM} to D+ or D-
Internal Pull-Down Resistor or D+ and D-	R_{PD_D}	14.3	19.5	24.8	kΩ	D+ to GND, D- to GND
Transceiver Input Capacitance	C_{IN_D}	—	—	20	pF	D+, D- pins to GND, Note 2
Interrupt Detector Threshold High	$V_{THL\_INT\_HI}$	**2.5**	3.0	**3.3**	V	—
Interrupt Detector Threshold Low	$V_{THL\_INT\_LO}$	**0.3**	0.5	**0.7**	V	—

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Test condition is +25°C unless otherwise specified. **Bold** values are valid for –40°C to +85°C, V_{BAT} = 3.6V, V_{DD_LGC} = 3.6V, V_{BUS} = 5.0V, V_{TRM} = 1 µF, C+ = 0.22 µF, C++ = 220 µF, C_{VBUS} = 10 µF. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Transceiver AC Characteristics - D+, D-						
Channel-to-Channel Isolation between D+, D- and ID Pins (in audio mode)	V_{C2C}	–60	—	—	dB	DC bias (pin to GND) = 0.4V AC signal = 600 mV_{PP} Freq. = 2 kHz Note 2
High-Z State Output Impedance	$Z_{OUT\_3S\_D}$	300	—	—	kΩ	0V < V_D < 3.6V, f = 2 kHz OE_INT/ = 1 Measured at D+, D- pins, with respect to GND Note 2
Data Rate						
I^2C Signaling Rate	F_{I2C}	**100**	400	—	kbps	V_{BAT} = 3.6V
		100	200	—		V_{BAT} = 3.0V
Driver Characteristics - Full Speed, T_A = +25°C						
Transition Rise/Fall Time	t_{R_FS}/t_{F_FS}	4	12.5	20	ns	C_L = 50 pF to 125 pF, Note 2
Rise/Fall Time Matching	t_R/t_F	90	—	111.11	%	(t_R/t_F)
Output Signal Crossover Voltage	V_{CRS}	1.3	—	2.0	V	—
Propagation Delay	t_{PLH}	—	—	18	ns	Low to High, Note 2
	t_{PHL}	—	—	18	ns	High to Low, Note 2
Driver Disable to Tri-State Delay, (Full or Low Speed)	t_{PDZ}	—	—	15	ns	High to Off, Note 2
		—	—	15	ns	Low to Off, Note 2
Driver Tri-State to Enable Delay, (Full or Low Speed)	t_{PZD}	—	—	15	ns	Off to High, Note 2
		—	—	15	ns	Off to Low, Note 2
Driver Characteristics - Low Speed, T_A = +25°C						
Transition Rise Time	t_{R_LS}	75	245	300	ns	C_L = 350 pF, Note 2
Transition Fall Time	t_{F_LS}	75	265	300	ns	C_L = 350 pF, Note 2
Rise/Fall Time Matching	t_R/t_F	80	90	125	%	(t_R/t_F)
Output Signal Crossover Voltage	V_{CRS}	1.3	1.7	2.0	V	—
Receiver Characteristics - Full Speed/Low Speed Differential Receiver						
Propagation Delay	t_{P_LH}	—	—	15	ns	Low to High, Note 2
	t_{P_HL}	—	—	15	ns	High to Low, Note 2
Single-Ended Receiver						
Propagation Delay	t_{P_LH}	—	—	18	ns	Low to High, Note 2
	t_{P_HL}	—	—	18	ns	High to Low, Note 2

Note 1: Specification for packaged product only.

2: Parameters are guaranteed by design. They are not production tested.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+125	°C	—
Maximum Junction Temperature	T_J	—	—	+150	°C	—
Operating Temperature Range	T_A	–40	—	+85	°C	—
Package Thermal Resistance						
Thermal Resistance, QFN 24-Ld	θ_{JA}	—	49	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: MIC2555 PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Description
1	RCV	O	Output from differential receiver.
2	SE0_VM_TX	I/O	= SE0 in USB DAT-SE0 mode = VM in VP-VM mode. = UART Transmit output when in UART Mode See Figure 2-1 and Figure 2-2.
3	DAT_VP_RX	I/O	= DAT in USB DAT-SE0 mode. = VP in VP-VM mode = UART Receive input when in UART mode See Figure 2-1 and Figure 2-2.
4	OE_INT/	I/O	A multi-mode pin controlling various functions in conjunction with control register bits. A logic low on this pin gives the following results: = OE (Output Enable): Enables D+, D- as USB outputs. = INT/ (Interrupt): Active-low output when register bits 'suspend' and 'oe_int_en' both = 1.
5	INT/	O	Interrupt (bar). Open-drain active-low output. May be wire-ORed with other interrupt signals.
6	GPIO_0_RX	I/O	= General purpose I/O. Open-drain output. = Alternate UART Receive input. See Figure 2-1 and Figure 2-2.
7	GPIO_1_TX	I/O	= General purpose I/O. Open-drain output. = Alternate UART Transmit output. See Figure 2-1 and Figure 2-2.
8	SCL	I/O	I^2C Clock
9	SDA	I/O	I^2C Data
10	ADR_0	I	Sets Address bit A0 of I^2C controller. This pin is a digital input and must not be left floating.
11	RESET/	I	System reset. Active-low.
12	GPIO_2	I/O	General purpose I/O. Open-drain output.
13	GND_D	I/O	System digital ground.
14	ID	I/O	Identification input. Monitors the ID pin of the USB connector and indicates both the presence of a device and type (USB or not USB).
15	D+	I/O	= USB D+ when in USB mode. = UART Receive in UART mode. = Right Speaker audio output in stereo mode. = Microphone signal from car kit.
16	D–	I/O	= USB D- when in USB mode. = UART Transmit out in UART mode. = Left Speaker audio output in stereo mode. = Monaural audio output to car kit.
17	VBUS	I/O	USB 5V power.
18	VTRM	I/O	Internal 3.3V supply. Sets USB signal levels.
19	CAP++	I	Positive lead for charge pump reservoir capacitor.
20	CAP+	I	Positive lead for charge pump capacitor.
21	VBAT	I	Positive voltage from battery. Supplies power to MIC2555 internal circuitry and power for charge pump when driving VBUS.

TABLE 2-1: MIC2555 PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Pin Type	Description
22	CAP–	I	Negative lead for charge pump capacitor.
23	GND_A	I	Analog ground. Isolated charge pump ground.
24	VDD_LGC	I	Logic supply voltage. Used to set logic levels between MIC2555 and System Controller/ASIC.

Interconnect Diagrams

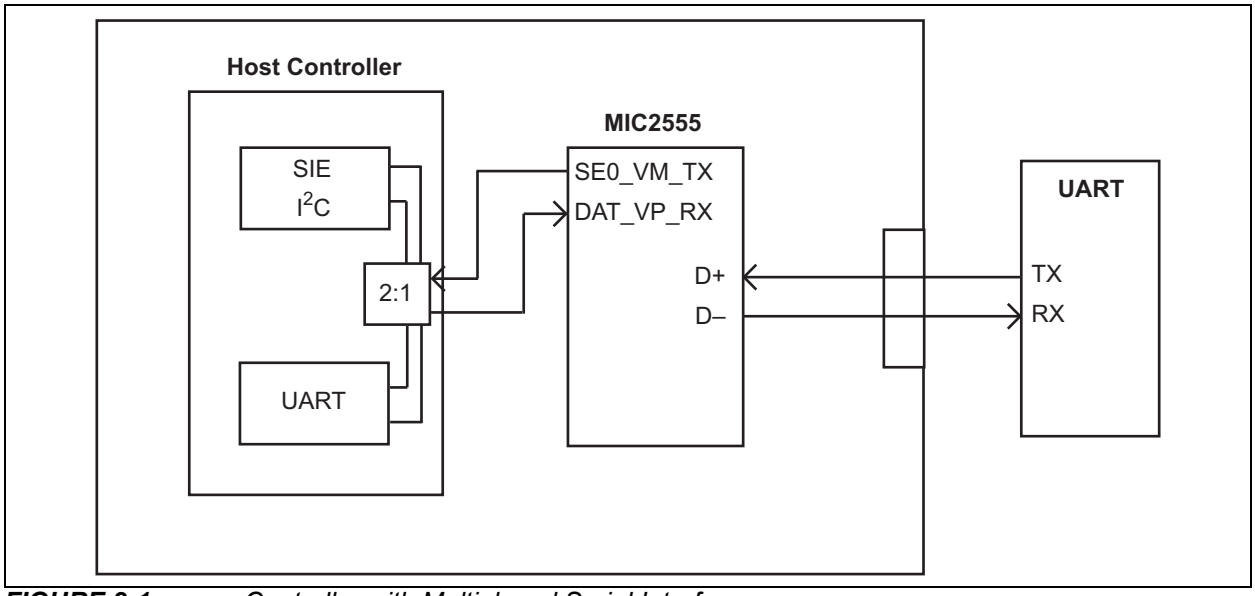


FIGURE 2-1: *Controller with Multiplexed Serial Interfaces.*

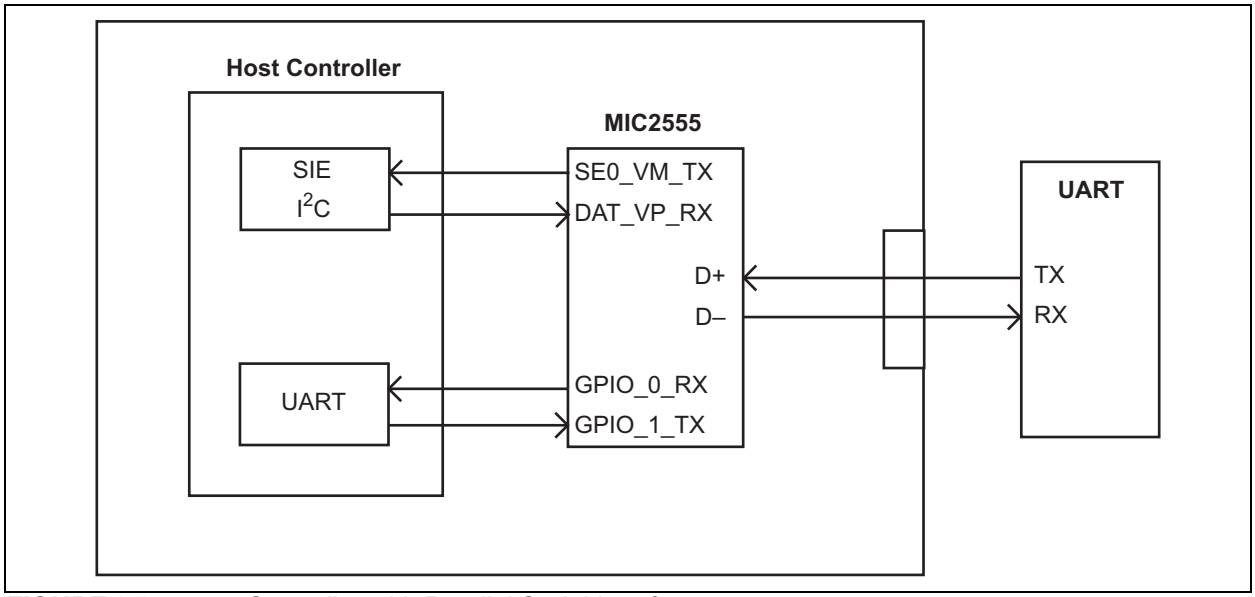


FIGURE 2-2: *Controller with Parallel Serial Interfaces.*

Note: Examples of a Host Controller include:
- Baseband Processor/IC
- µProcessor
- Modem

3.0 PIN DESCRIPTIONS

3.1 VBAT

This pin is an input and supplies power to the transceiver. Transceiver typical operational voltages are between $3.0V \le V_{BAT} \le 4.5V$ and $1.6V \le V_{DD\_LGC} \le V_{BAT}$.

3.2 VDD_LGC

This input is used to set the logic thresholds of the following logic signals:

- DAT_VP_RX
- SE0_VM_TX
- RCV
- OE_INT/
- INT/
- ADR0
- RESET/
- GPIO

It is important to note that V_{DD_LGC} can be at a voltage less than or equal to V_{BAT}, but never higher than V_{BAT}. Doing so will forward bias internal pad protection diodes and current will flow from V_{DD_LGC} to V_{BAT}. For this reason, systems should not allow V_{BAT} to go to zero while V_{DD_LGC} remains powered. This condition may damage the MIC2555 and could put a severe load on V_{DD_LGC} as it attempts to power the MIC2555 and all other circuits attached to the V_{BAT} line.

3.3 VBUS

This pin functions as both an input to, and output from, the transceiver. Unlike standard USB transceivers, however, the MIC2555 always derives its operating power from V_{BAT} and never from V_{BUS}. The MIC2555 will supply power to V_{BUS} when acting as a host device and when petitioning another OTG, capable device to become the host. To do so the vbus_chrg bit is asserted. To power V_{BUS}, as a host device, the vbus_drv bit is asserted. The difference between these two controls is vbus_chg applies V_{TRM} (3.3V) to V_{BUS}, whereas vbus_driv uses the 5V charge pump output. While V_{TRM} is sufficient for signaling purposes, it does not meet the 4.4V minimum for V_{BUS}.

3.4 VTRM

V_{TRM} supplies a regulated 3.3V to the D+, D- output drivers, pull-up resistors and other circuitry internal to the MIC2555. A small filter capacitor is required to insure the regulator remains stable under all operating conditions. A good quality 1 µF capacitor is sufficient for this purpose.

V_{TRM} can be used to supply small amounts of current to other system functions, typically 3 mA or less. However, trying to source more current can reduce output drive on D+, D- by stealing current from the differential driver.

3.5 ID

ID detects the arrival or departure of a peripheral device, and differentiates between USB and non-USB devices. To accomplish this, ID is pulled-up by a resistance of approximately 100 kΩ connected to V_{BAT} and the voltage at ID is monitored by a set of comparators. When no device is present, ID is pulled high and a NO DEVICE condition is reported. When a Mini-A plug is inserted into the system's Mini-AB receptacle, ID is connected to ground by the Mini-A plug, which triggers the MIC2555 to indicate a USB device is present.

Non-USB peripherals use a modified Mini-A plug or non-standard cable assembly with a resistor connected between ID and ground. When connected, this forms a resistor divider such that a voltage of approximately ½ V_{BAT} appears at MIC2555's ID pin, indicating a non-USB device is present.

Additionally, ID can be used to signal non-USB devices. This is accomplished by grounding ID through a low value resistor (~1 kΩ), dropping the ID voltage from ½ V_{BAT} to nearly zero, which can be detected by the attached device. This switch is activated by the id_gnd_out bit in Control Register 2.

3.6 C–, C+, C++

C-, C+, and C++ are the capacitors required for charge pump operation. C- and C+ are the connections to the 'flying' capacitor that creates the pumping effect. C++ is the reservoir capacitor that stores the 5V supplied to V_{BUS} when vbus_drv is asserted.

Because the input source is a low voltage and the charge pump's regulator is set to limit V_{OUT} to 5V, these capacitors need only be rated at 6V DC, which helps reduce physical size and cost.

3.7 GND_A, GND_D

MIC2555 uses separate ground lines within the chip to isolate digital noise from analog signals. Ultimately, these two grounds need to be tied together. This is best done by having both grounds return separately to the power source and join at the bypass capacitor.

3.8 RESET/

System reset returns all control register bits to their default settings. MIC2555 is not equipped with an internal power-on reset generator, and thus relies upon the system for its reset at power up.

3.9 DAT_VP_RX, SE0_VM_TX, RCV

DAT_VP_RX, SE0_VM_TX and RCV provide the data transfer interface between the system controller and MIC2555. RCV is an output only pin, supplying the output of a differential receiver monitoring the D+, D- pins, while DAT_VP_RX, SE0_VM_TX are bi-directional (I/O) pins and change function in accordance with different USB and UART mode selections.

In UART mode, DAT_VP_RX and SE0_VM_TX are the primary data transmit and receive pins.

In USB mode, the setting of the dat_se0 determines their action, as described in the tables of the Serial Controller section.

3.10 OE_INT/

The “output enable – interrupt bar” (OE_INT/) pin has three modes of operation, shown in the table below. Suspend modes are controlled by the oe_int_en bit found in Control Register 1.

TABLE 3-1: OE_INT/ OPERATING MODES

suspend	oe_int_en	I/O	Description
0	X	Input	OE_INT/ acts as output enable, and controls direction of DAT_VP_RX, SE0_VM_TX, D+, and D–.
1	0	Input	OE_INT/ is an input, but does not control anything.
1	1	Output	OE_INT/ is asserted low if interrupt condition exists.

3.11 SCL, SDA

The serial clock (SCL) and serial data (SDA) signals implement a two-wire I^2C serial bus for control of the MIC2555. As with all I^2C busses, the MIC2555 shares a common external pull-up resistor on each line.

3.12 INT/

The interrupt (INT/) pin is asserted while an interrupt condition exists. It is an open drain output so that it can be wire-ORed with other interrupt signals and requires an external pull-up resistor to provide a logic output. The pull-up voltage must not be greater than V_{BAT}.

3.13 ADR0

Because some systems may have more than one transceiver on the I^2C bus, OTG transceivers have been assigned four I^2C address locations by convention.

MIC2555 address: 01011xxb (Bit order: A6 to A0)

The ADR0 pin and MIC2555’s ‘dash number’ control the ‘xx’ of MIC2555’s address, where –0 or –1 specifies the higher order bit’s value where “x” indicates the state of ADR0.

TABLE 3-2: MIC2555 ADDRESS RANGE

Part Number	Address Range
MIC2555YML-0	0x
MIC2555YML-1	1x

3.14 D+, D–

The data plus (D+) and data minus (D–) pins output the USB data signals. When operating as a non-USB transceiver, the role of D+, D– changes.

In UART mode, D+ equals RXD and D– equals TXD.

3.15 GPIO_1_TX, GPIO_0_RX, GPIO_2

GPIO_0, GPIO_1, and GPIO_2 are general purpose I/Os that can be used as data ports or interrupt sources for the system controller, display drivers, or power switches for actuators or annunciators.

These GPIO have open-drain outputs capable of sinking at least 10 mA, can be wire ORed together, and may be pulled above the MIC2555’s operating supply voltage, but not beyond the 6V absolute maximum allowed. As logic inputs, the GPIO logic thresholds are standard CMOS thresholds set by V_{DD_LGC} voltage.

The GPIO Input Register is a read-only register and shows real-time status of the GPIOs, independent of other I/O settings. The GPIO Output Register holds the desired output value for each I/O. Each I/O can act as an independent interrupt source and can be programmed for triggering on T to F, F to T, or both transitions simultaneously.

The GPIO pins serve double duty as active signal pins when called into action by the appropriate control bit:

- GPIO_0 = Secondary UART Receive input.
- GPIO_1 = Secondary UART Transmit output.
- GPIO_2 = External charge pump oscillator input.

TABLE 3-3: AUDIO MODE

Pin	Mode	Notes
D+	Stereo	These are generally agreed upon, but are not mandatory.
D–		
D+	Mono	
D–	Mic.	

4.0 FUNCTIONAL DESCRIPTION

The MIC2555 is designed to provide full USB On-the-Go (OTG) connectivity in mobile systems where low power and small size are key considerations. Intended for use in self-powered systems, the MIC2555 draws no current from VBUS for its operation, but will supply a minimum of 10 mA at 5V to VBUS, from an on-chip charge pump, when operating as an A-device. The MIC2555 meets USB physical layer specifications while operating with logic supply voltages as low as 1.6V and battery voltages down to 3.0V.

MIC2555 operation is controlled through an I^2C bus by reading and/or writing to registers within the MIC2555. Control registers are used to set the operational mode to USB, Audio, or UART ('RS232' format). Other features include VBUS comparators for SRP detection and ID pin recognition of USB and non-USB peripherals.

The MIC2555 minimizes collateral components, requiring only four external capacitors and two resistors. All USB required pull-up/pull-down resistors are on-chip. 8 kV ESD protection on all pins exposed to user contact (VBUS, D+, D-, ID and GND) eliminates the need for external ESD transient protection devices.

4.1 Definitions and Conventions

- Car Kit: A non-USB target device
- I^2C: Inter IC Bus (I^2C)
- NUT: Non-USB target device
- OTG: On-The-Go (Note 1)
- SIE: Serial Interface Engine
- SE0: Single-Ended Zero
- SRP: Session Request Protocol
- USB: Universal Serial Bus
- USB-IF: USB Implementers Forum
- Serial Controller: Means the I^2C control function within MIC2555.
- UPPER CASE: IC pins
- Lower case: Control Register Bits

Note 1: An 'OTG Controller' is understood to be any integrated circuit, or system, possessing a built-in USB OTG Host/Device control function but lacking the USB physical layer interface.

5.0 SYSTEM DESCRIPTION

5.1 Overview

The MIC2555 OTG Transceiver provides the physical interface for ASICs, µPs, and SOCs that have an On-the-Go Serial Interface Engine (SIE), but that lack a physical interface capable of driving cables, or generating and detecting the necessary voltages to operate as a USB host.

MIC2555 goes beyond the confines of the USB OTG standard and provides flexible communication between many kinds of digital devices. Point-to-point UART and Audio communications can also be accomplished using the MIC2555 and any and all of these formats can be utilized by a single system.

All communications are accomplished via the D+ and D- I/O pins. The information passed through D+ and D-, such as USB, UART, or audio, depends upon the mode of communication. The system controls the mode of communication through the MIC2555's control registers.

5.2 Modes of Operation

The MIC2555 OTG Transceiver has three distinct operating modes:

- **USB mode:** Operates as a USB OTG transceiver.
- **UART mode:** Operates as a UART transceiver.
- **Audio mode:** Operates as a passive device within the audio path, but actively monitoring for digital control signals.

5.2.1 USB MODE

The two modes of USB operation involve the way data is transferred between the SIE and the transceiver. These modes are:

- **DAT-SE0 mode:**
  - DAT_VP_RX to.DAT: single ended data I/O
  - SE0_VM_TX to SEO: detects or sends the SE0 condition.
  - RCV is not used
- **VP-VM mode:**
  - DAT_VP_RX to VP: D+ data to transceiver output.
  - SE0_VM_TX to VM: D- data to transceiver output.
  - RCV to Output of the differential receiver.

Data flow direction:

Transmit to OE_INT/ = 0

Receive to OE_INT/ = 1

Conditions for USB mode:

uart_en = 0

Speed = Low speed =0

Full speed = 1

5.2.2 UART MODE

There are two UART modes of operation:

- **Direct UART**
  - UART TX to SE0_VM_TX pin, data is output on D-
  - UART RX from DAT_VP_RX pin receives UART data from D+
- **Secondary UART**
  - UART TX to GPIO_1_TX pin, data is output on D-
  - UART RX from GPOI_0_RX pin, received from D+

Conditions for UART mode:

uart_en = 1

speed = 1

uart_io = Direct UART = 0

Secondary UART inputs (GPIO) = 1

Note that it is not necessary to reset uart_io when switching from UART to USB mode; uart_io is deactivated when uart_en = 0, so its setting will not affect DAT_VP_RX or SE0_VM_TX's operation in USB mode.

5.2.3 AUDIO MODE

There is one mode of Audio operation. In audio mode, the MIC2555's D+ and D- outputs are tri-stated (high impedance) and the OTG controller or system components can send and receive audio signals via the D+, D- lines. The MIC2555 will monitor the D+ line for voltages crossing one of two levels, as a means of detecting a car kit interrupt signal. These interrupt events are captured and flagged by the Serial Controller.

Conditions:

uart_en = 0

OE_INT/ = 1

cr_int_sel = detect @ 3.0V = 1

detect @ 0.5V = 0

Note that the MIC2555 has no provision to connect or disconnect audio devices from the D+, D- lines, so the designer is cautioned to be sure that when the MIC2555 is operating as a data transceiver, no damage will ensue if the system's audio components are exposed to USB or UART digital signal levels.

5.3 Power Management

The transceiver's power modes are:

5.3.1 ACTIVE POWER

All functions active, transceiver fully powered.

Conditions:

suspend = 0

pwr_dn = 0

5.3.2 SUSPEND POWER

The differential transmitter and receiver are turned off to conserve power, but the USB interface is still active (i.e., pull-ups and pull-downs still active, VBUS generation on, etc.).

Conditions:

suspend = 1

pwr_dn = 0

5.3.3 POWER DOWN

Only the serial interface is still active and the transceiver is able to detect SRP. The ID pin sensing may be turned on or off with a control bit in the control registers.

Conditions:

suspend = 1

pwr_dn = 1

TABLE 5-1: POWER MANAGEMENT TABLE

Functions Powered Down by Control Bit	Control Bit		
	suspend	pwr_dn	cp_off
Differential Driver	X	—	—
Differential Receiver	X	—	—
UART TXD	X	—	—
D+ Interrupt Comparators	X	—	—
V_{BUS} Comparators	—	X	—
V_{TRM} LDO	—	X	—
VBUS Output	—	X	—
Internal Biasing Circuits and Band Gap Reference	—	X	—
Charge Pump Off	—	X	X

Note that the Suspend and Power-Down bits operate independently of each other. Activating Power-Down does not automatically invoke Suspend.

For lowest power operation, Suspend, Power-Down and Charge Pump OFF modes must be activated.

Conditions:

suspend = 1

pwr_dn = 1

cp_off = 1

Circuits still operating:

ID detect and D- receiver continue to function. This includes the ID comparators, ID pull-up circuits, and D- data receiver.

5.4 Serial Controller Block

The Serial Controller manages MIC2555 operations. Turning ON/OFF features, changing operating modes, setting and selecting interrupts are all handled by the Serial Controller. MIC2555's Serial Controller communicates with the OTG Controller as an I^2C slave using the SCL and SDA pins.

The Serial Controller includes the following functions:

- Control registers
- Status registers
- Interrupt latches
- Interrupt enable registers
- Interrupt clear registers
- Interrupt generator

5.5 VBUS Charge Pump and 5V Regulator

The charge pump draws power from VBAT and boosts the voltage to the requisite 5V to power VBUS. This subsystem is a combination of a charge pump circuit and a control loop that gates the charge pump's oscillator. If the output voltage is below 5V, then the oscillator is ON; otherwise, the oscillator is gated OFF. The charge pump's maximum output is controlled by the magnitude of V_{BAT}. When V_{BAT} is at 3.0V, the charge pump is designed to support loads of at least 8 mA on VBUS. As V_{BAT} increases, the maximum charge pump output current also increases. For proper operation the charge pump circuit requires two capacitors; one for the voltage doubler, connected between C- and C+, and a reservoir/filter capacitor between C++ and ground. The charge pump's nominal operating frequency is 200 kHz, which is set by an on-chip oscillator. A special feature of MIC2555 is that an external oscillator can drive the charge pump as well, allowing the designer to shift radiated noise away from sensitive frequencies when necessary. Also, when 5V power is not required from VBUS, the charge pump can be shut down to conserve power.

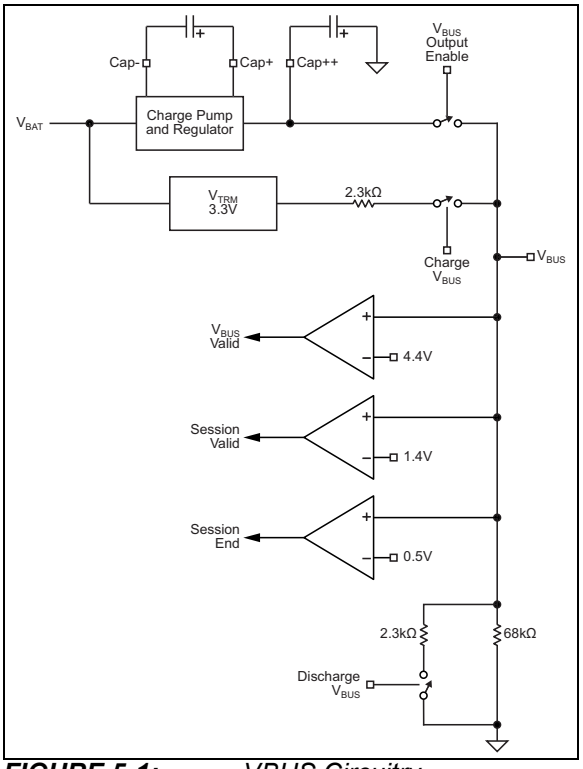


FIGURE 5-1: *VBUS Circuitry.*

5.6 VBUS Resistors and Switches

MIC2555 is able to:

- charge up VBUS through a resistor
- initiate SRP
- pull down VBUS through a resistor to ground
- discharge VBUS before initiating SRP
- switch VBUS power from the charge pump ON/OFF

Dedicated bits in the control registers control all of these functions. Because these bits act independently, it is possible to have VBUS both charging and discharging at the same time. This situation will not harm the MIC2555.

To prevent system leakage currents from biasing VBUS to a voltage that would mimic a session valid condition, the MIC2555 maintains a 68 kΩ resistor between VBUS and ground to ensure that at no time will VBUS assume a floating condition.

5.7 VBUS Comparators

VBUS comparators monitor the voltage level of VBUS. As described in the USB On-the-Go Supplement, VBUS not only supplies power but also is used to signal various operational conditions as part of the SRP protocol. Depending upon the voltage on VBUS, three states of operation can be defined:

- VBUS Valid
- Session Valid
- Session End

5.7.1 VBUS VALID COMPARATOR

This comparator is used by an A-device to determine whether the voltage on VBUS is at a valid level for operation. The minimum threshold for the VBUS valid comparator is 4.4V. Any voltage on VBUS below the threshold of the VBUS valid comparator is considered a fault. During power up, it is expected that this comparator's output will be ignored.

5.7.2 SESSION VALID COMPARATOR

The session valid comparator determines when V_{BUS} is high enough for a session to start. Both the A-device and B-device use this comparator to detect when a session is being started. The A-device also uses this comparator to indicate when a session is over.

The session valid window for an A-device is 0.8 to 2.0V while the session valid window for a B-device is 0.8 to 4.0V. Because these ranges overlap, the A-device window is typically chosen to service both requirements and a single comparator can be used. This is the case with MIC2555.

5.7.3 SESSION END COMPARATOR

The USB OTG Supplement specifies that a B-device cannot initiate SRP unless V_{BUS} is below the B-device Session End threshold of 0.8V. Monitoring VBUS with a comparator will give an exact and positive determination of when V_{BUS} has dropped below 0.8V, but the USB OTG supplement allows that the 0.8V limit can also be inferred, by discharging VBUS through a low value resistor for a predetermined period. The MIC2555 provides both a session-end comparator and a discharging resistor. To accommodate either technique, the designer can use them individually or, in concert as he so chooses.

5.8 Pull-Up/Down Resistors on D+/D–

MIC2555 supplies the pull-up and pull-down resistors for termination and signaling required by USB specifications. These resistors are integrated within the chip and switched into the circuit, as needed, via individual control bits in the control registers.

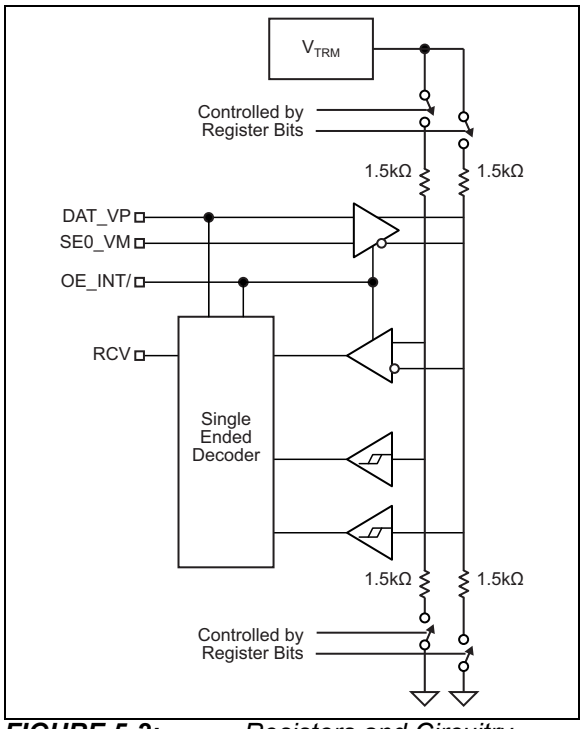


FIGURE 5-2: *Resistors and Circuitry Associated with D+, D– Pins.*

5.9 ID Detector

The ID function, defined within the USB On-the-Go supplement, represents a new addition to the USB standard. It is used to detect the presence or removal of a peripheral device as well as to differentiate between USB and non-USB peripherals. ID is unique to the mini-USB connectors and receptacles.

MIC2555's ID detector is operational in both the Active and Suspended power modes, and differentiates between three conditions:

TABLE 5-2: ID DETECTOR STATES

ID Pin Condition	Device Status	V_{ID}
Floating	No device present	$V_{ID} > 0.85V_{BAT}$
Grounded	USB device present	$V_{ID} < 0.15V_{BAT}$
Grounded through a Resistor	Non-USB device present	$0.15V_{BAT} < V_{ID} > 0.85V_{BAT}$

Here, “Grounded through a Resistor” means a resistor of a considerable value, typically 100 kΩ. The ID comparators are set to ignore the modest resistances contributed by the cables and connector contacts.

That a non-USB device is present (ID = resistive) is inferred from the interrupt register by the indication of an interrupt (ID has changed state) and that neither ID = GND or ID = Float are true. Viewing the Interrupt source register will give the real-time status of the ID comparator outputs. Viewing this register is necessary to determine the true state of affairs as insertion of the USB plug can produce multiple rail-to-rail transitions. These will trigger both comparators and produce a conflicting result: ID = GND and ID = Float. The Interrupt source register contains the debounced steady state value of ID.

After the nature of the newly connected device has been determined, activating a current source in series with the internal ID pull-up resistor can reduce power consumption caused by ID sensing. This is accomplished by clearing rcs_dis in Control Register 3.

When the connected device is removed, and the ID pin is pulled high by the current source (ID = GND is no longer true), MIC2555 automatically resets rcs_dis, disabling the current source.

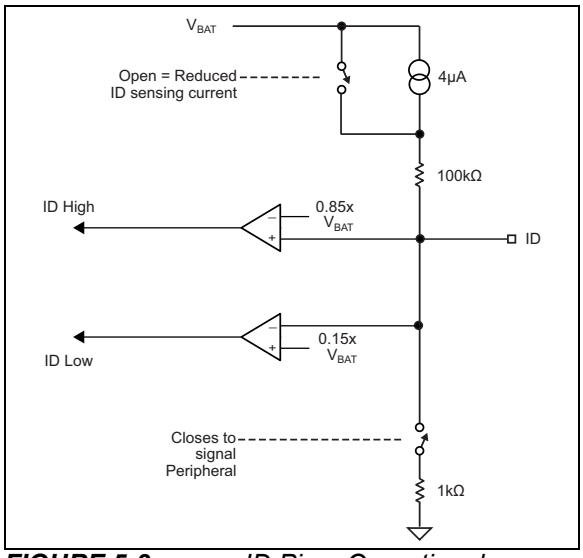


FIGURE 5-3: *ID Pin – Operational Diagram.*

5.10 VTRM

VBAT powers VTRM, which supplies 3.3V power to the differential USB transmitter and the UART drivers and receivers. As V_{BAT} drops below 3.4V, V_{TRM} is no longer able to regulate and follows V_{BAT} at about 0.1V less than V_{BAT}. When this occurs, output drive levels for USB and UART are reduced accordingly.

5.11 Interrupt Detector

When in Audio mode, the MIC2555 does not participate in the audio transmissions, but monitors the D+ line for interrupt pulses. If the Serial Controller is configured to flag interrupt pulses, the system controller can exchange both audio signals and digital information with the target device.

MIC2555 is designed to detect two different interrupt pulses, those exceeding 3.0V and those crossing the 0.5V level. Under normal circumstances, the audio signal seen on D+ is transposed on a DC level and limited to voltage excursions between the 0.5V and 3.0V levels, so only interrupt pulses should cross these thresholds. Signaling is typically done with only one polarity pulse so MIC2555 is designed to monitor only one threshold at a time. Threshold selection is done with the cr_int_sel bit, and the interrupt (cr_int) can be set to trigger on pulses of either polarity.

5.12 UART Mux

System controllers with UART communication ability may or may not be able to route their UART signals through the VP, VM or DAT, SE0 pins. For those with independent UART connectivity, MIC2555 provides a secondary UART I/O port. The MUX, under direction of the Serial Controller, selects which UART I/O is used by the OTG controller.

Condition:

uart_io = 0 SEO_VM_TX = transmit
DAT_VP_RX = receive
uart_io = 1 GPIO_1_TX = transmit
GPIO_0_RX = receive

5.13 Differential Driver/Differential Receiver

Operation of the Differential Driver and Differential Receiver is described in Table 5-3, Table 5-4, and Table 5-5. The register bits used in the column headings are described in the Serial Controller section of this data sheet.

TABLE 5-3: USB MODE: UART_EN = 0

suspend	dat_se0	OE_INT/	RCV	DAT_VP	SE0_VM	D+	D–
0	0	0	DIFF	TX data	TX data	DAT_VP	SE0_VM
0	0	1	DIFF	SE_DP	SE_DM	RX data	RX data
0	1	0	Z	TX data	TX data	TX_DAT	TX_SE0
0	1	1	Z	DIFF	DIFF	RX data	RX data
1	0	1	Z	SE_DP	SE_DM	RX data	RX data
1	1	1	Z	SE_DP	RX_SE0	RX data	RX data

DIFF = Differential receiver output

RX_SE0 = Not (SE_DP) and not (SE_DM)

TX_DAT = DAT_VP and not (SE0_VM)

TX_SE0 = Not (DAT_VP) and not (SE0_VM)

Z = Tri-State

TABLE 5-4: USB TRANSMIT OPERATION

USB Mode	Inputs		Outputs		
	DAT_VP_RX	SE0_VM_TX	D+	D–	RCV
DAT-SE0	0	0	0	1	unused
	1	0	1	0	unused
	0	1	0	0	unused
	1	1	0	0	unused
VP-VM	0	0	0	0	undefined
	1	0	1	0	1
	0	1	0	1	0
	1	1	1	1	undefined

The transceiver receives USB data from D+, D- lines when the following conditions are met:

Uart_en = 0

OE_INT/ = 0

Operation of the DAT_VP_RX, SE0_VM_TX and RCV pins during receive follows Table 5-5.

TABLE 5-5: USB RECEIVE OPERATION

USB Mode	Suspend	Inputs		Outputs		
		D+	D–	DAT_VP_RX	SE0_VM_TX	RCV
DAT-SE0	0	0	0	undefined	1	N/A
	0	1	0	1	0	N/A
	0	0	1	0	0	N/A
	0	1	1	undefined	0	N/A
	1	0	0	0	1	N/A
	1	1	0	1	0	N/A
	1	0	1	0	0	N/A
	1	1	1	1	0	N/A

TABLE 5-5: USB RECEIVE OPERATION (CONTINUED)

USB Mode	Suspend	Inputs		Outputs		
		D+	D–	DAT_VP_RX	SE0_VM_TX	RCV
VP-VM	0	0	0	0	0	undefined
	0	1	0	1	0	1
	0	0	1	0	1	0
	0	1	1	1	1	undefined
	1	0	0	0	0	N/A
	1	1	0	1	0	N/A
	1	0	1	0	1	N/A
	1	1	1	1	1	N/A

If the transceiver is in the DAT-SE0 mode, and the suspend bit has not been set, then the DAT_VP_RX pin always follows the output of the differential receiver during receive operation. The DAT_SE0 pin is not gated by the outputs of the single-ended receivers. In the VP-VM mode, the RVC pin always follows the output of the differential receiver. The RVC pin is not gated by the outputs of the singled ended receivers.

TABLE 5-6: UART MODE: UART_EN = 1

suspend	DAT_VP	SE0_VM	D+	D–
0	SE_DP	TX data	RX data	SE0_VM
1	Z	Z	Z	Z

Z = Tri-State

5.14 Single-Ended Receivers

The Single-Ended Receivers detect the logic levels on the D+ and D- lines and provide this information to the Single-Ended Decoder.

5.15 Single-Ended Decoder

Behavior of the Single-Ended Decoder is dependent upon the power mode of the transceiver. If the transceiver is in Suspend power mode, and dat_se0 = 1 (DAT-SE0 mode), then the DAT_VP_RX pin will reflect the output of the D+ single-ended receiver. This is necessary so that a controller connected to the transceiver can detect data pulsing while the transceiver is in suspended mode.

6.0 SERIAL CONTROLLER

TABLE 6-1: REGISTER MAP

Register Name	Address	Access	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Vendor ID	00	R	x8D							
	01	R	x05							
Product ID	02	R	xB0 (Note 1)							
	03	R	x55 (Note 1)							
Control Register 1	04	R/S	uart_io	uart_en	oe_int_en	bdis_acon_en	test bit	dat_se0	suspend	speed
	05	R/C								
Control Register 2	06	R/S	vbus_chrg	vbus_dis-chrg	vbus_drv	id_gnd_out	dm_pull-down	dp_pull-down	dm_pull-up	dp_pull-up
	07	R/C								
Interrupt Source	08	R	cr_int	bdis_acon (sess_end)	id_float	se_dm	id_gnd_in	se_dp	sess_vld	vbus_vld
Undefined	09	—	—	—	—	—	—	—	—	—
Interrupt Latch	0A	R/S	cr_int	bdis_acon (sess_end)	id_float	se_dm	id_gnd_in	se_dp	sess_vld	vbus_vld
	0B	R/C								
Interrupt Mask False	0C	R/S	cr_int	bdis_acon (sess_end)	id_float	se_dm	id_gnd_in	se_dp	sess_vld	vbus_vld
	0D	R/C								
Interrupt Mask True	0E	R/S	cr_int	bdis_acon (sess_end)	id_float	se_dm	id_gnd_in	se_dp	sess_vld	vbus_vld
	0F	R/C								
Undefined	10	—	—	—	—	—	—	—	—	—
	11	—								
Control Register 3	12	R/S	scl_en	rcs_dis	ext_osc	sess_end_en	cr_int_sel	id_det_off	cp_off	pwr_dn
	13	R/C								
GPIO Output Enable	14	R/S	0	0	0	0	0	GPIO_2	GPIO_1	GPIO_0
	15	R/C								
GPIO Output	16	R/S	0	0	0	0	0	GPIO_2	GPIO_1	GPIO_0
	17	R/C								
GPIO Input	18	R	0	0	0	0	0	GPIO_2	GPIO_1	GPIO_0
Undefined	19	—	—	—	—	—	—	—	—	—
GPIO Interrupt	1A	R/S	scl_en	rcs_dis	ext_osc	sess_end_en	cr_int_sel	id_det_off	cp_off	pwr_dn
	1B	R/C								
GPIO Mask False	1C	R/S	0	0	0	0	0	GPIO_2	GPIO_1	GPIO_0
	1D	R/C								
GPIO Mask True	1E	R/S	0	0	0	0	0	GPIO_2	GPIO_1	GPIO_0
	1F	R/C								

Note 1: These values will change with chip revision level and are assigned by Micrel at the time of manufacture.

2: All bits reset to zero, except those listed in **WHITE**, which reset to one.

3: Register bits not listed are undefined.

4: The upper five bits of the GPIO registers always read zero.

TABLE 6-2: CONTROL BIT LOCATOR

Control Bit	Location				
	Control Register 1	Control Register 2	Control Register 3	Interrupt Source	GPIO Interrupt
bdis_acon, (sess_end)	—	—	—	B6	—
bdis_acon_en	B4	—	—	—	—
cp_off	—	—	B1	—	—
cr_int	—	—	—	B7	—
cr_int_sel	—	—	B3	—	—
dat_se0	B2	—	—	—	—
dm_pull-down	—	B3	—	—	—
dm_pull-up	—	B1	—	—	—
dp_pull-down	—	B2	—	—	—
dp_pull-up	—	B0	—	—	—
ext_osc	—	—	B5	—	—
GPIO_0	—	—	—	—	B0
GPIO_1	—	—	—	—	B1
GPIO_2	—	—	—	—	B2
id_det_off	—	—	B2	—	—
id_float	—	—	—	B5	—
id_gnd_in	—	—	—	B3	—
id_gnd_out	—	B4	—	—	—
oe_int_en	B5	—	—	—	—
rcs_dis	—	—	B6	—	—
scl_en	—	—	B7	—	—
se_dm	—	—	—	B4	—
se_dp	—	—	—	B2	—
sess_end_en	—	—	B4	—	—
sess_vld	—	—	—	B1	—
pwr_dn	—	—	B0	—	—
speed	B0	—	—	—	—
suspend	B1	—	—	—	—
test bit	B3	—	—	—	—
uart_en	B6	—	—	—	—
uart_io	B7	—	—	—	—
vbus_chrg	—	B7	—	—	—
vbus_dischrg	—	B6	—	—	—
vbus_drv	—	B5	—	—	—
vbus_vld	—	—	—	B0	—

6.1 Serial Controller Register Bits

In the table below, “Access” type “rd/s/c” denotes a field that can be read, set to 1, or cleared to 0. The register can be read from either of the Addresses indicated. When writing to the “set” Address, any 1s that are written cause the associated bit to be set. When writing to the “clr” (Clear) address, any 1s that are written cause the associated bit to be cleared.

TABLE 6-3: SERIAL CONTROLLER REGISTER BITS

Field Name	Size (bits)	Access	Register Address(es)	Description
Device ID Registers				
—	—	—	—	MSB: Higher byte of two byte word LSB: Lower byte of two byte word
vendor_id	16	rd	00h	USB-IF Vendor ID number. Address 00h contains lower byte of Vendor ID. Address 01h contains upper byte of Vendor ID.
product_id	16	rd	02h	A number unique to each manufacturer, for each device type produced. The manufacturer assigns this number. Address 02h contains lower byte. Address 03h contains upper byte.
Control Register 1				
Set & Clear	—	—	set – 04h clr – 05h	1 to set = 1 1 to clr = 0
speed	1	rd/s/c	bit 0	0 = USB Low Speed mode 1 = USB Full Speed mode
suspend	1	rd/s/c	bit 1	0 = Full power mode 1 = Low power mode
dat_se0	1	rd/s/c	bit 2	0 = VP-VM USB mode 1 = DAT-SE0 USB mode
test bit	1	rd/s/c	bit 3	Not used
bdis_acon_en	1	rd/s/c	bit 4	0 = No action. 1 = Attaches pull-up resistor to D+ after detecting SE0 condition and sets interrupt flag.
oe_int_en	1	rd/s/c	bit 5	0 = OE_INT/ is an input. 1 = OE_INT/ becomes an output and is asserted low when interrupt occurs, if suspend = 1. If suspend = 0, pin remains an input.
uart_en	1	rd/s/c	bit 6	0 = USB mode 1 = UART mode
uart_io	1	rd/s/c	bit 7	0 = GPIO pins operate as standard GPIO. 1 = GPIO_0 = 2nd UART RX GPIO_1 = 2nd UART TX GPIO_2 = standard GPIO
Control Register 2				
Set & Clear	—	—	set – 06h clr – 07h	1 to set = 1 1 to clr = 0
dp_pull-up	1	rd/s/c	bit 0	1 = Connect pull-up to D+
dm_pull-up	1	rd/s/c	bit 1	1 = Connect pull-up to D-
dp_pull-down	1	rd/s/c	bit 2	1 = Connect pull-down to D+
dm_pull-down	1	rd/s/c	bit 3	1 = Connect pull-down to D-
id_gnd_out	1	rd/s/c	bit 4	1 = Connect ID pin to ground
vbus_drv	1	rd/s/c	bit 5	1 = Power VBUS with charge pump
vbus_dischrg	1	rd/s/c	bit 6	1 = Discharge VBUS through a resistor

TABLE 6-3: SERIAL CONTROLLER REGISTER BITS (CONTINUED)

Field Name	Size (bits)	Access	Register Address(es)	Description
vbus_chrg	1	rd/s/c	bit 7	1 = Charge VBUS through a resistor
Control Register 3				
Set & Clear	—	—	set – 12h clr – 13h	1 to set = 1 1 to clr = 0
pwr_dn	1	rd/s/c	bit 0	1 = Power Down mode.
cp_off	1	rd/s/c	bit 1	1 = Turns charge pump OFF. (Charge pump generates 5V for powering V_{BUS})
id_det_off	1	rd/s/c	bit 2	0 = ID comparators ON. 1 = Turns ID comparators OFF. Note: Powering down ID comparators does not shut off ID pin pull-up.
cr_int_sel	1	rd/s/c	bit 3	Car Kit interrupt select: 0 = Detect < 0.5V level on D+ 1 = Detect > 3.0V level on D+
sess_end_en	1	rd/s/c	bit 4	0 = No action. 1 = When bdis_acon_en = 0, switches Bit 6 of the Interrupt Register to indicate Session End comparator status.
ext_osc	1	rd/s/c	bit 5	0 = Internal oscillator drives charge pump 1 = External oscillator drives charge pump (Input source = GPIO_2)
rcs_dis	1	rd/s/c	bit 6	0 = Activate current source. Weak pull-up on ID pin. 1 = Disable (bypass) current source pull-up on ID pin. Strong pull-up on ID pin.
scl_en	1	rd/s/c	bit 7	0 = I^2C clock line only transmits. 1 = Bi-directional I^2C clock line. Bi-directional clock is required if target device is to be able to control data rate by holding SCL low.
Interrupt Source Register				
Interrupt Status	—	—	rd - 08h	Indicates the current state of signals that can generate an interrupt.
vbus_vld	1	rd	bit 0	1 = V_{BUS} > 4.4V (VBUS valid comparator)
sess_vld	1	rd	bit 1	1 = 0.8V < V_{BUS} < 2.0V. (Session valid comparator)
se_dp	1	rd	bit 2	1 = D+ pin is HIGH
id_gnd_in	1	rd	bit 3	1 = ID pin grounded
se_dm	1	rd	bit 4	1 = D- pin is HIGH
id_float	1	rd	bit 5	1 = ID pin floating
bdis_acon (sess_end)	1	rd	bit 6	If: bdis_acon_en = 1 1 = SE0 has been detected, transceiver asserted dp_pullup after detecting B-device disconnect. If bdis_acon_en = 0, sess_end_en = 1 1 = V_{BUS} < 0.8V. (Session End comparator output = TRUE)
cr_int	1	rd	bit 7	1 = Car kit interrupt, D+ pin has seen a pulse above the interrupt level

TABLE 6-3: SERIAL CONTROLLER REGISTER BITS (CONTINUED)

Field Name	Size (bits)	Access	Register Address(es)	Description
Interrupt Latch 1				
Interrupt Source	—	—	set - 0Ah clr - 0Bh	Indicates which sources have interrupted. 1 = interrupt.
vbus_vld	1	rd/s/c	bit 0	—
sess_vld	1	rd/s/c	bit 1	—
se_dp	1	rd/s/c	bit 2	—
id_gnd_in	1	rd/s/c	bit 3	—
se_dm	1	rd/s/c	bit 4	—
id_float	1	rd/s/c	bit 5	—
bdis_acon (sess_end)	1	rd/s/c	bit 6	—
cr_int	1	rd/s/c	bit 7	—
Interrupt Mask False				
False Interrupt Mask	—	—	set - 0Ch clr - 0Dh	Enables interrupts on transition from TRUE to FALSE 1 to set = 1, Interrupt on T to F. 1 to clr = 0, no interrupt.
vbus_vld	1	rd/s/c	bit 0	—
sess_vld	1	rd/s/c	bit 1	—
se_dp	1	rd/s/c	bit 2	—
id_gnd_in	1	rd/s/c	bit 3	—
se_dm	1	rd/s/c	bit 4	—
id_float	1	rd/s/c	bit 5	—
bdis_acon (sess_end)	1	rd/s/c	bit 6	—
cr_int	1	rd/s/c	bit 7	—
Interrupt Mask True				
True Interrupt Mask	—	—	set - 0Eh clr - 0Fh	Enables interrupts on transition from FALSE to TRUE 1 to set = 1, Interrupt on F to T. 1 to clr = 0, no interrupt.
vbus_vld	1	rd/s/c	bit 0	—
sess_vld	1	rd/s/c	bit 1	—
se_dp	1	rd/s/c	bit 2	—
id_gnd_in	1	rd/s/c	bit 3	—
se_dm	1	rd/s/c	bit 4	—
id_float	1	rd/s/c	bit 5	—
bdis_acon (sess_end)	1	rd/s/c	bit 6	—
cr_int	1	rd/s/c	bit 7	—
GPIO Output Enable				
Set & Clear	—	—	set - 14h clr - 15h	1 to set = 1, GPIO = OUTPUT. 1 to clr = 0, GPIO = INPUT.
GPIO_0	1	rd/s/c	bit 0	—
GPIO_1	1	rd/s/c	bit 1	—
GPIO_2	1	rd/s/c	bit 2	—
—	1	rd/s/c	bit 3	—
—	1	rd/s/c	bit 4	—

TABLE 6-3: SERIAL CONTROLLER REGISTER BITS (CONTINUED)

Field Name	Size (bits)	Access	Register Address(es)	Description
—	1	rd/s/c	bit 5	—
—	1	rd/s/c	bit 6	—
—	1	rd/s/c	bit 7	—
GPIO Output				
Set & Clear	—	—	set - 16h clr - 17h	1 to set = 1 at GPIO OUTPUT. 1 to clr = 0 at GPIO OUTPUT.
GPIO_0	1	rd/s/c	bit 0	—
GPIO_1	1	rd/s/c	bit 1	—
GPIO_2	1	rd/s/c	bit 2	—
—	1	rd/s/c	bit 3	—
—	1	rd/s/c	bit 4	—
—	1	rd/s/c	bit 5	—
—	1	rd/s/c	bit 6	—
—	1	rd/s/c	bit 7	—
GPIO Input				
Read Status	—	—	rd - 18h	Read current state of GPIO input
GPIO_0	1	rd	bit 0	—
GPIO_1	1	rd	bit 1	—
GPIO_2	1	rd	bit 2	—
—	1	rd	bit 3	—
—	1	rd	bit 4	—
—	1	rd	bit 5	—
—	1	rd	bit 6	—
—	1	rd	bit 7	—
GPIO Interrupt Latch				
Set & Clear	—	—	set - 1Ah clr - 1Bh	Indicates which sources have interrupted. 1 = interrupt.
GPIO_0	1	rd/s/c	bit 0	—
GPIO_1	1	rd/s/c	bit 1	—
GPIO_2	1	rd/s/c	bit 2	—
—	1	rd/s/c	bit 3	—
—	1	rd/s/c	bit 4	—
—	1	rd/s/c	bit 5	—
—	1	rd/s/c	bit 6	—
—	1	rd/s/c	bit 7	—
GPIO Interrupt Mask False				
Set & Clear	—	—	set - 1Ch clr - 1Dh	Enables interrupts on transition from TRUE to FALSE 1 to set = 1, Interrupt on T to F. 1 to clr = 0, no interrupt.
GPIO_0	1	rd/s/c	bit 0	—
GPIO_1	1	rd/s/c	bit 1	—
GPIO_2	1	rd/s/c	bit 2	—
—	1	rd/s/c	bit 3	—
—	1	rd/s/c	bit 4	—

TABLE 6-3: SERIAL CONTROLLER REGISTER BITS (CONTINUED)

Field Name	Size (bits)	Access	Register Address(es)	Description
—	1	rd/s/c	bit 5	—
—	1	rd/s/c	bit 6	—
—	1	rd/s/c	bit 7	—
GPIO Interrupt Mask True				
Set & Clear	—	—	set - 1Eh clr - 1Fh	Enables interrupts on transition from FLASE to TRUE 1 to set = 1, Interrupt on F to T. 1 to clr = 0, no interrupt.
GPIO_0	1	rd/s/c	bit 0	—
GPIO_1	1	rd/s/c	bit 1	—
GPIO_2	1	rd/s/c	bit 2	—
—	1	rd/s/c	bit 3	—
—	1	rd/s/c	bit 4	—
—	1	rd/s/c	bit 5	—
—	1	rd/s/c	bit 6	—
—	1	rd/s/c	bit 7	—

Remember that Access type “rd/s/c” denotes a field that can be read, set to 1 or cleared to 0. The register can be read from either of the Addresses indicated. When writing to the “set” Address, any 1’s that are written cause the associated bit to be set. When writing to the “clr” (Clear) Address, any 1s that are written cause the associated bit to be cleared.

6.2 Example Serial Controller Register Settings

TABLE 6-4: EXAMPLE

Location	Condition	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Target register	Initial state	0	0	1	0	1	0	0	0
‘Set’ register	Data loaded into ‘set’ register	1	0	0	0	1	0	0	0
Target register	Resulting state	1	0	1	0	1	0	0	0
‘Clear’ register	Data loaded into ‘clear’ register	1	0	0	0	1	0	0	0
Target register	Resulting state	0	0	1	0	0	0	0	0

7.0 PCB LAYOUT RECOMMENDATIONS

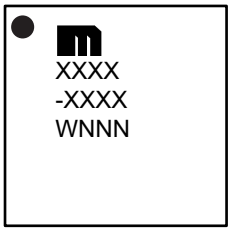
Although the USB standard and applications are not based in an impedance-controlled environment, a properly designed PCB layout is recommended for optimal transceiver performance. The suggested PCB layout hints are as follows:

- Match signal line traces (VP/VM, D+, D–) and try to keep them as short as possible.
- For every signal line trace width (w), separate the signal lines by 1.5 to 2 widths. Place all other traces at >2 widths from all signal line traces.
- Control signal line impedances to ±10%.
- Keep R_{SERIES} as close to the IC as possible, with equal distance between R_{SERIES} and the IC for both D+ and D–.

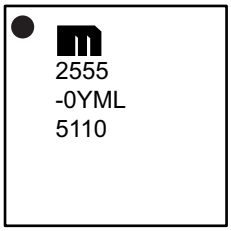
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

24-Lead QFN*



Example

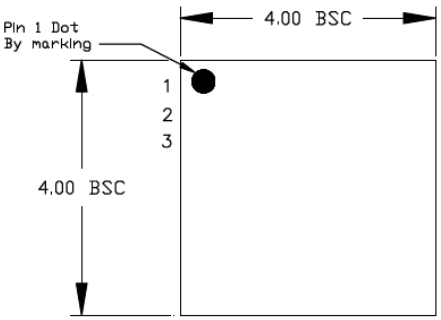


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

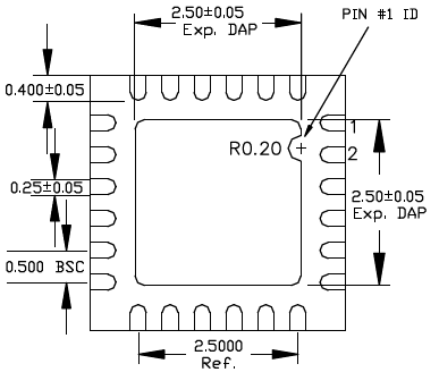
24-Lead QFN 4 mm x 4 mm Package Outline and Recommended Land Pattern

TITLE
24 LEAD QFN 4x4mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN44-24LD-PL-1	UNIT	MM

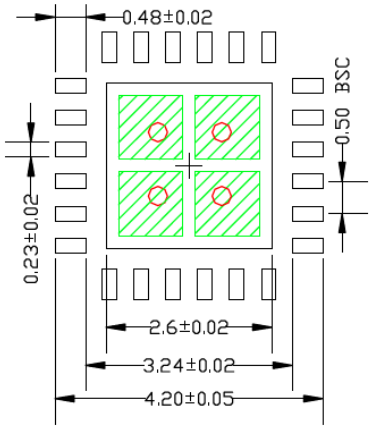


TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3

SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) Indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 1.00x1.00 MM IN SIZE, 1.20 MM PITCH.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (March 2019)

- Converted Micrel document MIC2555 to Microchip data sheet template DS20006182A.
- Minor grammatical text changes throughout.
- Updated ESD Rating values in the Absolute Maximum Ratings † section.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	-X	X	XX	-XX
Part No.	Address	Junction Temp. Range	Package	Media Type

Device:	MIC2555:	USB OTG Transceiver
Address:	0 = 0x 1 = 1x	
Junction Temperature Range:	Y =	–40°C to +85°C
Package:	ML =	24-Lead QFN
Media Type:	TR =	5,000/Reel

Examples:

a) MIC2555-0YML-TR: MIC2555, 0x Address, –40°C to +85°C Temperature Range, 24-Lead QFN, 5,000/Reel

b) MIC2555-1YML-TR: MIC2555, 1x Address, –40°C to +85°C Temperature Range, 24-Lead QFN, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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