THE DATASHEET OF

AD7679ASTZ

18-Bit, 2.5 LSB INL, 570 kSPS SAR ADC

AD7679

FEATURES

18-bit resolution with no missing codes
No pipeline delay (SAR architecture)
Differential input range: ±V_{REF} (V_{REF} up to 5 V)
Throughput: 570 kSPS
INL: ±2.5 LSB max (±9.5 ppm of full scale)
Dynamic range : 103 dB typ (V_{REF} = 5 V)
S/(N+D): 100 dB typ @ 2 kHz (V_{REF} = 5 V)
Parallel (18-,16-, or 8-bit bus) and serial 5 V/3 V interface
SPI®/QSPI™/MICROWIRE™/DSP compatible
On-board reference buffer
Single 5 V supply operation
Power dissipation: 76 mW @ 500 kSPS
150 µW @ 1 kSPS
48-lead LQFP or 48-lead LFCSP package
Pin-to-pin compatible upgrade of AD7674/AD7676/AD7678

APPLICATIONS

CT scanners
High dynamic data acquisition
Geophone and hydrophone sensors
Σ-Δ replacement (low power, multichannel)
Instrumentation
Spectrum analysis
Medical instruments

FUNCTIONAL BLOCK DIAGRAM

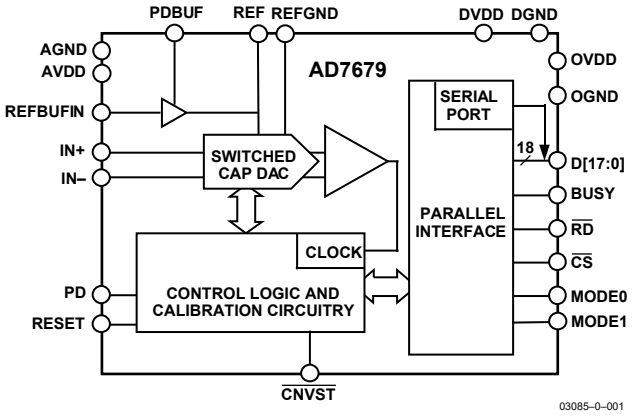

Figure 1. Functional Block Diagram

Table 1. PulSAR Selection

Type/kSPS	100–250	500–570	800–1000
Pseudo-Differential	AD7651 AD7660/AD7661	AD7650/AD7652 AD7664/AD7666	AD7653 AD7667
True Bipolar	AD7663	AD7665	AD7671
True Differential	AD7675	AD7676	AD7677
18-Bit	AD7678	AD7679	AD7674
Multichannel/ Simultaneous		AD7654 AD7655	

GENERAL DESCRIPTION

The AD7679 is an 18-bit, 570 kSPS, charge redistribution SAR, fully differential analog-to-digital converter that operates on a single 5 V power supply. The part contains a high speed 18-bit sampling ADC, an internal conversion clock, an internal reference buffer, error correction circuits, and both serial and parallel system interface ports.

The part is available in a 48-lead LQFP or 48-lead LFCSP with operation specified from –40°C to +85°C.

PRODUCT HGHLIGHTS

1. High Resolution, Fast Throughput.
   The AD7679 is a 570 kSPS, charge redistribution, 18-bit SAR ADC (no latency).
2. Excellent Accuracy.
   The AD7679 has a maximum integral nonlinearity of 2.5 LSB with no missing 18-bit codes.
3. Serial or Parallel Interface.
   Versatile parallel (18-, 16-, or 8-bit bus) or 3-wire serial interface arrangement compatible with both 3 V and 5 V logic.

Rev. B

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REVISION HISTORY

8/2020—Rev. A to Rev. B

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6/2009—Rev. 0 to Rev. A

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7/2003—Revision 0: Initial Version

SPECIFICATIONS

–40°C to +85°C, V_{REF} = 4.096 V, AVDD = DVDD= 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		18			Bits
ANALOG INPUT					
Voltage Range	$V_{IN+} - V_{IN-}$	$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage	V_{IN+}, V_{IN-} to AGND	–0.1		AVDD+0.1	V
Analog Input CMRR	f_{IN} = 100 kHz		68		dB
Input Current	570 kSPS Throughput		25		µA
Input Impedance[1]					
THROUGHPUT SPEED					
Complete Cycle				1.75	µs
Throughput Rate		0		570	kSPS
DC ACCURACY					
Integral Linearity Error		–2.5		+2.5	LSB[2]
Differential Linearity Error		–1		+1.75	LSB
No Missing Codes		18			Bits
Transition Noise	V_{REF} = 5 V		0.7		LSB
Zero Error, T_{MIN} to T_{MAX}		–40		+40	LSB
Zero Error Temperature Drift			±0.5		ppm/°C
Gain Error, T_{MIN} to T_{MAX}[3]		–0.048	See Note 3	+0.048	% of FSR
Gain Error Temperature Drift			±1.6		ppm/°C
Power Supply Sensitivity	AVDD = 5 V ± 5%		±4		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 2 kHz, V_{REF} = 5 V		101		dB[4]
	V_{REF} = 4.096 V	97.5	99		dB
	f_{IN} = 10 kHz, V_{REF} = 4.096 V		98		dB
	f_{IN} = 100 kHz, V_{REF} = 4.096 V		97		dB
Dynamic Range	$V_{IN+} = V_{IN-} = V_{REF}/2$ = 2.5 V		103		dB
Spurious-Free Dynamic Range	f_{IN} = 2 kHz		120		dB
	f_{IN} = 10 kHz		118		dB
	f_{IN} = 100 kHz		105		dB
Total Harmonic Distortion	f_{IN} = 2 kHz		–115		dB
	f_{IN} = 10 kHz		–113		dB
	f_{IN} = 100 kHz		–98		dB
Signal-to-(Noise + Distortion)	f_{IN} = 2 kHz, V_{REF} = 4.096 V		98		dB
	f_{IN} = 2 kHz, –60 dB Input		40		dB
–3 dB Input Bandwidth			26		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			250	ns
Overvoltage Recovery				250	ns
REFERENCE					
External Reference Voltage Range	REF	3	4.096	AVDD + 0.1	V
REF Voltage with Reference Buffer	REFBUFIN = 2.5 V	4.05	4.096	4.15	V
Reference Buffer Input Voltage Range	REFBUFIN	1.8	2.5	2.6	V
REFBUFIN Input Current		–1		+1	µA
REF Current Drain	570 kSPS Throughput		235		µA

Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}		2.0		DVDD + 0.3	V
I_{IL}		–1		+1	µA
I_{IH}		–1		+1	µA
DIGITAL OUTPUTS					
Data Format[5]					
Pipeline Delay[6]					
V_{OL}	ISINK = 1.6 mA			0.4	V
V_{OH}	ISOURCE = –500 µA	OVDD – 0.6			V
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		DVDD + 0.3[7]	V
Operating Current	500 kSPS Throughput				
AVDD	PDBUF High		10.8		mA
DVDD[8]			4.5		mA
OVDD[8]			50		µA
POWER DISSIPATION[8]	PDBUF High @ 500 kSPS		76	90	mW
	PDBUF High @ 1 kSPS		150		µW
	PDBUF Low @ 500 kSPS		89	103	mW
TEMPERATURE RANGE[9]					
Specified Performance	TMIN to TMAX	–40		+85	°C

[1] See Analog Inputs section.
[2] LSB means Least Significant Bit. With the ±4.096 V input range, 1 LSB is 31.25 µV.
[3] See Definition of Specifications section. The nominal gain error is not centered at zero and is –0.029% of FSR. This specification is the deviation from this nominal value. These specifications do not include the error contribution from the external reference, but do include the error contribution from the reference buffer if used.
[4] All specifications in dB are referred to a full-scale input, FS. Tested with an input signal at 0.5 dB below full scale unless otherwise specified.
[5] Parallel or Serial 18-Bit.
[6] Conversion results are available immediately after completed conversion.
[7] The max should be the minimum of 5.25 V and DVDD + 0.3 V.
[8] Tested in Parallel Reading mode.
[9] Contact factory for extended temperature range.

TIMING SPECIFICATIONS

–40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
Refer to Figure 33 and Figure 34					
Convert Pulsewidth	t_1	10			ns
Time between Conversions	t_2	1.75			µs
$\overline{\text{CNVST}}$ LOW to BUSY HIGH Delay	t_3			35	ns
BUSY HIGH All Modes Except Master Serial Read after Convert	t_4			1.5	µs
Aperture Delay	t_5		2		ns
End of Conversion to BUSY LOW Delay	t_6	10			ns
Conversion Time	t_7			1.5	µs
Acquisition Time	t_8	250			ns
RESET Pulsewidth	t_9	10			ns
Refer to Figure 35, Figure 36, and Figure 37 (Parallel Interface Modes)					
$\overline{\text{CNVST}}$ LOW to Data Valid Delay	t_{10}			1.5	µs
Data Valid to BUSY LOW Delay	t_{11}	20			ns
Bus Access Request to Data Valid	t_{12}			45	ns
Bus Relinquish Time	t_{13}	5		15	ns
Refer to Figure 39 and Figure 40 (Master Serial Interface Modes) [1]					
$\overline{\text{CS}}$ LOW to SYNC Valid Delay	t_{14}			10	ns
$\overline{\text{CS}}$ LOW to Internal SCLK Valid Delay	t_{15}			10	ns
$\overline{\text{CS}}$ LOW to SDOUT Delay	t_{16}			10	ns
$\overline{\text{CNVST}}$ LOW to SYNC Delay	t_{17}		525		ns
SYNC Asserted to SCLK First Edge Delay[2]	t_{18}	3			ns
Internal SCLK Period[2]	t_{19}	25		40	ns
Internal SCLK HIGH[2]	t_{20}	12			ns
Internal SCLK LOW[2]	t_{21}	7			ns
SDOUT Valid Setup Time[2]	t_{22}	4			ns
SDOUT Valid Hold Time[2]	t_{23}	2			ns
SCLK Last Edge to SYNC Delay[2]	t_{24}	3			ns
$\overline{\text{CS}}$ HIGH to SYNC HI-Z	t_{25}			10	ns
$\overline{\text{CS}}$ HIGH to Internal SCLK HI-Z	t_{26}			10	ns
$\overline{\text{CS}}$ HIGH to SDOUT HI-Z	t_{27}			10	ns
BUSY HIGH in Master Serial Read after Convert[2]	t_{28}		See Table 4		
$\overline{\text{CNVST}}$ LOW to SYNC Asserted Delay	t_{29}		1.5		µs
SYNC Deasserted to BUSY LOW Delay	t_{30}		25		ns
Refer to Figure 41 and Figure 42 (Slave Serial Interface Modes)					
External SCLK Setup Time	t_{31}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{32}	3		18	ns
SDIN Setup Time	t_{33}	5			ns
SDIN Hold Time	t_{34}	5			ns
External SCLK Period	t_{35}	25			ns
External SCLK HIGH	t_{36}	10			ns
External SCLK LOW	t_{37}	10			ns

[1] In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.
[2] In Serial Master Read during Convert mode. See Table 4 for Serial Master Read after Convert mode.

Table 4. Serial Clock Timings in Master Read after Convert

DIVSCLK[1] **DIVSCLK[0]**	**Symbol**	**0** **0**	**0** **1**	**1** **0**	**1** **1**	**Unit**
SYNC to SCLK First Edge Delay Minimum	t_{18}	3	17	17	17	ns
Internal SCLK Period Minimum	t_{19}	25	60	120	240	ns
Internal SCLK Period Maximum	t_{19}	40	80	160	320	ns
Internal SCLK HIGH Minimum	t_{20}	12	22	50	100	ns
Internal SCLK LOW Minimum	t_{21}	7	21	49	99	ns
SDOUT Valid Setup Time Minimum	t_{22}	4	18	18	18	ns
SDOUT Valid Hold Time Minimum	t_{23}	2	4	30	89	ns
SCLK Last Edge to SYNC Delay Minimum	t_{24}	3	60	140	300	ns
Busy High Width Maximum	t_{28}	2.25	3	4.5	7.5	µs

ABSOLUTE MAXIMUM RATINGS

Table 5.AD7679 Absolute Maximum Ratings[1]

Parameter	Rating
Analog Inputs	
IN+[2], IN–[2], REF, REFBUFIN, REFGND to AGND	AVDD + 0.3 V to AGND – 0.3 V
Ground Voltage Differences	
AGND, DGND, OGND	±0.3 V
Supply Voltages	
AVDD, DVDD, OVDD	–0.3 V to +7 V
AVDD to DVDD, AVDD to OVDD	±7 V
DVDD to OVDD	–0.3 V to +7 V
Digital Inputs	–0.3 V to DVDD + 0.3 V
Internal Power Dissipation[3]	700 mW
Internal Power Dissipation[4]	2.5 W
Junction Temperature	150°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	300°C

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] See Analog Inputs section.
[3] Specification is for device in free air: 48-Lead LQFP: θ_{JA} = 91°C/W, θ_{JC} = 30°C/W.
[3] Specification is for device in free air: 48-Lead LFCSP: θ_{JA} = 26°C/W.

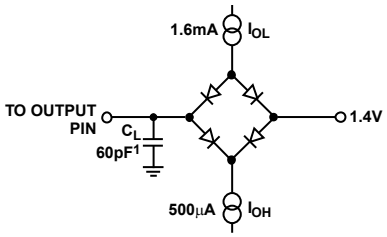


Figure 2. Load Circuit for Digital Interface Timing SDOUT, SYNC, SCLK Outputs, C_L = 10 pF

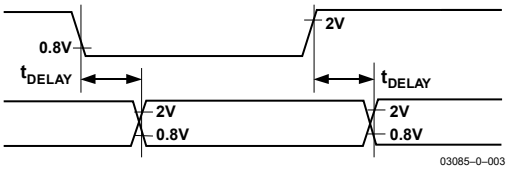
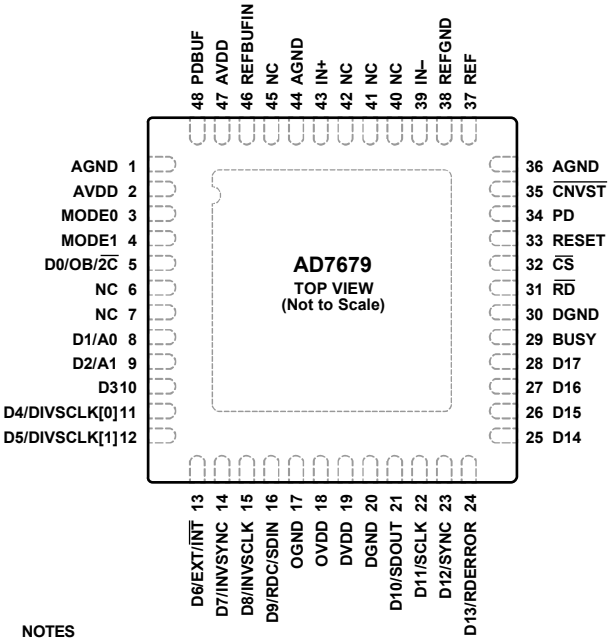


Figure 3. Voltage Reference Levels for Timing

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

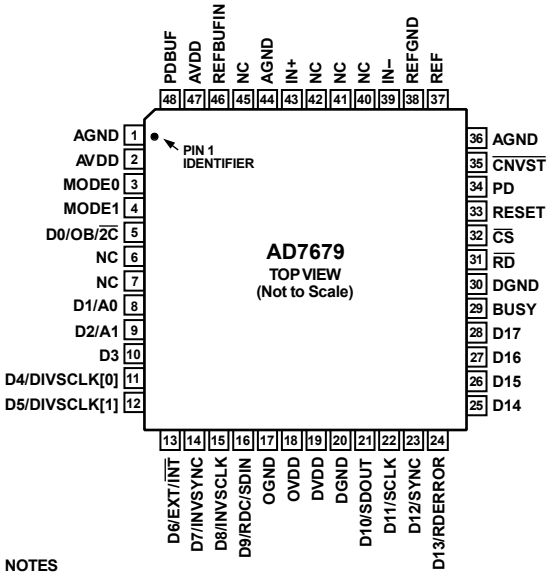
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD IS INTERNALLY CONNECTED TO AGND. THIS CONNECTION IS NOT REQUIRED TO MEET THE ELECTRICAL PERFORMANCES HOWEVER, FOR INCREASED RELIABILITY OF THE SOLDER JOINTS, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE ANALOG GROUND OF THE SYSTEM.

03085-050

Figure 4. 48-Lead LFCSP Pin Configuration



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD IS INTERNALLY CONNECTED TO AGND. THIS CONNECTION IS NOT REQUIRED TO MEET THE ELECTRICAL PERFORMANCES HOWEVER, FOR INCREASED RELIABILITY OF THE SOLDER JOINTS, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE ANALOG GROUND OF THE SYSTEM.

03085-004

Figure 5. 48-Lead LQFP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 44	AGND	P	Analog Power Ground Pin.
2, 47	AVDD	P	Input Analog Power Pins. Nominally 5 V.
3	MODE0	DI	Data Output Interface Mode Selection.
4	MODE1	DI	Data Output Interface Mode Selection:

Interface MODE	MODE1	MODE0	Description
0	0	0	18-Bit Interface
1	0	1	16-Bit Interface
2	1	0	Byte Interface
3	1	1	Serial Interface

5	D0/OB/$\overline{2C}$	DI/O	When MODE = 0 (18-bit interface mode), this pin is Bit 0 of the parallel port data output bus and the data coding is straight binary. In all other modes, this pin allows choice of straight binary/binary twos complement. When OB/$\overline{2C}$ is HIGH, the digital output is straight binary; when LOW, the MSB is inverted, resulting in a twos complement output from its internal shift register.
6, 7, 40–42, 45	NC		No Connect.
8	D1/A0	DI/O	When MODE = 0 (18-bit interface mode), this pin is Bit 1 of the parallel port data output bus. In all other modes, this input pin controls the form in which data is output, as shown in Table 7.
9	D2/A1	DI/O	When MODE = 0 or 1 (18-bit or 16-bit interface mode), this pin is Bit 2 of the parallel port data output bus. In all other modes, this input pin controls the form in which data is output, as shown in Table 7.
10	D3	DO	In all modes except MODE = 3, this output is used as Bit 3 of the parallel port data output bus. This pin is always an output, regardless of the interface mode.
11, 12	D[4:5]or DIVSCLK[0:1]	DI/O	In all modes except MODE = 3, these pins are Bit 4 and Bit 5 of the parallel port data output bus. When MODE = 3 (serial mode), EXT/$\overline{INT}$ is LOW, and RDC/SDIN is LOW (serial master read after convert), these inputs, part of the serial port, are used to slow down, if desired, the internal serial clock that clocks the data output. In other serial modes, these pins are not used.

Pin No.	Mnemonic	Type[1]	Description
13	D6 or EXT/$\overline{INT}$	DI/O	In all modes except MODE = 3, this output is used as Bit 6 of the parallel port data output bus. When MODE = 3 (serial mode), this input, part of the serial port, is used as a digital select input for choosing the internal data clock or an external data clock. With EXT/$\overline{INT}$ tied LOW, the internal clock is selected on the SCLK output. With EXT/$\overline{INT}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	D7 or INVSYNC	DI/O	In all modes except MODE = 3, this output is used as Bit 7 of the parallel port data output bus. When MODE = 3 (serial mode), this input, part of the serial port, is used to select the active state of the SYNC signal. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.
15	D8 or INVSCLK	DI/O	In all modes except MODE = 3, this output is used as Bit 8 of the parallel port data output bus. When MODE = 3 (serial mode), this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave mode.
16	D9 or RDC/SDIN	DI/O	In all modes except MODE = 3, this output is used as Bit 9 of the parallel port data output bus. When MODE = 3 (serial mode), this input, part of the serial port, is used as either an external data input or a read mode selection input depending on the state of EXT/$\overline{INT}$. When EXT/ $\overline{INT}$ is HIGH, RDC/SDIN could be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 18 SCLK periods after the initiation of the read sequence. When EXT/$\overline{INT}$ is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output on SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Output Interface Digital Power. Nominally at the same supply as the host interface (5 V or 3 V). Should not exceed DVDD by more than 0.3 V.
19	DVDD	P	Digital Power. Nominally at 5 V.
20	DGND	P	Digital Power Ground.
21	D10 or SDOUT	DO	In all modes except MODE = 3, this output is used as Bit 10 of the parallel port data output bus. When MODE = 3 (serial mode), this output, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The AD7679 provides the conversion result, MSB first, from its internal shift register. The data format is determined by the logic level of OB/$\overline{2C}$. In serial mode when EXT/$\overline{INT}$ is LOW, SDOUT is valid on both edges of SCLK. In serial mode when EXT/$\overline{INT}$ is HIGH and INVSCLK is LOW, SDOUT is updated on the SCLK rising edge and is valid on the next falling edge; if INVSCLK is HIGH, SDOUT is updated on the SCLK falling edge and is valid on the next rising edge.
22	D11 or SCLK	DI/O	In all modes except MODE = 3, this output is used as Bit 11 of the parallel port data output bus. When MODE = 3 (serial mode), this pin, part of the serial port, is used as a serial data clock input or output, dependent upon the logic state of the EXT/$\overline{INT}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK pin.
23	D12 or SYNC	DO	In all modes except MODE = 3, this output is used as Bit 12 of the parallel port data output bus. When MODE = 3 (serial mode), this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock (EXT/$\overline{INT}$ = Logic LOW). When a read sequence is initiated and INVSYNC is LOW, SYNC is driven HIGH and remains HIGH while the SDOUT output is valid. When a read sequence is initiated and INVSYNC is HIGH, SYNC is driven LOW and remains LOW while SDOUT output is valid.
24	D13 or RDERROR	DO	In all modes except MODE = 3, this output is used as Bit 13 of the parallel port data output bus. In MODE = 3 (serial mode) and when EXT/ $\overline{INT}$ is HIGH, this output, part of the serial port, is used as an incomplete read error flag. In slave mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed high.
25–28	D[14:17]	DO	Bit 14 to Bit 17 of the Parallel Port Data Output Bus. These pins are always outputs regardless of the interface mode.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started. Remains HIGH until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY could be used as a data ready clock signal.
30	DGND	P	Must Be Tied to Digital Ground.
31	$\overline{RD}$	DI	Read Data. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{CS}$	DI	Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the AD7679. Current conversion, if any, is aborted. If not used, this pin could be tied to DGND.

Pin No.	Mnemonic	Type[1]	Description
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current one is completed.
35	$\overline{\text{CNVST}}$	DI	Start Conversion. If $\overline{\text{CNVST}}$ is held HIGH when the acquisition phase (t_8) is complete, the next falling edge on $\overline{\text{CNVST}}$ puts the internal sample/hold into the hold state and initiates a conversion. If $\overline{\text{CNVST}}$ is held LOW when the acquisition phase is complete, the internal sample/hold is put into the hold state and a conversion is started immediately.
36	AGND	P	Must Be Tied to Analog Ground.
37	REF	AI	Reference Input Voltage and Internal Reference Buffer Output. Apply an external reference on this pin if the internal reference buffer is not used. Should be decoupled effectively with or without the internal buffer.
38	REFGND	AI	Reference Input Analog Ground.
39	IN–	AI	Differential Negative Analog Input.
43	IN+	AI	Differential Positive Analog Input.
46	REFBUFIN	AI	Reference Buffer Input Voltage. The internal reference buffer has a fixed gain. It outputs 4.096 V typically when 2.5 V is applied on this pin.
48	PDBUF	DI	Allows Choice of Buffering Reference. When LOW, buffer is selected. When HIGH, buffer is switched off.
49 (EPAD)	Exposed Pad (EPAD)		The exposed pad is internally connected to AGND. This connection is not required to meet the electrical performances however, for increased reliability of the solder joints, it is recommended that the pad be soldered to the analog ground of the system.

[1]AI = Analog Input; AO = Analog Output; DI = Digital Input; DI/O = Bidirectional Digital; DO = Digital Output; P = Power.

Table 7. Data Bus Interface Definitions

MODE	MODE1	MODE0	D0/OB/$\overline{\text{2C}}$	D1/A0	D2/A1	D[3]	D[4:9]	D[10:11]	D[12:15]	D[16:17]	Description
0	0	0	R[0]	R[1]	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	18-Bit Parallel
1	0	1	OB/$\overline{\text{2C}}$	A0:0	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	16-Bit High Word
1	0	1	OB/$\overline{\text{2C}}$	A0:1	R[0]	R[1]	All Zeros				16-Bit Low Word
2	1	0	OB/$\overline{\text{2C}}$	A0:0	A1:0	All Hi-Z		R[10:11]	R[12:15]	R[16:17]	8-Bit HIGH Byte
2	1	0	OB/$\overline{\text{2C}}$	A0:0	A1:1	All Hi-Z		R[2:3]	R[4:7]	R[8:9]	8-Bit MID Byte
2	1	0	OB/$\overline{\text{2C}}$	A0:1	A1:0	All Hi-Z		R[0:1]	All Zeros		8-Bit LOW Byte
2	1	0	OB/$\overline{\text{2C}}$	A0:1	A1:1	All Hi-Z		All Zeros		R[0:1]	8-Bit LOW Byte
3	1	1	OB/$\overline{\text{2C}}$	All Hi-Z			Serial Interface				Serial Interface

R[0:17] is the 18-bit ADC value stored in its output register.

DEFINITION OF SPECIFICATIONS

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Gain Error
The first transition (from 000…00 to 000…01) should occur for an analog voltage ½ LSB above the nominal –full scale (–4.095991 V for the ±4.096 V range). The last transition (from 111…10 to 111…11) should occur for an analog voltage 1½ LSB below the nominal full scale (4.095977 V for the ±4.096 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Zero Error
The zero error is the difference between the ideal midscale input voltage (0 V) from the actual voltage producing the midscale output code.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input, and is expressed in bits. It is related to S/(N+D) by the following formula:

$$ENOB = (S/[N+D]dB - 1.76)/6.02$$

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal, and is expressed in decibels.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (S/[N+D])
S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

Aperture Delay
Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the $\overline{\text{CNVST}}$ input to when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the AD7679 to achieve its rated accuracy after a full-scale step function is applied to its input.

TYPICAL PERFORMANCE CHARACTERISTICS

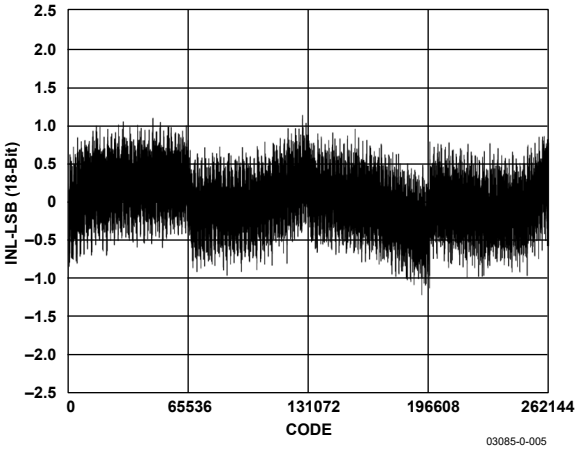


Figure 6. Integral Nonlinearity vs. Code

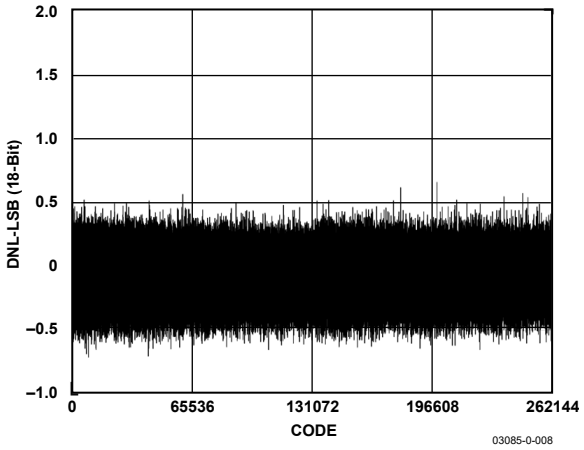


Figure 9. Differential Nonlinearity vs. Code

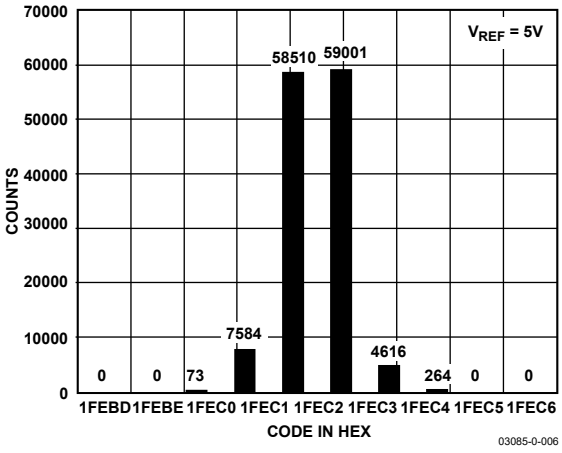


Figure 7. Histogram of 131,072 Conversions of a DC Input at the Code Transition

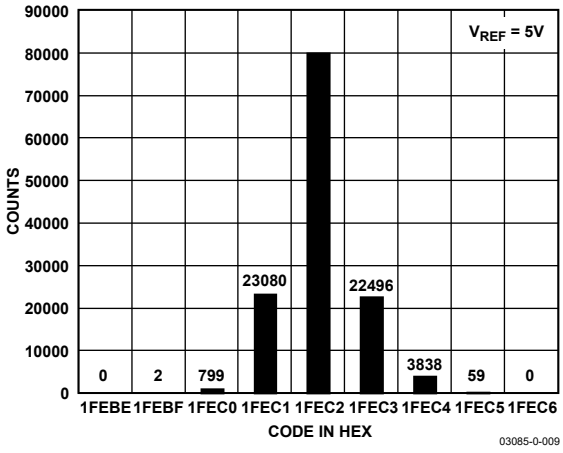


Figure 10. Histogram of 131,072 Conversions of a DC Input at the Code Center

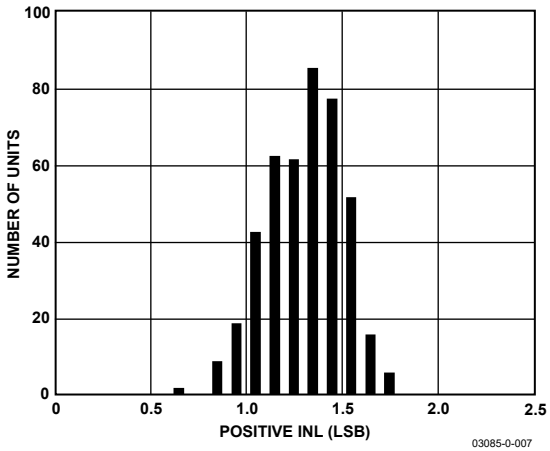


Figure 8. Typical Positive INL Distribution (424 Units)

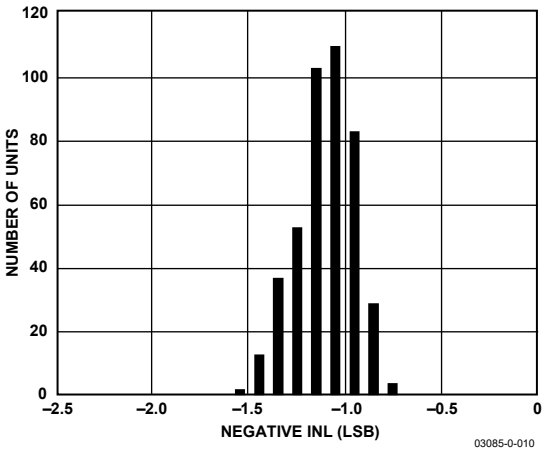


Figure 11. Typical Negative INL Distribution (424 Units)

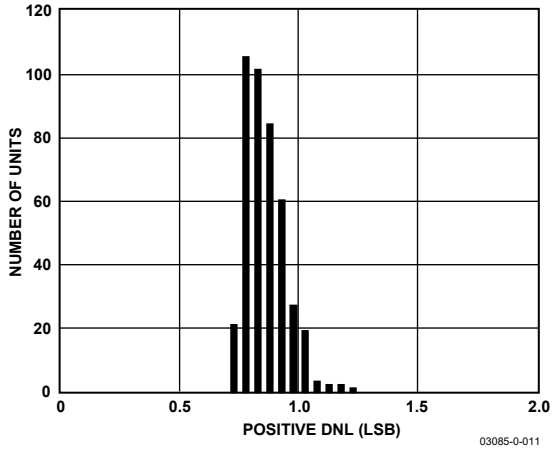


Figure 12. Typical Positive DNL Distribution (424 Units)

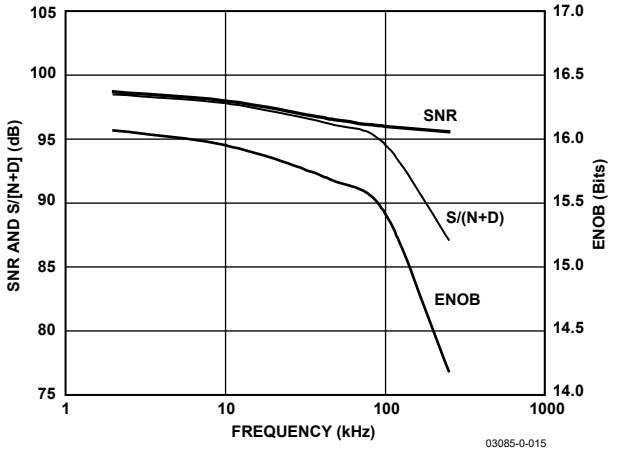


Figure 15. SNR, S/(N+D), and ENOB vs. Frequency

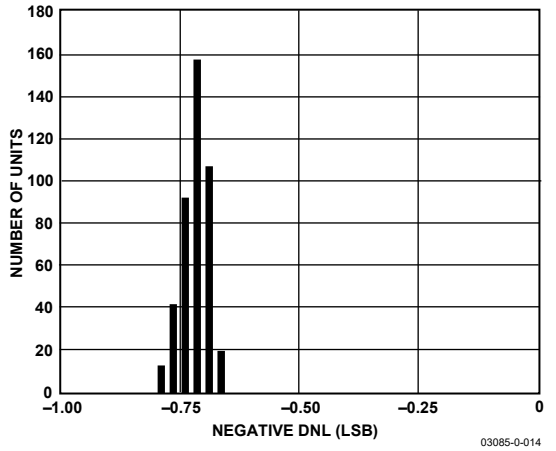


Figure 13. Typical Negative DNL Distribution (424 Units)

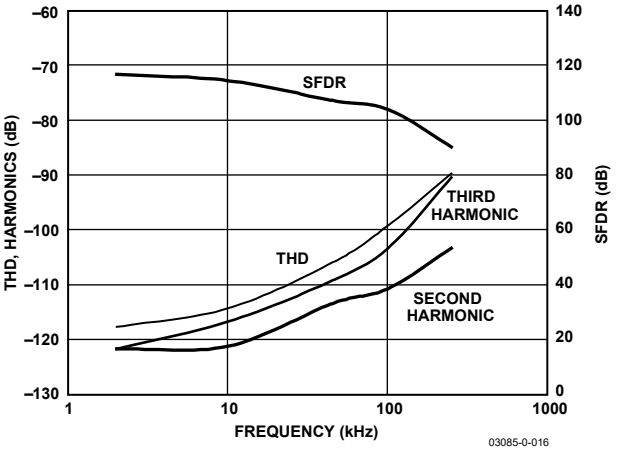


Figure 16. THD, SFDR, and Harmonics vs. Frequency

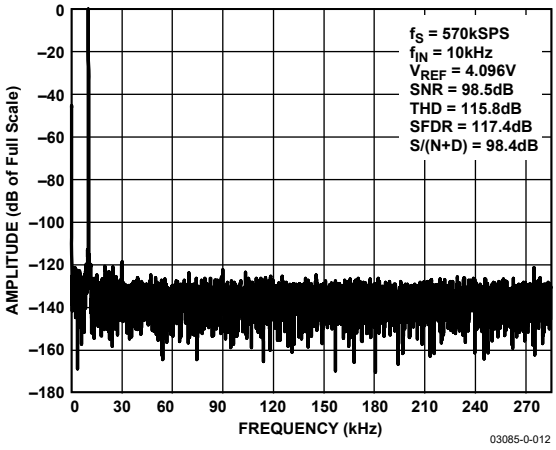


Figure 14. FFT (10 kHz Tone)

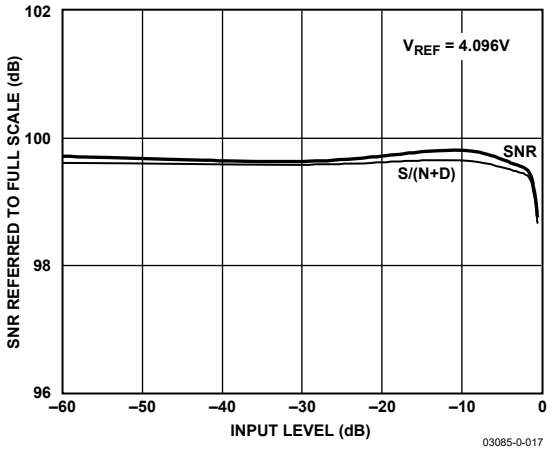


Figure 17. SNR and S/(N+D) vs. Input Level

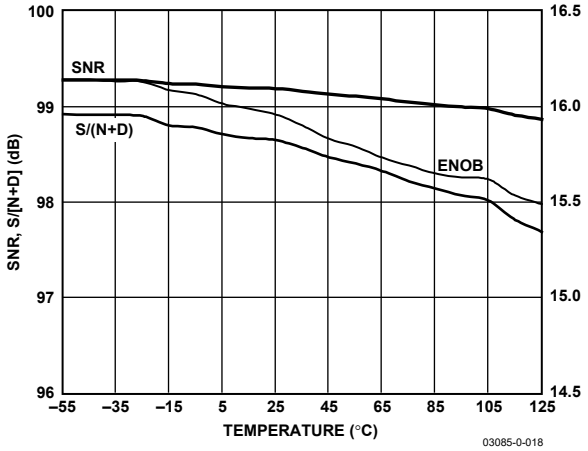


Figure 18. SNR, S/(N+D), and ENOB vs. Temperature

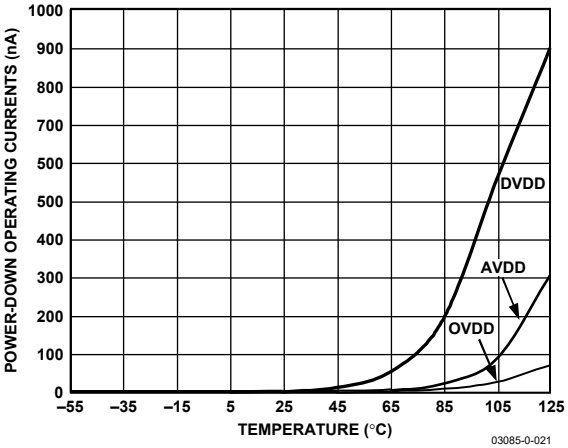


Figure 21. Power-Down Operating Currents vs. Temperature

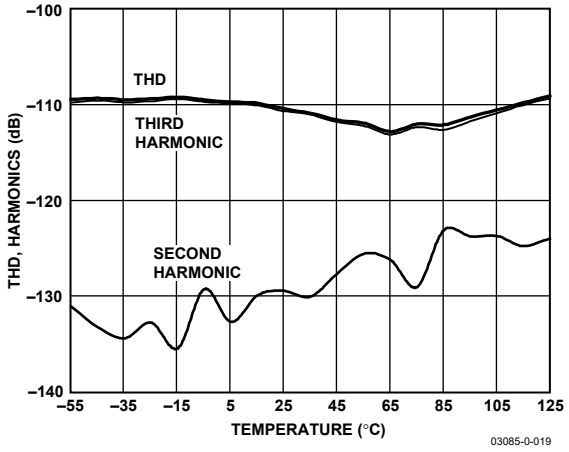


Figure 19. THD and Harmonics vs. Temperature

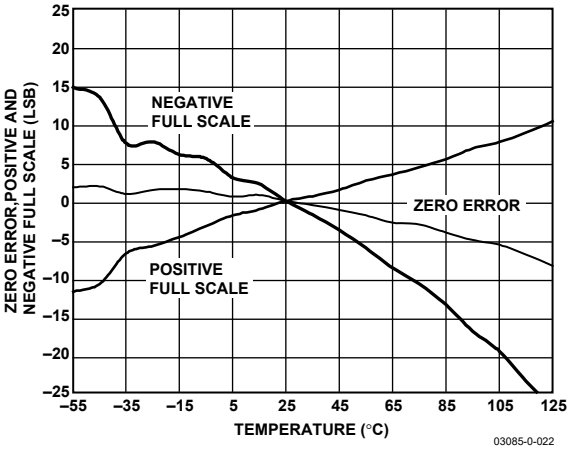


Figure 22. Zero Error Positive and Negative Full Scale vs. Temperature

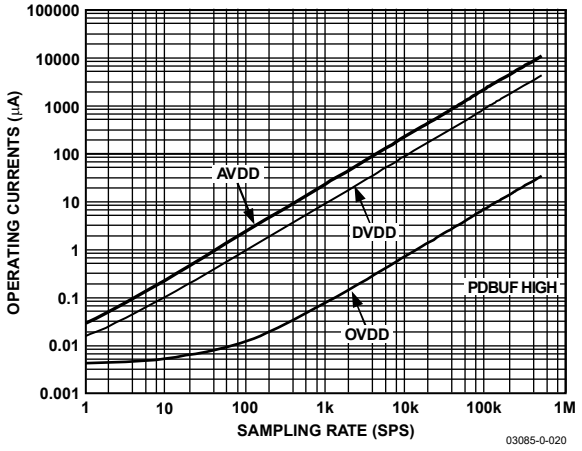


Figure 20. Operating Current vs. Sampling Rate

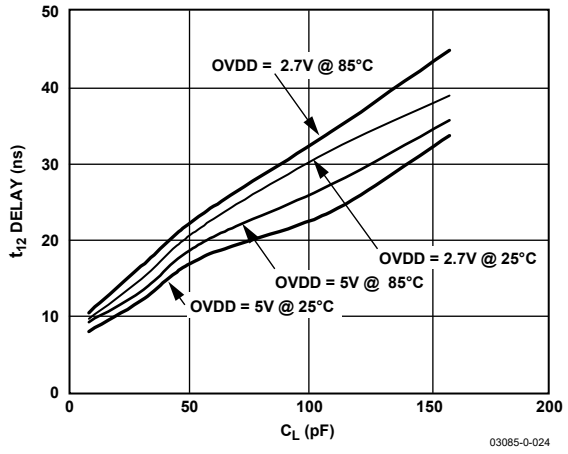


Figure 23. Typical Delay vs. Load Capacitance C_L

CIRCUIT INFORMATION

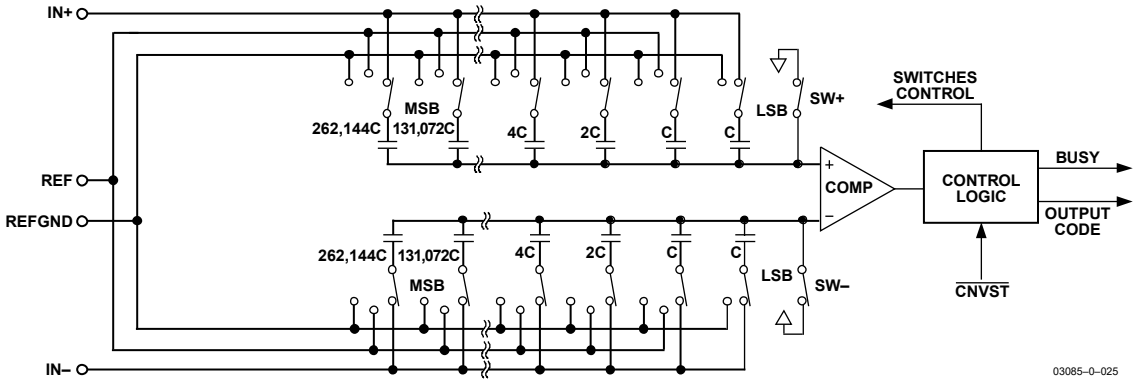


Figure 24. ADC Simplified Schematic

The AD7679 is a very fast, low power, single-supply, precise 18-bit analog-to-digital converter (ADC) using successive approximation architecture.

The AD7679's linearity and dynamic range are similar or better than many Σ-Δ ADCs. With the advantages of its successive architecture, which ease multiplexing and reduce power with throughput, it can be advantageous in applications that normally use Σ-Δ ADCs.

The AD7679 provides the user with an on-chip track/hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7679 can be operated from a single 5 V supply and can be interfaced to either 5 V or 3 V digital logic. It is housed in a 48-lead LQFP, or a tiny 48-lead LFCSP that offers space savings and allows for flexible configurations as either a serial or parallel interface. The AD7679 is pin-to-pin compatible with the AD7674, AD7676, and AD7678.

CONVERTER OPERATION

The AD7679 is a successive approximation ADC based on a charge redistribution DAC. Figure 24 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 18 binary weighted capacitors that are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW+ and SW–. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on IN+ and IN– inputs. When the acquisition phase is complete and the $\overline{\text{CNVST}}$ input goes low, a conversion phase is initiated. When the conversion phase begins, SW+ and SW– are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between the IN+ and IN– inputs captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$...$V_{REF}/262144$). The control logic toggles these switches, starting with the MSB first, to bring the comparator back into a balanced condition. After completing this process, the control logic generates the ADC output code and brings the BUSY output low.

Transfer Functions

Except in 18-bit interface mode, the AD7679 offers straight binary and twos complement output coding when using OB/$\overline{2C}$. See Figure 25 and Table 8 for the ideal transfer characteristic.

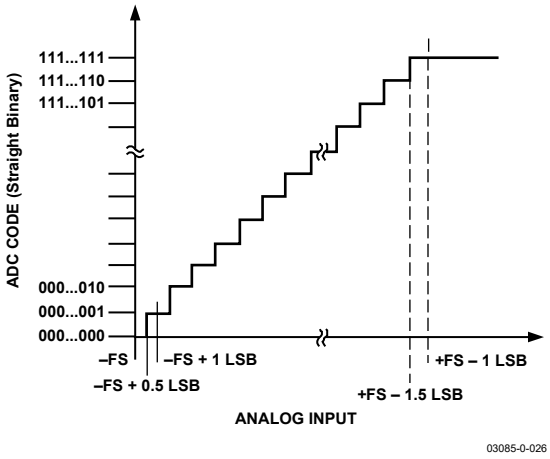


Figure 25. ADC Ideal Transfer Function

Table 8. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 4.096 V	Straight Binary (Hex)	Twos Complement (Hex)
FSR –1 LSB	4.095962 V	3FFFF[1]	1FFFF[1]
FSR – 2 LSB	4.095924 V	3FFFE	1FFFE
Midscale + 1 LSB	31.25 µV	20001	00001
Midscale	0 V	20000	00000
Midscale – 1 LSB	–31.25 µV	1FFFF	3FFFF
–FSR + 1 LSB	-4.095962 V	00001	20001
–FSR	-4.096 V	00000[2]	20000[2]

[1] This is also the code for overrange analog input ($V_{IN+} – V_{IN–}$ above $V_{REF} – V_{REFGND}$).
[2] This is also the code for underrange analog input ($V_{IN+} – V_{IN–}$ below $–V_{REF} + V_{REFGND}$).

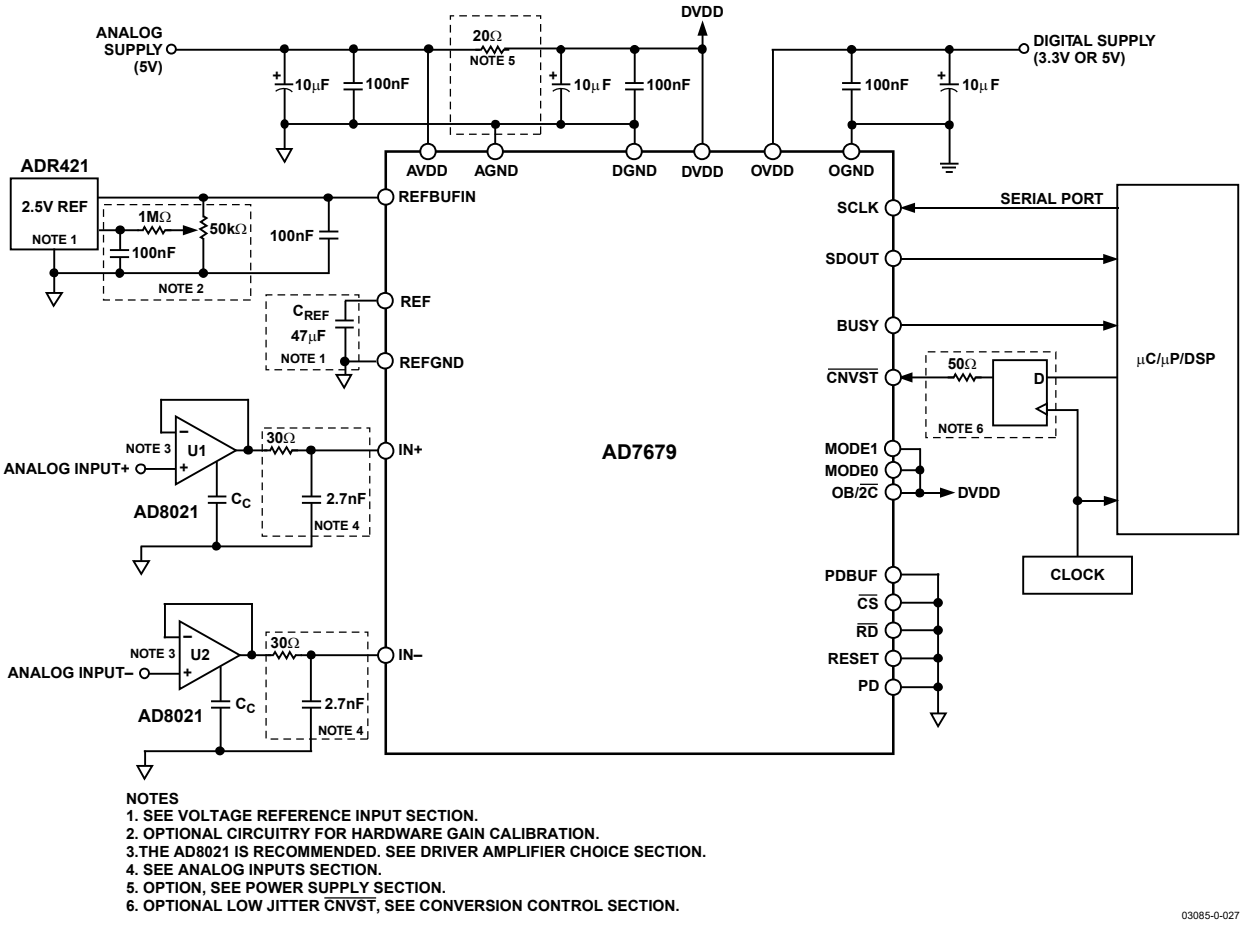


Figure 26. Typical Connection Diagram (Internal Reference Buffer, Serial Interface)

TYPICAL CONNECTION DIAGRAM

Figure 26 shows a typical connection diagram for the AD7679. Different circuitry shown on this diagram is optional and is discussed later in this data sheet.

Analog Inputs

Figure 27 shows a simplified analog input section of the AD7679. The diodes shown in Figure 27 provide ESD protection for the inputs. Care must be taken to ensure that the analog input signal never exceeds the absolute ratings on these inputs. This will cause these diodes to become forward biased and start conducting current. These diodes can handle a forward-biased current of 120 mA max. This condition could eventually occur when the input buffer's U1 or U2 supplies are different from AVDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

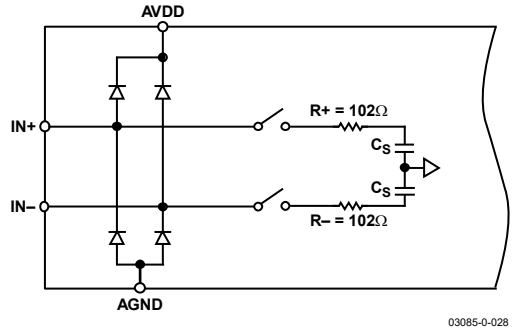


Figure 27. Simplified Analog Input

This analog input structure is a true differential structure. By using these differential inputs, signals common to both inputs are rejected as shown in Figure 28, which represents typical CMRR over frequency.

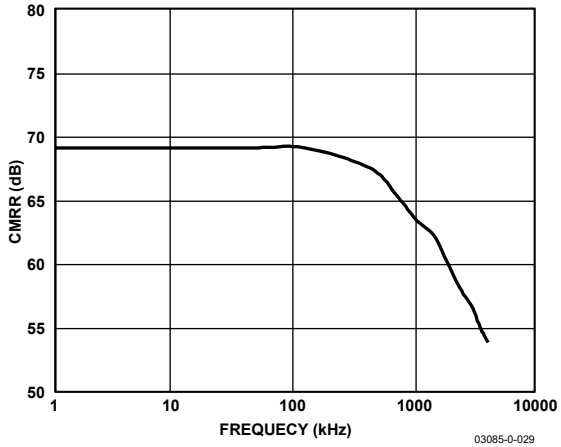


Figure 28. Analog Input CMRR vs. Frequency

During the acquisition phase for ac signals, the AD7679 behaves like a 1-pole RC filter consisting of the equivalent resistance, R+, R–, and C_S. Resistors R+ and R– are typically 102 Ω and are lumped components made up of a serial resistor and the on resistance of the switches. C_S is typically 60 pF and mainly consists of the ADC sampling capacitor. This 1-pole filter with a –3 dB cutoff frequency of 26 MHz typ reduces any undesirable aliasing effect and limits the noise coming from the inputs.

Because the input impedance of the AD7679 is very high, the part can be driven directly by a low impedance source without gain error. This allows the user to put an external 1-pole RC filter between the amplifier output and the ADC analog inputs, as shown in Figure 26, to even further improve the noise filtering done by the AD7679 analog input circuit. However, the source impedance has to be kept low because it affects the ac performance, especially the total harmonic distortion (THD). The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of source impedance and the maximum input frequency, as shown in Figure 29.

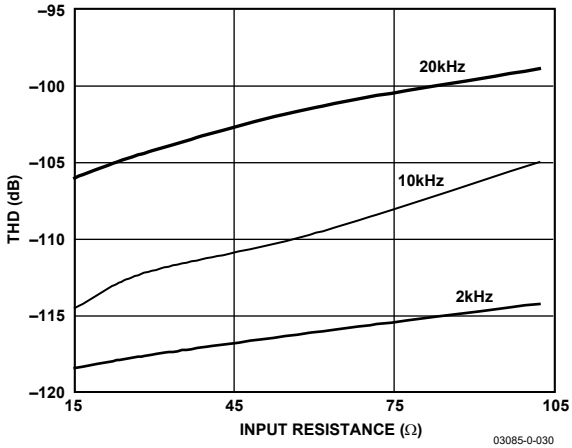


Figure 29. THD vs. Analog Input Frequency and Source Resistance

Driver Amplifier Choice

Although the AD7679 is easy to drive, the driver amplifier needs to meet the following requirements:

- The driver amplifier and the AD7679 analog input circuit have to be able to settle for a full-scale step of the capacitor array at an 18-bit level (0.0004%). In the amplifier's data sheet, settling at 0.1% or 0.01% is more commonly specified. This could differ significantly from the settling time at an 18-bit level and, therefore, should be verified prior to driver selection. The tiny op amp AD8021, which combines ultralow noise and high gain-bandwidth, meets this settling time requirement.
- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7679. The noise coming from the driver is filtered by the AD7679 analog input circuit 1-pole low-pass filter made by R+, R–, and C_S.

The SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{25}{\sqrt{625+\pi f_{-3dB}(Ne_N)^2}}\right)$$

where:

f_{-3dB} is the –3 dB input bandwidth in MHz of the AD7679 (26 MHz) or the cutoff frequency of the input filter, if used.

N is the noise factor of the amplifiers (1 if in buffer configuration).

e_N is the equivalent input noise voltage of each op amp in nV/√Hz.

For instance, for a driver with an equivalent input noise of 2 nV/√Hz (e.g., AD8021) configured as a buffer, thus with a noise gain of +1, the SNR degrades by only 0.34 dB with the filter in Figure 26, and by 1.8 dB without it.

- The driver needs to have a THD performance suitable to that of the AD7679.

The AD8021 meets these requirements and is usually appropriate for almost all applications. The AD8021 needs a 10 pF external compensation capacitor, which should have good linearity as an NPO ceramic or mica type.

The AD8022 could be used if a dual version is needed and gain of 1 is present. The AD829 is an alternative in applications where high frequency (above 100 kHz) performance is not required. In gain of 1 applications, it requires an 82 pF compensation capacitor. The AD8610 is another option when low bias current is needed in low frequency applications.

Single-to-Differential Driver

For applications using unipolar analog signals, a single-ended-to-differential driver will allow for a differential input into the part. The schematic is shown in Figure 30. When provided an input signal of 0 to V_{REF}, this configuration will produce a differential $\pm V_{REF}$ with midscale at $V_{REF}/2$.

If the application can tolerate more noise, the AD8138, differential driver can be used.

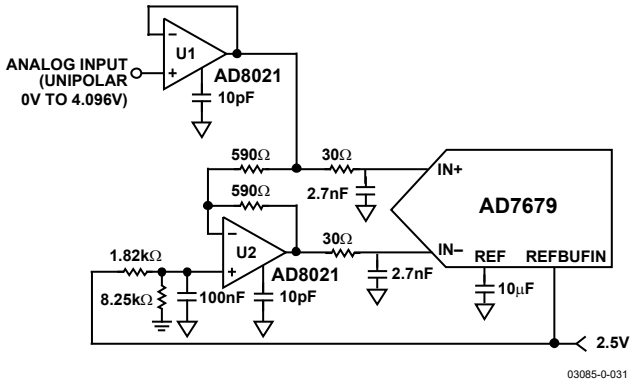


Figure 30. Single-Ended-to-Differential Driver Circuit (Internal Reference Buffer Used)

Voltage Reference

The AD7679 allows the use of an external voltage reference either with or without the internal reference buffer.

Using the internal reference buffer is recommended when sharing a common reference voltage between multiple ADCs is desired.

However, the advantages of using the external reference voltage directly are

- The SNR and dynamic range improvement (about 1.7 dB) resulting from the use of a reference voltage very close to the supply (5 V) instead of a typical 4.096 V reference when the internal buffer is used.
- The power saving when the internal reference buffer is powered down (PDBUF high).

To use the internal reference buffer, PDBUF should be LOW. A 2.5 V reference voltage applied on the REFBUFIN input will result in a 4.096 V reference on the REF pin.

In both cases, the voltage reference input REF has a dynamic input impedance and therefore requires an efficient decoupling between REF and REFGND inputs. The decoupling consists of a low ESR 47 μF tantalum capacitor connected to the REF and REFGND inputs with minimum parasitic inductance.

Care should also be taken with the reference temperature coefficient of the voltage reference, which directly affects the full-scale accuracy if this parameter matters. For instance, a ±4 ppm/°C temperature coefficient of the reference changes the full scale by ±1 LSB/°C.

Power Supply

The AD7679 uses three sets of power supply pins: an analog 5 V supply (AVDD), a digital 5 V core supply (DVDD), and a digital output interface supply (OVDD). The OVDD supply defines the output logic level and allows direct interface with any logic working between 2.7 V and DVDD + 0.3 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply, as shown in Figure 26. The AD7679 is independent of power supply sequencing once OVDD does not exceed DVDD by more than 0.3 V, and is therefore free from supply voltage induced latch-up. Additionally, it is very insensitive to power supply variations over a wide frequency range (see Figure 31).

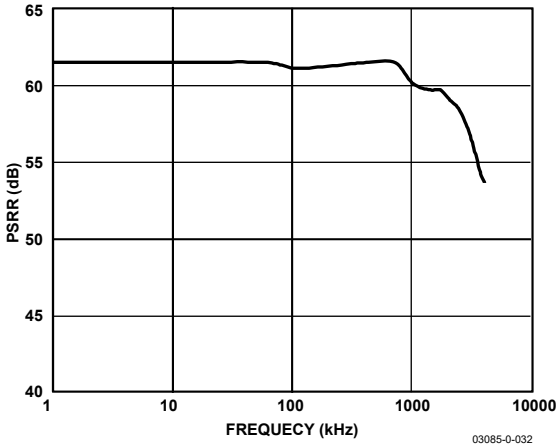


Figure 31. PSRR vs. Frequency

POWER DISSIPATION VERSUS THROUGHPUT

The AD7679 automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low, which allows for a significant power savings when the conversion rate is reduced, as shown in Figure 32. This feature makes the AD7679 ideal for very low power battery applications.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, the digital inputs need to be driven close to the power rails (DVDD and DGND), and OVDD should not exceed DVDD by more than 0.3 V.

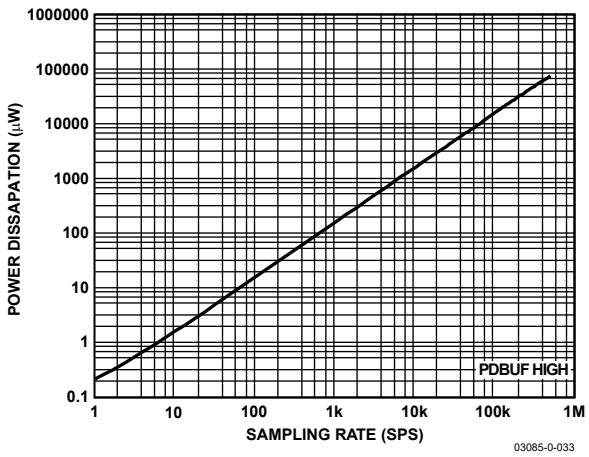


Figure 32. Power Dissipation vs. Sample Rate

CONVERSION CONTROL

Figure 33 shows the detailed timing diagrams of the conversion process. The AD7679 is controlled by the $\overline{\text{CNVST}}$ signal, which initiates conversion. Once initiated, it cannot be restarted or aborted, even by PD, until the conversion is complete. The $\overline{\text{CNVST}}$ signal operates independently of $\overline{\text{CS}}$ and $\overline{\text{RD}}$.

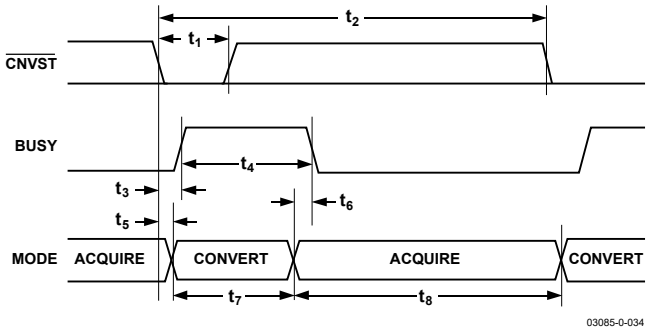


Figure 33. Basic Conversion Timing

Although $\overline{\text{CNVST}}$ is a digital signal, it should be designed with special care with fast, clean edges and levels with minimum overshoot and undershoot or ringing.

For applications where SNR is critical, the $\overline{\text{CNVST}}$ signal should have very low jitter. This may be achieved by using a dedicated oscillator for $\overline{\text{CNVST}}$ generation, or to clock it with a high frequency low jitter clock, as shown in Figure 26.

For other applications, conversions can be automatically initiated. If $\overline{\text{CNVST}}$ is held low when BUSY is low, the AD7679 controls the acquisition phase and automatically initiates a new conversion. By keeping $\overline{\text{CNVST}}$ low, the AD7679 keeps the conversion process running by itself. It should be noted that the analog input has to be settled when BUSY goes low. Also, at power-up, $\overline{\text{CNVST}}$ should be brought low once to initiate the conversion process. In this mode, the AD7679 could sometimes run slightly faster than the guaranteed limits of 570 kSPS.

DIGITAL INTERFACE

The AD7679 has a versatile digital interface; it can be interfaced with the host system by using either a serial or parallel interface. The serial interface is multiplexed on the parallel data bus. The AD7679 digital interface also accommodates both 3 V and 5 V logic by simply connecting the AD7679's OVDD supply pin to the host system interface digital supply. Finally, by using the OB/$\overline{2C}$ input pin in any mode but 18-bit interface mode, both twos complement and straight binary coding can be used.

The two signals, $\overline{CS}$ and $\overline{RD}$, control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{CS}$ allows the selection of each AD7679 in multicircuit applications, and is held low in a single AD7679 design. $\overline{RD}$ is generally used to enable the conversion result on the data bus.

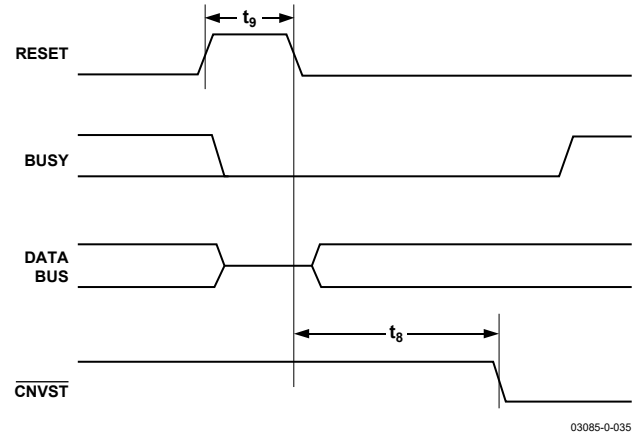


Figure 34. RESET Timing

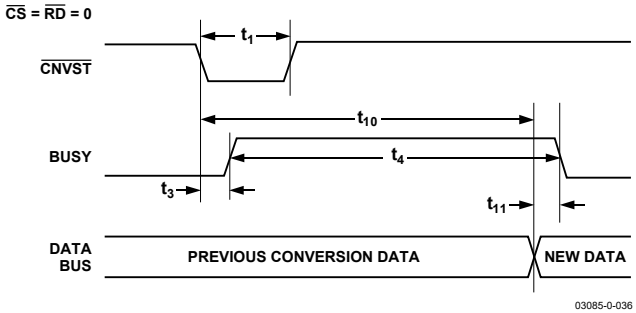


Figure 35. Master Parallel Data Timing for Reading (Continuous Read)

PARALLEL INTERFACE

The AD7679 is configured to use the parallel interface with an 18-bit, a 16-bit, or an 8-bit bus width, according to Table 7. The data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion, as shown in Figure 36 and Figure 37, respectively. When the data is read during the conversion, however, it is recommended that it is read only during the first half of the conversion phase. This avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry. Refer to Table 7 for a detailed description of the different options available.

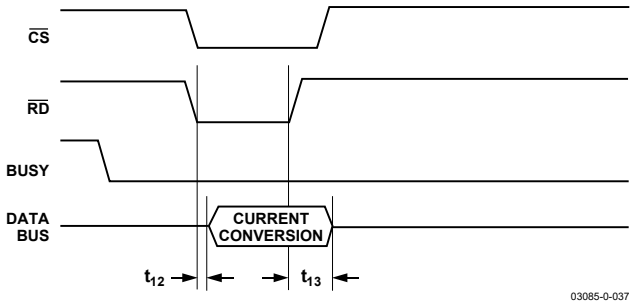


Figure 36. Slave Parallel Data Timing for Reading (Read after Convert)

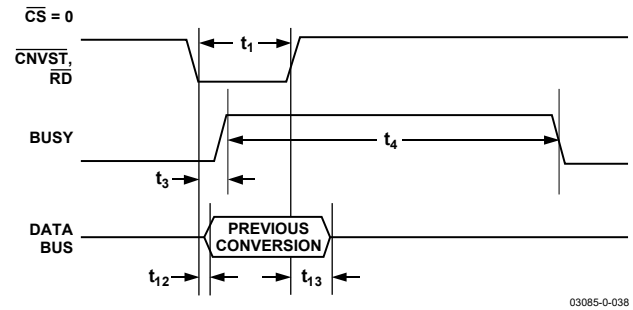


Figure 37. Slave Parallel Data Timing for Reading (Read during Convert)

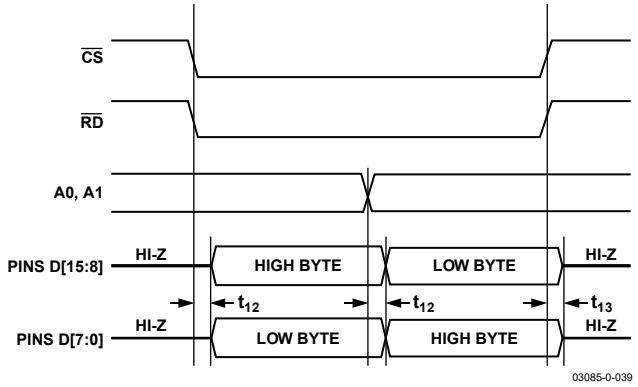


Figure 38. 8-Bit and 16-Bit Parallel Interface

SERIAL INTERFACE

The AD7679 is configured to use the serial interface when MODE0 and MODE1 are held high. The AD7679 outputs 18 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 18 clock pulses provided on the SCLK pin. The output data is valid on both the rising and falling edge of the data clock.

MASTER SERIAL INTERFACE

Internal Clock

The AD7679 is configured to generate and provide the serial data clock SCLK when the EXT/$\overline{\text{INT}}$ pin is held low. The AD7679 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted if desired. Depending on the RDC/SDIN input, the data can be read after each conversion or during the following conversion. Figure 39 and Figure 40 show the detailed timing diagrams of these two modes.

Usually, because the AD7679 is used with a fast throughput, the mode master read during conversion is the most recommended serial mode.

In Read during Conversion mode, the serial clock and data toggle at appropriate instants, minimizing potential feedthrough between digital activity and critical conversion decisions.

In Read after Conversion mode, it should be noted that unlike in other modes, the BUSY signal returns low after the 18 data bits are pulsed out and not at the end of the conversion phase, which results in a longer BUSY width.

To accommodate slow digital hosts, the serial clock can be slowed down by using DIVSCLK.

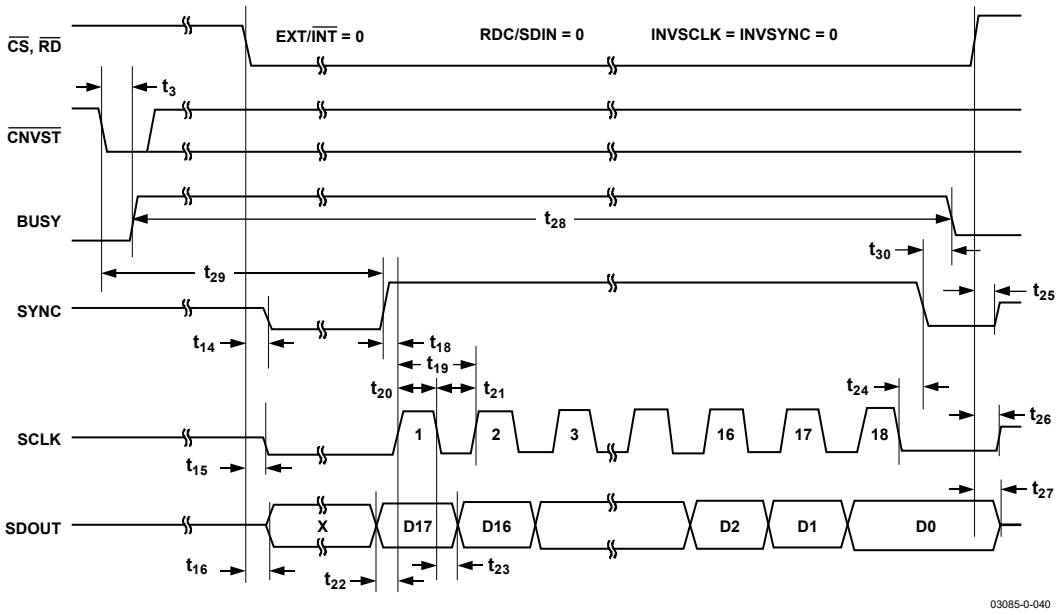


Figure 39. Master Serial Data Timing for Reading (Read after Convert)

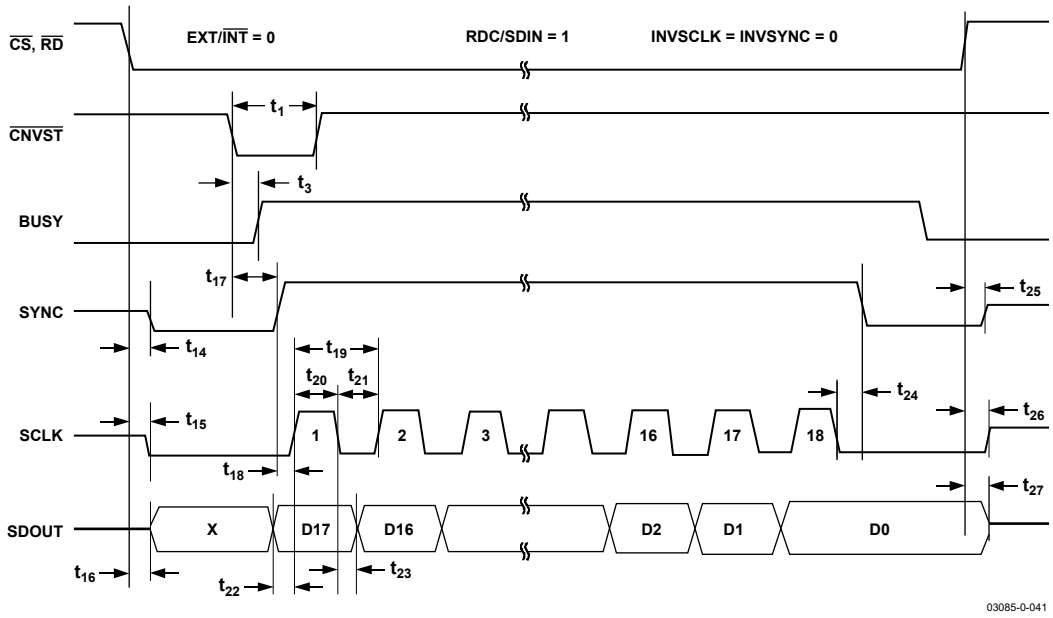


Figure 40. Master Serial Data Timing for Reading (Read Previous Conversion during Convert)

SLAVE SERIAL INTERFACE

External Clock

The AD7679 is configured to accept an externally supplied serial data clock on the SCLK pin when the EXT/$\overline{\text{INT}}$ pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{\text{CS}}$. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or a discontinuous clock. A discontinuous clock can be either normally high or normally low when inactive. Figure 41 and Figure 42 show the detailed timing diagrams of these methods.

While the AD7679 is performing a bit decision, it is important that voltage transients not occur on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the AD7679 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that toggles only when BUSY is low or, more importantly, that it does not transition during the latter half of BUSY high.

External Discontinuous Clock Data Read after Conversion

This mode is the most recommended of the serial slave modes. Figure 41 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning low, the result of this conversion can be read while both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low. Data is shifted out MSB first with 18 clock pulses, and is valid on the rising and falling edge of the clock.

Among the advantages of this method, the conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process. Also, data can be read at speeds up to 40 MHz, accommodating both slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7679 provides a daisy-chain feature using the RDC/SDIN input pin to cascade multiple converters together. This feature is useful for reducing component count and wiring connections when desired (for instance, in isolated multiconverter applications).

An example of the concatenation of two devices is shown in Figure 43. Simultaneous sampling is possible by using a common $\overline{\text{CNVST}}$ signal. It should be noted that the RDC/SDIN input is latched on the edge of SCLK opposite the one used to shift out data on SDOUT. Thus, the MSB of the upstream converter follows the LSB of the downstream converter on the next SCLK cycle.

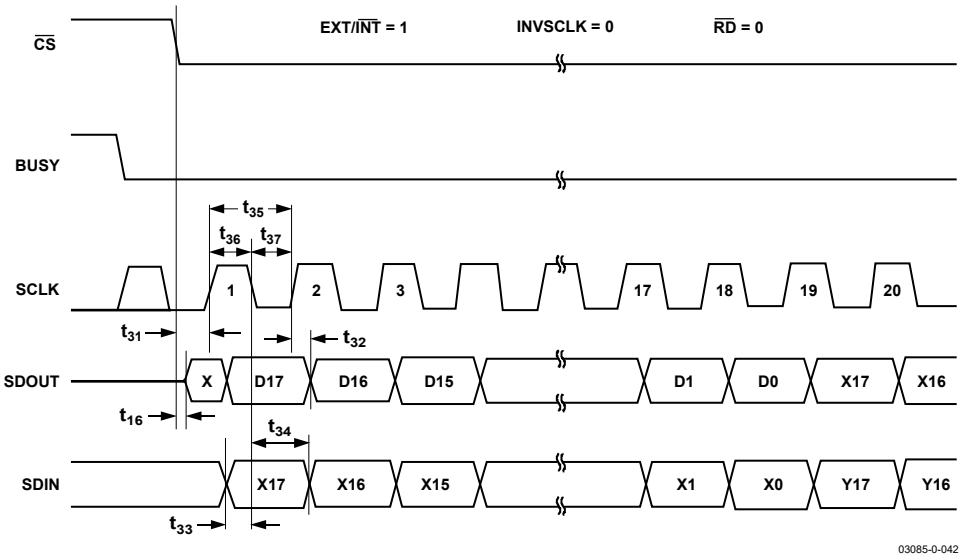


Figure 41. Slave Serial Data Timing for Reading (Read after Convert)

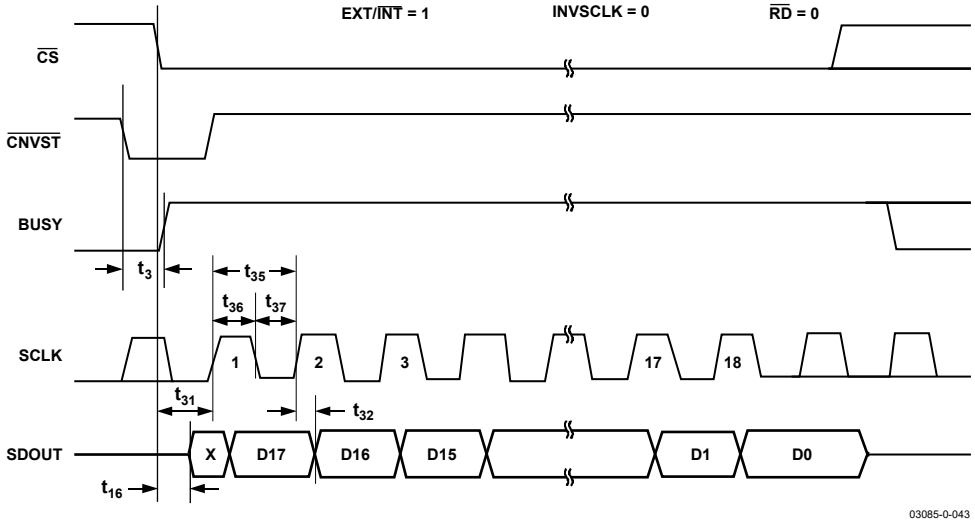


Figure 42. Slave Serial Data Timing for Reading (Read Previous Conversion during Convert)

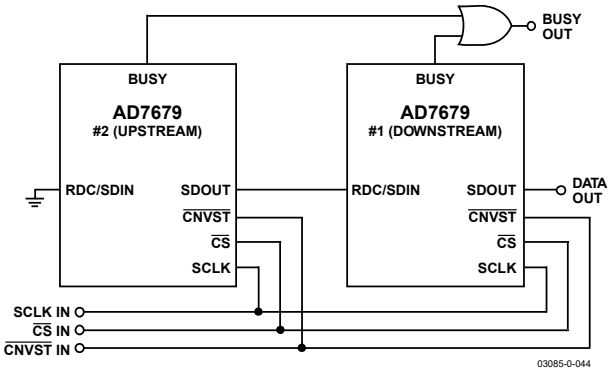


Figure 43. Two AD7679s in a Daisy-Chain Configuration

External Clock Data Read during Conversion

Figure 42 shows the detailed timing diagrams of this method. During a conversion, while both $\overline{CS}$ and $\overline{RD}$ are low, the result of the previous conversion can be read. The data is shifted out MSB first with 18 clock pulses, and is valid on both the rising and falling edge of the clock. The 18 bits have to be read before the current conversion is complete. If that is not done, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no daisy-chain feature in this mode, and the RDC/SDIN input should always be tied either high or low.

To reduce performance degradation due to digital activity, a fast discontinuous clock is recommended to ensure that all bits are read during the first half of the conversion phase. It is also possible to begin to read the data after conversion and continue to read the last bits even after a new conversion has been initiated.

MICROPROCESSOR INTERFACING

The AD7679 is ideally suited for traditional dc measurement applications supporting a microprocessor, and for ac signal processing applications interfacing to a digital signal processor. The AD7679 is designed to interface either with a parallel 8-bit or 16-bit wide interface, or with a general-purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7679 to prevent digital noise from coupling into the ADC. The following section illustrates the use of the AD7679 with an SPI equipped DSP, the ADSP-219x.

SPI Interface (ADSP-219x)

Figure 44 shows an interface diagram between the AD7679 and the SPI equipped ADSP-219x. To accommodate the slower speed of the DSP, the AD7679 acts as a slave device, and data must be read after conversion. This mode also allows the daisy-chain feature. The convert command could be initiated in response to an internal timer interrupt. The 18-bit output data are read with 3-byte SPI access. The reading process could be initiated in response to the end-of-conversion signal (BUSY going low) using an interrupt line of the DSP. The serial interface (SPI) on the ADSP-219x is configured for master mode (MSTR) = 1, Clock Polarity Bit (CPOL) = 0, Clock Phase Bit (CPHA) = 1, and SPI interrupt enable (TIMOD) = 00, by writing to the SPI Control register (SPICLTx). It should be noted that to meet all timing requirements, the SPI clock should be limited to 17 Mbits/s, which allow it to read an ADC result in about 1.1 µs. When a higher sampling rate is desired, use of one of the parallel interface modes is recommended.

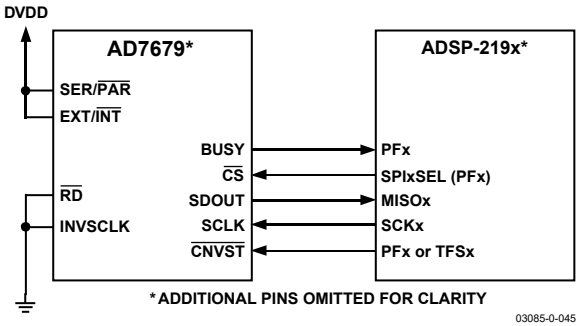


Figure 44. Interfacing the AD7679 to an SPI Interface

APPLICATION HINTS

LAYOUT

The AD7679 has very good immunity to noise on the power supplies. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD7679 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7679, or at least as close to the AD7679 as possible. If the AD7679 is in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at one point only, a star ground point that should be established as close to the AD7679 as possible.

The user should avoid running digital lines under the device, as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7679 to avoid noise coupling. Fast switching signals like $\overline{\text{CNVST}}$ or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of feedthrough through the board. The power supply lines to the AD7679 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supply's impedance presented to the AD7679 and to reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed close to and ideally right up against each power supply pin (AVDD, DVDD, and OVDD) and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located near the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7679 can be a separate supply or can come from the analog supply, AVDD, or the digital interface supply, OVDD. When the system digital supply is noisy or when fast switching digital signals are present, and if no separate supply is available, the user should connect the DVDD digital supply to the analog supply AVDD through an RC filter, (see Figure 26), and connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high frequency spikes.

The AD7679 has four different ground pins: REFGND, AGND, DGND, and OGND. REFGND senses the reference voltage and should be a low impedance return to the reference because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. The decoupling capacitor should be close to the ADC and should be connected with short and large traces to minimize parasitic inductances.

EVALUATING THE AD7679'S PERFORMANCE

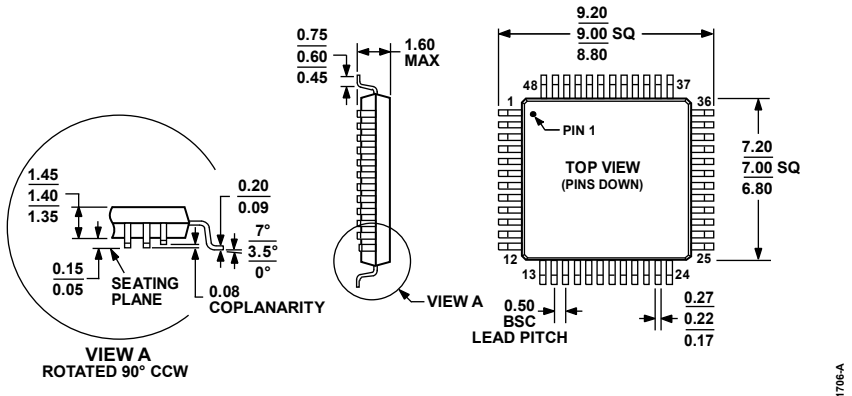
An evaluation board for the AD7679 allows a quick means to measure both dc (histograms and time domain) and ac (time and frequency domain) performances of the converter. The EVAL-AD7679CBZ is an evaluation board package that includes a fully assembled and tested evaluation board, documentation, and software. The accompanying software requires the use of a capture board, which must be ordered separately from the evaluation board (see the Ordering Guide for information). The evaluation board can also be used in a standalone configuration and does not use the software when in this mode. Refer to the EVAL-AD76XXEDZ and EVAL-AD76XXCBZ data sheets available from www.analog.com for evaluation board details.

Two types of data capture boards can be used with the EVAL-AD7679CBZ:

- USB based (EVAL-CED1Z recommended)
- Parallel port based (EVAL-CONTROL BRD3Z not recommended because many newer PCs do not include parallel ports any longer)

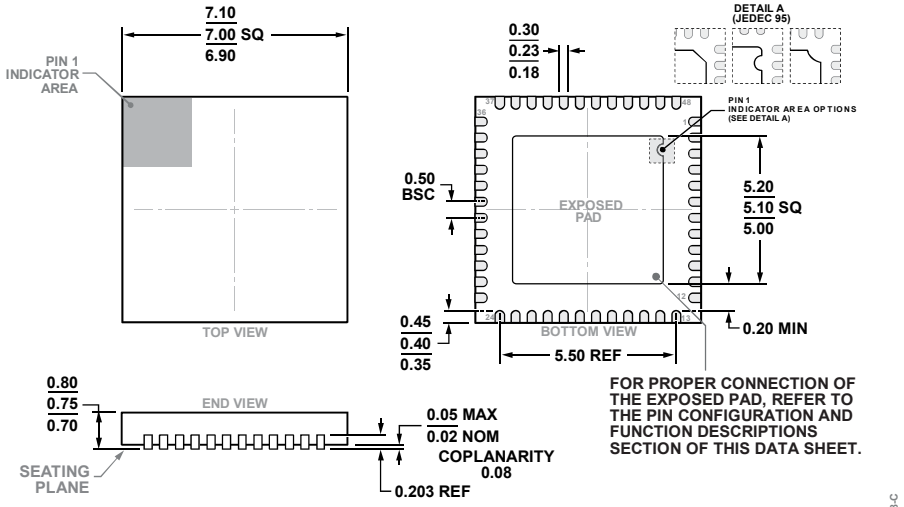
The recommended board layout for the AD7679 is outlined in the evaluation board data sheet.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 45. 48-Lead Low Profile Quad Flat Package [LQFP] (ST-48)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD-4

Figure 46. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7679ASTZ[1]	–40°C to +85°C	48-Lead LQFP	ST-48
AD7679ASTZRL[1]	–40°C to +85°C	48-Lead LQFP	ST-48
AD7679ACPZ[1]	–40°C to +85°C	48-Lead LFCSP	CP-48-4
AD7679ACPZRL[1]	–40°C to +85°C	48-Lead LFCSP	CP-48-4
EVAL-AD7679CBZ[1, 2]		Evaluation Board	
EVAL-CONTROL BRD2Z[1, 3]		Parallel Port Capture Board, 32k RAM	
EVAL-CONTROL BRD3Z[1, 3]		Parallel Port Capture Board, 128k RAM	
EVAL-CED1Z[1]		USB Data Capture Board	

[1] Z = RoHS Compliant Part.
[2]This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRD2 for evaluation/demonstration purposes.
[3]These capture boards allow a PC to control and communicate with all Analog Devices evaluation boards ending in ED for EVAL-CED1Z and CB for EVAL-CONTROL BRDxZ (x = 2, 3).

NOTES

NOTES

D03085-8/20(B)

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