THE DATASHEET OF

MT66R7072A10AB5ZZW.ZCA TR

Product Brief
LPDDR2-PCM and Mobile LPDDR2 121-Ball MCP

MT66R7072A10AB5ZZW.ZCA, MT66R7072A10ACUXZW.ZCA
MT66R5072A10ACUXZW.ZFA

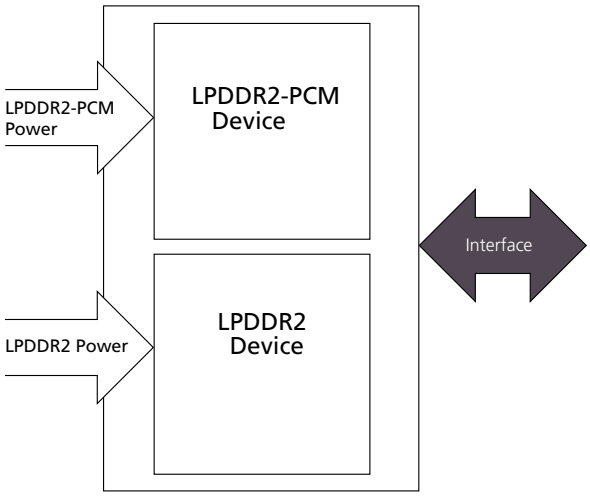
Features

- Micron® LPDDR2-PCM and LPDDR2 components
- RoHS-compliant, "green" package
- Shared LPDDR2-PCM and LPDDR2 interfaces
- Space-saving multichip package
- Ultra low-voltage core and I/O power supplies
  - V_{DD1} = 1.7–1.95V
  - V_{DDCA}/V_{DDQ} = 1.14–1.3V
  - V_{DD2} = 1.14–1.3V
- Wireless temperature range: –25°C to +85°C

LPDDR2-PCM Specific Features

- Memory interface
  - 16-bit data bus width
  - Two data transfers per clock cycle
  - Clock frequency up to 400 MHz
  - Active to read/write delay: ^{t}RCD = 86ns
  - Configurable output drive strength
- Memory architecture
  - 4-row data buffers (RDB)
  - Row data buffer size: 32B
  - 4-row address buffers (RAB)
  - Emulated block size: 128KB
- Program/erase performance
  - Legacy programming mode up to 10MB/s (TYP)
  - Overwrite up to 3 MB/s (TYP)
  - Legacy block erase time: 60ms (TYP)
- Dual operations
  - PROGRAM/ERASE in one partition while READ in other partitions
  - No delay between READ and WRITE operations
- Locking scheme
  - All blocks locked at power-up
  - 8Mb lock region
  - Any combination of regions can be locked
  - Absolute write protection with $V_{ACC} = V_{SS}$
- Quality and reliability
  - Minimum 100k WRITE cycles/row

Figure 1: MCP Block Diagram



Mobile LPDDR2-Specific Features

- Programmable read and write latencies
- Programmable burst lengths: 4, 8, or 16
- Partial-array self refresh (PASR)
- Deep power-down (DPD) mode
- Selectable output drive strength
- Adjustable clock frequency and clock stop capabilities

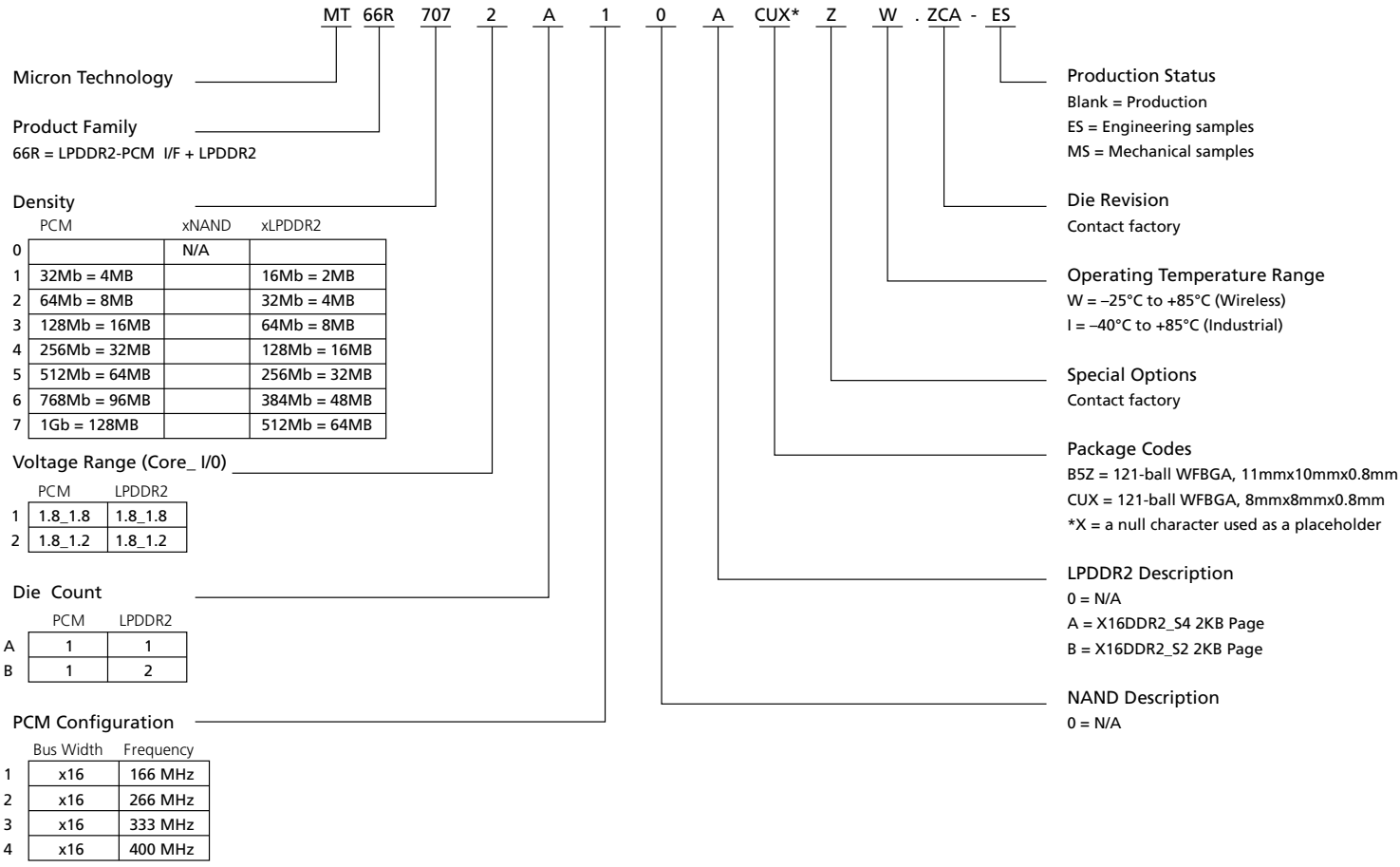
Note: This product brief does not provide detailed device information. For the complete data sheet, which covers device functionality, operating modes, and specifications, or for further information on any aspect of the product, contact the Micron sales office.

Part Number: The MT66R5072A10ACUXZW.ZFA is available as an engineering sample only.

Part Numbering Information

Micron LPDDR2-PCM and LPDDR2 devices are available in different configurations and densities. The MCP/PoP part numbering guide is available at www.micron.com/numbering.

Figure 2: Part Number Chart



	PCM	xNAND	xLPDDR2
0		N/A	
1	32Mb = 4MB		16Mb = 2MB
2	64Mb = 8MB		32Mb = 4MB
3	128Mb = 16MB		64Mb = 8MB
4	256Mb = 32MB		128Mb = 16MB
5	512Mb = 64MB		256Mb = 32MB
6	768Mb = 96MB		384Mb = 48MB
7	1Gb = 128MB		512Mb = 64MB

	PCM	LPDDR2
1	1.8_1.8	1.8_1.8
2	1.8_1.2	1.8_1.2

	PCM	LPDDR2
A	1	1
B	1	2

	Bus Width	Frequency
1	x16	166 MHz
2	x16	266 MHz
3	x16	333 MHz
4	x16	400 MHz

Note: 1. The MT66R5072A10ACUXZW.ZFA is available as an engineering sample only. This MCP will be packaged as 512Mb LPDDR-PCM and 512Mb LPDDR2, 121-ball, 8mm x 8mm x 0.8mm.

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder. To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/csn.

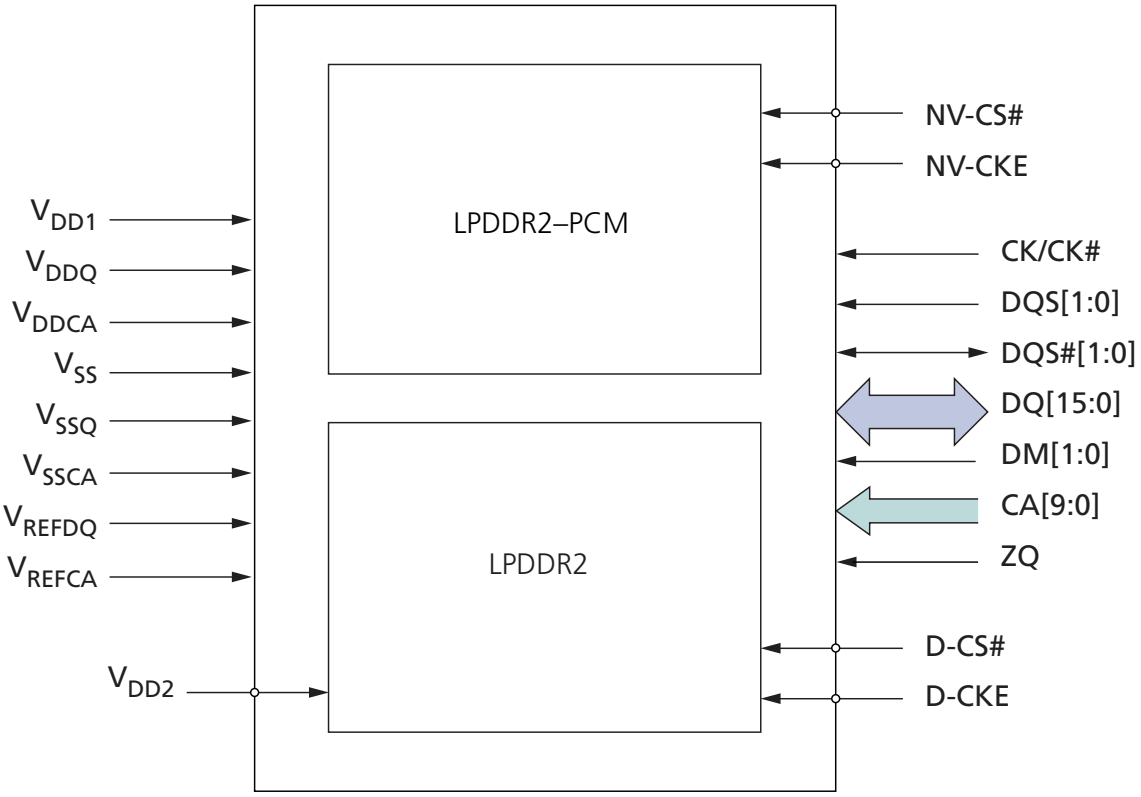
MCP General Description

Micron MCP products combine LPDDR2-PCM and Mobile LPDDR2 devices in a single MCP. These products target mobile applications with low-power, high-performance, and minimal package-footprint design requirements. The LPDDR2-PCM and Mobile LPDDR2 devices are also members of the Micron discrete memory products portfolio.

The bus architecture of this device also supports separate LPDDR2-PCM and Mobile LPDDR2 functionality without concern for device interaction.

Device Diagrams

Figure 3: 121-Ball (LPDDR2-PCM and LPDDR2) Functional Block Diagram



Ball Assignments and Descriptions

Figure 4: 121-Ball VFBGA (LPDDR2-PCM x16; LPDDR2 x16) Ball Assignments

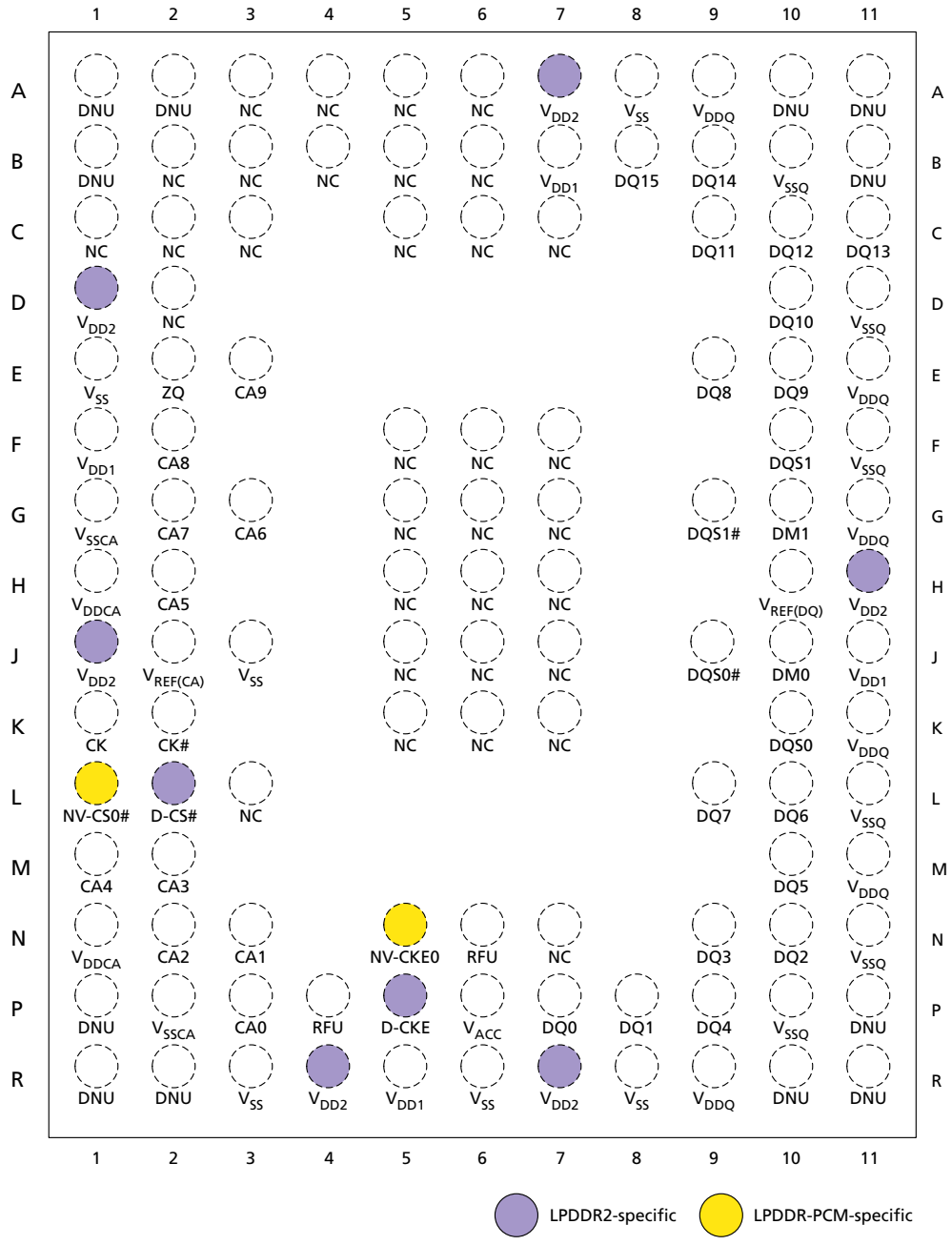


Table 1: x16 LPDDR2-PCM Ball Descriptions

Symbol	Type	Description
NV-CS#	Input	Chip select: CS# is considered part of the command code and is sampled at the rising edge of CK. When registered, CS# LOW enables, and CS# HIGH disables, the command decoder. All commands are masked when CS# is registered HIGH.
NV-CKE	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled at the rising edge of CK.

Table 2: x16 Mobile LPDDR2 Ball Descriptions

Symbol	Type	Description
D-CKE	Input	Clock enable. D-CKE is used for a single LPDDR2. For the signal description, refer to NV-CKE description.
D-CS#	Input	Chip select: D-CS# is used for a single LPDDR2. For the signal description, refer to NV-CS# description.

Table 3: LPDDR2 Ball Descriptions

Symbol	Type	Description
CA[9:0]	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All CA inputs are sampled on both the positive and negative edge of CK. CS and CKE inputs are sampled at the positive edge of CK. AC timings are referenced to clock.
DM[1:0]	Input	Data mask:DM is an input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[1:0] is DM for each of the two data bytes, respectively.
DQ[15:0]	Input/ output	Data bus: Data inputs/outputs.
DQS[3:0] DQS#[3:0]	Input/ output	Data strobe: Coordinates READ/WRITE transfers of data; one DQS/DQS# pair per DQ byte.
V_{DD1}	Supply	V_{DD1}: LPDDR2 power supply 1.
V_{DD2}	Supply	V_{DD2}: LPDDR2 power supply 2.
V_{DDCA}	Supply	V_{DDCA}: LPDDR2 CA power supply.
V_{DDQ}	Supply	V_{DDQ}: LPDDR2 I/O power supply.
V_{REFCA}	Supply	V_{REFCA}: LPDDR2 reference for CA pins.
V_{REFDQ}	Supply	V_{REFDQ}: LPDDR2 reference for DQ pins.
V_{SSCA}	Supply	V_{SSCA}: LPDDR2 I/O ground.
V_{SSQ}	Supply	V_{SSQ}: LPDDR2 I/O ground.
V_{SS}	Supply	V_{SS}: Shared ground.
ZQ	Input	External impedance (240-Ohm): This signal is used to calibrate the device output impedance.

Table 4: Non-Device-Specific Descriptions

Symbol	Type	Description
DNU	–	Do not use: Must be grounded or left floating.
NC	–	No connect: Not internally connected.

Phase Change Memory General Description

PCM is a new class of nonvolatile memory devices that stores information through a reversible structural phase change in a chalcogenide material. The material exhibits a change in both electrical and optical properties when changed from the amorphous (disordered) to the polycrystalline (regularly ordered) state. The amorphous state corresponds to the reset state (0); the polycrystalline state corresponds to the set state (1). In PCM, information is stored during the change in resistance the chalcogenide material undergoes during a phase change

The device uses a DDR architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and row buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock. The device also uses a DDR architecture on the DQ pins to achieve high-speed operation.

The LPDDR2-PCM device uses a complete set of commands that are compatible with the JEDEC industry-standard specification No. JESD209-2E.

The DDR architecture is essentially a 4n-prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access effectively consists of a single, 4n-bit wide, one-clock-cycle data transfer at the internal core and four corresponding, n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

The device is organized into four RABs and RDBs, 32 bytes each. Read or write accesses to device are performed issuing a sequence of PREACTIVE commands to deliver part of the row address to one of four RABs in the device; ACTIVATE commands to fill one of the four RDBs in the device; and READ or WRITE commands.

Operations other than array reads are performed by accessing an overlay window that is mapped over the array space of the memory. The overlay window base address is programmed using the mode registers.

The device can be erased electrically at block level and programmed in-system on a word-by-word basis using a V_{DD1} supply for the circuitry and V_{DDQ} supply for the I/O pins. An optional V_{ACC} power supply is provided for factory programming.

A multiple partition architecture allows dual operations: While writing or erasing in one partition, READ operations are possible in other partitions. Only one partition at a time can be in write or erase mode.

Erase can be suspended to perform a WRITE or READ operation in any other block except for the one being erased, and then resumed. Writing can be suspended to read data at any memory location except the one being modified, and then resumed.

To issue embedded commands like PROGRAM or ERASE, the operation code and data are written to the overlay window of the memory. An internal program/erase controller manages the timings necessary for embedded operations. The end of a WRITE or ERASE operation can be detected and any error conditions identified in the status register. The command set required to control the memory is consistent with the JEDEC standard.

Read and write accesses to the device are burst oriented at different frequencies using a differential clock up to 400 MHz. Accesses start at a selected location and continue for a configured number of locations.

The device features a power-down mode. When clock enable (CKE) is registered LOW, power-down mode is enabled. In this condition, the power consumption is reduced to the standby value.

The device features an individual locking region scheme that allows any region to be locked or unlocked, enabling code and data protection. The array is divided into 8Mb locking regions. All locking regions have three levels of protection. They can be locked and locked down individually, preventing any accidental writing or erasure. There is also additional hardware protection against writing and erasing. When $V_{ACC} < V_{ACCLK}$, all lock regions are protected against program or erase. All lock regions are locked at power-up.

V_{ACC} shall not change during the period starting from at least 1µs prior to the initiation of any embedded operation until that embedded operation is complete.

The device includes a 64-bit segment area, containing a unique 64-bit device number and a 256-bit (16-word) protection register area that is one-time programmable (OTP) by the user. The user-programmable region can be permanently protected, programming the 16-bit protection register lock. See Security Features and Protection Registers for more details.

PCM offers bit alterability or an overwrite feature: PCM technology supports the ability to change each memory bit independently from 0 to 1 or 1 to 0 without erasing the block first. Bit alterability enables software to write to the nonvolatile memory similar to writing to RAM or EEPROM without the overhead of erasing blocks prior to writing. Bit-alterable writes use command sequences similar to word writes and buffer writes. This mode is often referred to as overwrite as opposed to program, in which only 0s are written and 1s are treated as masks.

The device is rated at 100,000 write alterations per row. The device is supplied with all the bits erased (set to 1).

LPDDR2-PCM Organization

Array

The 512Mb device has a 512-block array and is divided into 64Mb partitions. There are 8 partitions containing 64 blocks of 128KB each.

The 1Gb device has a 1024-block array and is divided into 64Mb partitions. There are 16 partitions containing 64 blocks of 128KB each.

Memory Map

Table 5: 512Mb LPDDR2-PCM

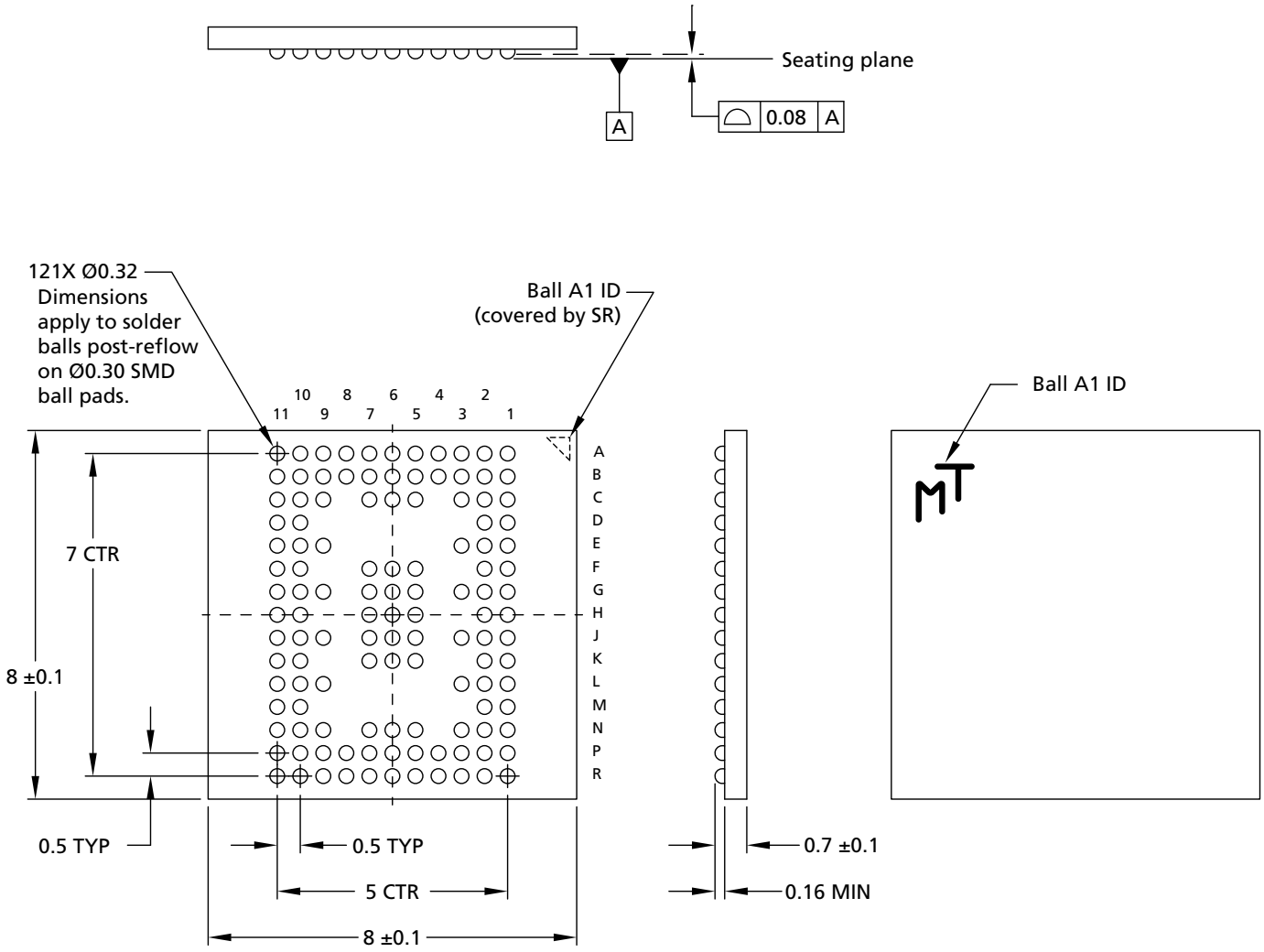
		Block Number	Size (KB)	Word Address Range
Partition 7	64Mb	511	128	1FF0000–1FFFFFF
		⋮	⋮	⋮
		448	128	1C00000–1C0FFFF
Partition 0	64Mb	63	128	03F0000–03FFFFF
		⋮	⋮	⋮
		0	128	0000000–000FFFF

Table 6: 1Gb LPDDR2-PCM

		Block Number	Size (KB)	Word Address Range
Partition 15	64Mb	1023	128	3FF0000–3FFFFFF
		⋮	⋮	⋮
		960	128	3C00000–3C0FFFF
Partition 0	64Mb	63	128	03F0000–03FFFFF
		⋮	⋮	⋮
		0	128	0000000–000FFFF

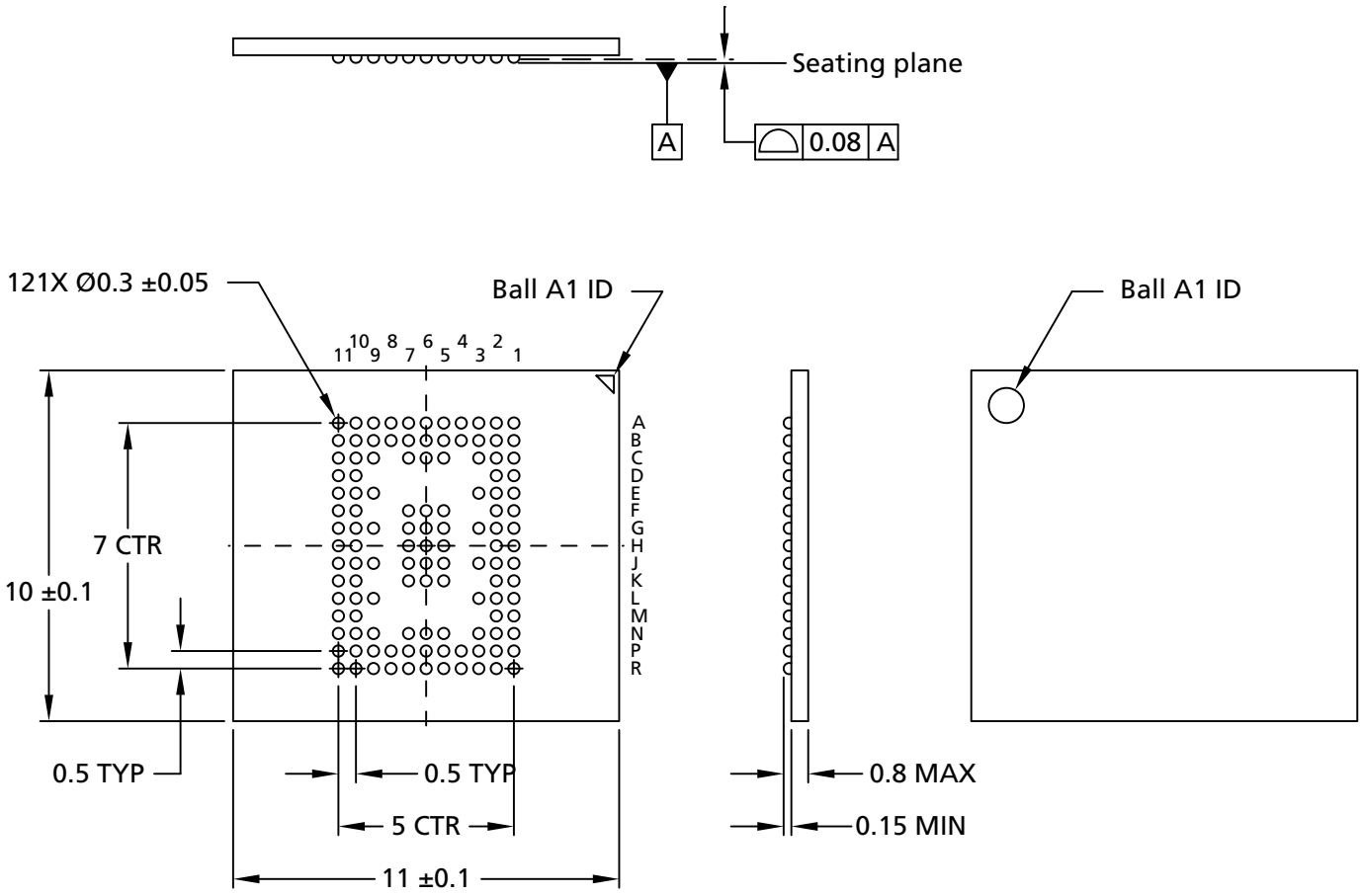
Package Dimensions

Figure 5: 121-Ball VFBGA – 8mm x 8mm x 0.8mm (Package Code: CU)



Note: 1. All dimensions are in millimeters.

Figure 6: 121-Ball VFBGA – 11m x 10mm x 0.8mm (Package Code: B5Z)



Note: 1. All dimensions are in millimeters.

Revision History

Rev. B – 12/12

- Added new part number

Rev. A – 08/12

- Initial release

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