



**THE DATASHEET OF
TSB12LV26PZTG4**



OHCI-Lynx™ PCI-Based IEEE 1394 Host Controller

FEATURES

- 3.3-V and 5-V PCI bus signaling
- 3.3-V supply (core voltage is internally regulated to 1.8 V)
- Serial bus data rates of 100M bits/s, 200M bits/s, and 400M bits/s
- Physical write posting of up to three outstanding transactions
- Serial ROM interface supports 2-wire devices
- External cycle timer control for customized synchronization
- PCI burst transfers and deep FIFOs to tolerate large host latency
- Two general-purpose I/Os
- Fabricated in advanced low-power CMOS process
- Packaged in 100-terminal LQFP (PZT)
- `PCI_CLKRUN` protocol

DESCRIPTION

The Texas Instruments TSB12LV26 device is a PCI-to-1394 host controller compliant with the *PCI Local Bus Specification*, *PCI Bus Power Management Interface Specification*, IEEE Std 1394-1995, and *1394 Open Host Controller Interface Specification*. The chip provides the IEEE 1394 link function and is compatible with 100M bits/s, 200M bits/s, and 400M bits/s serial bus data rates.

As required by the *1394 Open Host Controller Interface Specification* (OHCI) and IEEE Std 1394a-2000, internal control registers are memory-mapped and nonprefetchable. The PCI configuration header is accessed through configuration cycles specified by PCI and provides plug-and-play (PnP) compatibility. Furthermore, the TSB12LV26 device is compliant with the *PCI Bus Power Management Interface Specification*, per the *PC 99 Design Guide* requirements. TSB12LV26 device supports the D0, D2, and D3 power states.

The TSB12LV26 design provides PCI bus master bursting and is capable of transferring a cacheline of data at 132M bytes/s after connection to the memory controller. Since PCI latency can be large, deep FIFOs are provided to buffer 1394 data.

The TSB12LV26 device provides physical write posting buffers and a highly-tuned physical data path for SBP-2 performance. The TSB12LV26 device also provides multiple isochronous contexts, multiple cacheline burst transfers, advanced internal arbitration, and bus-holding buffers on the PHY/link interface.

An advanced CMOS process achieves low power consumption and allows the TSB12LV26 device to operate at PCI clock rates up to 33 MHz.

NOTE:


This product is for high-volume PC applications only. For a complete datasheet or more information contact support@ti.com.



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSB12LV26PZT	ACTIVE	TQFP	PZT	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	0 to 70	TSB12LV26 F731652A	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TSB12LV26 :

- Enhanced Product: [TSB12LV26-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

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