



**THE DATASHEET OF
DG509BEY-T1-E3**





Precision 8-Channel / Dual 4-Channel CMOS Analog Multiplexers

DESCRIPTION

The DG508B is an 8-channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). The DG509B is a dual 4-channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address (A_0, A_1). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer / demultiplexer to all switches off for stacking several devices. All control inputs, addresses (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

The DG508B and DG509B are fabricated on an enhanced SG-II CMOS process that achieves improved performance on: reduced charge injection, lower device leakage, and minimized parasitic capacitance.

As the DG508, DG509 has a long history in the industry with many suppliers offering copies - and in some cases improved variations - with the best in class improvements, the Vishay Siliconix new version of the DG508B, DG509B are the superior alternatives to what is currently available.

Applications for the DG508B, DG509B include high speed and high precision data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

The DG508B and DG509B have the absolute maximum voltage rating extended to 44 V. Additionally, single supply operation is also allowed. An epitaxial layer prevents latch-up.

The DG508B and DG509B are both available in 16-lead SOIC, TSSOP, PDIP, and miniQFN (1.8 mm x 2.6 mm) package options with extended temperature range of -40 °C to +125 °C.

For more information, refer to Vishay Siliconix DG508B, DG509B evaluation board note.

FEATURES

- Operate with single or dual power supply
- V+ to V- analog signal swing range
- 44 V power supply maximum rating
- Extended operate temperature range: -40 °C to +125 °C
- Low leakage typically < 3 pA
- Low charge injection - $Q_{INJ} = 2$ pC
- Low power - $I_{SUPPLY} = 10$ μ A
- TTL compatible logic
- > 250 mA latch-up current per JESD78
- Available in SOIC16, TSSOP16, PDIP, and miniQFN16 packages
- Superior alternative to:
 - ADG508A, DG508A, HI-508
 - ADG509A, DG509A, HI-509
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

BENEFITS

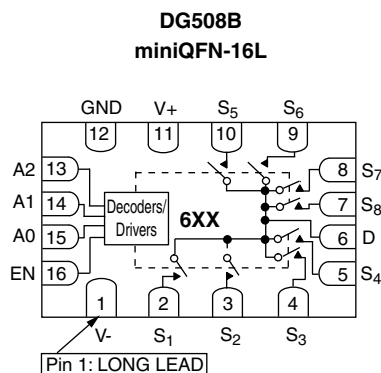
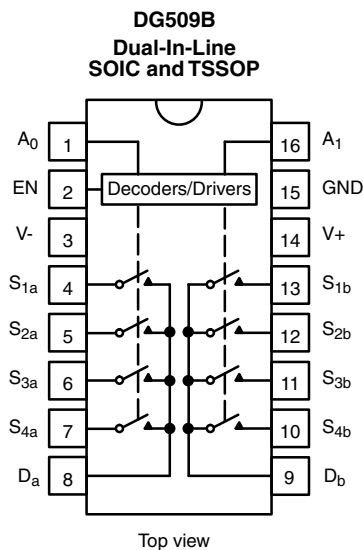
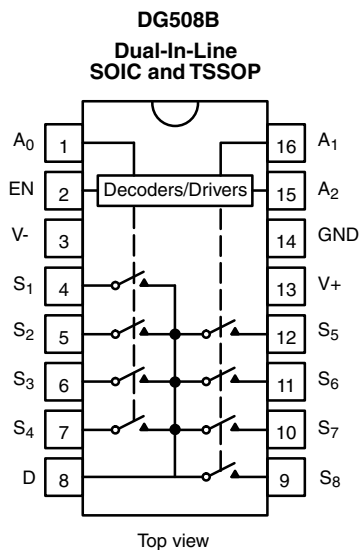
- Reduced switching errors
- Reduced glitching
- Improved data throughput
- Reduced power consumption
- Increased ruggedness
- Wide supply ranges (± 5 V to ± 20 V)

APPLICATIONS

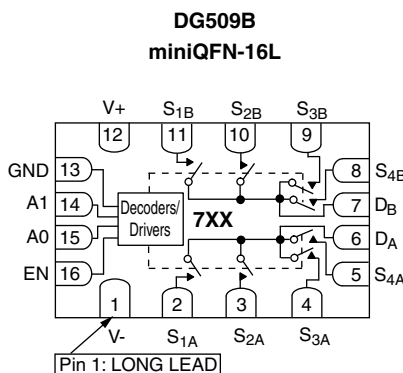
- Data acquisition systems
- Audio and video signal routing
- ATE systems
- Medical instrumentation



FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View
Device Marking: 6XX
Traceability Code:
6 is DG508BEN
XX = Date/Lot



Top View
Device Marking: 7XX
Traceability Code:
7 is DG509BEN
XX = Date/Lot

TRUTH TABLES AND ORDERING INFORMATION

TRUTH TABLE (DG508B)				
A ₂	A ₁	A ₀	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE (DG509B)			
A ₁	A ₀	EN	ON SWITCH
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = V_{IL} ≤ 0.8 V
Logic "1" = V_{IH} ≥ 2 V
X = Do not care



ORDERING INFORMATION (DG508B)		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +125 °C ^a	16-Pin SOIC	DG508BEY-T1-E3
	16-Pin TSSOP	DG508BEQ-T1-E3
	16-Pin PDIP	DG508BEJ-E3
	16-Pin MiniQFN	DG508BEN-T1-GE4

ORDERING INFORMATION (DG509B)		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +125 °C ^a	16-Pin SOIC	DG509BEY-T1-E3
	16-Pin TSSOP	DG509BEQ-T1-E3
	16-Pin PDIP	DG509BEJ-E3
	16-Pin MiniQFN	DG509BEN-T1-GE4

Note

a. -40 °C to +85 °C datasheet limits apply.

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		LIMIT	UNIT
Voltages Referenced to V-	V+	44	V
	GND	25	
Digital Inputs ^a , V _S , V _D		(V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first	
Current (Any terminal)		30	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature	(EY, EQ, EJ, EN suffix)	-65 to +150	°C
Power Dissipation (Packages) ^b	16-Pin Narrow SOIC ^c	600	mW
	16-Pin TSSOP ^d	450	
	16-Pin PDIP ^e	510	
	16-Pin miniQFN ^f	525	
Thermal Resistance (θ _{JA}) ^b	16-Pin Narrow SOIC ^c	125	°C/W
	16-Pin TSSOP ^d	178	
	16-Pin PDIP ^e	159.6	
	16-Pin miniQFN ^f	152	

Notes

- Signals on SX, DX or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads soldered or welded to PC board.
- Derate 8 mW/°C above 70 °C.
- Derate 5.6 mW/°C above 70 °C.
- Derate 6.3 mW/°C above 70 °C.
- Derate 6.6 mW/°C above 70 °C.



SPECIFICATIONS										
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED $V_+ = 15\text{ V}, V_- = -15\text{ V} (\pm 10\%)$ $V_{AX}, V_{EN} = 2\text{ V}, 0.8\text{ V}^a$	TEMP. ^b	TYP. ^c	-40 °C to +125 °C		-40 °C to +85 °C		UNIT	
					MIN. ^d	MAX. ^d	MIN. ^d	MAX. ^d		
Analog Switch										
Analog Signal Range ^e	V_{ANALOG}		Full	-	-15	15	-15	15	V	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_D = \pm 10\text{ V}, I_S = -1\text{ mA}$	Room	180	-	380	-	380	Ω	
			Full	-	-	480	-	450		
$R_{DS(on)}$ Matching	$\Delta R_{DS(on)}$	$V_D = \pm 10\text{ V}$	Room	10	-	-	-	-		
Source Off Leakage Current	$I_{S(off)}$	$V_D = \pm 10\text{ V}$ $V_S = \mp 10\text{ V}$ $V_{EN} = 0\text{ V}$	Room	-	-1	1	-1	1	nA	
Drain Off Leakage Current	$I_{D(off)}$		DG508B	Room	-	-1	1	-1		1
				Full	-	-100	100	-100		100
			DG509B	Room	-	-1	1	-1		1
				Full	-	-50	50	-50		50
Drain On Leakage Current	$I_{D(on)}$		DG508B	Room	-	-1	1	-1		1
		Full		-	-100	100	-100	100		
		DG509B	Room	-	-1	1	-1	1		
			Full	-	-50	50	-50	50		
Digital Control										
Logic High Input Voltage	V_{INH}		Full	-	2	-	2	-	V	
Logic Low Input Voltage	V_{INL}		Full	-	-	0.8	-	0.8		
Logic High Input Current	I_{IH}	$V_{AX}, V_{EN} = 2\text{ V}$	Full	-	-1	1	-1	1	μA	
Logic Low Input Current	I_{IL}	$V_{AX}, V_{EN} = 0.8\text{ V}$	Full	-	-1	1	-1	1		
Logic Input Capacitance ^e	C_{IN}	$f = 1\text{ MHz}$	Room	4	-	-	-	-	pF	
Dynamic Characteristics										
Transition Time	t_{TRANS}	$V_{S1} = +10\text{ V}/-10\text{ V},$ $V_{S8} = -10\text{ V}/+10\text{ V},$ $R_L = 1\text{ M}\Omega, C_L = 35\text{ pF}$	Room	145	-	300	-	300		
			Full	-	-	400	-	400		
Break-Before-Make Interval	t_{OPEN}	$V_{S1} = V_{S8} = 5\text{ V}, C_L = 35\text{ pF},$ $R_L = 1\text{ k}\Omega$	Room	37	15	-	15	-	ns	
			Full	-	1	-	1	-		
Enable Turn-On Time	$t_{ON(EN)}$	$V_{S1} = 5\text{ V}, V_{S2} \text{ to } V_{S8} = 0\text{ V},$ $R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$	Room	100	-	250	-	250		
			Full	-	-	340	-	340		
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	90	-	240	-	240		
			Full	-	-	300	-	300		
Charge Injection ^e	Q_{INJ}	$C_L = 1\text{ nF}, R_{GEN} = 0\text{ W}, V_{GEN} = 0\text{ V}$	Full	2	-	-	-	-	pC	
Off Isolation ^e	OIRR	$C_L = 5\text{ pF}, R_L = 50\text{ }\Omega, f = 1\text{ MHz}$	Room	-81	-	-	-	-	dB	
Crosstalk ^e	X_{TALK}		Room	-88	-	-	-	-		
-3 dB Bandwidth ^e	BW	$R_L = 50\text{ }\Omega$	Room	250	-	-	-	-	MHz	
Total Harmonic Distortion ^e	THD	$R_L = 10\text{ k}\Omega, 5\text{ V}_{rms}$ $f = 20\text{ Hz to } 20\text{ kHz}$	Room	0.04	-	-	-	-	%	
Source Off Capacitance ^e	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	3	-	-	-	-	pF	
Drain Off Capacitance ^e	$C_{D(off)}$		DG508B	Room	13	-	-	-		-
			DG509B	Room	8	-	-	-		-
Drain On Capacitance ^e	$C_{D(on)}$		DG508B	Room	18	-	-	-		-
		DG509B	Room	11	-	-	-	-		
Power Supply										
Positive Supply Current	I+	$V_{AX}, V_{EN} = 0.8\text{ V or } 2.4\text{ V}$	Room	0.01	-	0.2	-	0.2	mA	
			Full	-	-	0.3	-	0.3		
Negative Supply Current	I-		Full	0.06	-10	-	-10	-	μA	



SPECIFICATIONS (Single Supply 12 V)										
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED $V_+ = 12\text{ V}$, $V_- = 0\text{ V}$ ($\pm 10\%$) V_{AX} , $V_{EN} = 2\text{ V}$, 0.8 V^a	TEMP. ^b	TYP. ^c	-40 °C to +125 °C		-40 °C to +85 °C		UNIT	
					MIN. ^d	MAX. ^d	MIN. ^d	MAX. ^d		
Analog Switch										
Analog Signal Range ^e	V_{ANALOG}		Full	-	0	12	0	12	V	
On-Resistance	$R_{DS(on)}$	$V_D = 10\text{ V}/0\text{ V}$, $I_S = 1\text{ mA}$	Room	265	-	500	-	500	Ω	
$R_{DS(on)}$ Matching	$\Delta R_{DS(on)}$		Full	-	-	650	-	600		
Switch Off Leakage Current	$I_{S(off)}$	$V_+ = 12\text{ V}$, $V_- = 0\text{ V}$ $V_D = 0\text{ V}/10\text{ V}$, $V_S = 10\text{ V}/0\text{ V}$	Room	-	-1	1	-1	1	nA	
			Full	-	-50	-50	-50	50		
	$I_{D(off)}$		Room	-	-1	1	-1	1		
			Full	-	-100	100	-100	100		
	$I_{D(off)}$		Room	-	-1	1	-1	1		
			Full	-	-50	50	-50	50		
Channel On Leakage Current	$I_{D(on)}$	$V_+ = 12\text{ V}$, $V_- = 0\text{ V}$ $V_S = V_D = 0\text{ V}/10\text{ V}$	DG508B	Room	-	-1	1	-1	1	nA
			DG508B	Full	-	-100	100	-100	100	
			DG509B	Room	-	-1	1	-1	1	
			DG509B	Full	-	-50	50	-50	50	
Digital Control										
Logic High Input Voltage	V_{INH}		Full	-	2	-	2	-	V	
Logic Low Input Voltage	V_{INL}		Full	-	-	0.8	-	0.8		
Logic High Input Current	I_{IH}	V_{AX} , $V_{EN} = 2\text{ V}$	Full	-	-1	1	-1	1	μA	
Logic Low Input Current	I_{IL}	V_{AX} , $V_{EN} = 0.8\text{ V}$	Full	-	-1	1	-1	1		
Logic Input Capacitance ^e	C_{IN}	$f = 1\text{ MHz}$	Room	4	-	-	-	-	pF	
Dynamic Characteristics										
Transition Time	t_{TRANS}	$V_{S1} = 10\text{ V}/0\text{ V}$, $V_{S8} = 0\text{ V}/10\text{ V}$, $R_L = 1\text{ M}\Omega$, $C_L = 35\text{ pF}$	Room	165	-	400	-	400	ns	
			Full	-	-	550	-	500		
Break-Before-Make Interval	t_{OPEN}	$V_{S1} = V_{S8} = 5\text{ V}$, $C_L = 35\text{ pF}$, $R_L = 1\text{ k}\Omega$	Room	37	15	-	15	-		
			Full	-	1	-	1	-		
Enable Turn-On Time	$t_{ON(EN)}$	$V_{S1} = 5\text{ V}$, V_{S2} to $V_{S8} = 0\text{ V}$, $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$	Room	125	-	300	-	300		
			Full	-	-	550	-	425		
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	75	-	250	-	250		
			Full	-	-	350	-	300		
Charge Injection ^e	Q_{INJ}		$C_L = 1\text{ nF}$, $R_{GEN} = 0\text{ }\Omega$, $V_{GEN} = 0\text{ V}$	Full	2.5	-	-	-	-	pC
Off Isolation ^e	OIRR		$C_L = 5\text{ pF}$, $R_L = 50\text{ }\Omega$ $f = 1\text{ MHz}$	Room	-80	-	-	-	-	dB
Crosstalk ^e	X_{TALK}	Room		-88	-	-	-	-		
-3 dB Bandwidth ^e	BW	$R_L = 50\text{ }\Omega$	Room	200	-	-	-	-	MHz	
Total Harmonic Distortion ^e	THD	$R_L = 10\text{ k}\Omega$, 5 V_{RMS} , $f = 20\text{ Hz}$ to 20 kHz	Room	0.26	-	-	-	-	%	
Source Off Capacitance ^e	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	2	-	-	-	-	pF	
Drain Off Capacitance ^e	$C_{D(off)}$			DG508B	13	-	-	-		-
				DG509B	8	-	-	-		-
Channel On Capacitance ^e	$C_{D(on)}$			DG508B	17	-	-	-		-
				DG509B	12	-	-	-		-

SPECIFICATIONS (Single Supply 12 V)									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED $V_+ = 12\text{ V}$, $V_- = 0\text{ V}$ ($\pm 10\%$) V_{AX} , $V_{EN} = 2\text{ V}$, 0.8 V ^a	TEMP. ^b	TYP. ^c	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN. ^d	MAX. ^d	MIN. ^d	MAX. ^d	
Power Supply									
Positive Supply Current	I+	V_{AX} , $V_{EN} = 0.8\text{ V}$ or 2.4 V	Room	0.01	-	0.2	-	0.2	mA
			Full	-	-	0.3	-	0.3	

Notes

- V_{AX} , V_{EN} = input voltage perform proper function.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- Guaranteed by design, not subject to production test.
- $\Delta R_{DS(on)} = R_{DS(on)} \text{ max.} - R_{DS(on)} \text{ min.}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

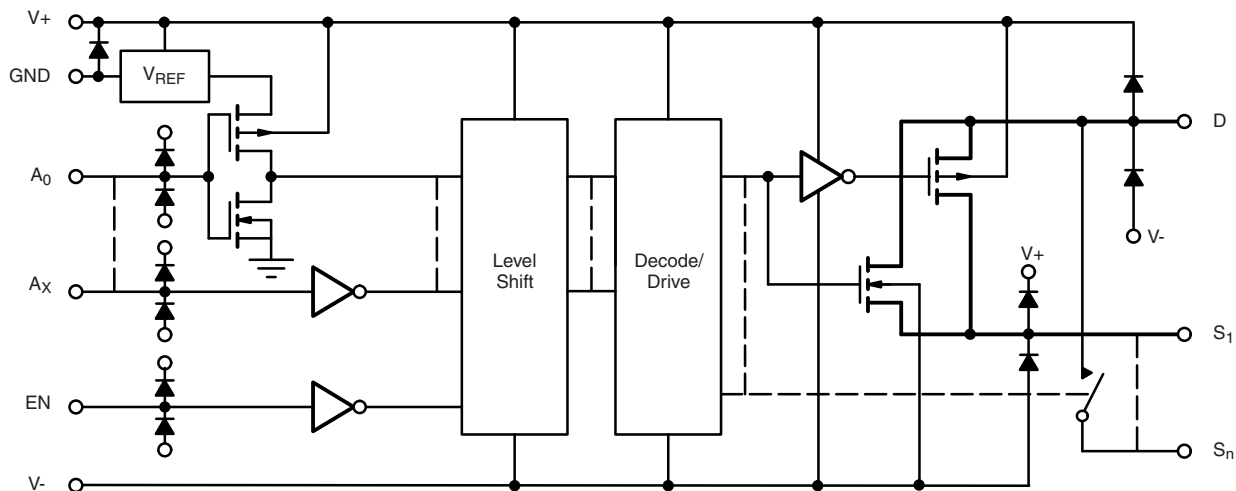
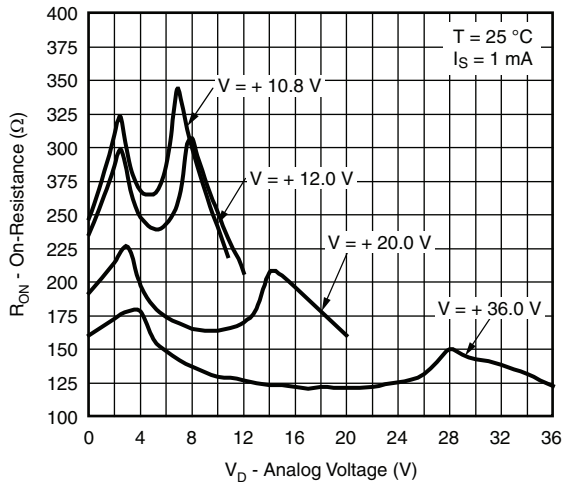
SCHEMATIC DIAGRAM (Typical Channel)


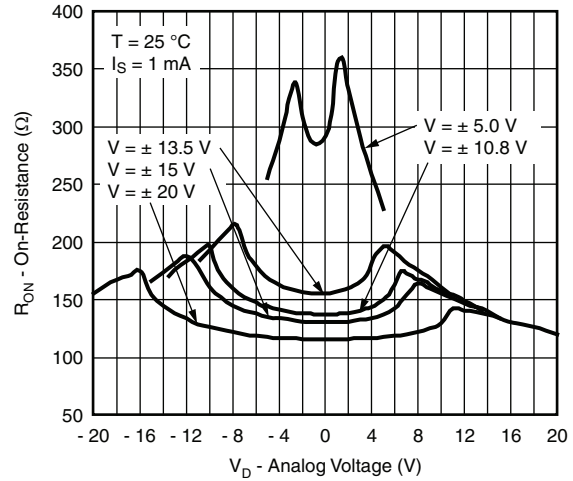
Fig. 1



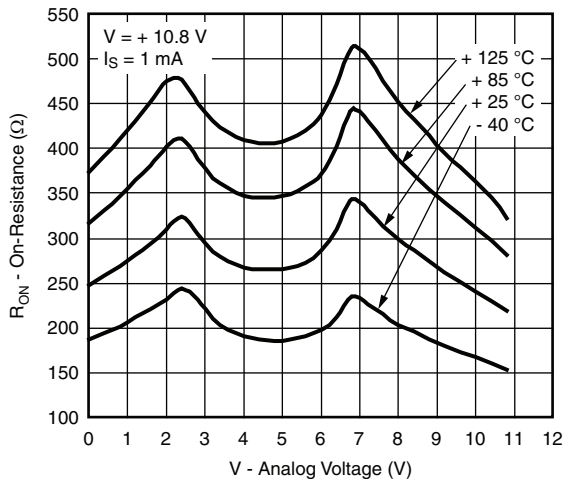
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



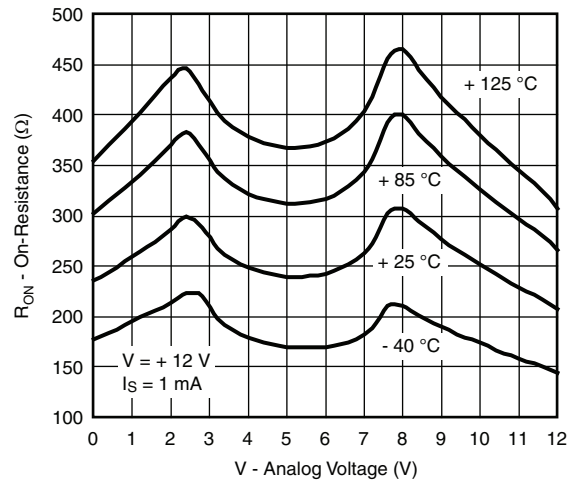
On-Resistance vs. V_D and Single Supply Voltage



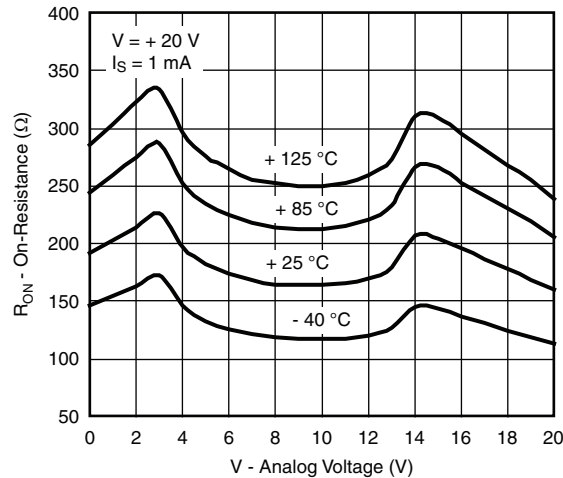
On-Resistance vs. V_D and Dual Supply Voltage



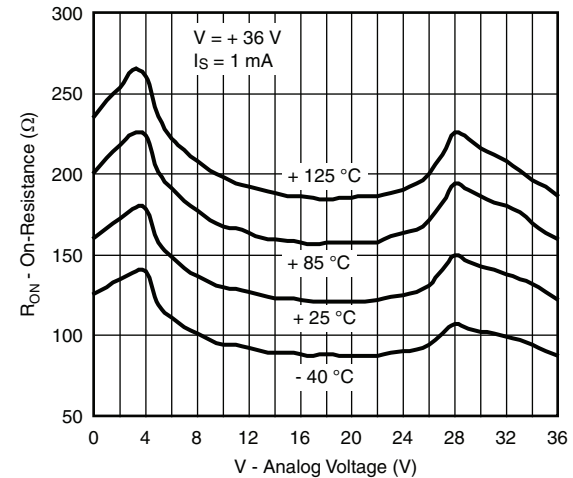
On-Resistance vs. Analog Voltage and Temperature



On-Resistance vs. Analog Voltage and Temperature



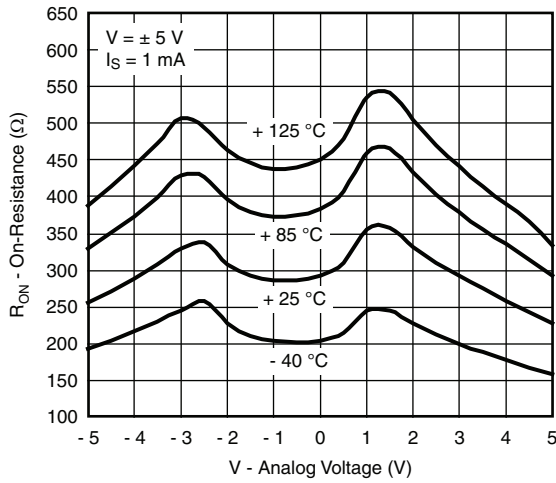
On-Resistance vs. Analog Voltage and Temperature



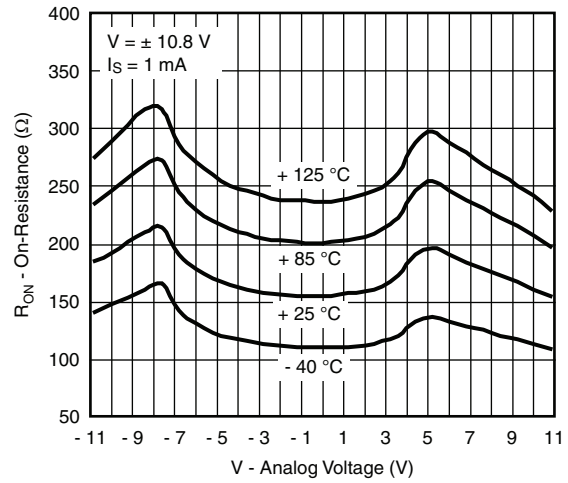
On-Resistance vs. Analog Voltage and Temperature



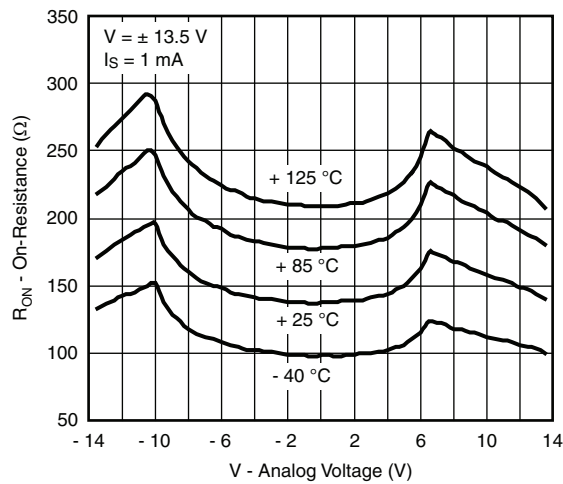
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



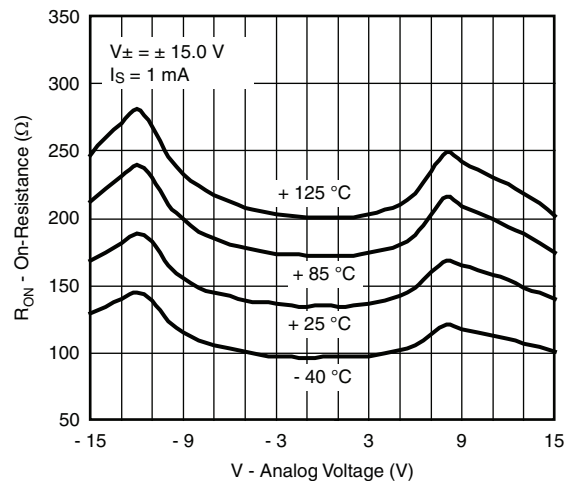
On-Resistance vs. Analog Voltage and Temperature



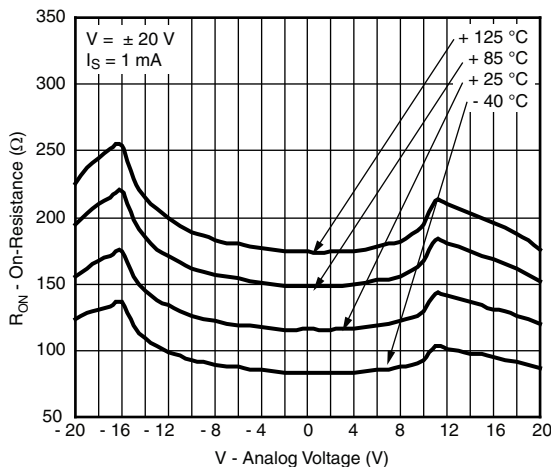
On-Resistance vs. Analog Voltage and Temperature



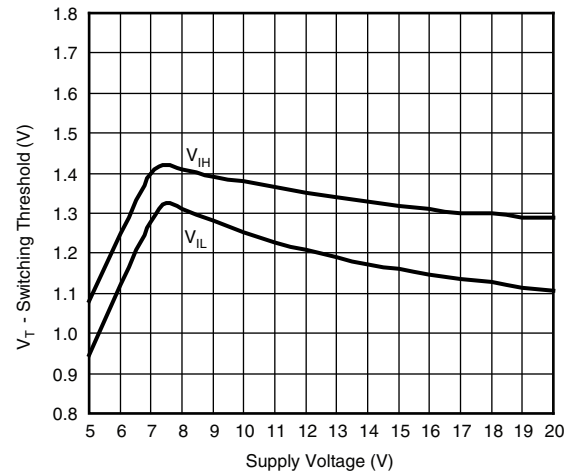
On-Resistance vs. Analog Voltage and Temperature



On-Resistance vs. Analog Voltage and Temperature



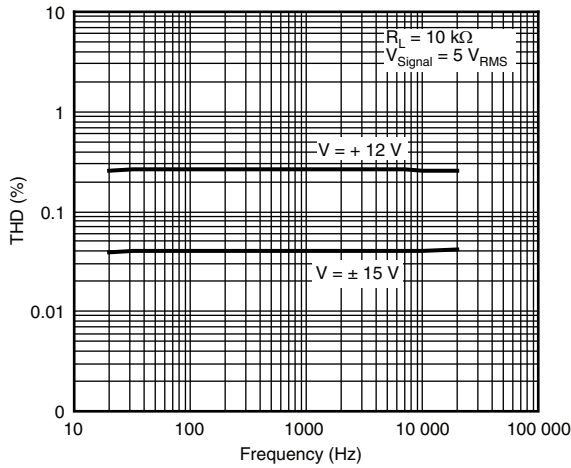
On-Resistance vs. Analog Voltage and Temperature



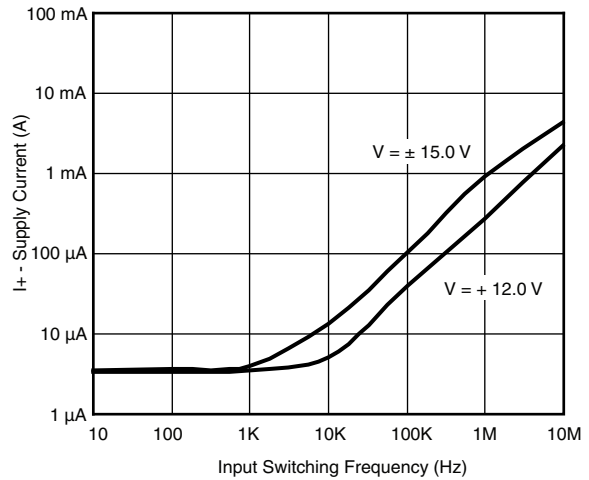
Switching Threshold vs. Supply Voltage



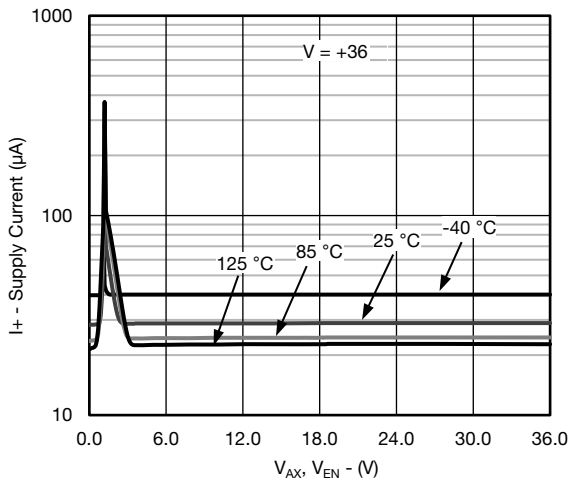
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



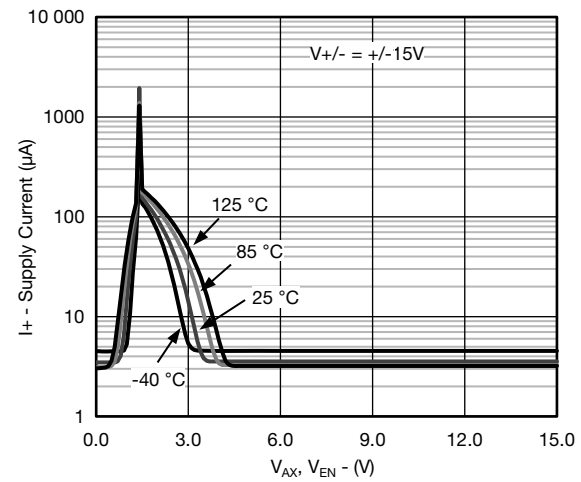
THD vs. Frequency



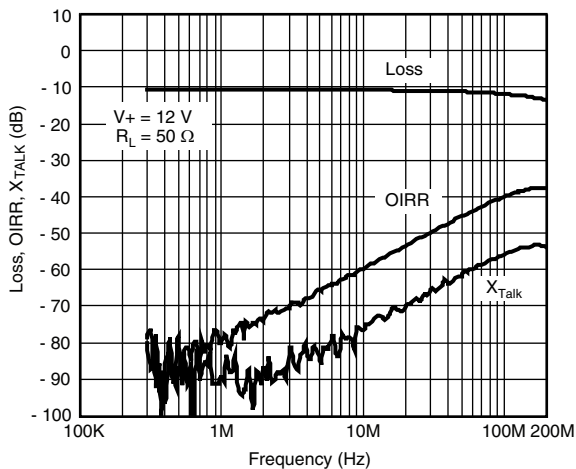
Supply Current vs. Input Switching Frequency



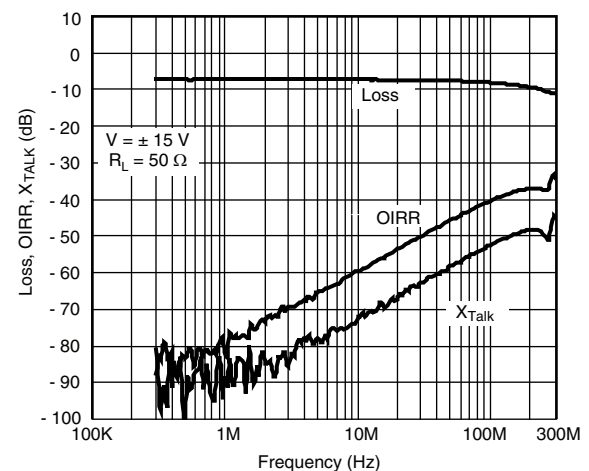
Supply Current vs. $V_{\text{AX}}, V_{\text{EN}}$



Supply Current vs. $V_{\text{AX}}, V_{\text{EN}}$



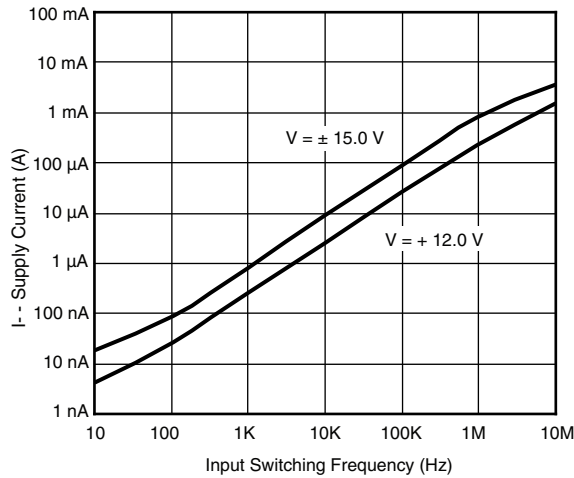
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



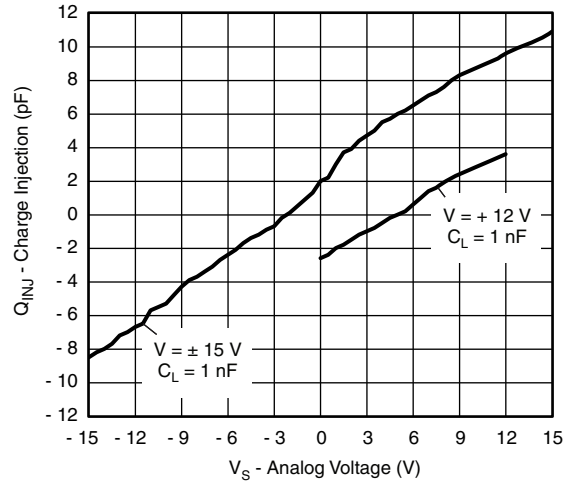
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



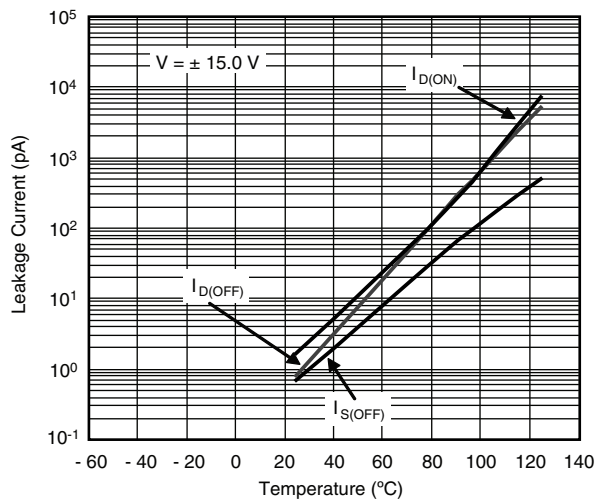
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



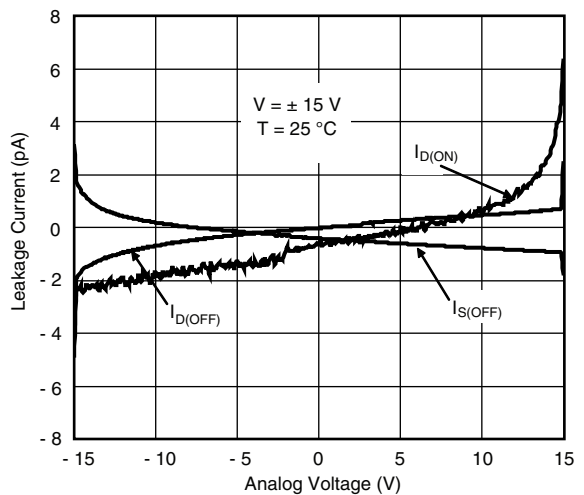
Supply Current vs. Input Switching Frequency



Charge Injection vs. Analog Voltage



Leakage Current vs. Temperature



Leakage Current vs. Analog Voltage

TEST CIRCUITS

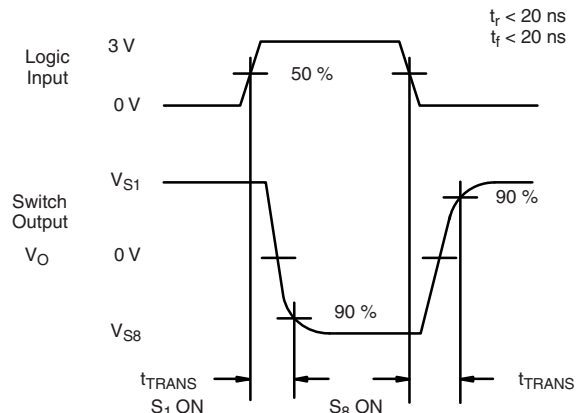
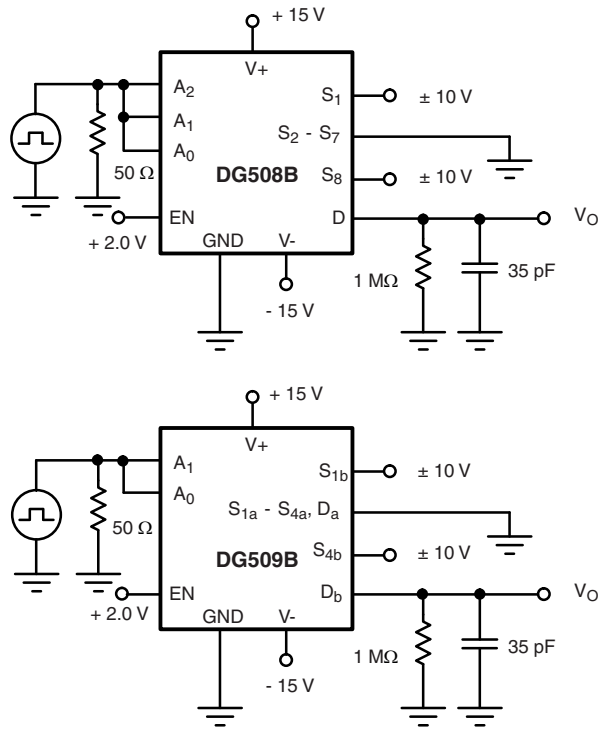


Fig. 2 - Transition Time

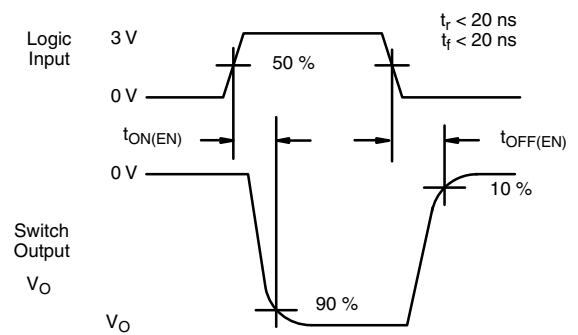
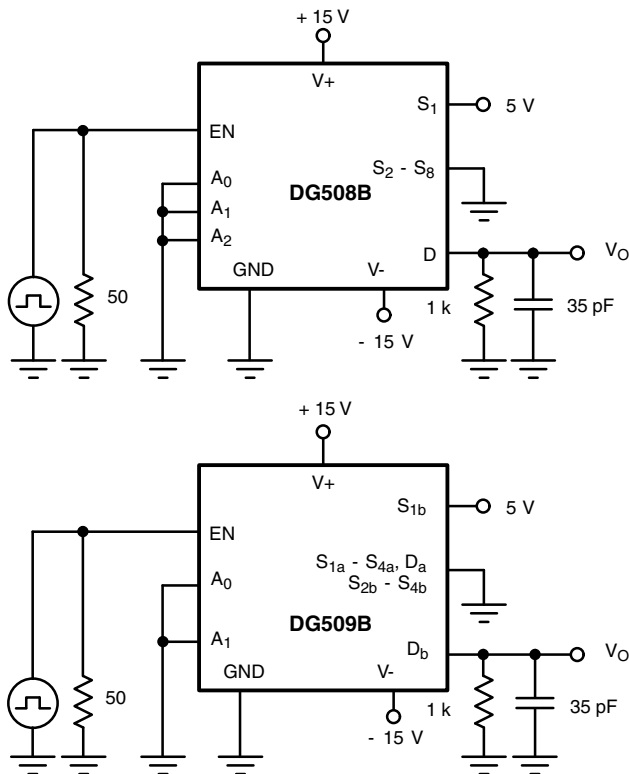


Fig. 3 - Enable Switching Time

TEST CIRCUITS

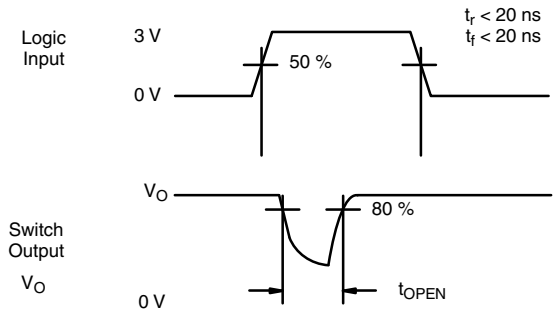
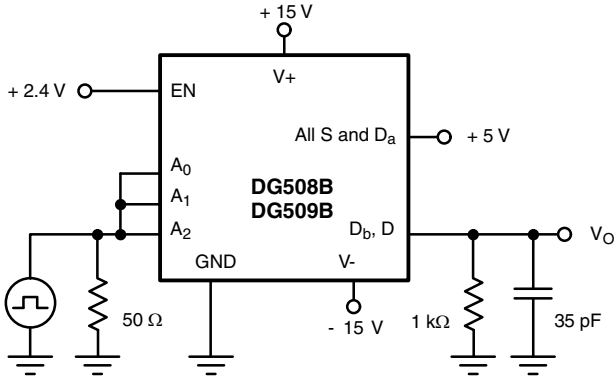


Fig. 4 - Break-Before-Make Interval

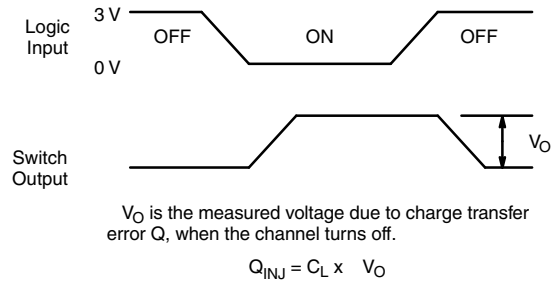
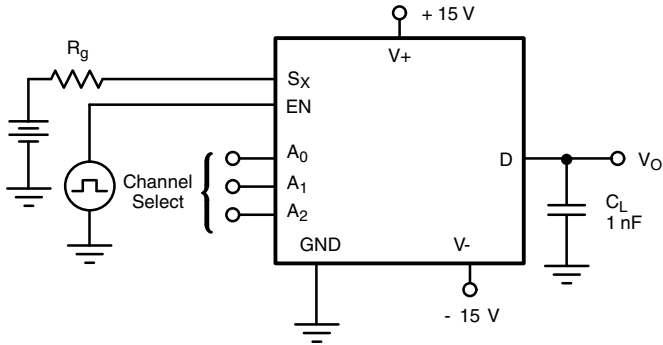


Fig. 5 - Charge Injection

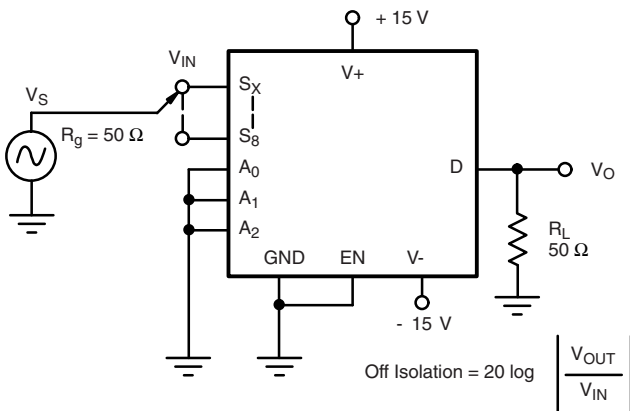


Fig. 6 - Off Isolation

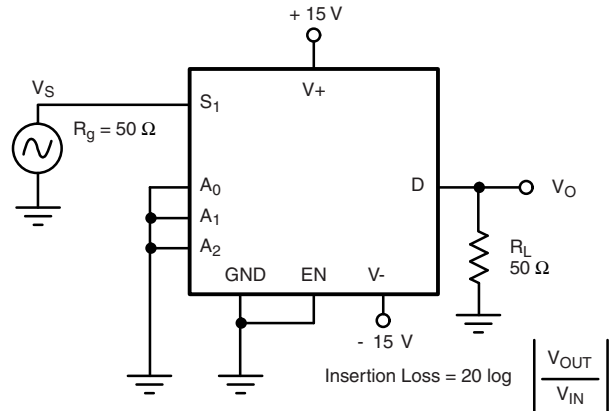
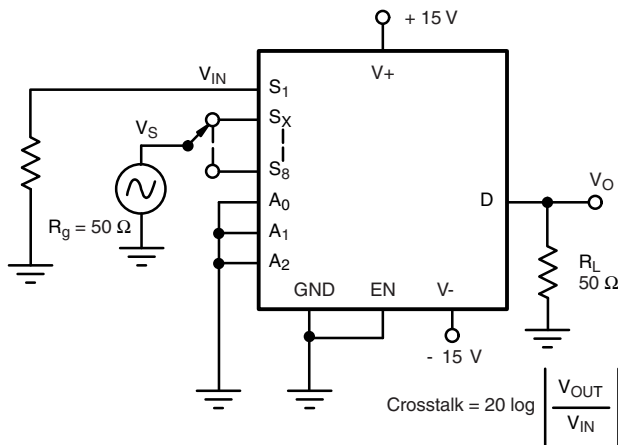
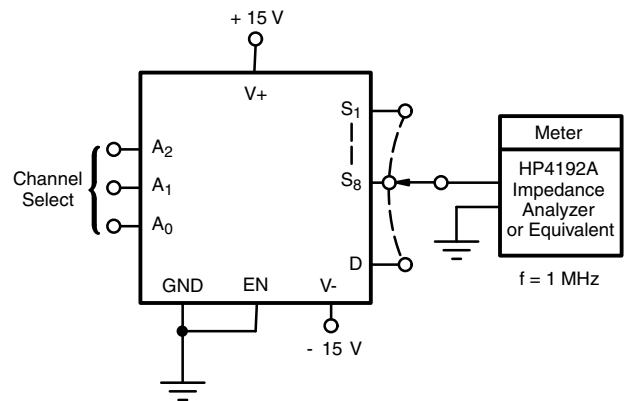
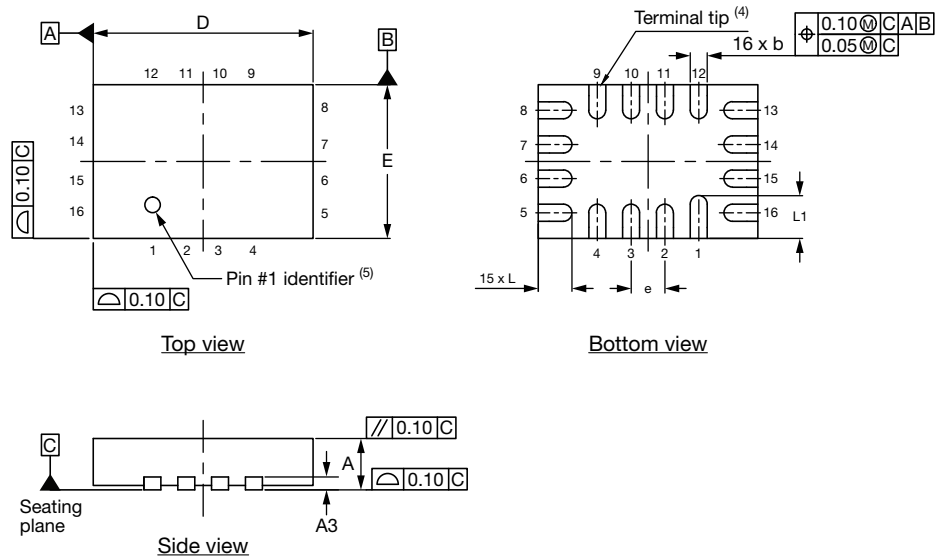


Fig. 7 - Insertion Loss

TEST CIRCUITS

Fig. 8 - Crosstalk

Fig. 9 - Source Drain Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?64821.

Thin miniQFN16 Case Outline



DIMENSIONS	MILLIMETERS ⁽¹⁾			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0	-	0.05	0	-	0.002
A3	0.15 ref.			0.006 ref.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.50	2.60	2.70	0.098	0.102	0.106
e	0.40 BSC			0.016 BSC		
E	1.70	1.80	1.90	0.067	0.071	0.075
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.018	0.020	0.022
N ⁽³⁾	16			16		
Nd ⁽³⁾	4			4		
Ne ⁽³⁾	4			4		

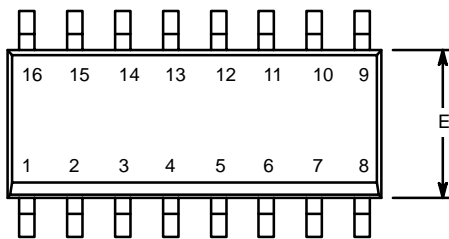
Notes

- (1) Use millimeters as the primary measurement.
- (2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
- (3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
- (4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
- (5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
- (6) Package warpage max. 0.05 mm.

ECN: T16-0226-Rev. B, 09-May-16
DWG: 6023

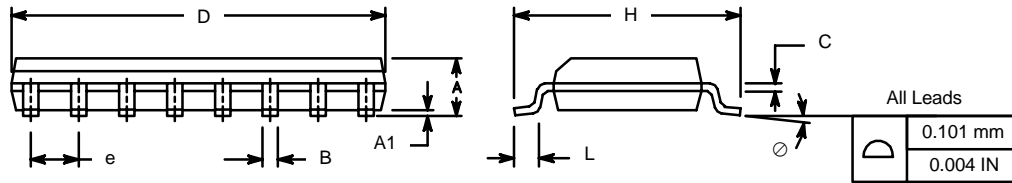


SOIC (NARROW): 16-LEAD
JEDEC Part Number: MS-012

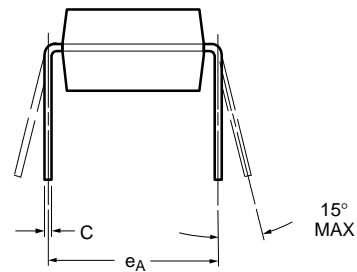
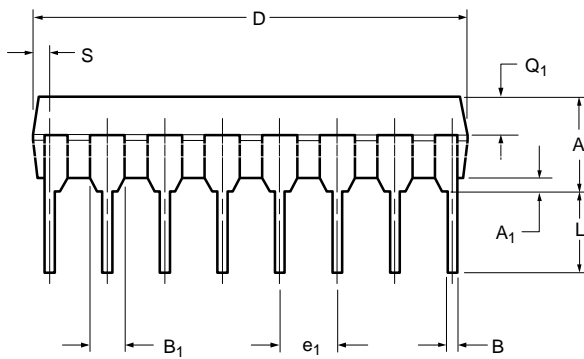
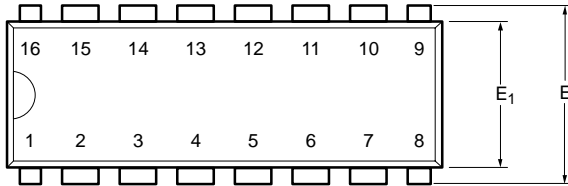


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
∅	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



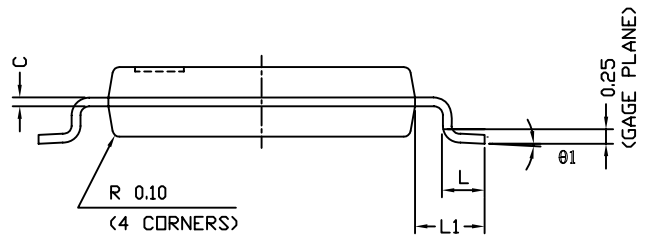
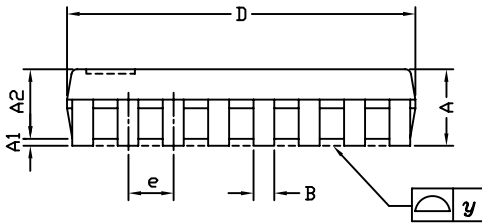
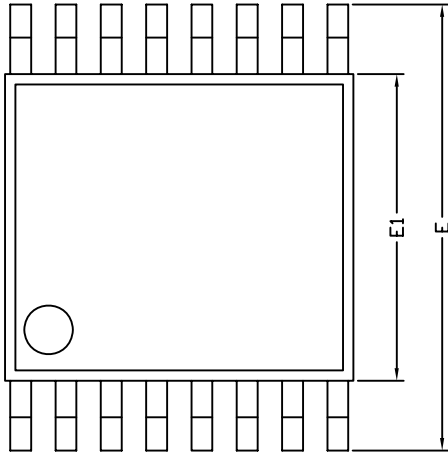
PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A₁	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B₁	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E₁	5.59	7.11	0.220	0.280
e₁	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q₁	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060

ECN: S-03946—Rev. D, 09-Jul-01
DWG: 5482

TSSOP: 16-LEAD

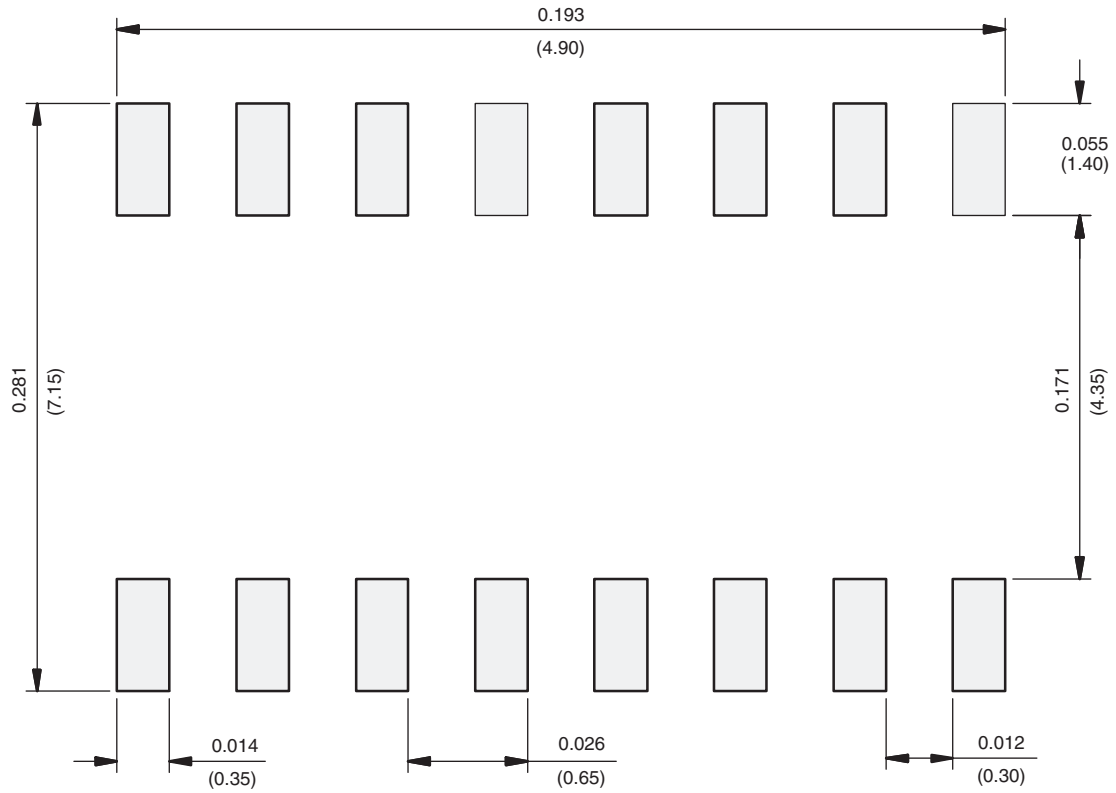


Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°

ECN: S-61920-Rev. D, 23-Oct-06
DWG: 5624

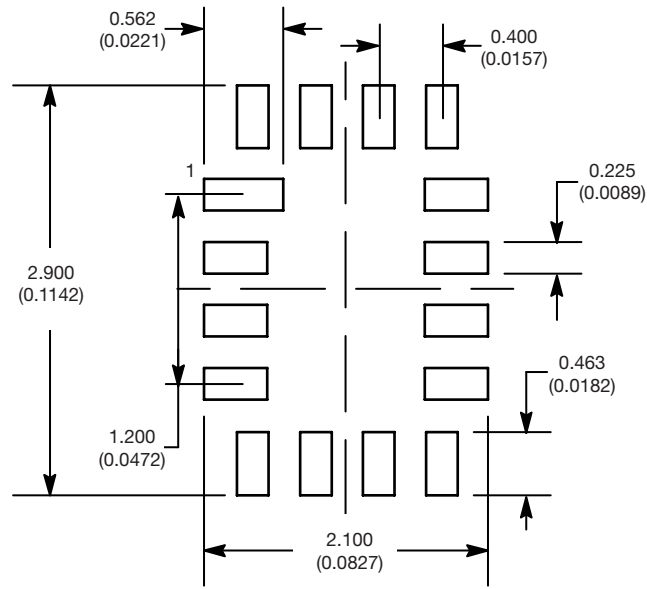


RECOMMENDED MINIMUM PAD FOR TSSOP-16



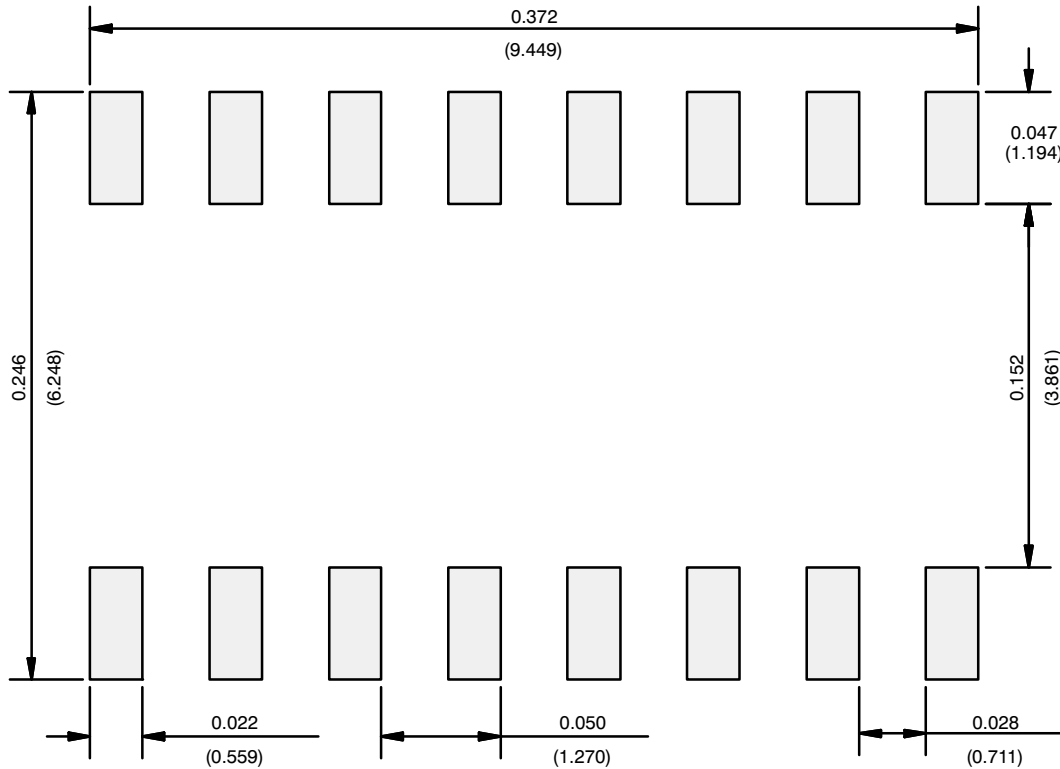
Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR MINI QFN 16L



Mounting Footprint
Dimensions in mm (inch)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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