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FSA6157 Low- R_{ON} SPDT (0.8 Ω) Negative-Swing Audio or Video Switch

Features

- 0.8 Ω Typical On Resistance (R_{ON}) for +2.7V Supply
- 0.45 Ω Maximum R_{ON} Flatness for +2.7V Supply
- -3db Bandwidth: > 50MHz
- Low I_{CC} Current Over an Expanded Control Input Range
- Packaged in Pb-free 6-Lead MicroPak™ (1.0 x 1.4mm)
- Power-Off Protection on All I/O Ports
- Broad V_{CC} Operating Range: 1.65 to 4.3V
- HBM JEDEC: JESD22-A114
 - I/O to GND: 12kV
- Power to GND: 16kV

Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-top Box

Description


The FSA6157 is a high-performance, Single Pole Double Throw (SPDT) analog switch that features a low R_{ON} of 0.8 Ω (typical) at 2.7V supply. The FSA6157 operates over a wide V_{CC} range of 1.65V to 4.3V and is designed for break-before-make operation. The select input is TTL-level compatible.

The FSA6157 features very low quiescent current even when the control voltage is lower than the V_{CC} supply. This feature suits mobile handset applications by allowing direct interface with baseband processor general-purpose I/Os with minimal battery consumption.

IMPORTANT NOTE:

For additional performance information, please contact analogswitch@fairchildsemi.com.

Ordering Information

Part Number	Top Mark	 Eco Status	Package Description
FSA6157L6X	GT	Green	6-Lead, MicroPak™, 1.0mm wide, JEDEC MO-255

 For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Analog Symbol

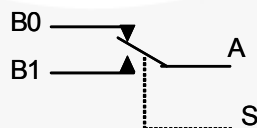


Figure 1. FSA6157

Pin Assignments

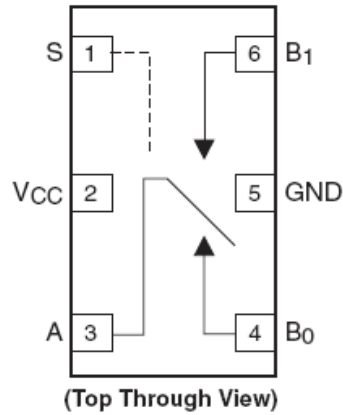


Figure 2. Pin Assignments for 6-Lead MicroPak™

Pin Descriptions

Name	Description
A, B ₀ , B ₁	Data Ports
S	Switch Select Pin

Truth Table

Control Input, S	Function
LOW	B ₀ connected to A
HIGH	B ₁ connected to A

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
V _{CC}	Supply Voltage		-0.5	4.6	V
V _{SW}	Switch I/O Voltage ⁽¹⁾	B0, B1, A Pins	V _{CC} - 5.5V	4.6	V
V _{SW-SW}	Switch I/O to Switch I/O Voltage Delta (Off State) ⁽¹⁾	B0, B1, A Pins		5.5	V
V _{CNTRL}	Control Input Voltage ⁽¹⁾	S	-0.5	4.6	V
I _{IK}	Input Clamp Diode Current			-50	mA
I _{SW}	Switch I/O Current (Continuous)			350	mA
I _{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)			500	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
T _J	Maximum Junction Temperature			+150	°C
T _L	Lead Temperature (Soldering, 10 seconds)			+260	°C
ESD	Human Body Model (JEDEC: JESD22-A114)	I/O to GND		12	kV
		Power to GND		16	
		All Other Pins		8	
	Charge Device Model (JEDEC: JESD22-C101)				2

Note:

- Input and output negative ratings may be exceeded if input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V _{CC}	Supply Voltage	1.65	4.3	V
V _{CNTRL} ⁽²⁾	Control Input Voltage – Select Pin	0	V _{CC}	V
V _{SW}	Switch I/O Voltage	V _{CC} - 4.3V	4.3	V
V _{SW-SW}	Switch I/O Voltage to Switch I/O Voltage (Off-State)		4.6	V
T _A	Operating Temperature	-40	85	°C

Note:

- Input and output negative ratings may be exceeded if input and output diode current ratings are observed.

DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V _{CC} (V)	T _A =+25°C			T _A =-40 to +85°C		Unit	
				Min.	Typ.	Max.	Min.	Max.		
	Analog Signal Range			V _{CC} -4.3V		V _{CC}			V	
V _{IK}	Clamp Diode Voltage		3.00					-1.2	V	
V _{IH}	Input Voltage High		3.60 to 4.30				1.4		V	
			2.70 to 3.60				1.3			
			2.30 to 2.70				1.3			
			1.65 to 1.95				0.9			
V _{IL}	Input Voltage Low		3.60 to 4.30					0.7	V	
			2.70 to 3.60					0.4		
			2.30 to 2.70					0.4		
			1.65 to 1.95					0.4		
I _{IN}	Control Input Leakage (S)	V _{IN} =0 to V _{CC}	4.30				-1	1	μA	
I _{NO(OFF)} , I _{NC(OFF)}	Off Leakage Current of Port B0 and B1	A=0.5V, V _{CC} - 0.5V B0 or B1=V _{CC} - 0.5V, 0.5V, or Floating; Figure 4	1.95 to 4.30	-100		100	-500	500	nA	
I _{A(ON)}	On Leakage Current of Port A	A=0.5V, V _{CC} - 0.5V B0 or B1=V _{CC} -0.5V, 0.5V, or Floating; Figure 5	4.30	-100		100	-250	250	nA	
I _{OFF}	Power-Off Leakage Current (All I/O Ports)	V _{A,BN} =0.3V to 4.3V or Floating,	0V or Floating				-40	40	μA	
R _{ON}	Switch On Resistance ^(3,6)		I _{ON} =100mA, B0 or B1=0, 0.7V, 3.6V, 4.3V; Figure 3	4.30		0.4			0.8	Ω
			I _{ON} =100mA, B0 or B1=0, 0.7V, 2.0V, 2.7V; Figure 3	2.70		0.8			1.0	
			I _{ON} =100mA, B0 or B1=0, 0.7V, 1.6V, 2.3V; Figure 3	2.30					1.5	
			I _{ON} =100mA, B0 or B1=0, 0.7V, 1.65V; Figure 3	1.65		1.3			2.0	
ΔR _{ON}	On Resistance Matching Between Channels ⁽⁴⁾	I _{ON} =100mA, B0 or B1=0.7V	2.30 to 4.30		0.050			0.130	Ω	
R _{FLAT(ON)}	On Resistance Flatness ⁽⁵⁾	I _{OUT} =100mA, B0 or B1=0V to V _{CC}	2.70 to 4.30					0.45	Ω	
I _{CC}	Quiescent Supply Current	V _{SW} =0 or V _{CC} , I _{OUT} =0	4.30	-100		100	-500	500	nA	
I _{OCT}	Increase in I _{CC} per Input	Input at 2.6V	4.30		3.0			10.0	μA	
		Input at 1.8V			7.0					

Notes:

- On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
- Δ R_{ON}=R_{ON max} - R_{ON min} measured at identical V_{CC}, temperature, and voltage.
- Flatness is defined as the difference between the maximum and minimum value of on resistance (R_{ON}) over the specified range of conditions.
- Guaranteed by characterization, not production tested.

AC Electrical Characteristics

All typical value are for V_{CC}=1.8V, 2.5V, 3.3V, and 4.0V at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V _{CC} (V)	T _A =+25°C			T _A =-40 to +85°C		Unit	Figure
				Min.	Typ.	Max.	Min.	Max.		
t _{ON}	Turn-On Time	B0 or B1=1.0V, R _L =50Ω, C _L =35pF	3.60 to 4.30	5		65	3	70	ns	Figure 6 Figure 7
			2.70 to 3.60	5		65	3	70		
			2.30 to 2.70	5		70	3	80		
			1.65 to 1.95	10		100	10	150		
t _{OFF}	Turn-Off Time	B0 or B1=1.0V, R _L =50Ω, C _L =35pF	3.60 to 4.30	1		35	1	45	ns	Figure 6 Figure 7
			2.70 to 3.60	1		35	1	45		
			2.30 to 2.70	2		45	2	50		
			1.65 to 1.95	2		70	2	95		
t _{BBM}	Break-Before-Make Time	B0 or B1=1.0V, R _L =50Ω, C _L =35pF	3.60 to 4.30				2		ns	Figure 8
			2.70 to 3.60				2			
			2.30 to 2.70				2			
			1.65 to 1.95				2			
Q	Charge Injection	C _L =1.0nF, V _S =0V, R _S =0Ω	3.60 to 4.30		25				pC	Figure 12
			2.70 to 3.60		15					
			2.30 to 2.70		12					
			1.65 to 1.95		5					
OIRR	Off Isolation	f=20kHz, R _L =50Ω, C _L =0pF	1.65 to 4.30		-60				dB	Figure 10
Xtalk	Crosstalk	f=20kHz, R _L =50Ω, C _L =0pF	1.65 to 4.30		-60				dB	Figure 11
BW	-3db Bandwidth	R _L =50Ω, C _L =0pF	1.65 to 4.30		>50				MHz	Figure 9
THD	Total Harmonic Distortion	f=20Hz to 20kHz, R _L =32Ω, V _{IN} =2V _{PP}	1.65 to 4.30		0.1				%	Figure 15
SNR	Signal to Noise Ratio	f=1kHz, R _L =32Ω, V _{IN} =0dBm, V _{BIAS} =0V	4.30		-70				dB	

Capacitance

Symbol	Parameter	Conditions	V _{CC} (V)	T _A =+25°C			Unit	Figure
				Min.	Typ.	Max.		
C _{IN}	Control Pin Input Capacitance	f=1MHz	0		3		pF	Figure 13
C _{OFF}	B Port Off Capacitance	f=1MHz	3.30			30	pF	Figure 13
C _{ON}	A Port On Capacitance	f=1MHz	3.30			150	pF	Figure 14

Test Diagrams

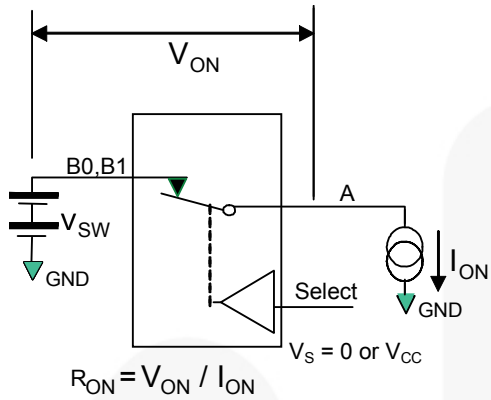


Figure 3. On Resistance

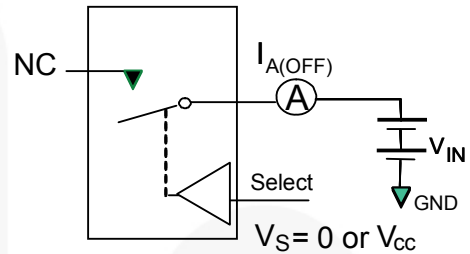


Figure 4. Off Leakage (Ports Tested Separately)

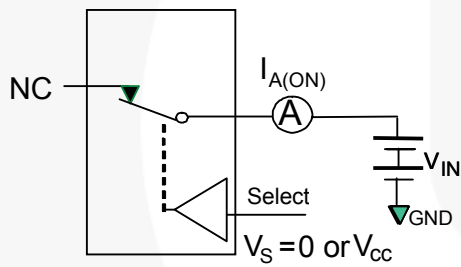


Figure 5. On Leakage

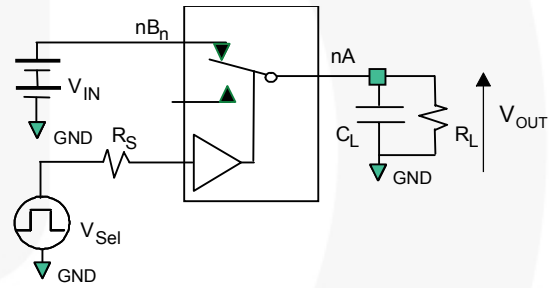


Figure 6. Test Circuit Load

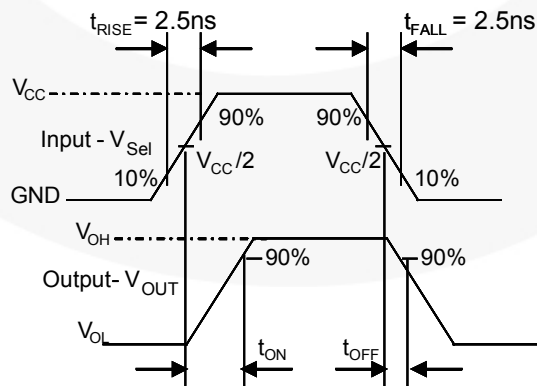


Figure 7. Turn-On / Turn-Off Waveforms

Test Diagrams (Continued)

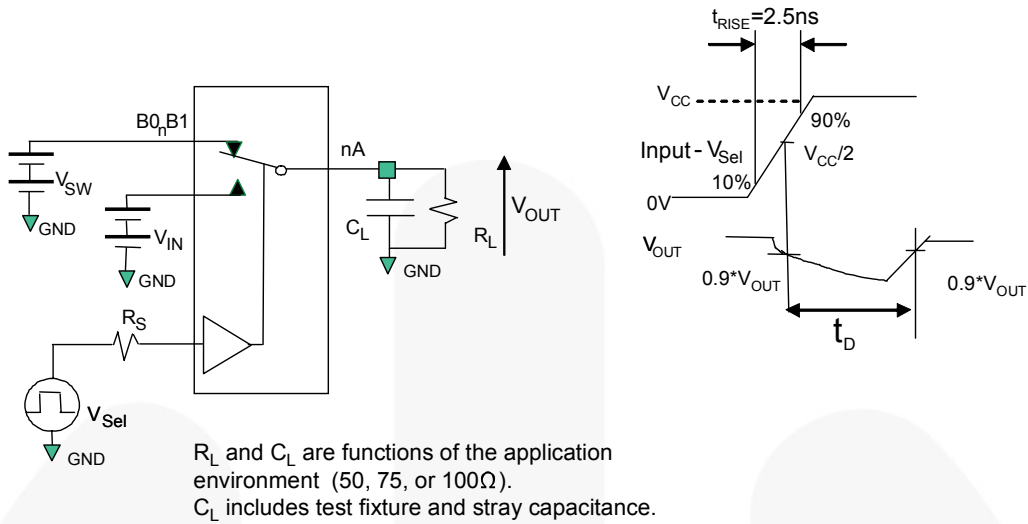


Figure 8. Break-Before-Make Interval Timing

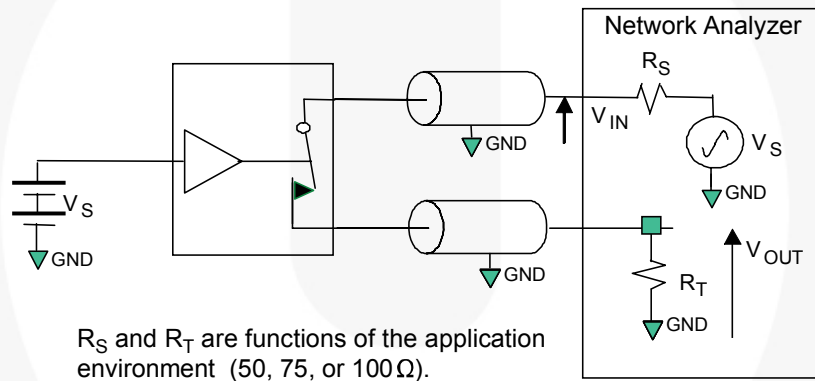


Figure 9. Bandwidth

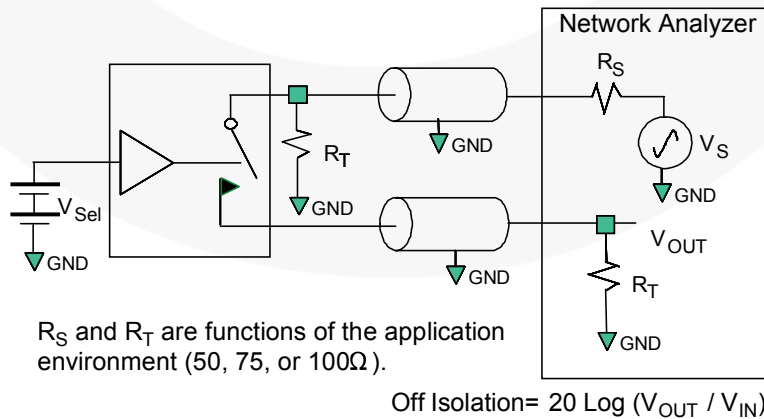


Figure 10. Channel Off Isolation

Test Diagrams (Continued)

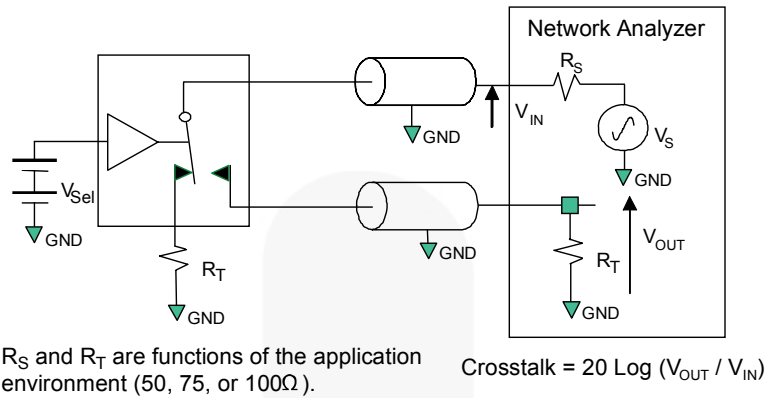


Figure 11. Adjacent Channel Crosstalk

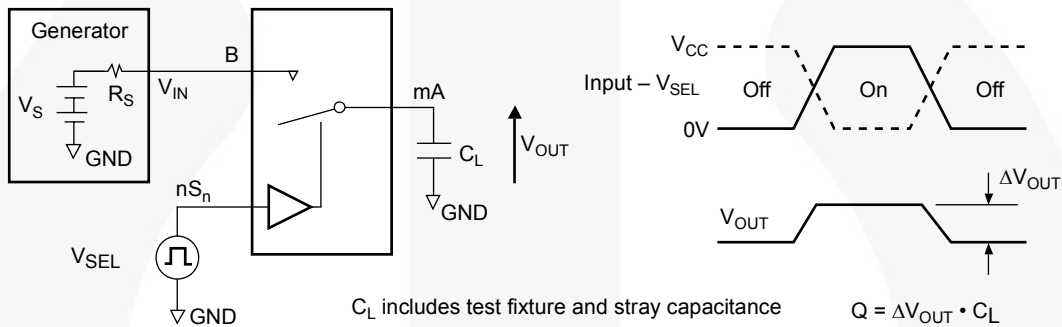


Figure 12. Charge Injection Test

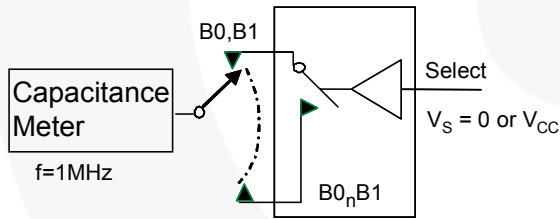


Figure 13. Channel Off Capacitance

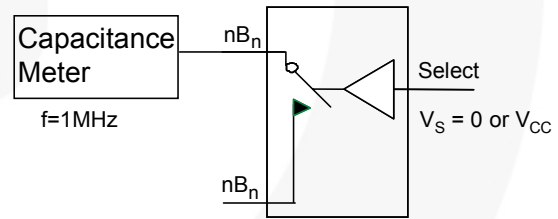


Figure 14. Channel On Capacitance

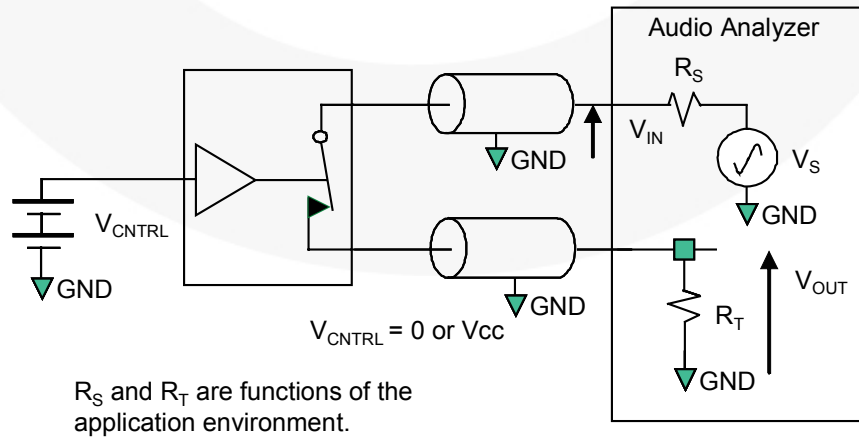
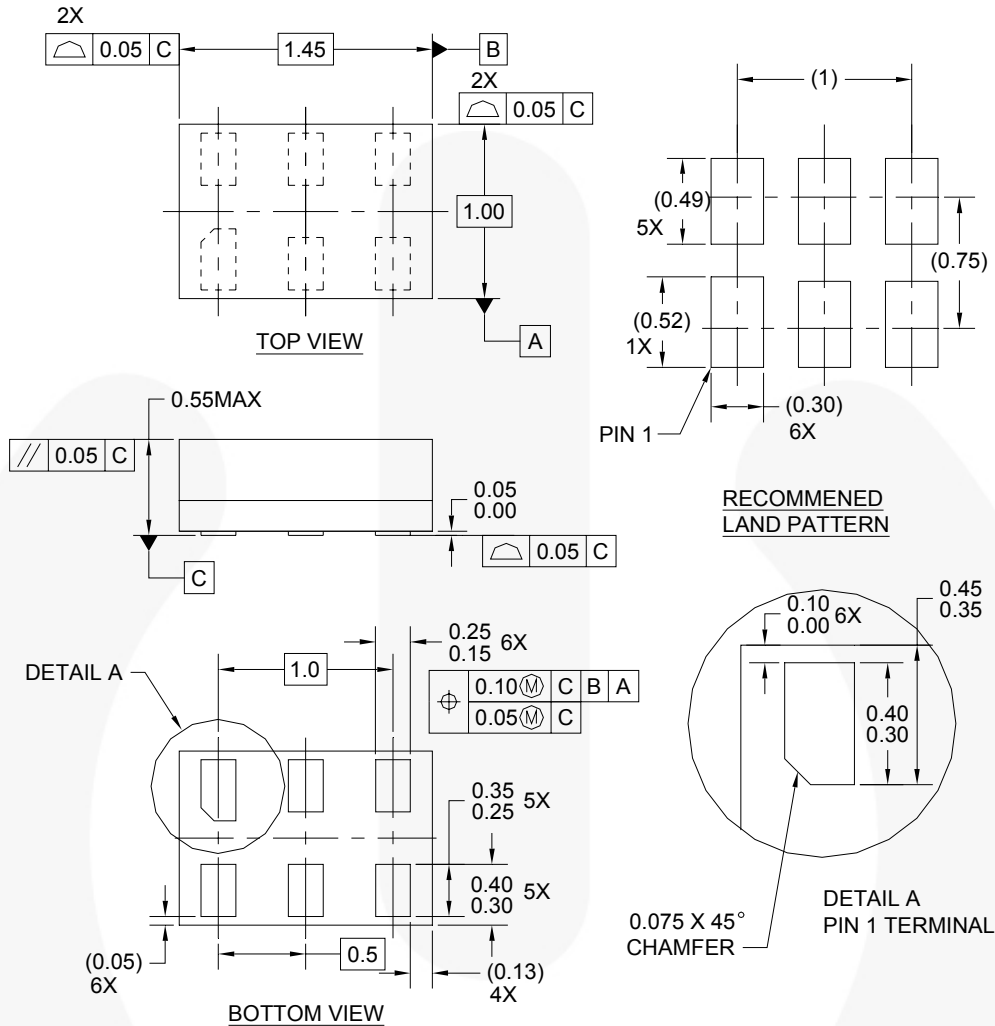


Figure 15. Total Harmonic Distortion

Physical Dimensions



MAC06AREVC

Figure 16. 6-Lead MicroPak™, 1.0mm Wide

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