THE DATASHEET OF

TPS2553DDBVT

TPS255xD Precision Adjustable Current-Limited Power-Distribution Switches

1 Features

- Up to 1.5 A Maximum Load Current
- ±6% Current-Limit Accuracy at 1.7 A (Typ)
- Meets USB Current-Limiting Requirements
- Backwards Compatible with TPS2550/51
- Adjustable Current Limit, 75 mA–1700 mA (Typ)
- Constant-Current (TPS2552D and TPS2553D)
- TPS2552D (Enable Low) and TPS2553D (Enable High)
- Fast Overcurrent Response - 2 µs (Typ)
- 85-mΩ High-Side MOSFET (DBV Package)
- Reverse Input-Output Voltage Protection
- Operating Range: 2.7 V to 6.5 V
- Built-in Soft-Start
- 15 kV ESD Protection per IEC 61000-4-2 (With External Capacitance)
- UL Listed – File No. E169910 and NEMKO IEC60950-1-am1 ed2.0
- See the TI Switch Portfolio

2 Applications

- USB Ports/Hubs
- Digital TV
- Set-Top Boxes
- VOIP Phones

3 Description

The TPS2552D and TPS2553D power-distribution switches are intended for applications where precision current limiting is required or heavy capacitive loads and short circuits are encountered and provide up to 1.5 A of continuous load current. These devices offer a programmable current-limit threshold between 75 mA and 1.7 A (typ) via an external resistor. Current-limit accuracy as tight as ±6% can be achieved at the higher current-limit settings. The power-switch rise and fall times are controlled to minimize current surges during turn on/off.

The TPS2552D/3D devices limit the output current to a safe level by using a constant-current mode when the output load exceeds the current-limit threshold. An internal reverse-voltage comparator disables the power-switch when the output voltage is driven higher than the input to protect devices on the input side of the switch. The FAULT output asserts low during overcurrent and reverse-voltage conditions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2552D	SOT-23 (6)	2.90 mm × 1.60 mm
TPS2553D	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

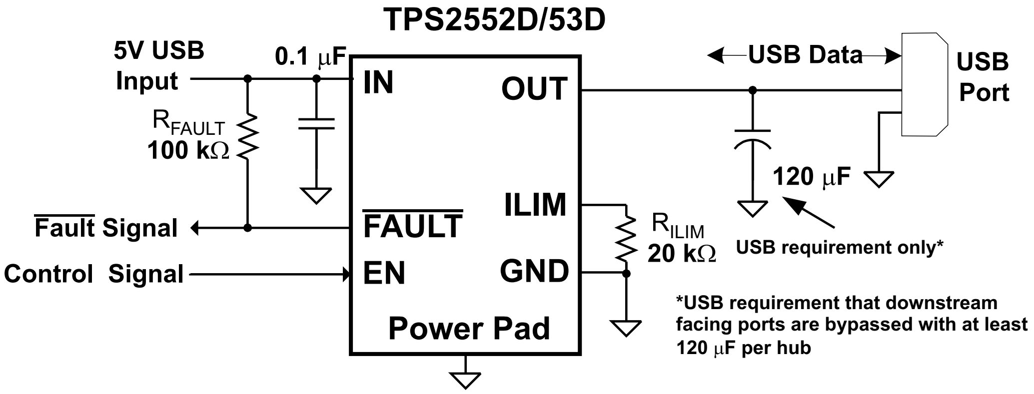


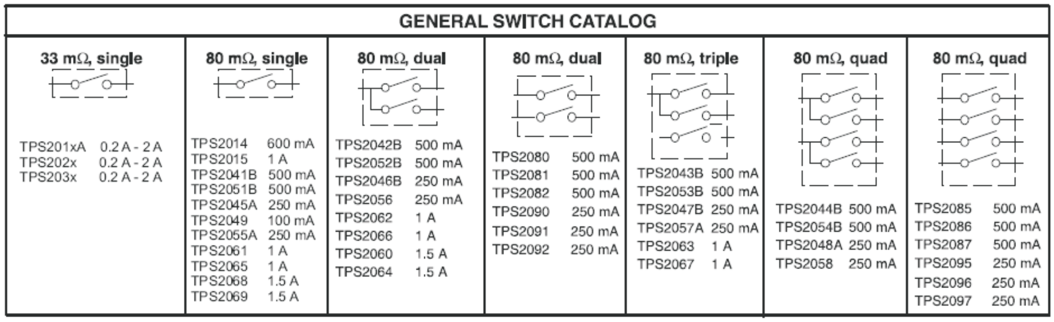
Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2016	*	Initial Release

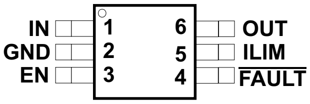
5 Device Comparison Table



GENERAL SWITCH CATALOG						
33 mΩ, single	**80 mΩ, single**	**80 mΩ, dual**	**80 mΩ, dual**	**80 mΩ, triple**	**80 mΩ, quad**	**80 mΩ, quad**
TPS201xA 0.2 A - 2 A TPS202x 0.2 A - 2 A TPS203x 0.2 A - 2 A	TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A	TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A	TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA	TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA

6 Pin Configuration and Functions

TPS2552D/3D
DBV Package
Top View



EN = Active Low for the TPS2552D

EN = Active High for the TPS2553D

Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS2552D	TPS2553D		
	DBV	DBV		
$\overline{\text{EN}}$	3	–	I	Enable input, logic low turns on power switch
EN	–	3	I	Enable input, logic high turns on power switch
GND	2	2		Ground connection; connect externally to PowerPAD
IN	1	1	I	Input voltage; connect a 0.1 µF or greater ceramic capacitor from IN to GND as close to the IC as possible.
$\overline{\text{FAULT}}$	4	4	O	Active-low open-drain output, asserted during overcurrent, overtemperature, or reverse-voltage conditions.
OUT	6	6	O	Power-switch output
ILIM	5	5	O	External resistor used to set current-limit threshold; recommended 15 kΩ ≤ R_{ILIM} ≤ 232 kΩ.
PowerPAD ™	–	–		Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND pin externally.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
	Voltage range on IN, OUT, EN , ILIM, $\overline{\text{FAULT}}$	–0.3	7	V
	Voltage range from IN to OUT	–7	7	V
I_O	Continuous output current	Internally Limited		
	Continuous total power dissipation	See the *Thermal Information*		
	Continuous $\overline{\text{FAULT}}$ sink current	0	25	mA
	ILIM source current	0	1	mA
T_J	Maximum junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are referenced to GND unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	
		IEC 61000-4-2 contact discharge(3)	±8000	
		IEC 61000-4-2 air-gap discharge(3)	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Surges per EN61000-4-2. 1999 applied to output terminals of EVM. These are passing test levels, not failure threshold.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, IN		2.7		6.5	V
$V_{\overline{EN}}$	Enable voltage	TPS2552D	0		6.5	V
V_{EN}		TPS2553D	0		6.5	
V_{EN}	Enable voltage		0		6.5	V
V_{IH}	High-level input voltage on EN		1.1			V
V_{IL}	Low-level input voltage on EN				0.66	
I_{OUT}	Continuous output current, OUT	–40 °C ≤ T_J ≤ 125 °C	0		1.2	A
		–40 °C ≤ T_J ≤ 105 °C	0		1.5	
R_{ILIM}	Current-limit threshold resistor range (nominal 1%) from ILIM to GND		15		232	KΩ
I_O	Continuous $\overline{\text{FAULT}}$ sink current		0		10	mA
	Input de-coupling capacitance, IN to GND		0.1			µF
T_J	Operating virtual junction temperature(1)	I_{OUT} ≤ 1.2 A	–40		125	°C
		I_{OUT} ≤ 1.5 A	–40		105	

(1) See "Dissipation Rating Table" and "Power Dissipation and Junction Temperature" sections for details on how to calculate maximum junction temperature for specific applications and packages.

7.4 Thermal Information

THERMAL METRIC[1]		TPS2552D	TPS2553D	UNIT
		DBV	DBV	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	182.6	182.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	122.2	122.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.4	29.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.8	20.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.9	28.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating conditions, V_{EN} = V_{IN}, R_{FAULT} = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
POWER SWITCH								
$r_{DS(on)}$	Static drain-source on-state resistance	DBV package, T_J = 25°C				85	95	mΩ
		DBV package, –40°C ≤T_J ≤125°C					135	
		DRV package, T_J = 25°C				100	115	
		DRV package, –40°C ≤T_J ≤105°C					140	
		DRV package, –40°C ≤T_J ≤125°C					150	
t_r	Rise time, output	V_{IN} = 6.5 V	C_L = 1 µF, R_L = 100 Ω, (see Figure 20)			1.1	1.5	ms
		V_{IN} = 2.5 V				0.7	1	
t_f	Fall time, output	V_{IN} = 6.5 V			0.2		0.5	
		V_{IN} = 2.5 V			0.2		0.5	
ENABLE INPUT EN OR $\overline{EN}$								
	Enable pin turn on/off threshold				0.66		1.1	V
I_{EN}	Input current	V_{EN} = 0 V or 6.5 V, $V_{\overline{EN}}$ = 0 V or 6.5 V			–0.5		0.5	µA
t_{on}	Turnon time	C_L = 1 µF, R_L = 100 Ω, (see Figure 20)					3	ms
t_{off}	Turnoff time						3	ms
CURRENT LIMIT								
I_{OS}	Current-limit threshold (Maximum DC output current I_{OUT} delivered to load) and Short-circuit current, OUT connected to GND		R_{ILIM} = 15 kΩ	–40°C ≤T_J ≤105°C	1610	1700	1800	mA
			R_{ILIM} = 20 kΩ	T_J = 25°C	1215	1295	1375	
				–40°C ≤T_J ≤125°C	1200	1295	1375	
			R_{ILIM} = 49.9 kΩ	T_J = 25°C	490	520	550	
				–40°C ≤T_J ≤125°C	475	520	565	
			R_{ILIM} = 210 kΩ		110	130	150	
			ILIM shorted to IN		50	75	100	
t_{IOS}	Response time to short circuit	V_{IN} = 5 V (see Figure 21)				2		µs
REVERSE-VOLTAGE PROTECTION								
	Reverse-voltage comparator trip point (V_{OUT} – V_{IN})				95	135	190	mV
	Time from reverse-voltage condition to MOSFET turn off	V_{IN} = 5 V			3	5	7	ms
SUPPLY CURRENT								
I_{IN_off}	Supply current, low-level output	V_{IN} = 6.5 V, No load on OUT, V_{EN} = 0 V				0.1	1	µA
I_{IN_on}	Supply current, high-level output	V_{IN} = 6.5 V, No load on OUT	R_{ILIM} = 20 kΩ			120	150	µA
			R_{ILIM} = 210 kΩ			100	130	µA
I_{REV}	Reverse leakage current	V_{OUT} = 6.5 V, V_{IN} = 0 V	T_J = 25 °C			0.01	1	µA
UNDERVOLTAGE LOCKOUT								
UVLO	Low-level input voltage, IN	V_{IN} rising				2.35	2.45	V
	Hysteresis, IN	T_J = 25 °C				25		mV
$\overline{FAULT}$ FLAG								
V_{OL}	Output low voltage, $\overline{FAULT}$	$I_{/FAULT}$ = 1 mA					180	mV
	Off-state leakage	$V_{/FAULT}$ = 6.5 V					1	µA
	$\overline{FAULT}$ deglitch	$\overline{FAULT}$ assertion or de-assertion due to overcurrent condition			5	7.5	10	ms
		$\overline{FAULT}$ assertion or de-assertion due to reverse-voltage condition			2	4	6	ms
THERMAL SHUTDOWN								
	Thermal shutdown threshold				155			°C
	Thermal shutdown threshold in current-limit				135			°C
	Hysteresis					10		°C

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

7.6 Typical Characteristics

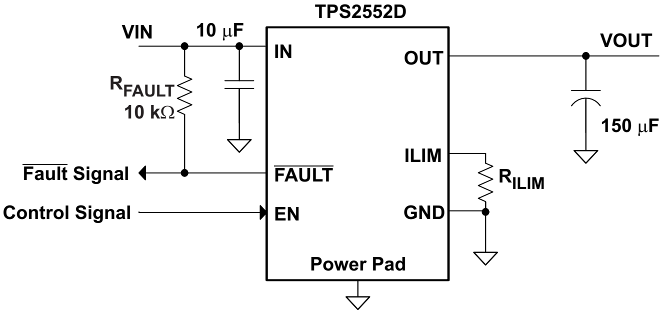


Figure 1. Typical Characteristics Reference Schematic

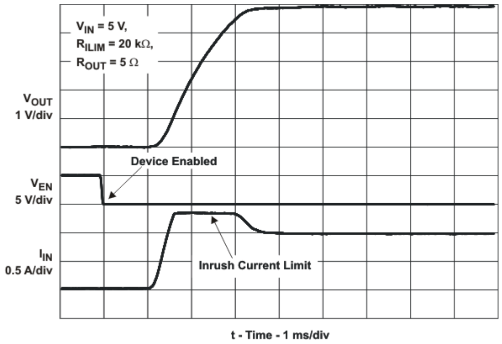


Figure 2. Turnon Delay and Rise Time

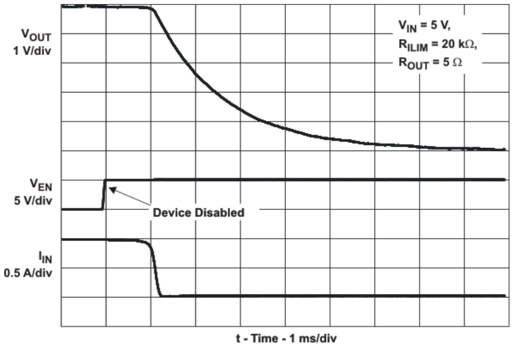


Figure 3. Turnoff Delay and Fall Time

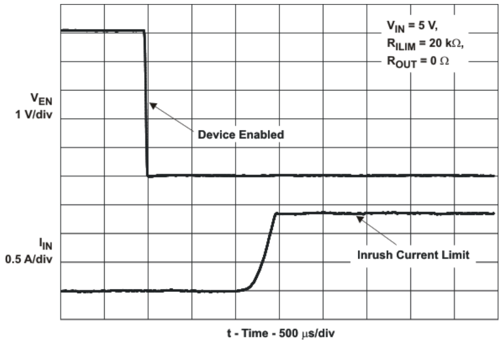


Figure 4. Device Enabled into Short-Circuit

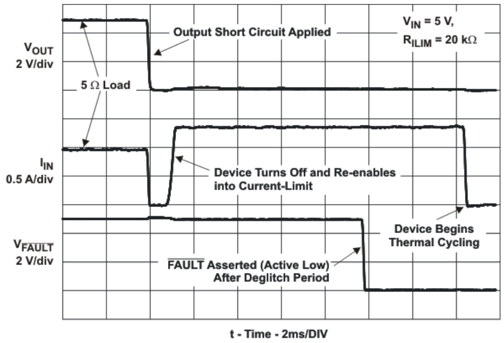


Figure 5. Full-Load to Short-Circuit Transient Response

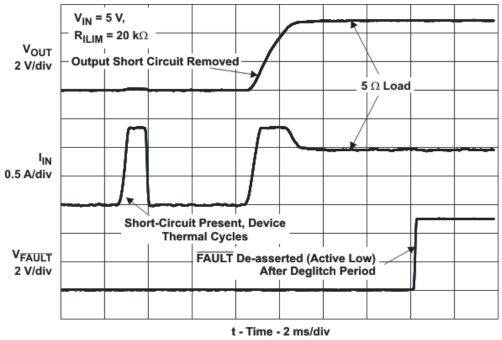


Figure 6. Short-Circuit to Full-Load Recovery Response

Typical Characteristics (continued)

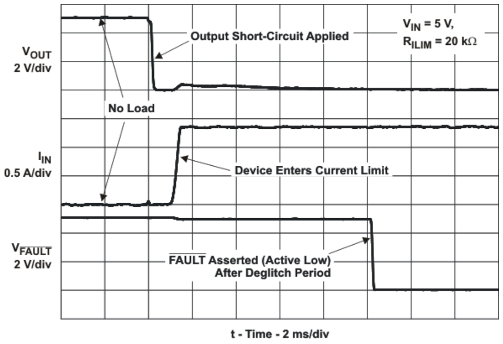


Figure 7. No-Load to Short-Circuit Transient Response

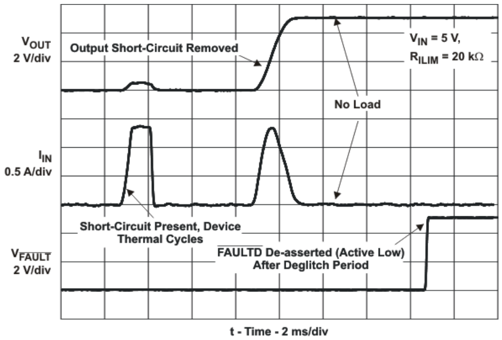


Figure 8. Short-Circuit to No-Load Recovery Response

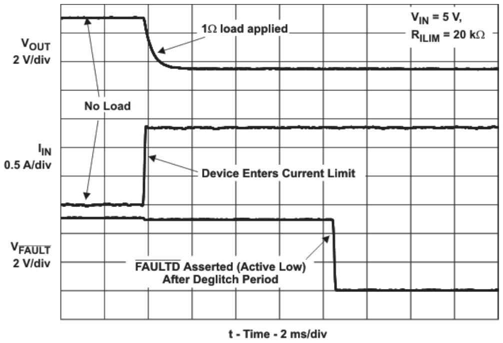


Figure 9. No Load to 1-Ω Transient Response

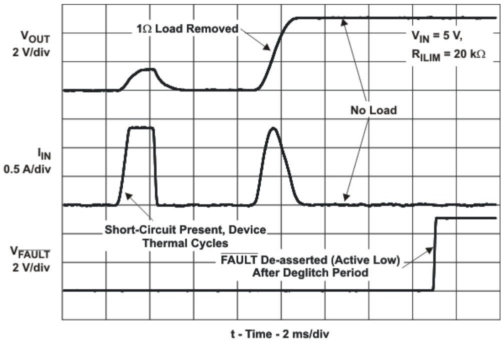


Figure 10. 1-Ω to No Load Transient Response

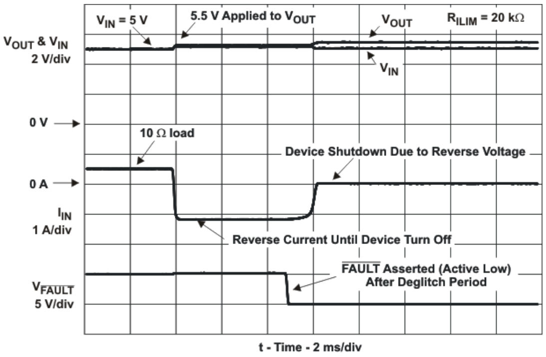


Figure 11. Reverse-Voltage Protection Response

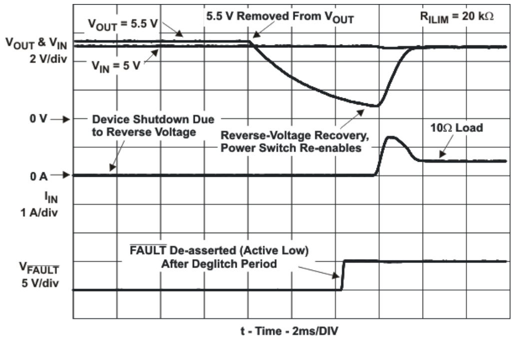


Figure 12. Reverse-Voltage Protection Recovery

Typical Characteristics (continued)

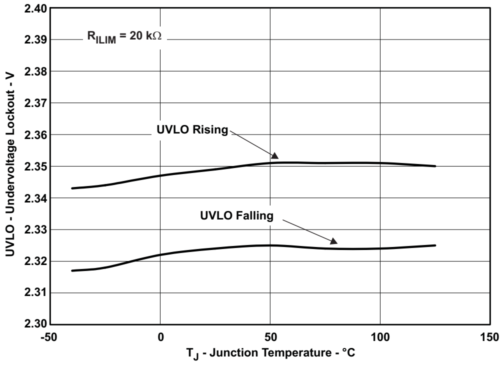


Figure 13. UVLO – Undervoltage Lockout – V

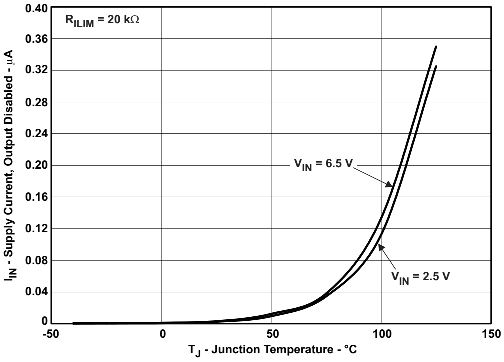


Figure 14. I_{IN} – Supply Current, Output Disabled – µA

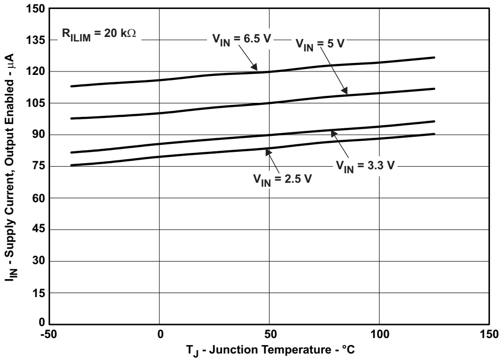


Figure 15. I_{IN} – Supply Current, Output Enabled – µA

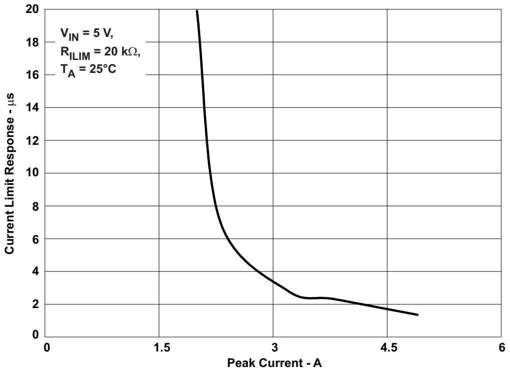


Figure 16. Current Limit Response – µs

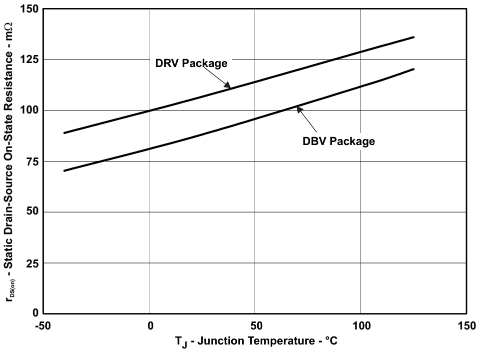


Figure 17. MOSFET $r_{DS(on)}$ Vs. Junction Temperature

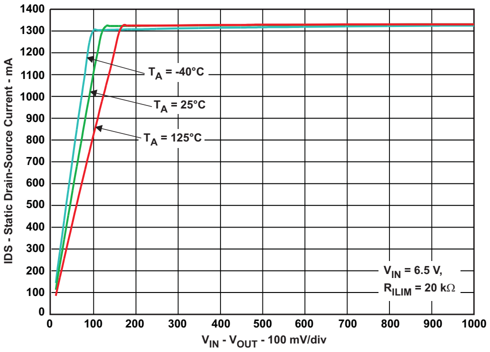


Figure 18. Switch Current Vs. Drain-Source Voltage Across Switch

Typical Characteristics (continued)

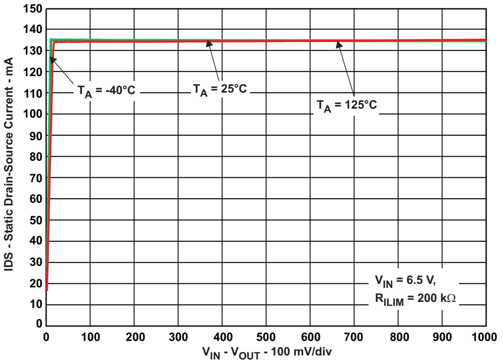


Figure 19. Switch Current Vs. Drain-Source Voltage Across Switch

8 Parameter Measurement Information

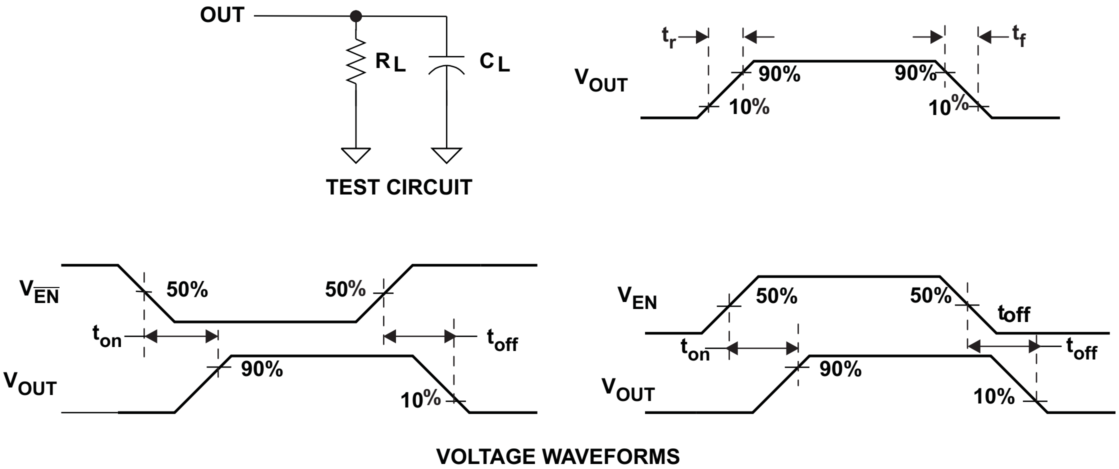


Figure 20. Test Circuit and Voltage Waveforms

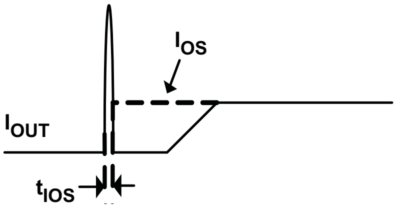


Figure 21. Response Time to Short Circuit Waveform

Parameter Measurement Information (continued)

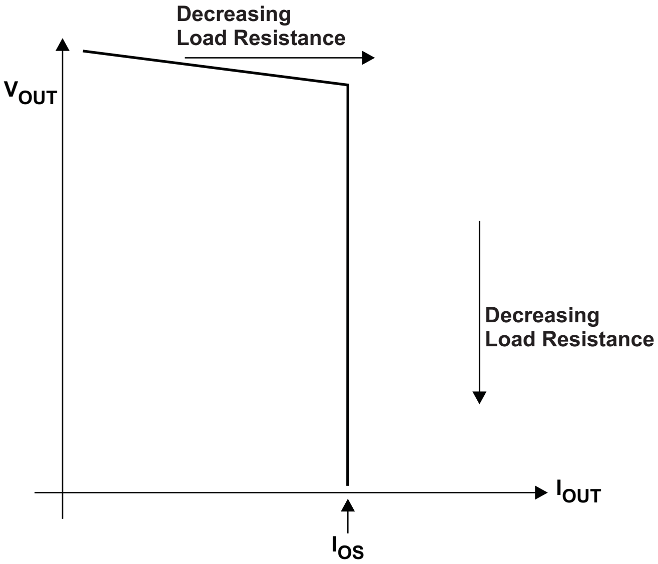


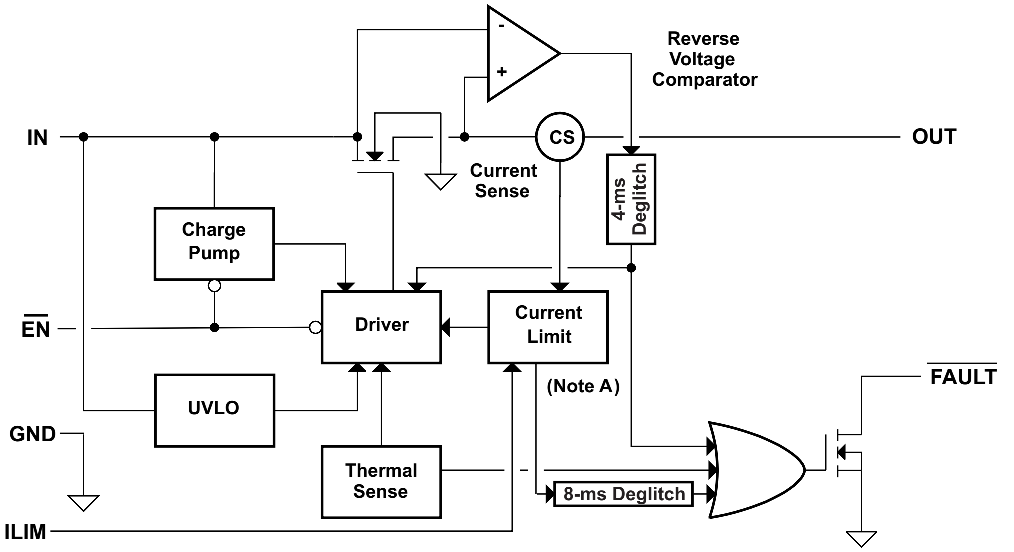
Figure 22. Output Voltage Vs. Current-Limit Threshold

9 Detailed Description

9.1 Overview

The TPS2552D and TPS2553D are current-limited, power-distribution switches using N-channel MOSFETs for applications where short circuits or heavy capacitive loads will be encountered and provide up to 1.5 A of continuous load current. These devices allow the user to program the current-limit threshold between 75 mA and 1.7 A (typ) via an external resistor. Additional device shutdown features include overtemperature protection and reverse-voltage protection. The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. There are two device families that handle overcurrent situations differently. The TPS255xD family enters constant-current mode when the load exceeds the current-limit threshold.

9.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

A. TPS255x parts enter constant current mode during current limit condition

9.3 Feature Description

9.3.1 Overcurrent Conditions

The TPS2552D and TPS2553D respiond to overcurrent conditions by limiting their output current to the I_{OS} levels shown in Figure 23. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS2552D and TPS2553D ramps the output current to I_{OS}. The TPS2552D and TPS2553D devices limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time t_{IOS} (see Figure 21). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and limits the output current to I_{OS}. Similar to the previous case, the TPS2552D and TPS2553D devices limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

Feature Description (continued)

The TPS2552D/53D thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (typ) while in current limit. The device remains off until the junction temperature cools 10°C (typ) and then restarts. The TPS2552D/53D cycle on/off until the overload is removed (see Figure 6 and Figure 8) .

9.3.2 Reverse-Voltage Protection

The reverse-voltage protection feature turns off the N-channel MOSFET whenever the output voltage exceeds the input voltage by 135 mV (typ) for 4-ms (typ).A reverse current of $(V_{OUT} – V_{IN})/r_{DS(on)})$ are present when this occurs. This prevents damage to devices on the input side of the TPS2552D/53D by preventing significant current from sinking into the input capacitance. The TPS2552D/53D devices allow the N-channel MOSFET to turn on once the output voltage goes below the input voltage for the same 4-ms deglitch time. The reverse-voltage comparator also asserts the $\overline{\text{FAULT}}$ output (active-low) after 4-ms.

9.3.3 $\overline{\text{FAULT}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an overcurrent, overtemperature or reverse-voltage condition. The TPS2552D/53D asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the device resumes normal operation. The TPS2552D/53D are designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal delay "deglitch" circuit for overcurrent (7.5-ms typ) and reverse-voltage (4-ms typ) conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving fault conditions. Overtemperature conditions are not deglitched and assert the $\overline{\text{FAULT}}$ signal immediately.

9.3.4 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges.

9.3.5 ENABLE

The logic enable controls the power switch, bias for the charge pump, driver, and other circuits to reduce the supply current. The supply current is reduced to less than 1-µA when a logic high is present on $\overline{\text{EN}}$ or when a logic low is present on EN. A logic low input on $\overline{\text{EN}}$ or a logic high input on EN enables the driver,A logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

9.3.6 Thermal Sense

The TPS2552D/53D self-protection features use two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. The TPS2552D/53D devices operate in constant-current mode during an overcurrent conditions, which increases the voltage drop across power-switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135°C (min) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 10°C.

The TPS2552D/3D also have a second ambient thermal sensor. The ambient thermal sensor turns off the power-switch when the die temperature exceeds 155°C (min) regardless of whether the power switch is in current limit and will turn on the power switch after the device has cooled approximately 10°C. The TPS2552D/53D families continue to cycle off and on until the fault is removed.

The open-drain fault reporting output $\overline{\text{FAULT}}$ is asserted (active low) immediately during an overtemperature shutdown condition.

9.4 Device Functional Modes

There are no other functional modes.

9.5 Programming

9.5.1 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable via an external resistor. The TPS2552D/53D use an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is 15 kΩ ≤ R_{ILIM} ≤ 232 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM}. The following equations and Figure 23 can be used to calculate the resulting overcurrent threshold for a given external resistor value (R_{ILIM}). Figure 23 includes current-limit tolerance due to variations caused by temperature and process. However, the equations do not account for tolerance due to external resistor variation, so it is important to account for this tolerance when selecting R_{ILIM}. The traces routing the R_{ILIM} resistor to the TPS2552D/53D should be as short as possible to reduce parasitic effects on the current-limit accuracy.

R_{ILIM} can be selected to provide a current-limit threshold that occurs 1) above a minimum load current or 2) below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(min)}$ curve and choose a value of R_{ILIM} below this value. Programming the current limit above a minimum threshold is important to ensure start up into full load or heavy capacitive loads. The resulting maximum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(max)}$ curve.

To design below a maximum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(max)}$ curve and choose a value of R_{ILIM} above this value. Programming the current limit below a maximum threshold is important to avoid current limiting upstream power supplies causing the input voltage bus to droop. The resulting minimum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(min)}$ curve.

Current-Limit Threshold Equations (I_{OS}):

$$I_{OSmax}(mA) = \frac{22980V}{R_{ILIM}{}^{0.94} k\Omega}$$

$$I_{OSnom}(mA) = \frac{23950V}{R_{ILIM}{}^{0.977} k\Omega}$$

$$I_{OSmin}(mA) = \frac{25230V}{R_{ILIM}{}^{1.016} k\Omega} \quad (1)$$

where 15 kΩ ≤ R_{ILIM} ≤ 232 kΩ.

While the maximum recommended value of RILIM is 232 kΩ, there is one additional configuration that allows for a lower current-limit threshold. The ILIM pin may be connected directly to IN to provide a 75 mA (typ) current-limit threshold. Additional low-ESR ceramic capacitance may be necessary from IN to GND in this configuration to prevent unwanted noise from coupling into the sensitive ILIM circuitry.

Programming (continued)

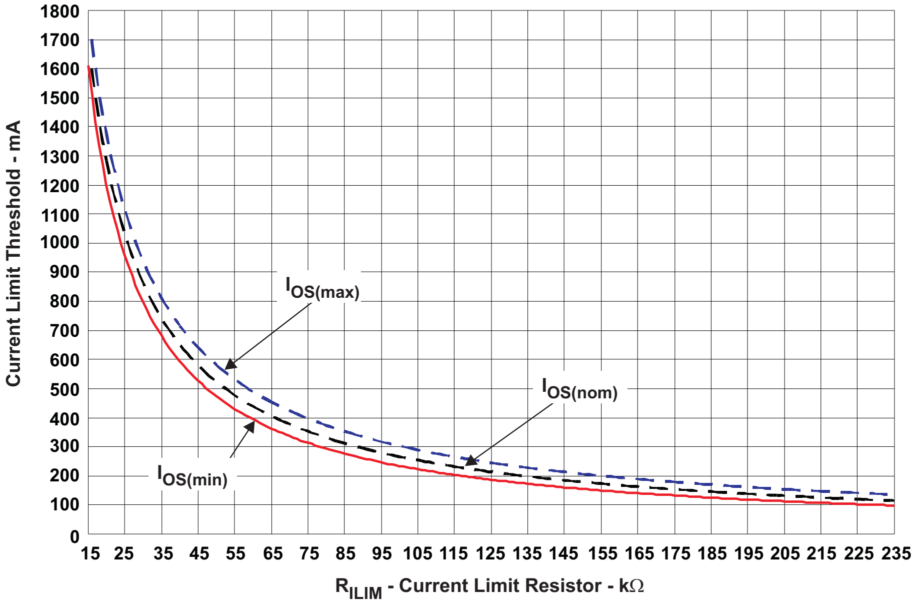


Figure 23. Current-Limit Threshold vs R_{ILIM}

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Constant-Current and Impact on Output Voltage

During normal operation the N-channel MOSFET is fully enhanced, and $V_{OUT} = V_{IN} - (I_{OUT} \times r_{DS(on)})$. The voltage drop across the MOSFET is relatively small compared to V_{IN}, and $V_{OUT} \not\approx V_{IN}$.

The TPS2552D/53D devices limit current to the programmed current-limit threshold set to R_{ILIM} by operating the N-channel MOSFET in the linear mode. During current-limit operation, the N-channel MOSFET is no longer fully-enhanced and the resistance of the device increases. This allows the device to effectively regulate the current to the current-limit threshold. The effect of increasing the resistance of the MOSFET is that the voltage drop across the device is no longer negligible ($V_{IN} \neq V_{OUT}$), and V_{OUT} decreases. The amount that V_{OUT} decreases is proportional to the magnitude of the overload condition. The expected V_{OUT} can be calculated by $I_{OS} \times R_{LOAD}$, where I_{OS} is the current-limit threshold and R_{LOAD} is the magnitude of the overload condition. For example, if I_{OS} is programmed to 1 A and a 1 Ω overload condition is applied, the resulting V_{OUT} is 1 V.

The TPS2552D/53D devices assert the $\overline{\text{FAULT}}$ flag after the deglitch period and continue to regulate the current to the current-limit threshold indefinitely. In practical circuits, the power dissipation in the package will increase the die temperature above the overtemperature shutdown threshold (135°C min), and the device will turn off until the die temperature decreases by the hysteresis of the thermal shutdown circuit (10°C typ). The device will turn on and continue to thermal cycle until the overload condition is removed. The TPS2552D/53D devices resume normal operation once the overload condition is removed.

10.2 Typical Applications

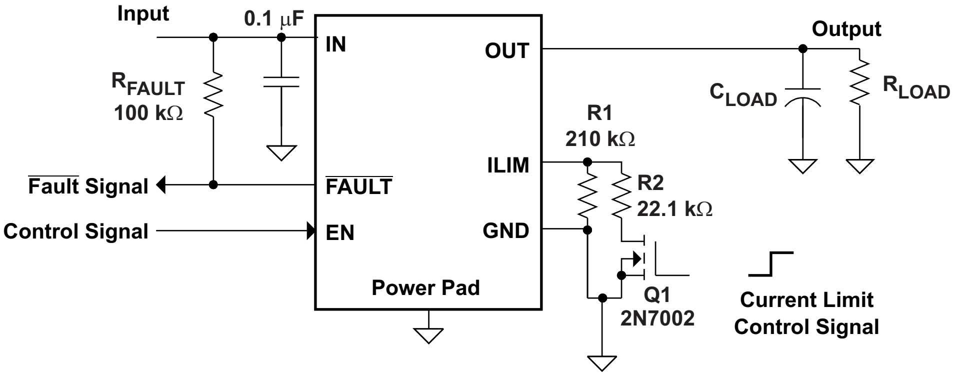
10.2.1 Two-Level Current-Limit Circuit

Some applications require different current-limit thresholds depending on external system conditions. Figure 24 shows an implementation for an externally controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see the *Programming the Current-Limit Threshold* section). A logic-level input enables/disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND. Additional MOSFET/resistor combinations can be used in parallel to Q1/R2 to increase the number of additional current-limit levels.

NOTE

ILIM should never be driven directly with an external signal.

Typical Applications (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 24. Two-Level Current-Limit Circuit

10.2.1.1 Design Requirements

For this example, use the parameters shown in Table 1.

Table 1. Design Requirements

PARAMETER	VALUE
Input voltage	5 V
Output voltage	5 V
Above a minimum current limit	1000 mA
Below a maximum current limit	500 mA

10.2.1.2 Detailed Design Procedures

10.2.1.2.1 Designing Above a Minimum Current Limit

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 1 A must be delivered to the load so that the minimum desired current-limit threshold is 1000 mA. Use the I_{OS} equations and Figure 23 to select R_{ILIM}.

$$I_{OSmin}(mA) = 1000mA$$
$$I_{OSmin}(mA) = \frac{25230V}{R_{ILIM}{}^{1.016}k\Omega}$$
$$R_{ILIM}(k\Omega) = \left(\frac{25230V}{I_{OSmin}mA}\right)^{\frac{1}{1.016}}$$
$$R_{ILIM}(k\Omega) = 24k\Omega \tag{2}$$

Select the closest 1% resistor less than the calculated value: R_{ILIM} = 23.7 kΩ. This sets the minimum current-limit threshold at 1 A . Use the I_{OS} equations, Figure 23, and the previously calculated value for R_{ILIM} to calculate the maximum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 23.7k\Omega$$
$$I_{OSmax}(mA) = \frac{22980V}{R_{ILIM}{}^{0.94}k\Omega}$$
$$I_{OSmax}(mA) = \frac{22980V}{23.7^{0.94}k\Omega}$$
$$I_{OSmax}(mA) = 1172.4mA \tag{3}$$

The resulting maximum current-limit threshold is 1172.4 mA with a 23.7 kΩ resistor.

10.2.1.2.2 Designing Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that the desired upper current-limit threshold must be below 500 mA to protect an up-stream power supply. Use the I_{OS} equations and Figure 23 to select R_{ILIM}.

$$I_{OSmax}(mA) = 500mA$$
$$I_{OSmax}(mA) = \frac{22980V}{R_{ILIM}{}^{0.94}k\Omega}$$
$$R_{ILIM}(k\Omega) = \left(\frac{22980V}{I_{OSmax}mA}\right)^{\frac{1}{0.94}}$$
$$R_{ILIM}(k\Omega) = 58.7k\Omega \tag{4}$$

Select the closest 1% resistor greater than the calculated value: R_{ILIM} = 59 kΩ. This sets the maximum current-limit threshold at 500 mA . Use the I_{OS} equations, Figure 23, and the previously calculated value for R_{ILIM} to calculate the minimum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 59k\Omega$$
$$I_{OSmin}(mA) = \frac{25230V}{R_{ILIM}{}^{1.016}k\Omega}$$
$$I_{OSmin}(mA) = \frac{25230V}{59^{1.016}k\Omega}$$
$$I_{OSmin}(mA) = 400.6mA \tag{5}$$

The resulting minimum current-limit threshold is 400.6 mA with a 59 kΩ resistor.

10.2.1.2.3 Accounting for Resistor Tolerance

The previous sections described the selection of R_{ILIM} given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focused only on the TPS2552D/53D performance and assumed an exact resistor value. However, resistors sold in quantity are not exact and are bounded by an upper and lower tolerance centered around a nominal resistance. The additional R_{ILIM} resistance tolerance directly affects the current-limit threshold accuracy at a system level. The following table shows a process that accounts for worst-case resistor tolerance assuming 1% resistor values. Step one follows the selection process outlined in the application examples above. Step two determines the upper and lower resistance bounds of the selected resistor. Step three uses the upper and lower resistor bounds in the I_{OS} equations to calculate the threshold limits. It is important to use tighter tolerance resistors, e.g. 0.5% or 0.1%, when precision current limiting is desired.

Table 2. Common R_{ILIM} Resistor Selections

DESIRED NOMINAL CURRENT LIMIT (mA)	IDEAL RESISTOR (kΩ)	CLOSEST 1% RESISTOR (kΩ)	RESISTOR TOLERANCE		ACTUAL LIMITS		
			1% LOW (kΩ)	1% HIGHT (kΩ)	IOS MIN (mA)	IOS NOM (mA)	IOS MAX (mA)
75	SHORT ILIM to IN				50.0	75.0	100.0
120	226.1	226	223.7	228.3	101.3	120.0	142.1
200	134.0	133	131.7	134.3	173.7	201.5	233.9
300	88.5	88.7	87.8	89.6	262.1	299.4	342.3
400	65.9	66.5	65.8	67.2	351.2	396.7	448.7
500	52.5	52.3	51.8	52.8	448.3	501.6	562.4
600	43.5	43.2	42.8	43.6	544.3	604.6	673.1
700	37.2	37.4	37.0	37.8	630.2	696.0	770.8
800	32.4	32.4	32.1	32.7	729.1	800.8	882.1
900	28.7	28.7	28.4	29.0	824.7	901.5	988.7
1000	25.8	26.1	25.8	26.4	908.3	989.1	1081.0
1100	23.4	23.2	23.0	23.4	1023.7	1109.7	1207.5
1200	21.4	21.5	21.3	21.7	1106.0	1195.4	1297.1
1300	19.7	19.6	19.4	19.8	1215.1	1308.5	1414.9
1400	18.3	18.2	18.0	18.4	1310.1	1406.7	1517.0
1500	17.0	16.9	16.7	17.1	1412.5	1512.4	1626.4
1600	16.0	15.8	15.6	16.0	1512.5	1615.2	1732.7
1700	15.0	15.0	14.9	15.2	1594.5	1699.3	1819.4

10.2.1.2.4 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1μF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise de-coupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power-supply.

Placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

10.2.1.3 Application Curves

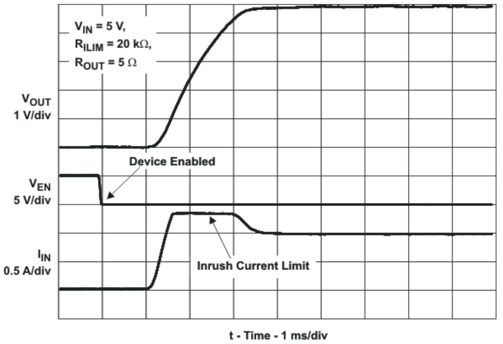


Figure 25. Turn on Delay and Rise Time

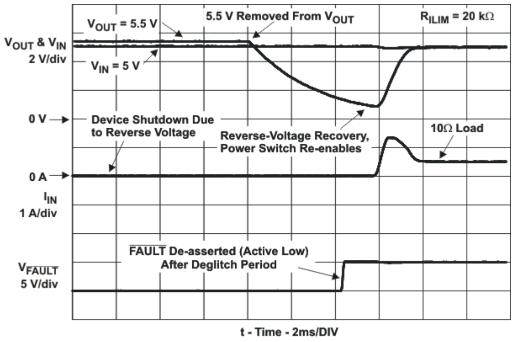


Figure 26. Reverse-Voltage Protection Recovery

10.2.2 Auto-Retry Functionality

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This *auto-retry* functionality can be implemented with an external resistor and capacitor. During a fault condition, $\overline{\text{FAULT}}$ pulls low disabling the part. The part is disabled when EN is pulled low, and $\overline{\text{FAULT}}$ goes high impedance allowing C_{RETRY} to begin charging. The part re-enables when the voltage on EN reaches the turnon threshold, and the auto-retry time is determined by the resistor/capacitor time constant. The device continues to cycle in this manner until the fault condition is removed.

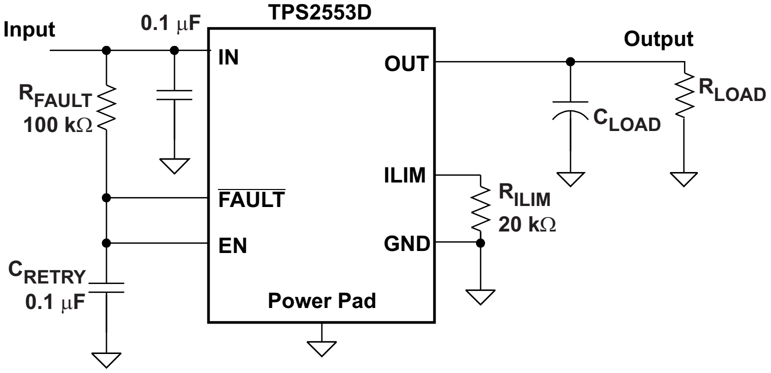


Figure 27. Auto-Retry Functionality

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. Figure 28 shows how an external logic signal can drive EN through R_{FAULT} and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

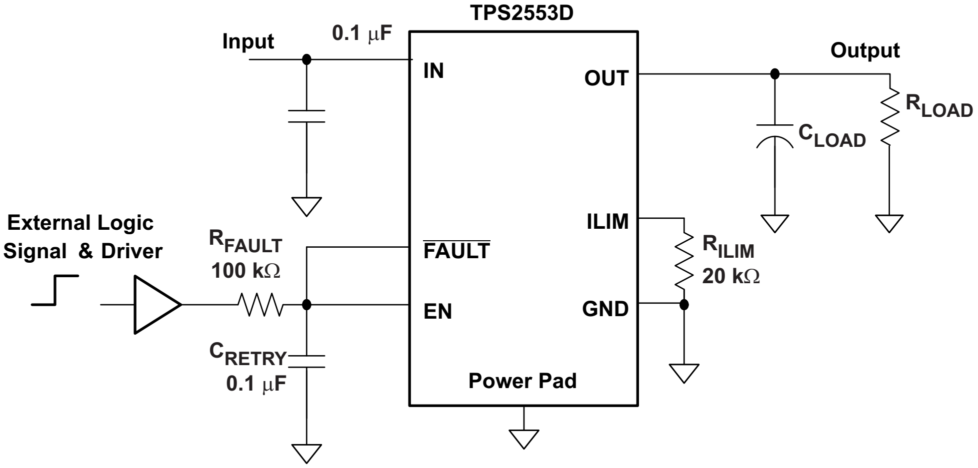


Figure 28. Auto-Retry Functionality With External EN Signal

10.2.2.1 Design Requirements

For this example, use the parameters shown in Table 3.

Table 3. Design Requirements

PARAMETER	VALUE
Input voltage	5 V
Output voltage	5 V
Current	1200 mA

10.2.2.2 Detailed Design Procedure

Refer to *Programming the Current-Limit Threshold* section for the current limit setting. For auto-retry functionality, once $\overline{\text{FAULT}}$ asserted, EN pull low, TPS2553D is disabled, $\overline{\text{FAULT}}$ des-asserted, C_{RETRY} is slowly charged to EN logic high via R_{FAULT}, then enable, after deglitch time, $\overline{\text{FAULT}}$ asserted again. In the event of an over-load, TPS2553D cycles and has output average current. ON-time with output current is decided by $\overline{\text{FAULT}}$ deglitch time. OFF-time without output current is decided by R_{FAULT} x C_{RETRY} constant time to EN logic high and t_{on} time. Therefore, set the $R_{FAULT} \times C_{RETRY}$ to get the desired output average current during overload.

10.2.3 Typical Application as USB Power Switch

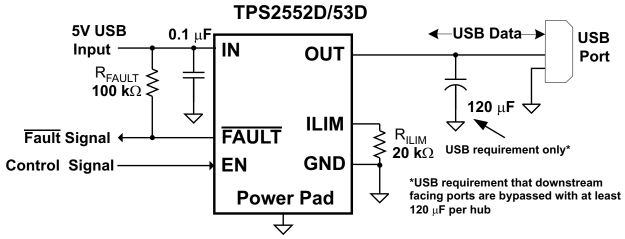


Figure 29. Typical Application as USB Power Switch

10.2.3.1 Design Requirements

For this example, use the parameters shown in Table 4.

Table 4. Design Requirements

PARAMETER	VALUE
Input voltage	5 V
Output voltage	5 V
Current	1200 mA

10.2.3.1.1 USB Power-Distribution Requirements

USB can be implemented in several ways regardless of the type of USB device being developed. Several power-distribution features must be implemented.

- SPHs must:
  - Current limit downstream ports
  - Report overcurrent conditions
- BPHs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2552D/53D meets each of these requirements. The integrated current limiting and overcurrent reporting is required by self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs and the input ports for bus-powered functions.

10.2.3.2 Detailed Design Procedure

10.2.3.2.1 Universal Serial Bus (USB) Power-Distribution Requirements

One application for this device is for current limiting in universal serial bus (USB) applications. The original USB interface was a 12-Mb/s or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). As the demand for more bandwidth increased, the USB 2.0 standard was introduced increasing the maximum data rate to 480-Mb/s. The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply. The USB specification classifies two different classes of devices depending on its maximum current draw. A device classified as low-power can draw up to 100 mA as defined by the standard. A device classified as high-power can draw up to 500 mA. It is important that the minimum current-limit threshold of the current-limiting power-switch exceed the maximum current-limit draw of the intended application. The latest USB standard should always be referenced when considering the current-limit threshold

The USB specification defines two types of devices as hubs and functions. A USB hub is a device that contains multiple ports for different USB devices to connect and can be self-powered (SPH) or bus-powered (BPH). A function is a USB device that is able to transmit or receive data or control information over the bus. A USB function can be embedded in a USB hub. A USB function can be one of three types included in the list below.

- Low-power, bus-powered function
- High-power, bus-powered function
- Self-powered function

SPHs and BPHs distribute data and power to downstream functions. The TPS2552D/53D have higher current capabilities than required for a single USB port allowing it to power multiple downstream ports.

11 Power Supply Recommendations

11.1 Self-Powered and Bus-Powered Hubs

A SPH has a local power supply that powers embedded functions and downstream ports. This power supply must provide between 4.75 V to 5.25 V to downstream facing devices under full-load and no-load conditions. SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

A BPH obtains all power from an upstream port and often contains an embedded function. It must power up with less than 100 mA. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This is accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than 100 mA. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

11.2 Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports. Low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 μF at power up, the device must implement inrush current limiting.

11.3 Power Dissipation and Junction Temperature

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated using Equation 6.

$$P_D = r_{DS(on)} \times I_{OUT}{}^2$$

where

- P_D = Total power dissipation (W)
- $r_{DS(on)}$ = Power switch on-resistance (Ω)
- I_{OUT} = Maximum current-limit threshold (A)
- This step calculates the total power dissipation of the N-channel MOSFET. (6)

Finally, calculate the junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A$$

where

- T_A = Ambient temperature (°C)
- θ_{JA} = Thermal resistance (°C/W)
- P_D = Total power dissipation (W) (7)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance θ_{JA}, and thermal resistance is highly dependent on the individual package and board layout. The *Thermal Information Table* provides example thermal resistances for specific packages and board layouts.

12 Layout

12.1 Layout Guidelines

- TI recommends placing the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low-inductance trace.
- TI recommends placing a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin is recommended when large transient currents are expected on the output.
- The traces routing the RILIM resistor to the device should be as short as possible to reduce parasitic effects on the current limit accuracy.
- The PowerPAD should be directly connected to PCB ground plane using wide and short copper trace.

12.2 Layout Example

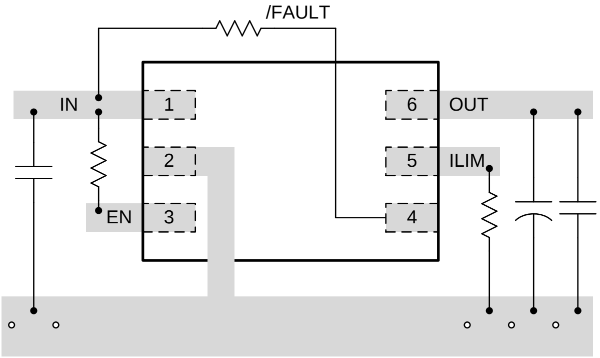


Figure 30. Layout Recommendation

13 Device and Documentation Support

13.1 Device Support

For the TI Switch Portfolio, go here.

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS2552D	Click here	Click here	Click here	Click here	Click here
TPS2553D	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2552DDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	15IL	Samples
TPS2552DDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	15IL	Samples
TPS2553DDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	15JL	Samples
TPS2553DDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	15JL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

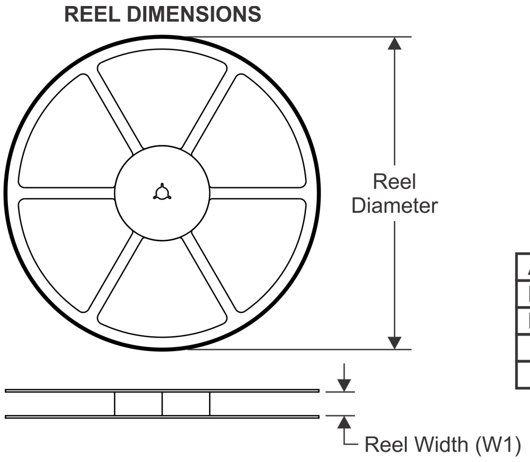
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

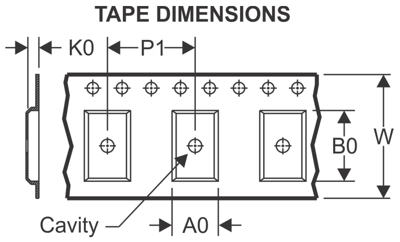
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

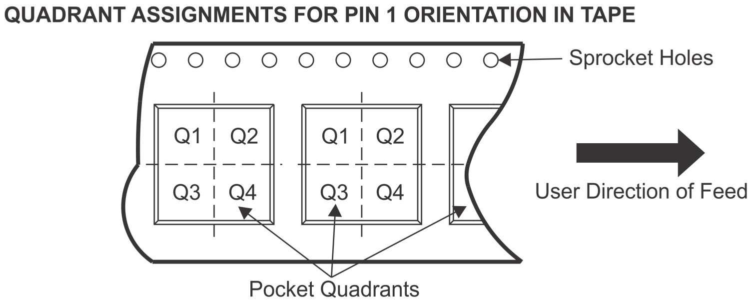
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





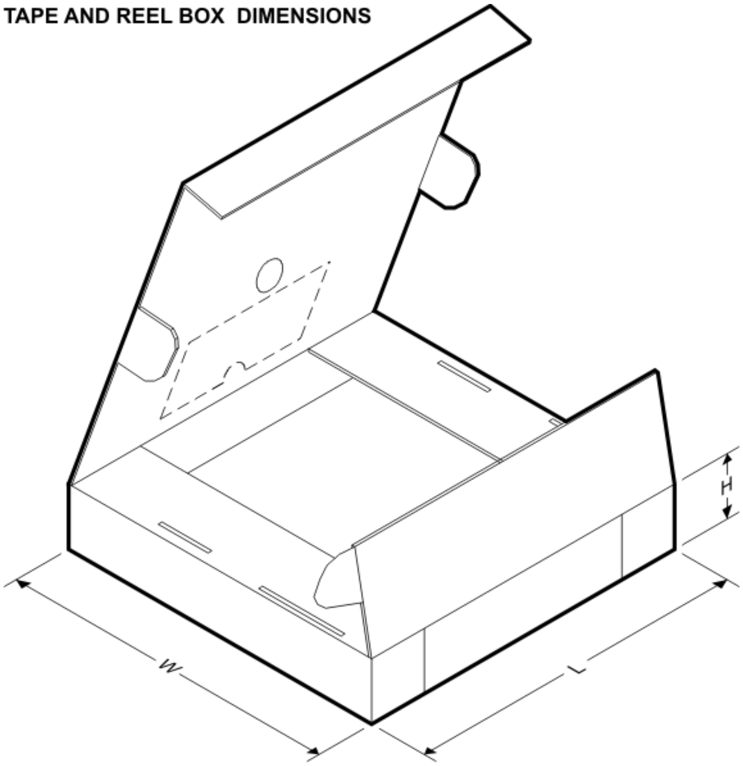
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

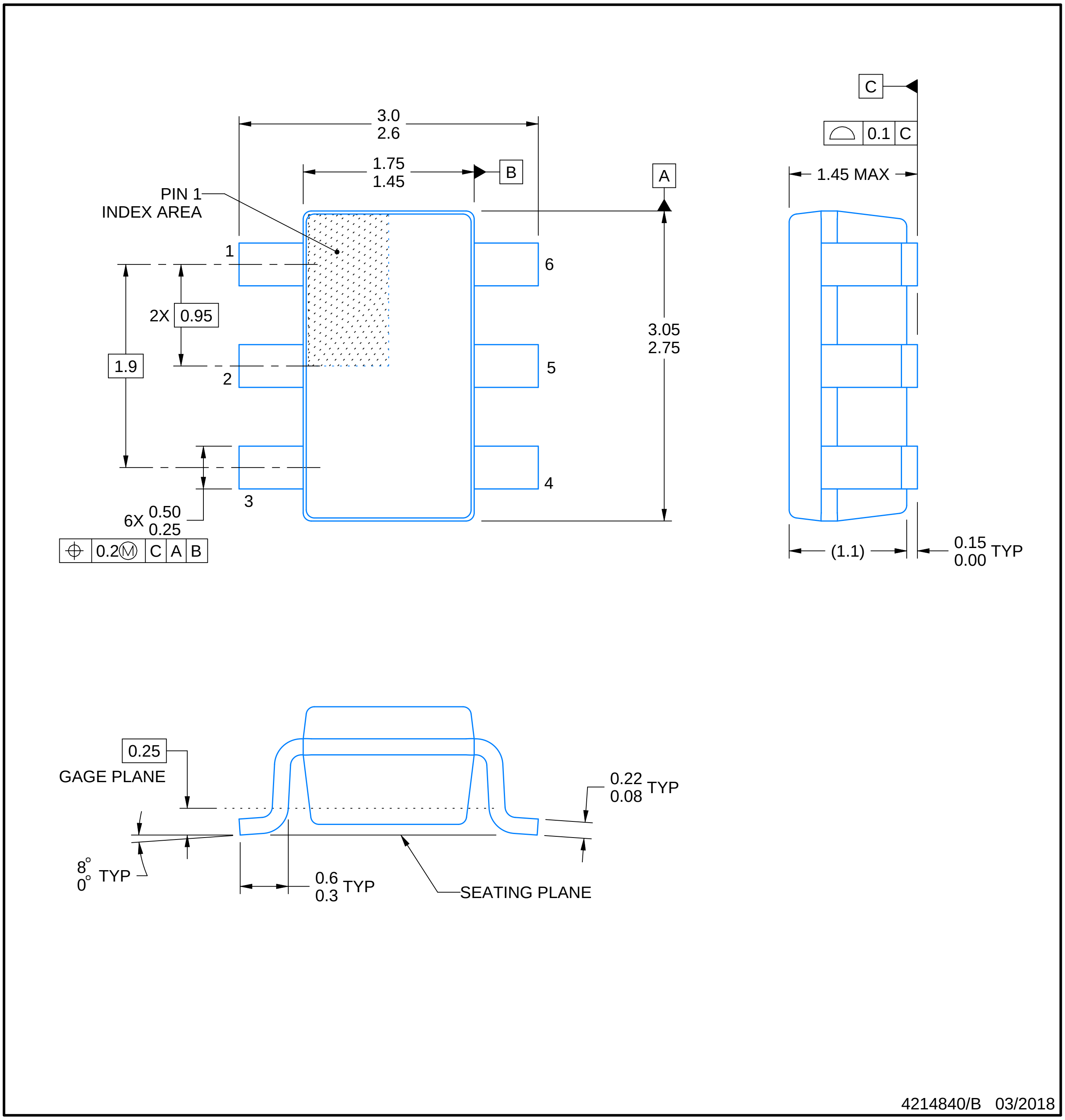
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2552DDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2552DDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2553DDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2553DDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



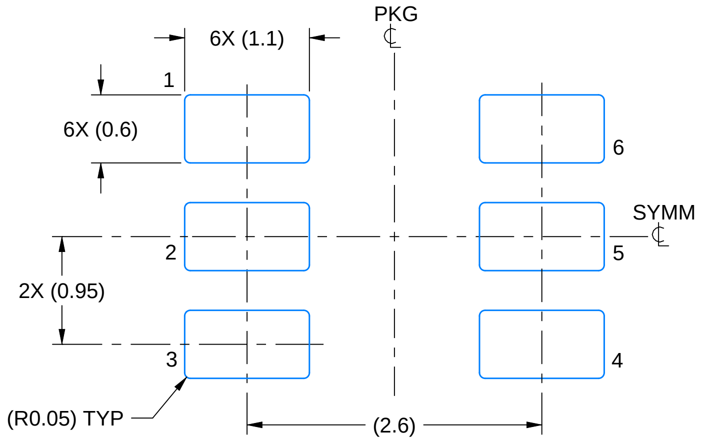
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2552DDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS2552DDBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
TPS2553DDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS2553DDBVT	SOT-23	DBV	6	250	210.0	185.0	35.0

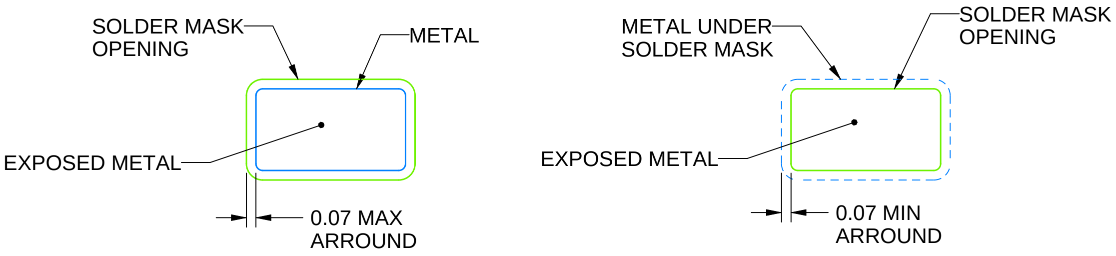


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



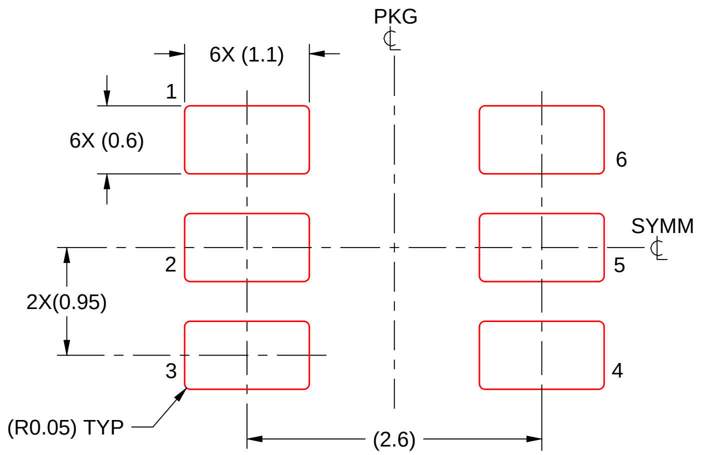
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated