THE DATASHEET OF

TLC5947RHBTG4

TLC5947 24-Channel, 12-Bit PWM LED Driver With Internal Oscillator

1 Features

- 24 Channels, Constant-Current Sink Output
- 30-mA Capability (Constant-Current Sink)
- 12-Bit (4096 Steps) PWM Grayscale Control
- LED Power-Supply Voltage Up to 30 V
- V_{CC} = 3.0 V to 5.5 V
- Constant-Current Accuracy:
  - Channel-to-Channel = ±2% (Typical)
  - Device-to-Device = ±2% (Typical)
- CMOS Logic Level I/O
- 30-MHz Data Transfer Rate (Standalone)
- 15-MHz Data Transfer Rate (Cascaded Devices, SCLK Duty = 50%)
- Shift Out Data Changes With Falling Edge to Avoid Data Shift Errors
- Auto Display Repeat
- 4-MHz Internal Oscillator
- Thermal Shutdown (TSD):
  - Automatic Shutdown at OverTemperature Conditions
  - Restart Under Normal Temperature
- Noise Reduction:
  - 4-Channel Grouped Delay to Prevent Inrush Current
- Operating Temperature: –40°C to 85°C

2 Applications

- Static LED Displays
- Message Boards
- Amusement Illumination
- TV Backlighting

3 Description

The TLC5947 is a 24-channel, constant-current sink LED driver. Each channel is individually adjustable with 4096 pulse-width modulated (PWM) steps. PWM control is repeated automatically with the programmed grayscale (GS) data. GS data are written via a serial interface port. The current value of all 24 channels is set by a single external resistor.

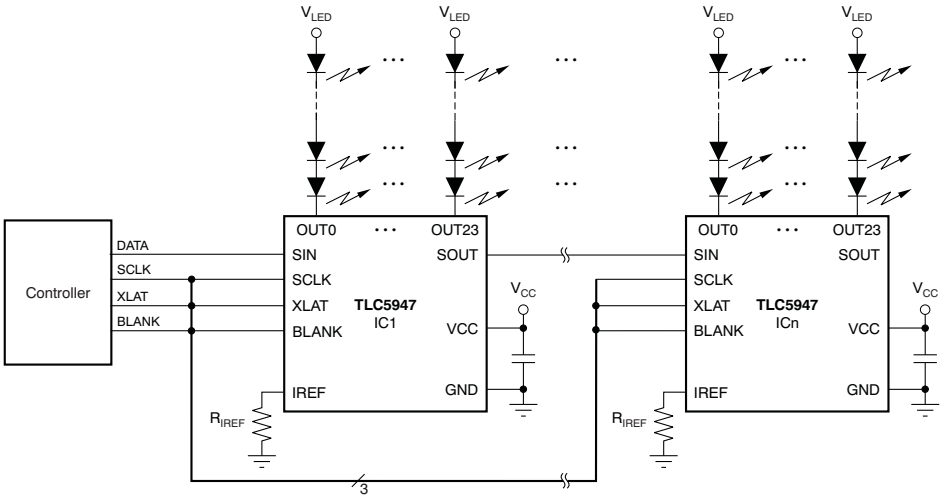
The TLC5947 has a thermal shutdown (TSD) function that turns off all output drivers during an over-temperature condition. All of the output drivers automatically restart when the temperature returns to normal conditions.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC5947	HTSSOP (32)	11.00 mm × 6.20 mm
	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Circuit



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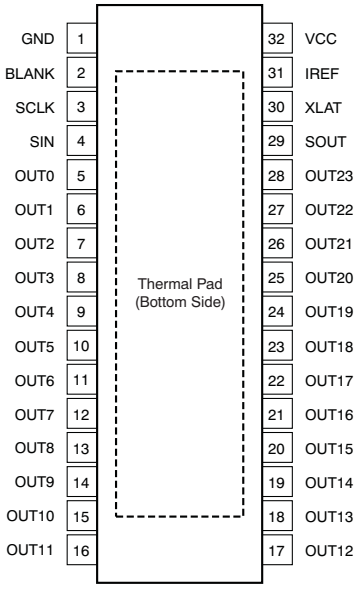
4 Revision History

Changes from Revision A (September 2008) to Revision B **Page**

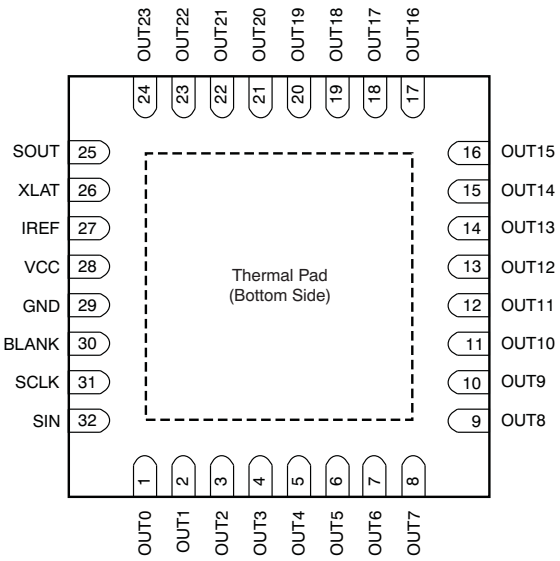
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

32-PINS DAP PACKAGE (TOP VIEW)



32-PINS RHB PACKAGE (TOP VIEW)



(1) This device is product preview.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	RHB NO.	DAP NO.		
BLANK	30	2	I	Blank (all constant-current outputs off). When BLANK is high, all constant-current outputs (OUT0 through OUT23) are forced off, the grayscale PWM timing controller initializes, and the grayscale counter resets to '0'. When BLANK is low, all constant-current outputs are controlled by the grayscale PWM timing controller.
GND	29	1	—	Power ground
IREF	27	31	I/O	This pin sets the constant-current value. OUT0 through OUT23 constant sink current is set to the desired value by connecting an external resistor between IREF and GND.
OUT0	1	5	O	Constant-current output. Multiple outputs can be tied together to increase the constant-current capability. Different voltages can be applied to each output.
OUT1	2	6	O	Constant-current output
OUT2	3	7	O	Constant-current output
OUT3	4	8	O	Constant-current output
OUT4	5	9	O	Constant-current output
OUT5	6	10	O	Constant-current output
OUT6	7	11	O	Constant-current output
OUT7	8	12	O	Constant-current output
OUT8	9	13	O	Constant-current output
OUT9	10	14	O	Constant-current output
OUT10	11	15	O	Constant-current output
OUT11	12	16	O	Constant-current output
OUT12	13	17	O	Constant-current output
OUT13	14	18	O	Constant-current output
OUT14	15	19	O	Constant-current output
OUT15	16	20	O	Constant-current output
OUT16	17	21	O	Constant-current output

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	RHB NO.	DAP NO.		
OUT17	18	22	O	Constant-current output
OUT18	19	23	O	Constant-current output
OUT19	20	24	O	Constant-current output
OUT20	21	25	O	Constant-current output
OUT21	22	26	O	Constant-current output
OUT22	23	27	O	Constant-current output
OUT23	24	28	O	Constant-current output
SCLK	31	3	I	Serial data shift clock. Schmitt buffer input. Data present on the SIN pin are shifted into the shift register with the rising edge of the SCLK pin. Data are shifted to the MSB side by 1-bit synchronizing of the rising edge of SCLK. The MSB data appears on SOUT at the falling edge of SCLK. A rising edge on the SCLK input is allowed 100 ns after an XLAT rising edge.
SIN	32	4	I	Serial input for grayscale data
SOUT	25	29	O	Serial data output. This output is connected to the shift register placed after the MSB of the grayscale shift register. Therefore, the MSB data of the grayscale shift register appears at the falling edge of SCLK. This function reduces the data shifting errors caused by small timing margins between SIN and SCLK.
VCC	28	32	—	Power-supply voltage
XLAT	26	30	I	The data in the grayscale shift register are moved to the grayscale data latch with a low-to-high transition on this pin. When the XLAT rising edge is input, all constant-current outputs are forced off until the next grayscale display period. The grayscale counter is not reset to zero with a rising edge of XLAT.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)(2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage: V_{CC}		–0.3	6.0	V
I_O	Output current (dc)	OUT0 to OUT23		38	mA
V_I	Input voltage	SIN, SCLK, XLAT, BLANK	–0.3	V_{CC} + 0.3	V
V_O	Output voltage	SOUT	–0.3	V_{CC} + 0.3	V
		OUT0 to OUT23	–0.3	33	V
$T_{J(MAX)}$	Operating junction temperature			150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

At T_A= –40°C to 85°C, unless otherwise noted.

			MIN	NOM	MAX	UNIT
DC CHARACTERISTICS: V_{CC} = 3 V to 5.5 V						
V_{CC}	Supply voltage		3.0		5.5	V
V_O	Voltage applied to output OUT0 to OUT23				30	V
V_{IH}	High-level input voltage		0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.3 × V_{CC}	V
I_{OH}	High-level output current SOUT				–3	mA
I_{OL}	Low-level output current SOUT				3	mA
I_{OLC}	Constant output sink current OUT0 to OUT23		2		30	mA
T_A	Operating free-air temperature range		–40		85	°C
T_J	Operating junction temperature		–40		125	°C
AC CHARACTERISTICS: V_{CC} = 3 V to 5.5 V						
f_{SCLK}	Data shift clock frequency	SCLK, Standalone operation			30	MHz
		SCLK, Duty 50%, cascade operation			15	MHz
T_{WH0}	Pulse duration	SCLK = High-level pulse width	12			ns
T_{WL0}		SCLK = Low-level pulse width	10			ns
T_{WH1}		XLAT, BLANK High-level pulse width	30			ns
T_{SU0}	Setup time	SIN–SCLK↑	5			ns
T_{SU1}		XLAT↑–SCLK↑	100			ns
T_{SU2}		XLAT↑–BLANK↓	30			ns
T_{H0}	Hold time	SIN–SCLK↑	3			ns
T_{H1}		XLAT↑–SCLK↑	10			ns

6.4 Thermal Information

THERMAL METRIC[1]		TLC5947 DAP 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	17.9	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	17.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Dissipation Ratings

PACKAGE	OPERATING FACTOR ABOVE T_A = 25°C	T_A < 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
HTSSOP-32 with PowerPAD™ soldered[1]	42.54 mW/°C	5318 mW	3403 mW	2765 mW
HTSSOP-32 with PowerPAD not soldered[2]	22.56 mW/°C	2820 mW	1805 mW	1466 mW
QFN-32[3]	27.86 mW/°C	3482 mW	2228 mW	1811 mW

(1) With PowerPAD soldered onto copper area on printed circuit board (PCB); 2 oz. copper. For more information, see SLMA002.
(2) With PowerPAD not soldered onto copper area on PCB.
(3) The package thermal impedance is calculated in accordance with JESD51-5.

6.6 Electrical Characteristics

At V_{CC} = 3.0 V to 5.5 V and T_A = –40°C to 85°C. Typical values at V_{CC} = 3.3 V and T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –3 mA at SOUT	V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 3 mA at SOUT			0.4	V
I_{IN}	Input current	V_{IN} = V_{CC} or GND at SIN, XLAT, and BLANK	–1		1	µA
I_{CC1}	Supply current (V_{CC})	SIN/SCLK/XLAT = low, BLANK = high, V_{OUTn} = 1 V, R_{IREF} = 24 kΩ		0.5	3	mA
I_{CC2}		SIN/SCLK/XLAT = low, BLANK = high, V_{OUTn} = 1 V, R_{IREF} = 3.3 kΩ		1	6	mA
I_{CC3}		SIN/SCLK/XLAT = low, BLANK = low, V_{OUTn} = 1 V, R_{IREF} = 3.3 kΩ, GSn = FFFh		15	45	mA
I_{CC4}		SIN/SCLK/XLAT = low, BLANK = low, V_{OUTn} = 1 V, R_{IREF} = 1.6 kΩ, GSn = FFFh		30	90	mA
I_{OLC}	Constant output current	All OUTn = ON, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.6 kΩ	27.7	30.75	33.8	mA
I_{OLK}	Output leakage current	BLANK = high, V_{OUTn} = 30 V, R_{IREF} = 1.6 kΩ, At OUT0 to OUT23			0.1	µA
ΔI_{OLC}	Constant-current error (channel-to-channel)(1)	All OUTn = ON, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.6 kΩ, At OUT0 to OUT23	–4%	±2%	4%	
ΔI_{OLC1}	Constant-current error (device-to-device)(2)	All OUTn = ON, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.6 kΩ	–7%	±2%	7%	
ΔI_{OLC2}	Line regulation(3)	All OUTn = ON, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.6 kΩ, At OUT0 to OUT23		±1	±3	%/V
ΔI_{OLC3}	Load regulation(4)	All OUTn = ON, V_{OUTn} = 1 V to 3 V, V_{OUTfix} = 1 V, R_{IREF} = 1.6 kΩ, At OUT0 to OUT23		±2	±6	%/V
T_{DOWN}	Thermal shutdown threshold	Junction temperature(5)	150	162	175	°C
T_{HYS}	Thermal error hysteresis	Junction temperature(5)	5	10	20	°C
V_{IREF}	Reference voltage output	R_{IREF} = 1.6 kΩ	1.16	1.20	1.24	V

(1) The deviation of each output from the average of OUT0–OUT23 constant-current. Deviation is calculated by the formula:

$$\Delta\,(\%) = \left(\frac{I_{OUTn}}{\frac{(I_{OUT0} + I_{OUT1} + \ldots + I_{OUT22} + I_{OUT23})}{24}} - 1 \right) \times 100$$

(2) The deviation of the OUT0–OUT23 constant-current average from the ideal constant-current value. Deviation is calculated by the following formula:

$$\Delta\,(\%) = \left(\frac{\frac{(I_{OUT0} + I_{OUT1} + \ldots I_{OUT22} + I_{OUT23})}{24} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the formula:

$$I_{OUT(IDEAL)} = 41 \times \left(\frac{1.20}{R_{IREF}} \right)$$

(3) Line regulation is calculated by this equation:

$$\Delta\,(\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5\text{ V}) - (I_{OUTn} \text{ at } V_{CC} = 3.0\text{ V})}{(I_{OUTn} \text{ at } V_{CC} = 3.0\text{ V})} \right) \times \frac{100}{5.5\text{ V} - 3\text{ V}}$$

(4) Load regulation is calculated by the equation:

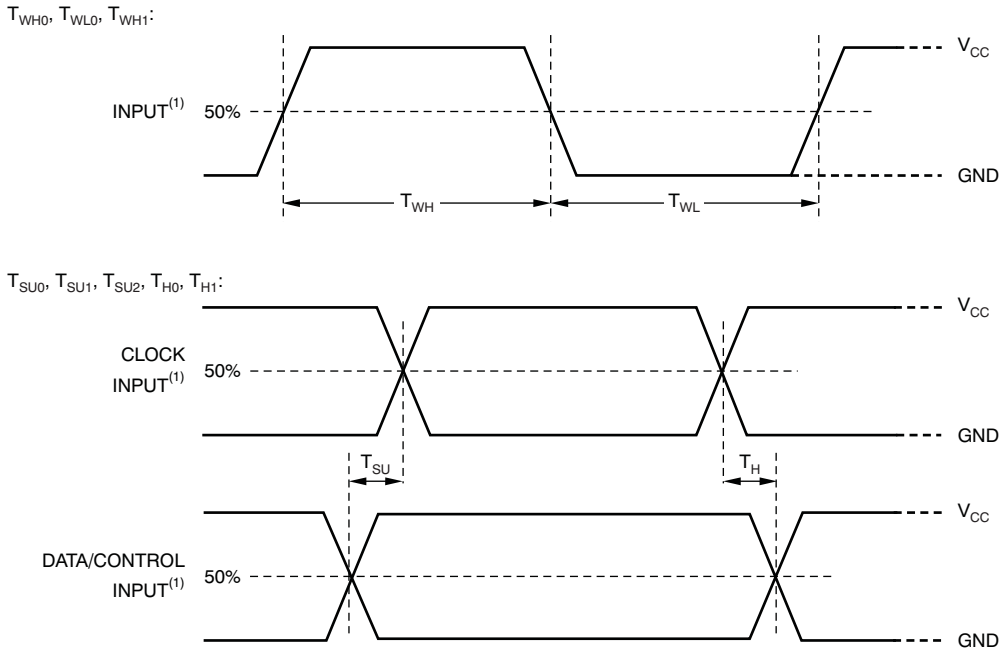
$$\Delta\,(\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3\text{ V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})}{(I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})} \right) \times \frac{100}{3\text{ V} - 1\text{ V}}$$

(5) Not tested. Specified by design.

6.7 Switching Characteristics

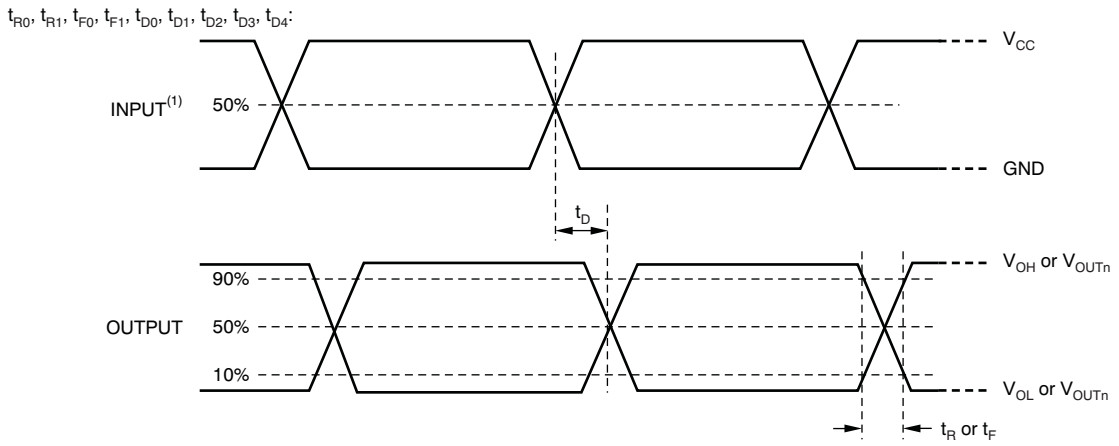
At V_{CC} = 3.0 V to 5.5 V, T_A = –40°C to 85°C, C_L = 15 pF, R_L = 150 Ω, R_{IREF} = 1.6 kΩ, and V_{LED} = 5.5 V. Typical values at V_{CC} = 3.3 V and T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{R0}	Rise time	SOUT		10	15	ns
t_{R1}		OUTn		15	40	ns
t_{F0}	Fall time	SOUT		10	15	ns
t_{F1}		OUTn		100	300	ns
f_{OSC}	Internal oscillator frequency		2.4	4	5.6	MHz
t_{D0}	Propagation delay time	SCLK↓ to SOUT		15	25	ns
t_{D1}		BLANK↑ to OUT0 sink current off		20	40	ns
t_{D2}		OUT0 current on to OUT1/5/9/13/17/21 current on	15	24	33	ns
t_{D3}		OUT0 current on to OUT2/6/10/14/18/22 current on	30	48	66	ns
t_{D4}		OUT0 current on to OUT3/7/11/15/19/23 current on	45	72	99	ns



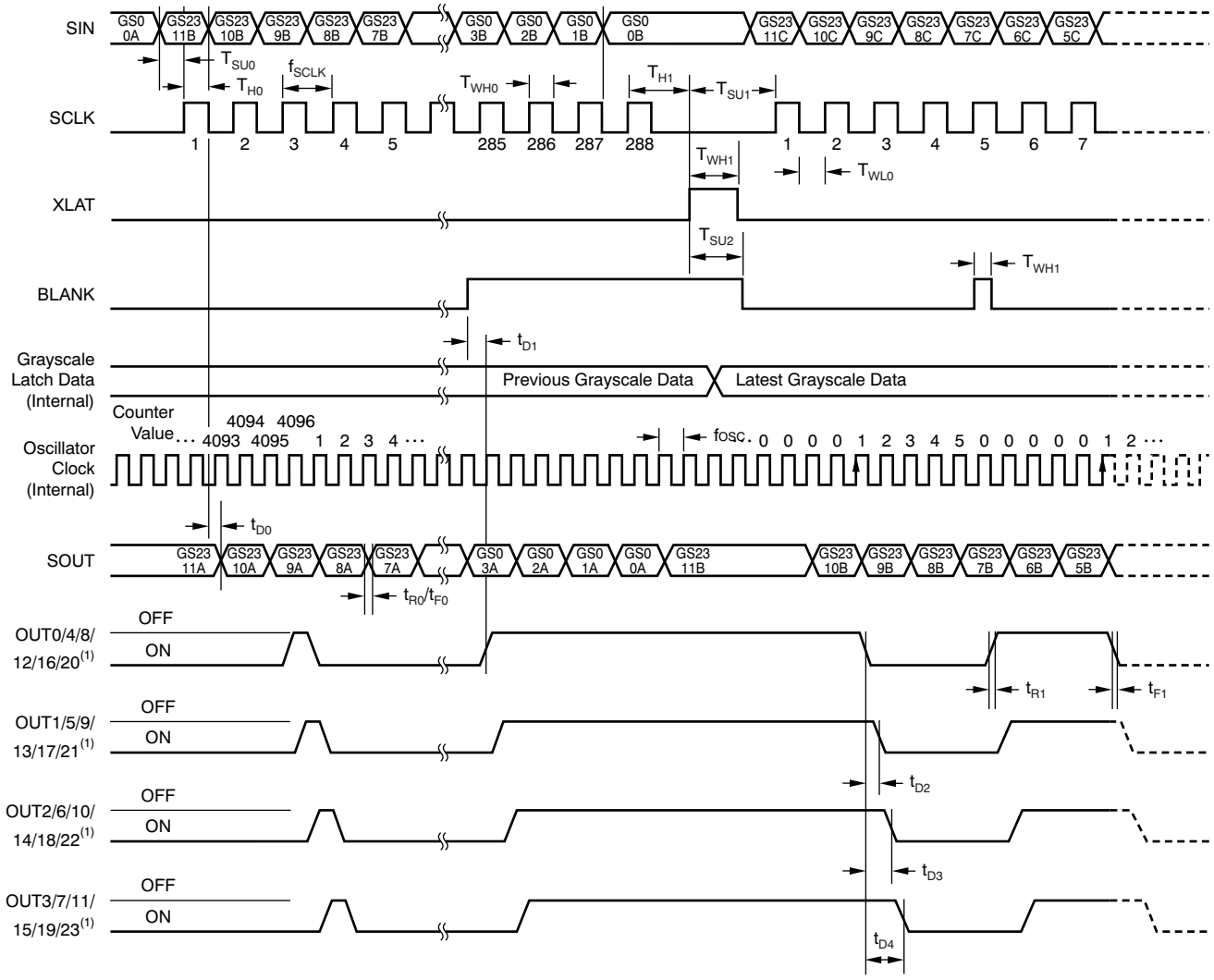
(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 1. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 2. Output Timing



(1) GS data = FFFh.

Figure 3. Grayscale Data Write and OUTn Operation Timing

6.8 Typical Characteristics

At V_{CC} = 3.3 V and T_A = 25°C, unless otherwise noted.

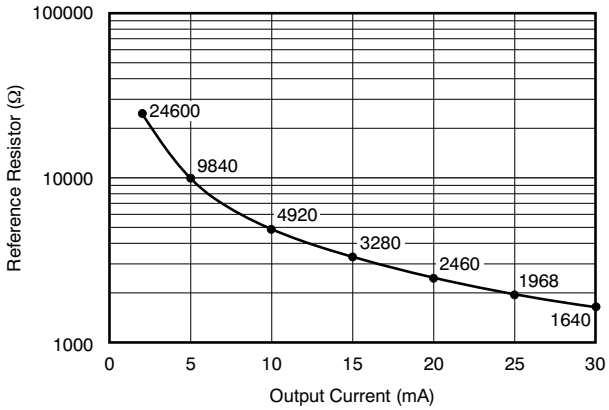


Figure 4. Reference Resistor vs Output Current

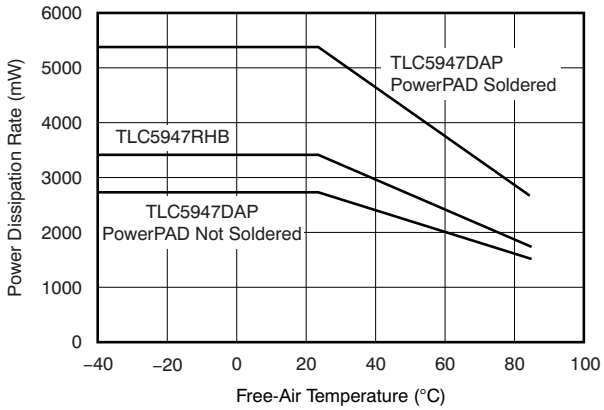


Figure 5. Power Dissipation Rate vs Free-Air Temperature

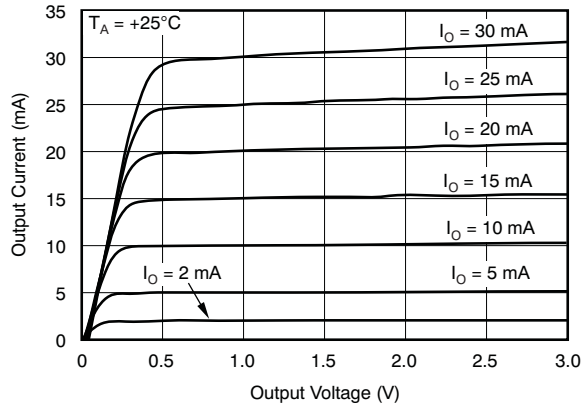


Figure 6. Output Current vs Output Voltage

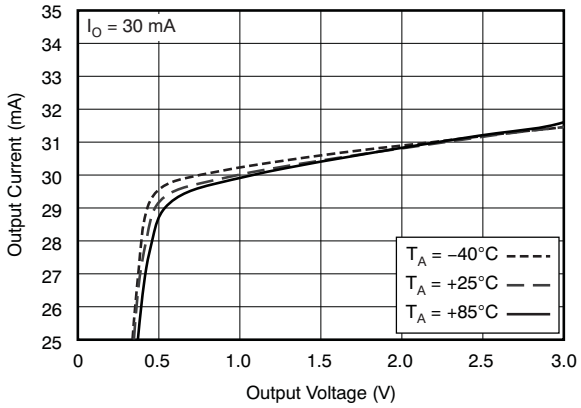


Figure 7. Output Current vs Output Voltage

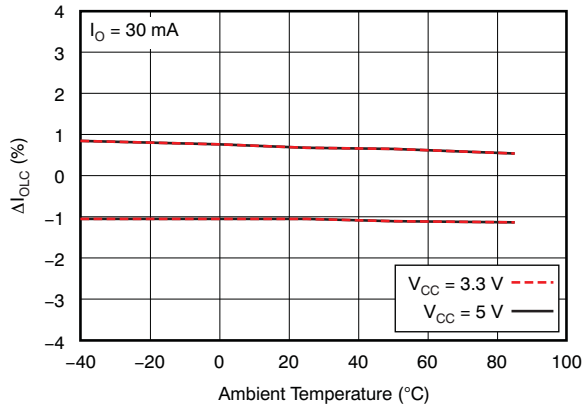


Figure 8. ΔI_{OLC} vs Ambient Temperature

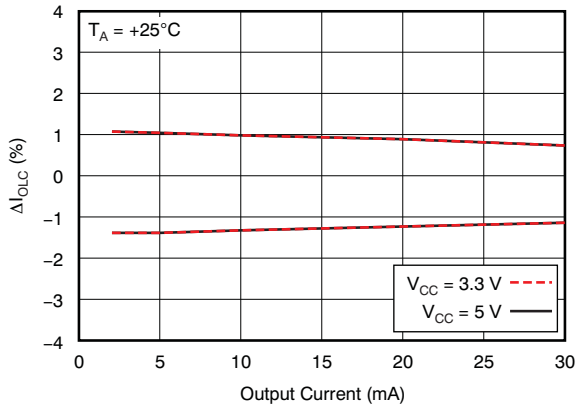


Figure 9. ΔI_{OLC} vs Output Current

Typical Characteristics (continued)

At V_{CC} = 3.3 V and T_A = 25°C, unless otherwise noted.

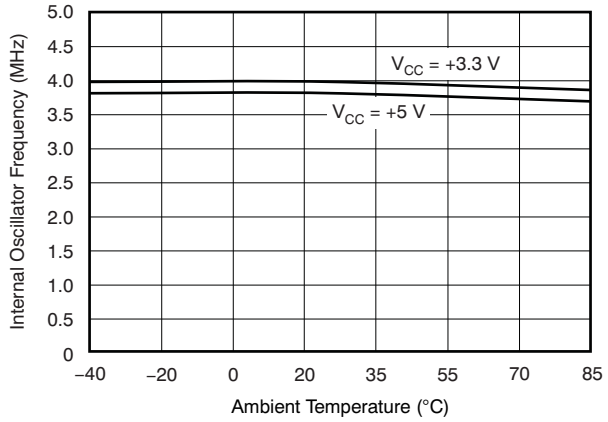


Figure 10. Internal Oscillator Frequency vs Ambient Temperature

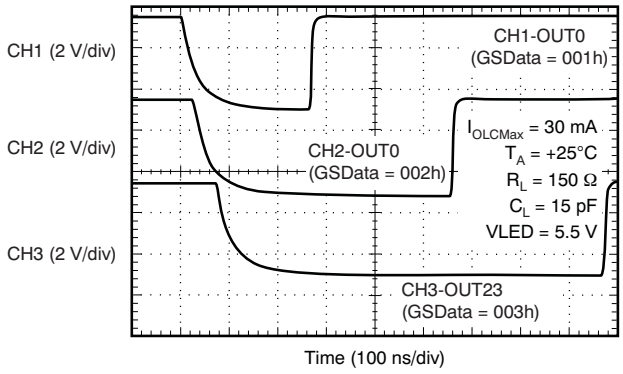


Figure 11. Constant-Current Output Voltage Waveform

7 Parameter Measurement Information

7.1 Pin Equivalent Input and Output Schematic Diagrams

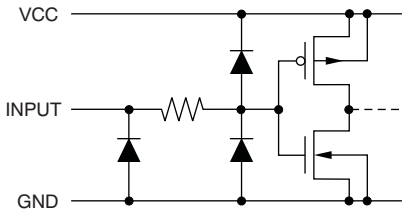


Figure 12. SIN, SCLK, XLAT, BLANK

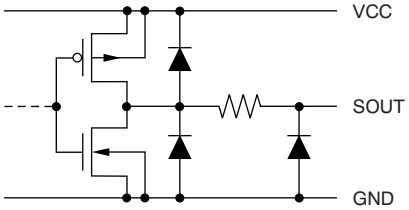


Figure 13. SOUT

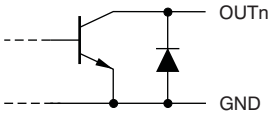


Figure 14. OUT0 Through OUT23

7.2 Test Circuits

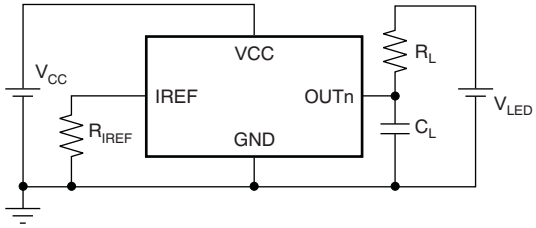


Figure 15. Rise Time and Fall Time Test Circuit for OUTn

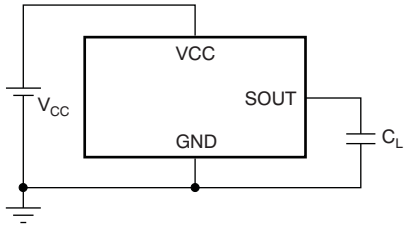


Figure 16. Rise Time and Fall Time Test Circuit for SOUT

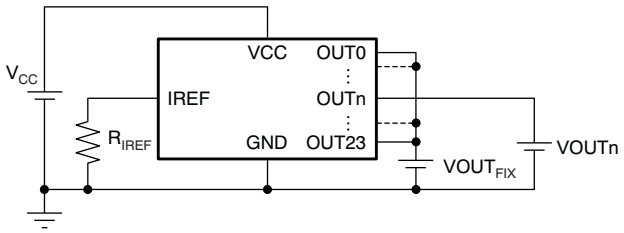


Figure 17. Constant-Current Test Circuit for OUTn

8 Detailed Description

8.1 Overview

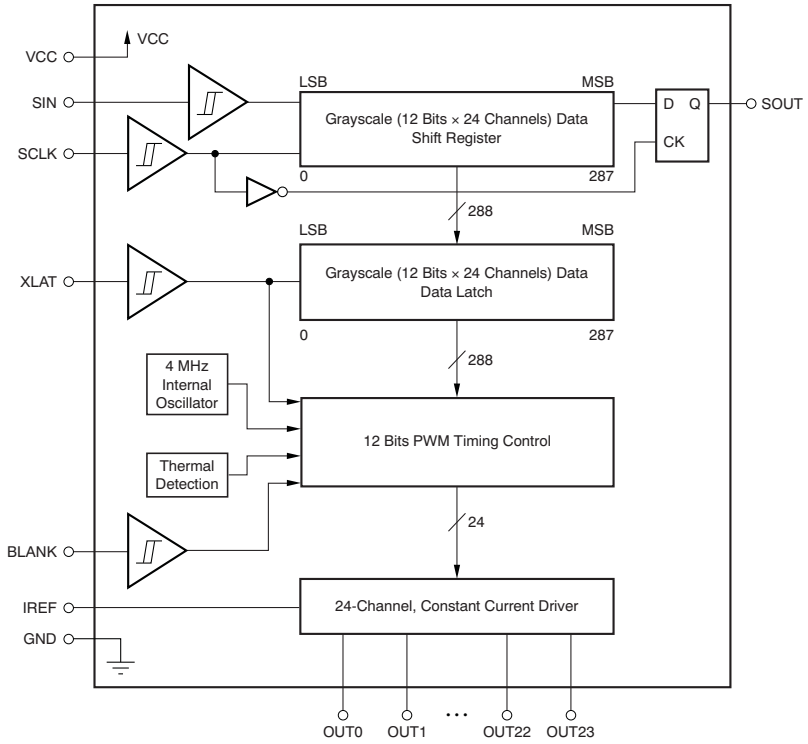
The TLC5947 is a 24-channel, constant-current sink driver. Each channel has an individually-adjustable, 4096-step, PWM grayscale (GS) brightness control. The GS data is input through a serial interface port.

The TLC5947 has a 30-mA current capability. The maximum current value of all channels is determined by an external resistor.

The TLC5947 can work without external CLK signals because the device is integrated with a 4-MHz internal oscillator.

The device has a thermal shutdown (TSD) function that turns off all output drivers at over temperature conditions. All of the output drivers automatically restart when the temperature returns to normal conditions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Grayscale (GS) Control Function

Each constant-current sink output OUT0–OUT23 (OUTn) turns on (starts to sink constant current) at the fifth rising edge of the grayscale internal oscillator clock after the BLANK signal transitions from high to low if the grayscale data latched into the grayscale data latch are not zero. After turn-on, the number of rising edges of the internal oscillator is counted by the 12-bit grayscale counter. Each OUTn output is turned off once its corresponding grayscale data values equal the grayscale counter or the counter reaches 4096d (FFFh). The PWM control operation is repeated as long as BLANK is low. OUTn is not turned on when BLANK is high. The timing is shown in Figure 18. All outputs are turned off at the XLAT rising edge. After that, each output is controlled again from the first clock of the internal oscillator for the next display period, based on the latest grayscale data.

Feature Description (continued)

When the IC is powered on, the data in the grayscale data shift register and latch are not set to default values. Therefore, grayscale data must be written to the GS latch before turning on the constant-current output. BLANK should be at a high level when powered on to keep the outputs off until valid grayscale data are written to the latch. This avoids the LED being randomly illuminated immediately after power-up. If having the outputs turn on at power-up is not a problem for the application, then BLANK does not need to be held high. The grayscale functions can be controlled directly by grayscale data writing, even though BLANK is connected to GND.

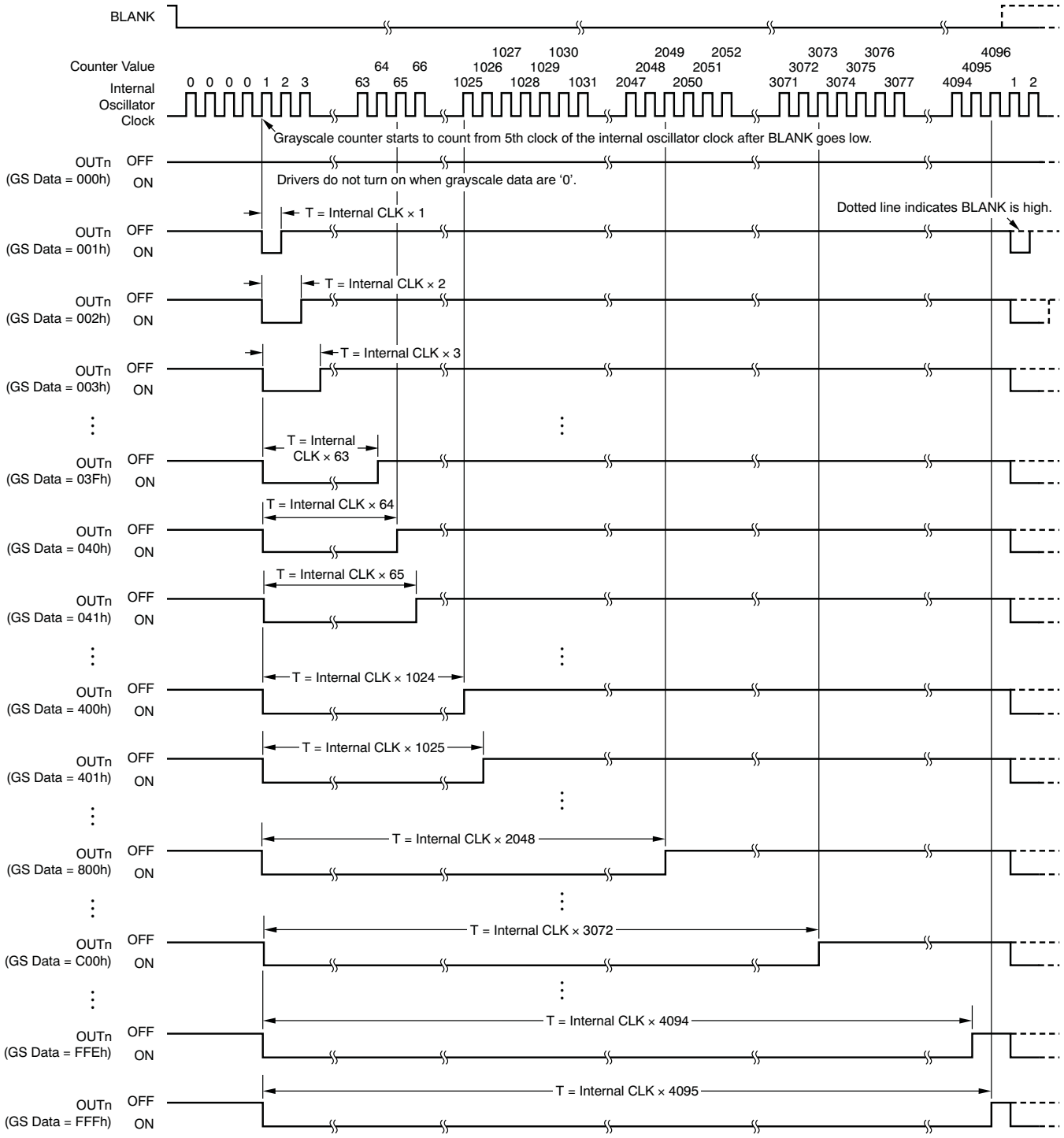


Figure 18. PWM Operation

Feature Description (continued)

8.3.2 Auto Display Repeat Function

This function can repeat the total display period without any timing control signal, as shown in Figure 19.

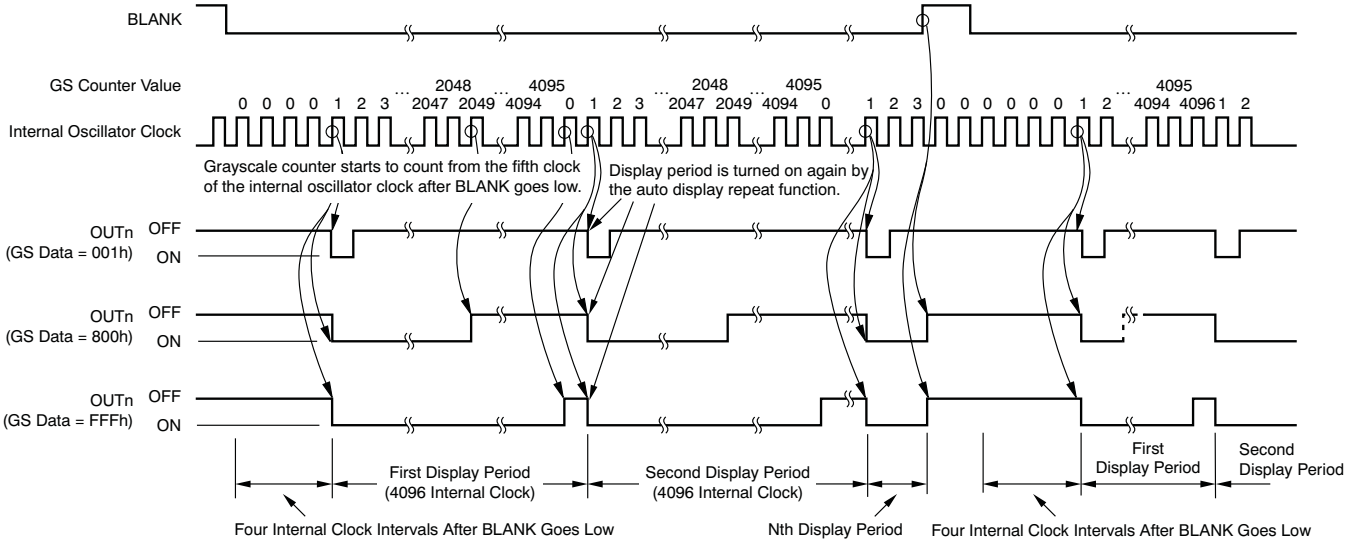


Figure 19. Auto Display Repeat Operation

8.3.3 Thermal Shutdown (TSD)

The thermal shutdown (TSD) function turns off all constant-current outputs immediately when the IC junction temperature exceeds the high temperature threshold ($T_{(TEF)}$ = +162° C, typ). The outputs will remain disabled as long as the over-temperature condition exists. The outputs are turned on again at the first clock after the IC junction temperature falls below the temperature of $T_{(TEF)} - T_{(HYS)}$. Figure 20 shows the TSD operation.

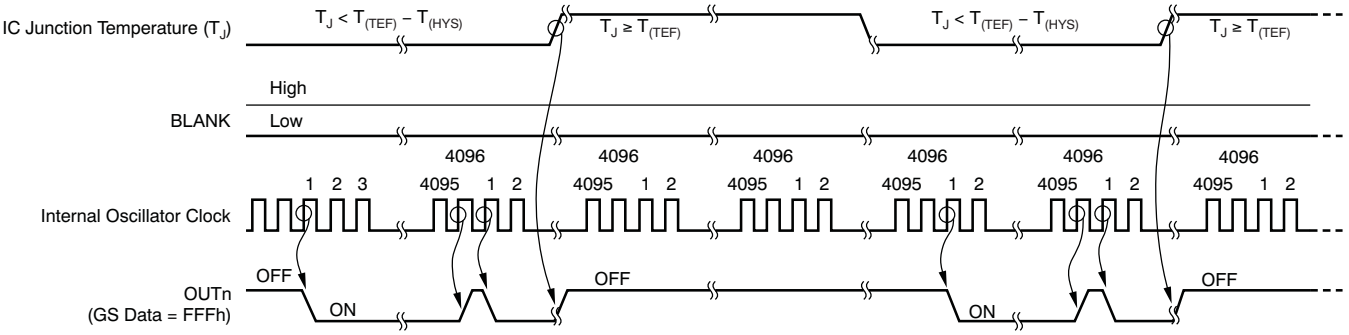


Figure 20. TSD Operation

8.3.4 Noise Reduction

Large surge currents may flow through the IC and the board on which the device is mounted if all 24 LED channels turn on simultaneously at the start of each grayscale cycle. These large current surges could introduce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC5947 turns on the LED channels in a series delay, to provide a current soft-start feature. The output current sinks are grouped into four groups of six channels each. The first group is OUT0, 4, 8, 12, 16, 20; the second group is OUT1, 5, 9, 13, 17, 21; the third group is OUT2, 6, 10, 14, 18, 22; and the fourth group is OUT3, 7, 11, 15, 19, 23. Each group turns on sequentially with a small delay between groups; see Figure 3. Both turn-on and turn-off are delayed.

8.4 Programming

8.4.1 Register Configuration

The TLC5947 has a grayscale (GS) data shift register and data latch. Both the GS data shift register and latch are 288 bits long and are used to set the PWM timing for the constant-current driver. Table 1 shows the on duty cycle for each GS data. Figure 21 shows the shift register and data latch configuration. The data at the SIN pin are shifted to the LSB of the shift register at the rising edge of the SCLK pin; SOUT data are shifted out on the falling edge of SCLK. The timing diagram for data writing is shown in Figure 22. The driver on duty is controlled by the data in the GS data latch.

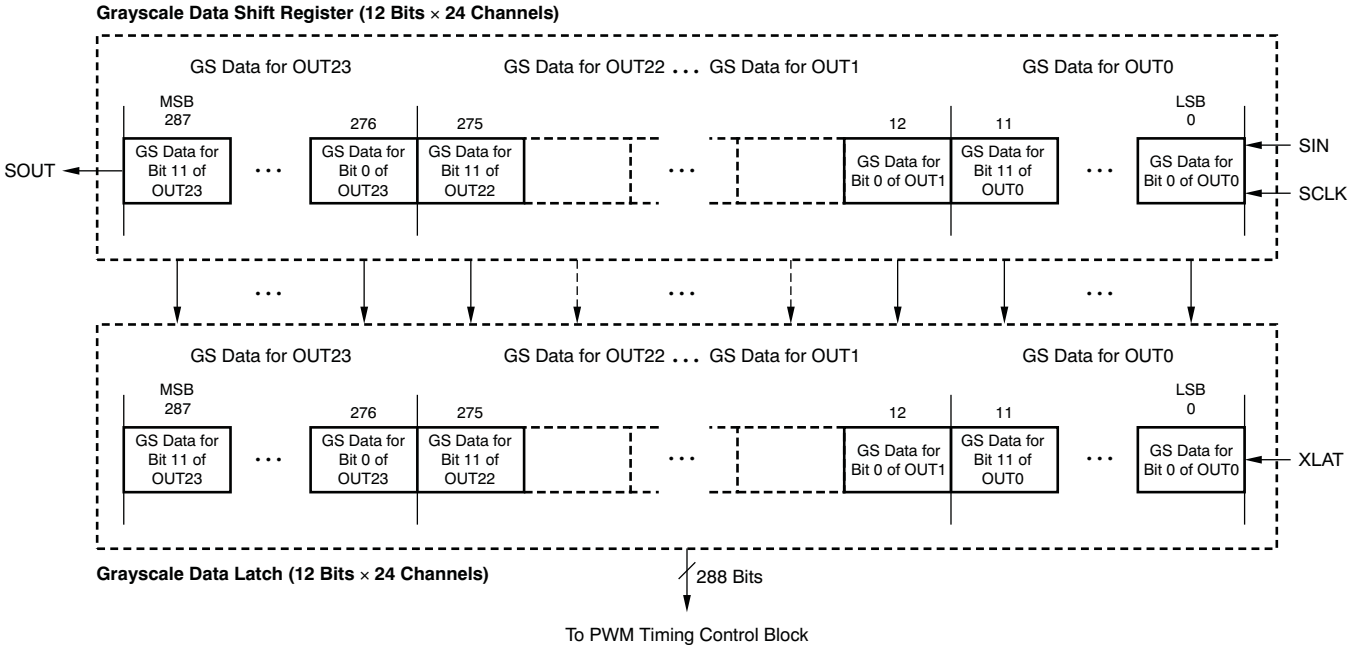


Figure 21. Grayscale Data Shift Register and Latch Configuration

Programming (continued)

Table 1. GS Data versus On Duty

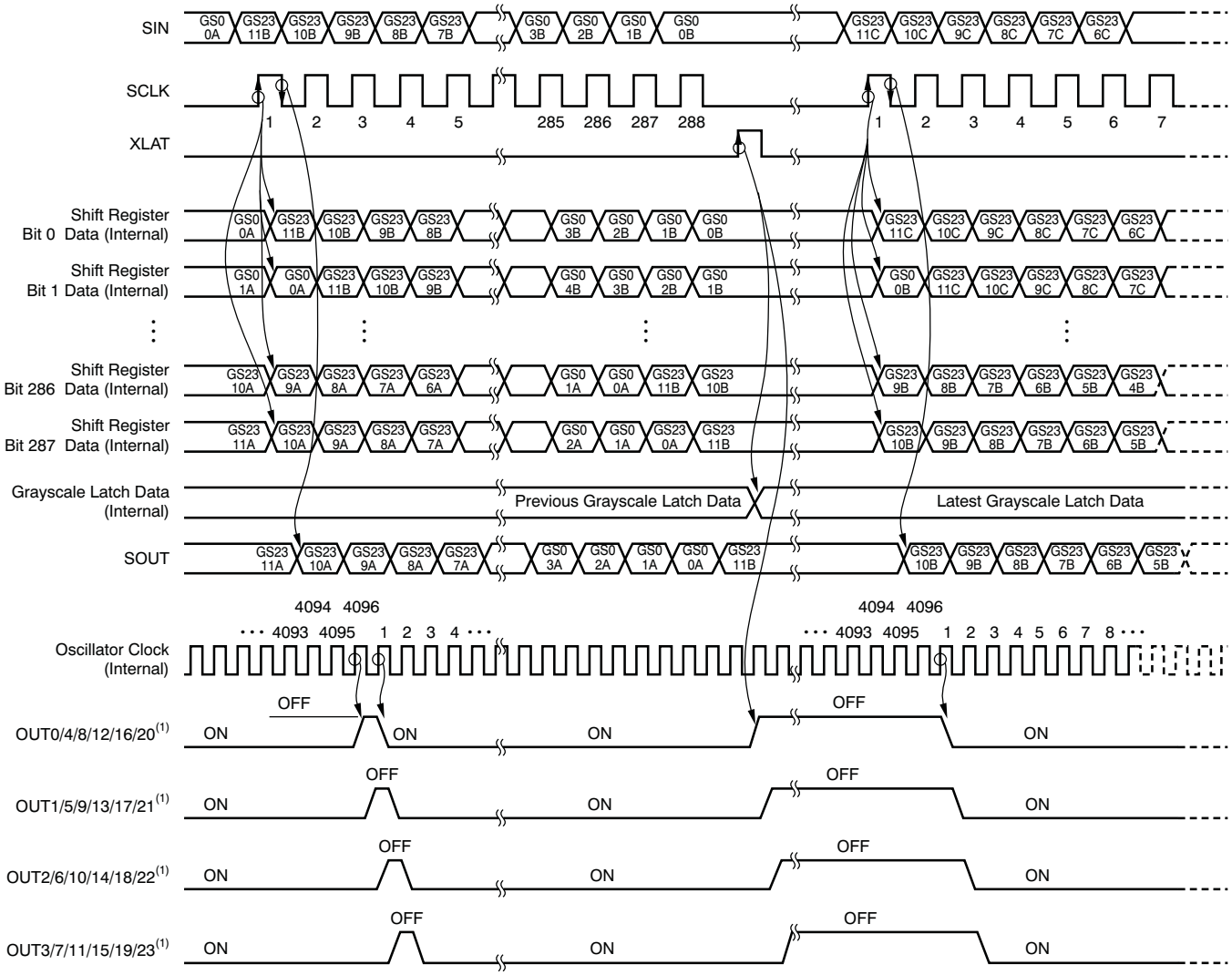
GS DATA (Binary)	GS DATA (Decimal)	GS DATA (Hex)	DUTY OF DRIVER TURN-ON TIME (%)
0000 0000 0000	0	000	0.00
0000 0000 0001	1	001	0.02
0000 0000 0010	2	002	0.05
0000 0000 0011	3	003	0.07
—	—	—	—
0111 1111 1111	2047	7FF	49.98
1000 0000 0000	2048	800	50.00
1000 0000 0001	2049	801	50.02
—	—	—	—
1111 1111 1101	4093	FFD	99.93
1111 1111 1110	4094	FFE	99.95
1111 1111 1111	4095	FFF	99.98

GS data are transferred from the shift register to the latch by the rising edge of XLAT. When powered up, the data in the grayscale shift register and data latch are not set to default values. Therefore, grayscale data must be written to the GS latch before turning on the constant-current output. BLANK should be at a high level when powered on to avoid falsely turning on the constant-current outputs due to random values in the latch at power-up. All of the constant-current outputs are forced off when BLANK is high. However, if the random values turning on at power-up is not a concern in the application, BLANK can be at any level. GS can be controlled correctly with the grayscale data writing functions, even if BLANK is connected to GND. Equation 1 determines each output on duty.

$$\text{On Duty (\%)} = \frac{GSn}{4096} \times 100 \quad (1)$$

where

- GSn = the programmed grayscale value for OUTn (GSn = 0 to 4095)



(1) GS data = FFFh.

Figure 22. Grayscale Data Write Operation

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The device is a 24-channel, constant sink current, LED driver. This device can be connected in series to drive many LED lamps with only a few controller ports. Output current control data and PWM control data can be written from the SIN input terminal. The PWM timing reference clock can be supplied from the internal oscillation.

9.2 Typical Application

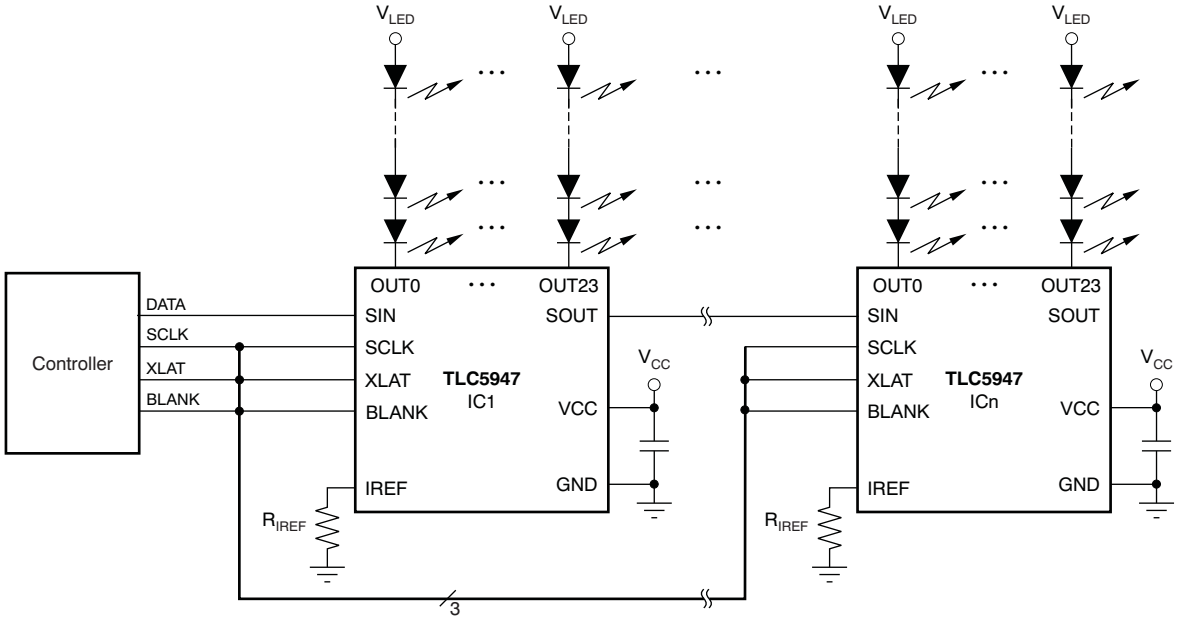


Figure 23. Typical Application Circuit (Multiple Daisy Chained TLC5947s)

9.2.1 Design Requirements

For this design example, use Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VCC input voltage range	3 V to 5.5 V
LED lamp (V_{LED}) input voltage range	Maximum LED forward voltage (V_F) + IC knee voltage
SIN, SCLK, LAT, and BLANK voltage range	Low level = GND, High level = VCC

9.2.2 Detailed Design Procedure

9.2.2.1 Define Basic Parameters

To begin the design process, a few parameters must be decided as following:

- Maximum output constant-current value for each color LED lamp
- Maximum LED forward voltage (V_F)
- Are auto display function used

9.2.2.2 Grayscale (GS) Data

There are a total of 24 sets of 12-bit GS data for the PWM control of each output. Select the GS data of each LED lamp and write the GS data to the register following the signal timing.

9.2.2.3 Auto-Display Function

There are a total of 24 sets of 12-bit GS data for the PWM control of each output. Select the GS data of each LED lamp and write the GS data to the register following the signal timing.

9.2.2.4 Setting for the Constant Sink Current Value

The constant-current value for all channels is set by an external resistor (R_{IREF}) placed between IREF and GND. The resistor (R_{IREF}) value is calculated by Equation 2.

$$R_{IREF}\ (\Omega) = 41 \times \frac{V_{IREF}\ (V)}{I_{OLC}\ (mA)} \quad (2)$$

where

- V_{IREF} = the internal reference voltage on the IREF pin (typically 1.20 V).

I_{OLC} must be set in the range of 2 mA to 30 mA. The constant sink current characteristic for the external resistor value is shown in Figure 4. Table 3 describes the constant-current output versus external resistor value.

Table 3. Constant-Current Output versus External Resistor Value

I_{OLC} (mA, Typical)	R_{IREF} (Ω)
30	1640
25	1968
20	2460
15	3280
10	4920
5	9840
2	24600

9.2.3 Application Curves

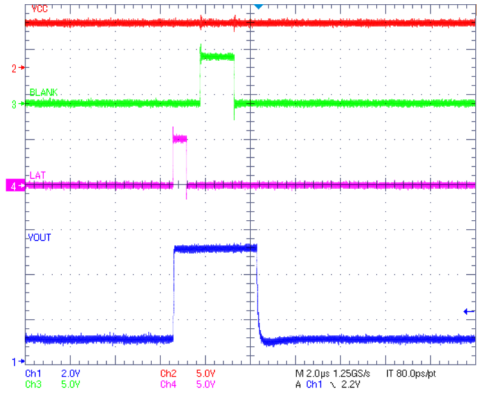


Figure 24. Output Waveform with GS Data Latch Input

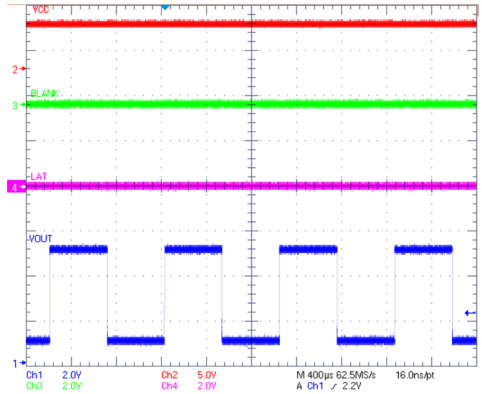


Figure 25. Output Waveform without GS Data Latch Input

10 Power Supply Recommendations

The VCC power supply voltage should be decoupled by placing a 0.1-µF ceramic capacitor close to the VCC pin and GND plane. Depending on the panel size, several electrolytic capacitors must be placed on the board equally distributed to get a well regulated LED supply voltage (V_{LED}). The V_{LED} voltage ripple must be less than 5% of its nominal value. Furthermore, the V_{LED} must be set to the voltage calculated by Equation 3:

$$V_{LED} > V_F + 0.4\ V \text{ (10-mA constant-current example)} \quad (3)$$

where

- V_F = maximum forward voltage of all LEDs.

11 Layout

11.1 Layout Guidelines

- Place the decoupling capacitor near the VCC pin and GND plane.
- Place the current programming resistor R_{IREF} close to the IREF pin and the IREFGND pin.
- Route the GND pattern as widely as possible for large GND currents.
- The routing wire between the LED cathode side and the device OUTXn pin must be as short and straight as possible to reduce wire inductance.
- When several ICs are chained, symmetric placements are recommended.

11.2 Layout Example

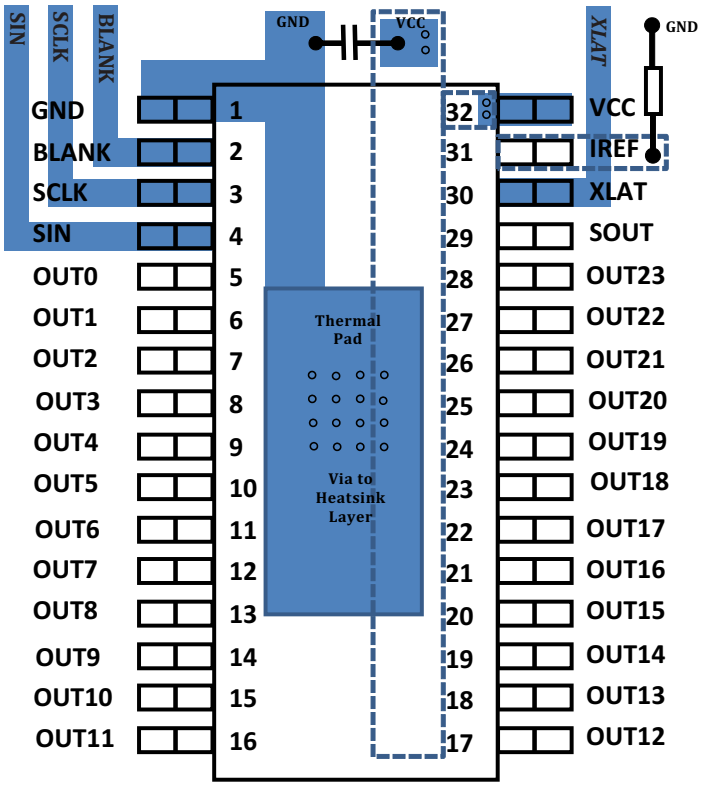


Figure 26. Layout Schematic

11.3 Power Dissipation

The device power dissipation must be below the power dissipation rate of the device package (illustrated in Figure 5) to ensure correct operation. Equation 4 calculates the power dissipation of the device:

$$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} \times I_{OLC} \times N \times d_{PWM}) \quad (4)$$

where

- V_{CC} = device supply voltage
- I_{CC} = device supply current
- V_{OUT} = OUTn voltage when driving LED current
- I_{OLC} = LED current adjusted by R_{IREF} resistor
- N = number of OUTn driving LED at the same time
- d_{PWM} = duty ratio defined by GS value

12 Device and Documentation Support

12.1 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA01054DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5947	Samples
HPA01116RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5947	Samples
TLC5947DAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5947	Samples
TLC5947DAPG4	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5947	Samples
TLC5947DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5947	Samples
TLC5947DAPRG4	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5947	Samples
TLC5947RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5947	Samples
TLC5947RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5947	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

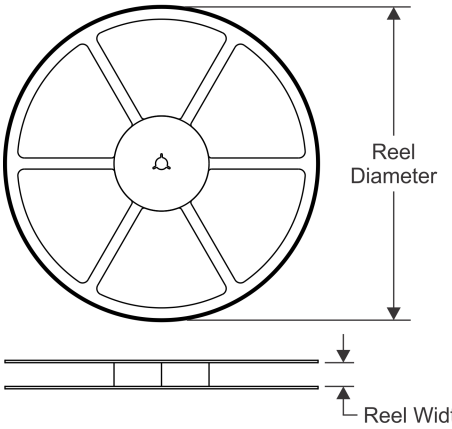
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

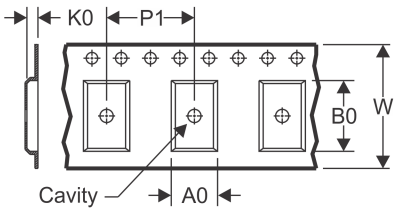
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

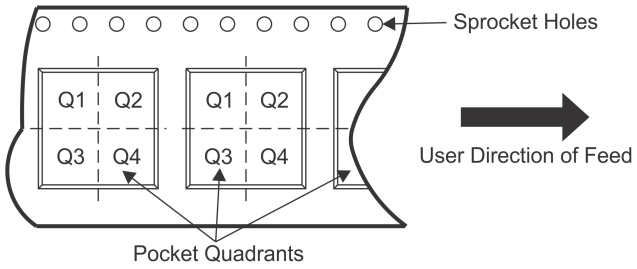


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

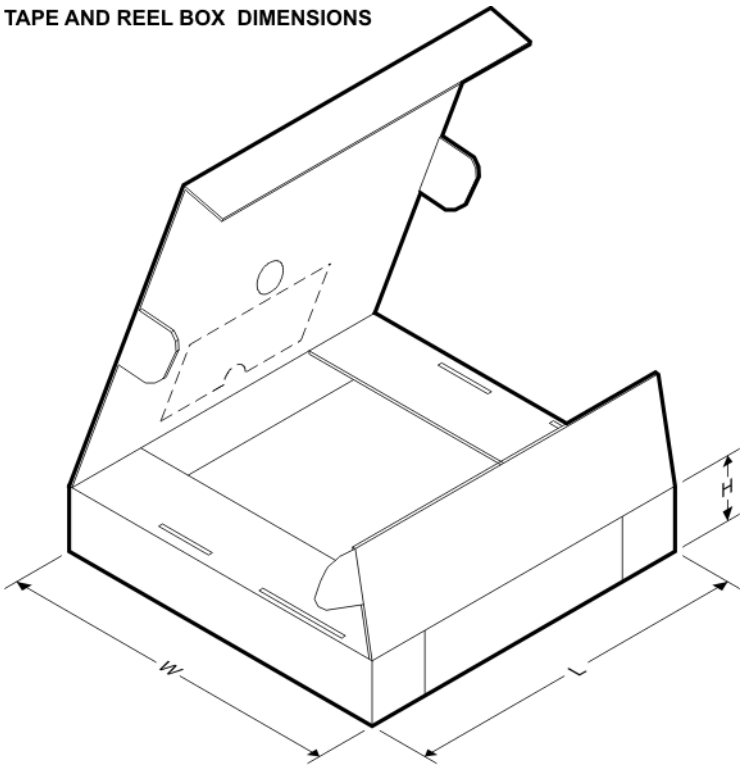
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5947DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TLC5947RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLC5947RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

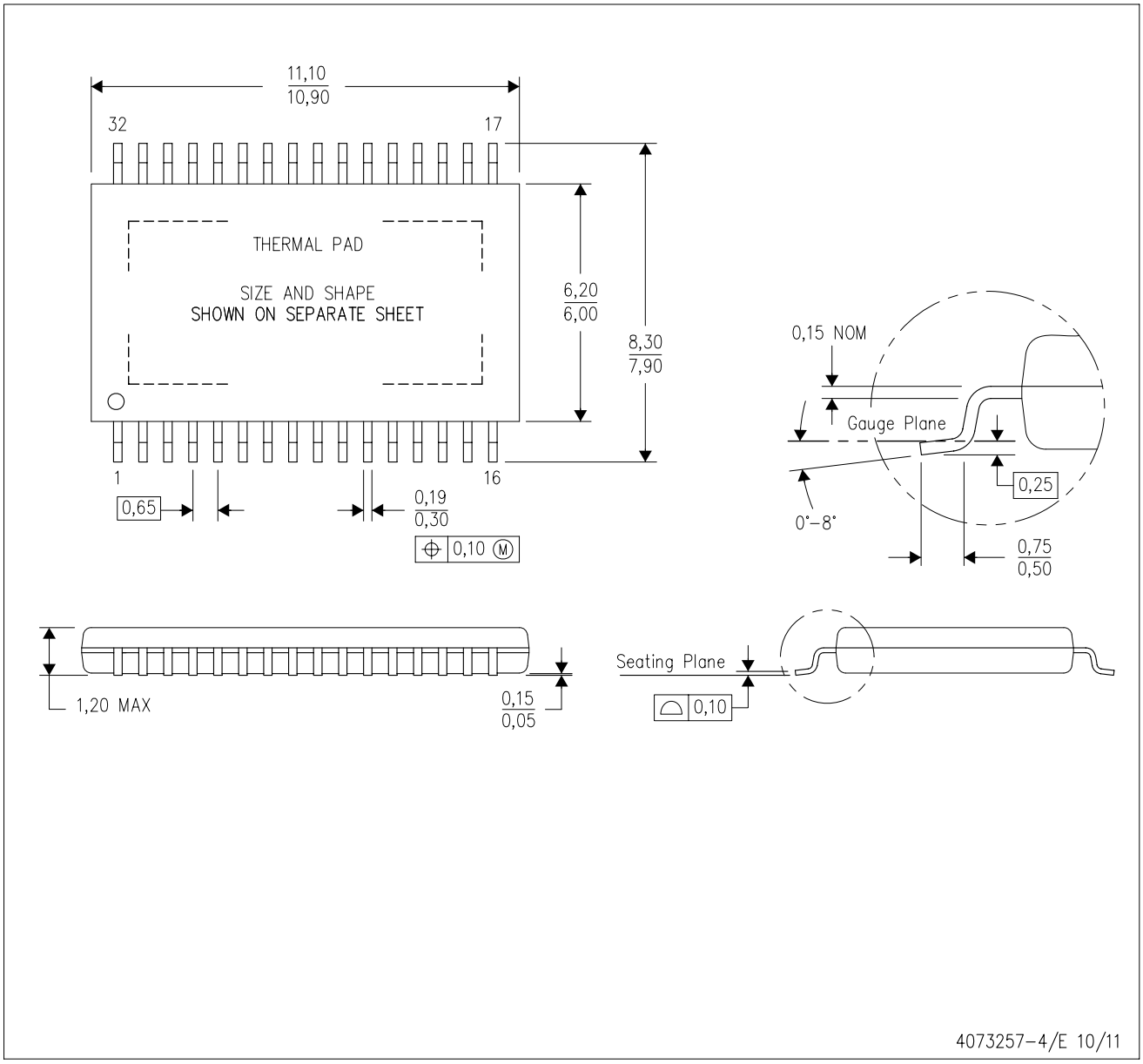
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5947DAPR	HTSSOP	DAP	32	2000	350.0	350.0	43.0
TLC5947RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TLC5947RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

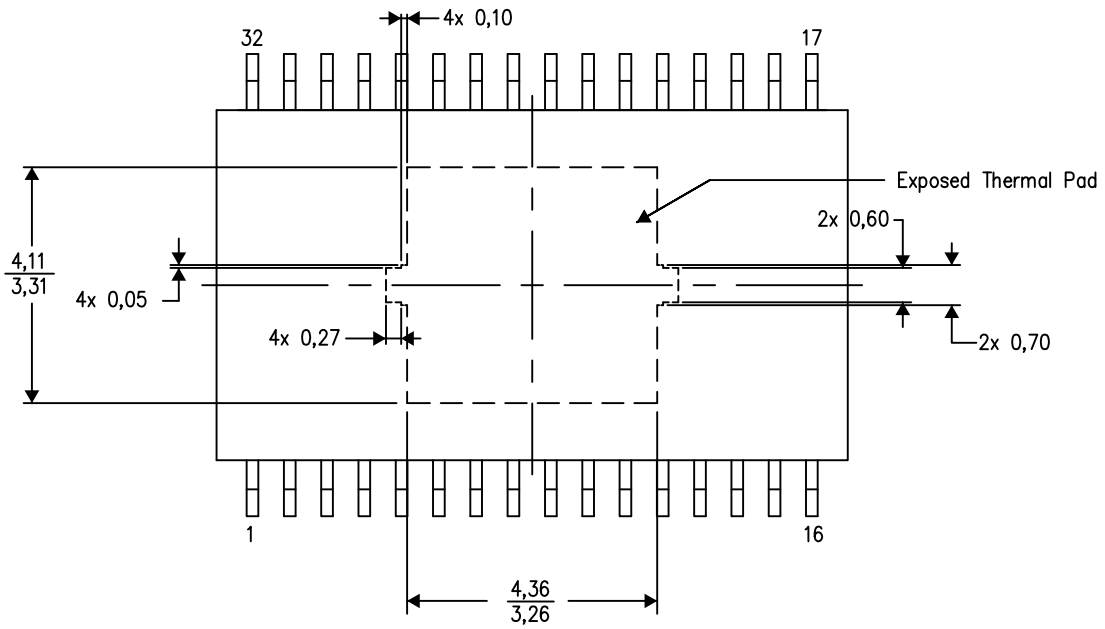
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

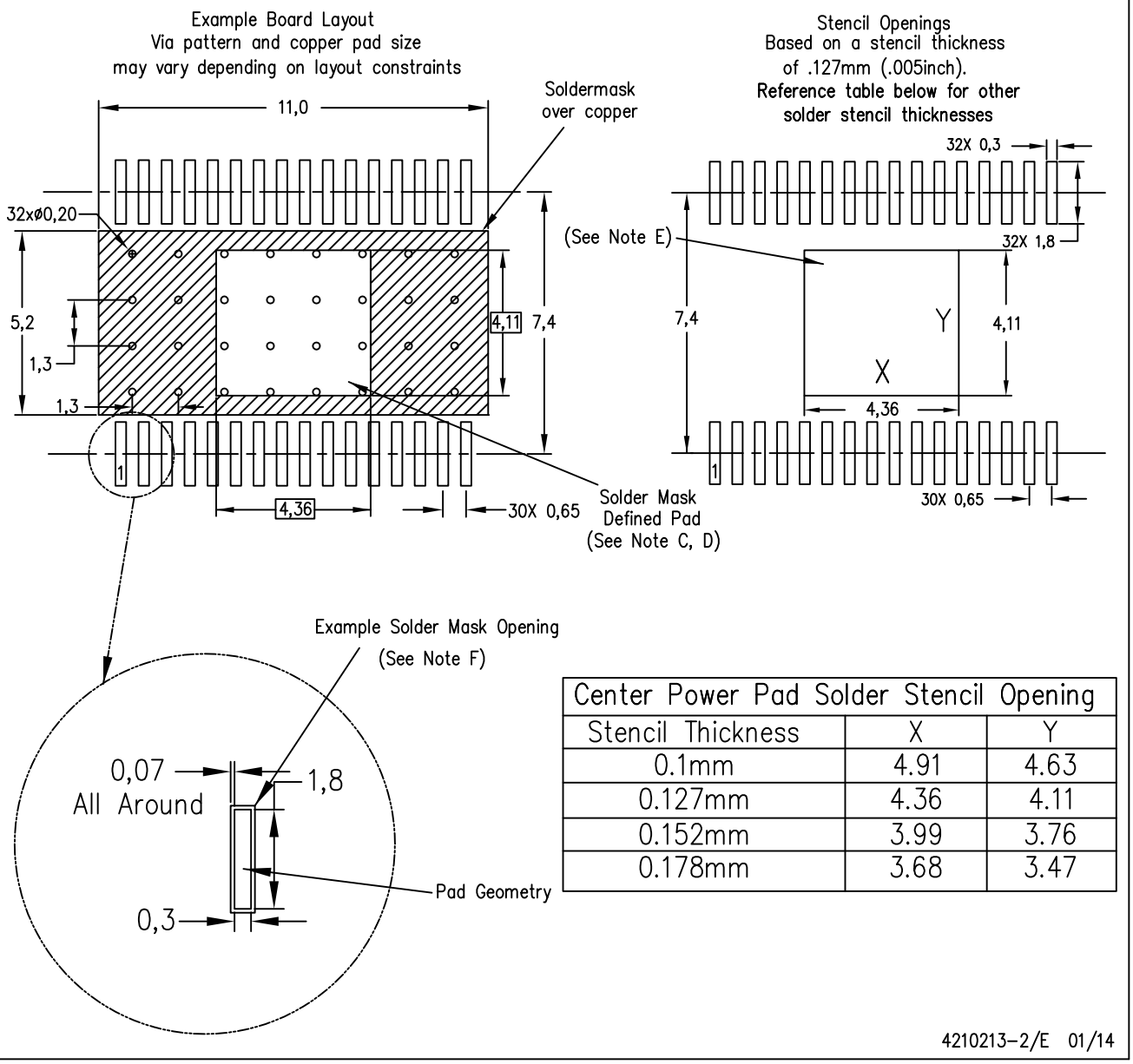
Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.91	4.63
0.127mm	4.36	4.11
0.152mm	3.99	3.76
0.178mm	3.68	3.47

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

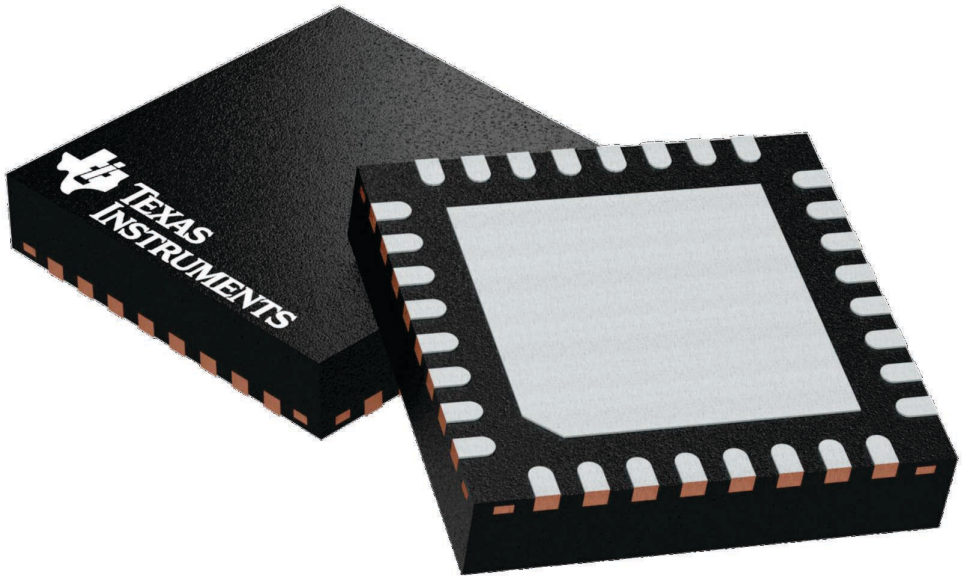
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

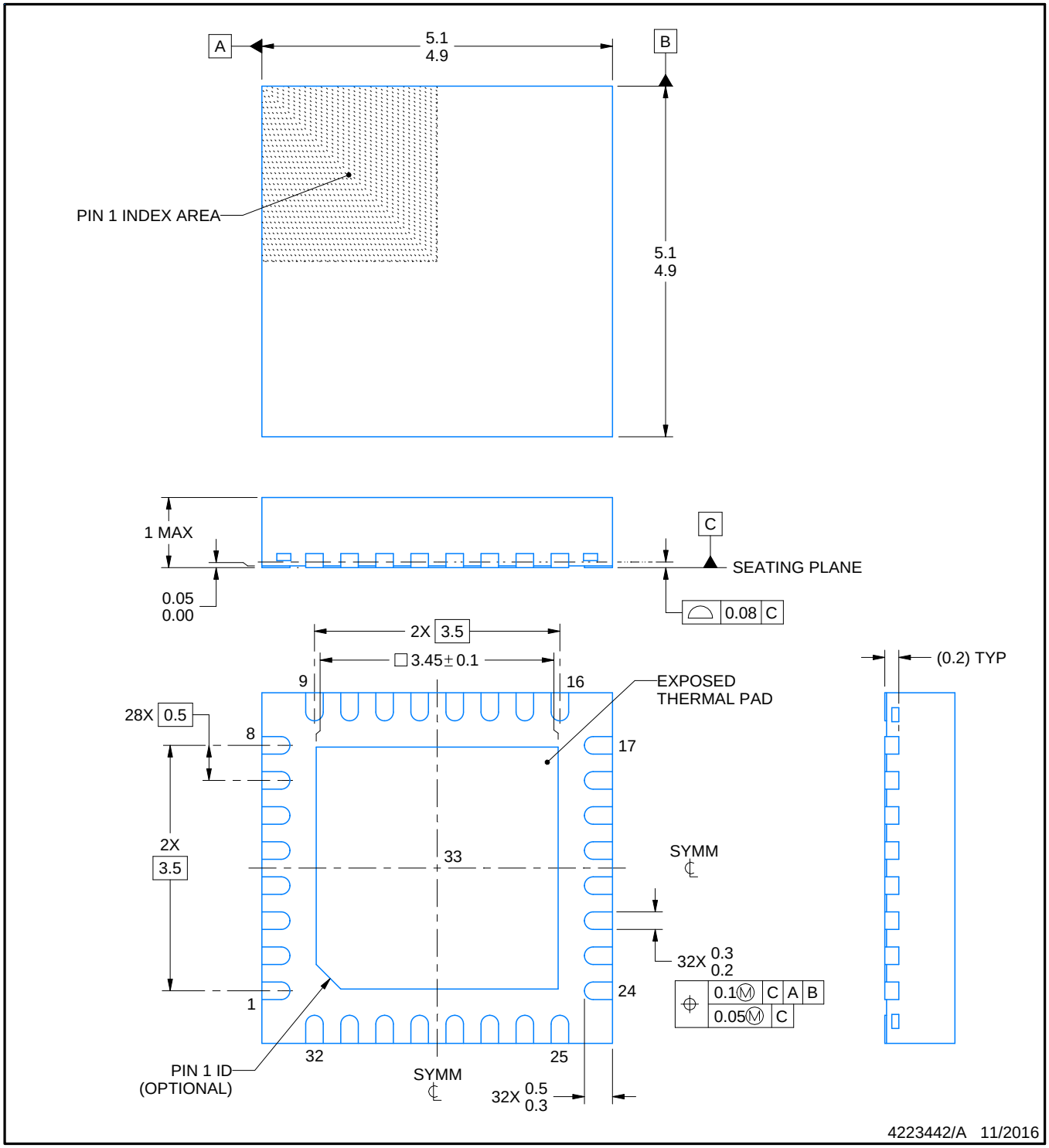
4224745/A

RHB0032E

PACKAGE OUTLINE

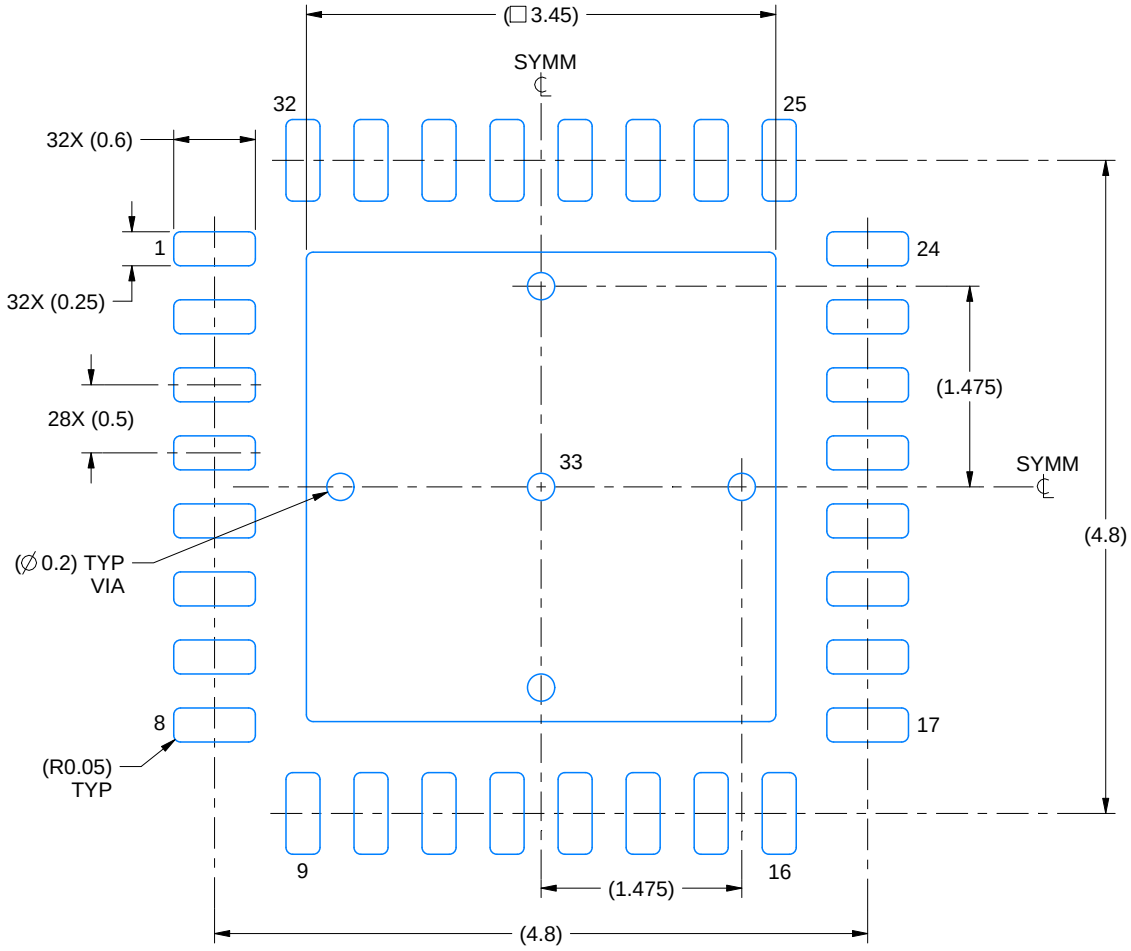
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

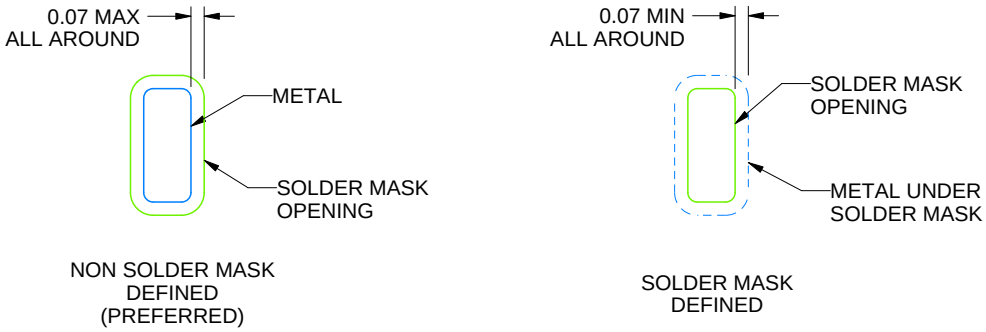


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

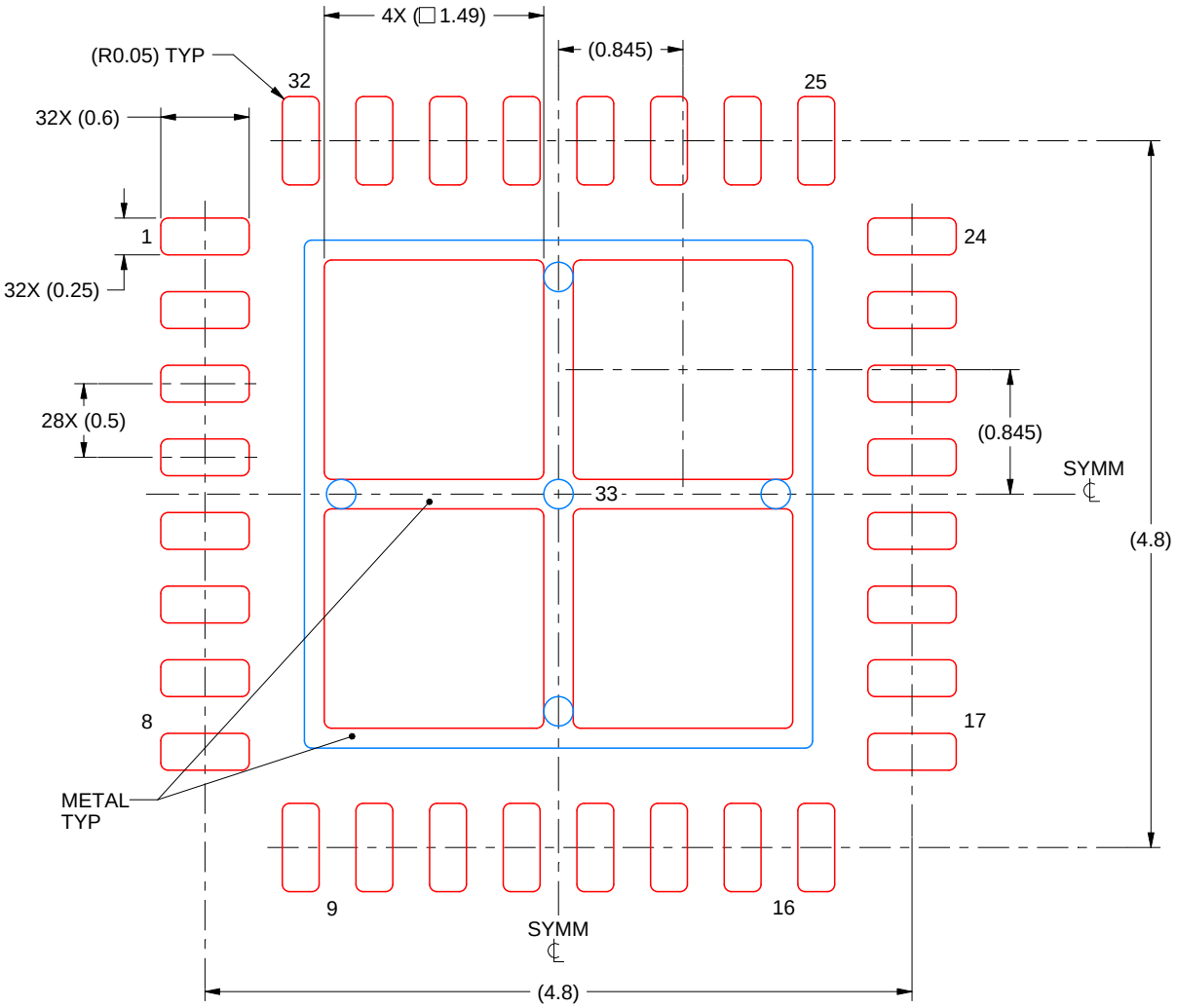


SOLDER MASK DETAILS

4223442/A 11/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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