



# THE DATASHEET OF RMPA2455



# RMPA2455

## 2.4–2.5 GHz 1 Watt InGaP HBT Linear Power Amplifier

### Features

- 30 dB small signal gain
- 30 dBm output power @ 1 dB compression
- 3% EVM at 22 dBm modulated power out
- 5.0 V positive collector supply operation
- Two power saving shutdown options (bias and logic control)
- Integrated power detector with 20 dB dynamic range
- Low profile 16 pin 3 x 3 x 0.9 mm leadless package
- Internally matched to 50Ω and DC blocked RF input/output
- Optimized for use in 802.11b/g Access Point applications

### General Description

The RMPA2455 power amplifier is designed for high performance WLAN access point applications in the 2.4–2.5 GHz frequency band. The low profile 16 pin 3 x 3 x 0.9 mm package with internal matching on both input and output to 50Ω minimizes next level PCB space and allows for simplified integration. The on-chip detector provides power sensing capability while the logic control provides power saving shutdown options. The PA's low power consumption and excellent linearity are achieved using our InGaP Heterojunction Bipolar Transistor (HBT) technology.

### Device



### Electrical Characteristics<sup>1</sup> 802.11g OFDM Modulation

(with 176 ms burst time, 100 ms idle time) 54 Mbps Data Rate, 16.7 MHz Bandwidth

| Parameter                                 | Min | Typ | Max | Units |
|---|-----|-----|-----|-------|
| Frequency                                 | 2.4 |     | 2.5 | GHz   |
| Collector Supply Voltage                  | 4.5 | 5.0 | 5.5 | V     |
| Mirror Supply Voltage                     | 2.8 | 3.3 | 3.6 | V     |
| Gain                                      |     | 30  |     | dB    |
| Total Current @ 22dBm P <sub>OUT</sub>    |     | 195 |     | mA    |
| EVM @ 22dBm P <sub>OUT</sub> <sup>2</sup> |     | 3.0 |     | %     |
| Detector Output @ 22dBm P <sub>OUT</sub>  |     | 960 |     | mV    |
| Detector Threshold <sup>3</sup>           |     | 4   |     | dBm   |

**Notes:**

1. VC1, VC2 = 5.0 Volts, VM12 = 3.3V, T<sub>A</sub> = 25°C, PA is constantly biased, 50Ω system.
2. Percentage includes system noise floor of EVM = 0.8%.
3. P<sub>OUT</sub> measured at P<sub>IN</sub> corresponding to power detection threshold.

**Electrical Characteristics<sup>1</sup> Single Tone**

| Parameter  | Min | Typ  | Max | Units |
|--|-----|------|-----|-------|
| Frequency  | 2.4 |      | 2.5 | GHz   |
| Collector Supply Voltage                         | 4.5 | 5.0  | 5.5 | V     |
| Mirror Supply Voltage                            | 2.8 | 3.3  | 3.6 | V     |
| Gain   |     | 30   |     | dB    |
| Total Quiescent Current                          |     | 140  |     | mA    |
| Bias Current at pin VM12 <sup>2</sup>            |     | 17   |     | mA    |
| P1dB Compression                                 |     | 30   |     | dBm   |
| Standby Current <sup>3</sup>                     |     | 0.7  |     | mA    |
| Shutdown Current (VM12 = 0V)                     |     | <1.0 |     | μA    |
| Input Return Loss                                |     | 12   |     | dB    |
| Output Return Loss                               |     | 10   |     | dB    |
| Detector Output at P1dB Comp                     |     | 4    |     | V     |
| Detector P <sub>OUT</sub> Threshold <sup>7</sup> |     | 6    |     | dBm   |
| 2nd Harmonic Output at P1dB                      |     | -40  |     | dBc   |
| 3rd Harmonic Output at P1dB                      |     | -40  |     | dBc   |
| Logic  |     |      |     |       |
| Shutdown Control (V <sub>L</sub> ):              |     |      |     |       |
| Device Off, Logic High Input                     | 2.0 | 2.4  |     | V     |
| Device On, Logic Low Input                       |     | 0.0  | 0.8 | V     |
| Logic Current                                    |     | 150  |     | μA    |
| Turn-on Time <sup>4</sup>                        |     | <1   |     | μS    |
| Turn-off Time                                    |     | <1   |     | μS    |
| Spurious (Stability) <sup>5</sup>                |     | -65  |     | dBc   |

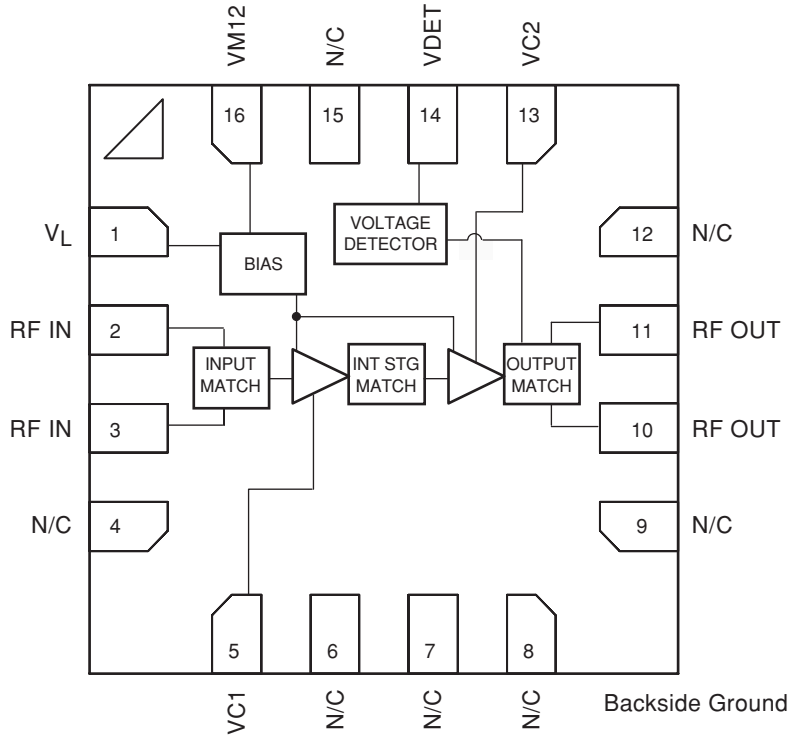
**Absolute Ratings<sup>6</sup>**

| Symbol            | Parameter                  | Ratings     | Units |
|-------------------|----------------------------|-------------|-------|
| VC1, VC2          | Positive Supply Voltage    | 6           | V     |
| IC1, IC2          | Supply Current             |             |       |
|                   | IC1                        | 120         | mA    |
|                   | IC2                        | 700         | mA    |
| VM12              | Positive Bias Voltage      | 4.0         | V     |
| V <sub>L</sub>    | Logic Voltage              | 5           | V     |
| P <sub>IN</sub>   | RF Input Power             | 10          | dBm   |
| T <sub>CASE</sub> | Case Operating Temperature | -40 to +85  | °C    |
| T <sub>STG</sub>  | Storage Temperature        | -55 to +150 | °C    |

**Notes:**

- VC1, VC2 = 5.0V, VM12 = 3.3V, T<sub>C</sub> = 25°C, 50Ω system.
- Mirror bias current is included in the total quiescent current.
- V<sub>L</sub> is set to Input Logic Level High for PA Off operation.
- Measured from Device On signal turn on (Logic Low) to the point where RF P<sub>OUT</sub> stabilizes to 0.5dB.
- Load VSWR is set to 8:1 and the angle is varied 360 degrees. P<sub>OUT</sub> = -30dBm to P1dB.
- No permanent damage with only one parameter set at extreme limit. Other parameters set to typical values
- P<sub>OUT</sub> measured at P<sub>IN</sub> corresponding to power detection threshold.

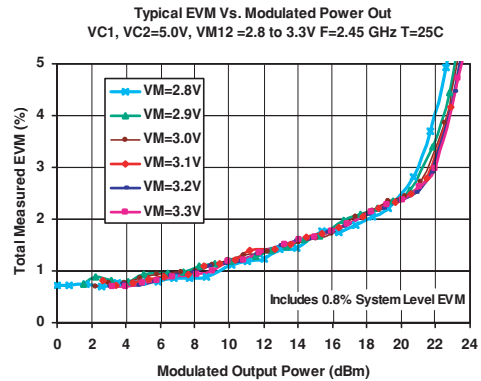
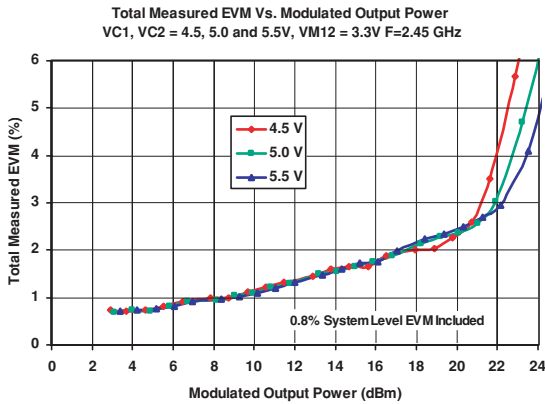
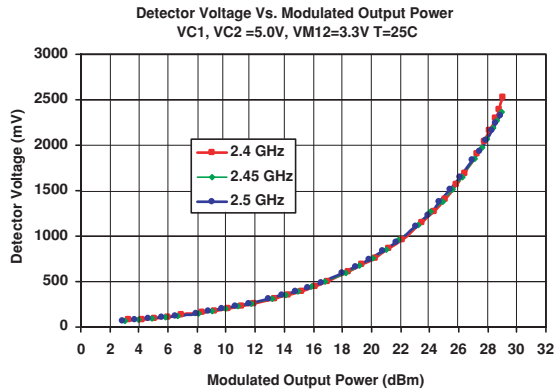
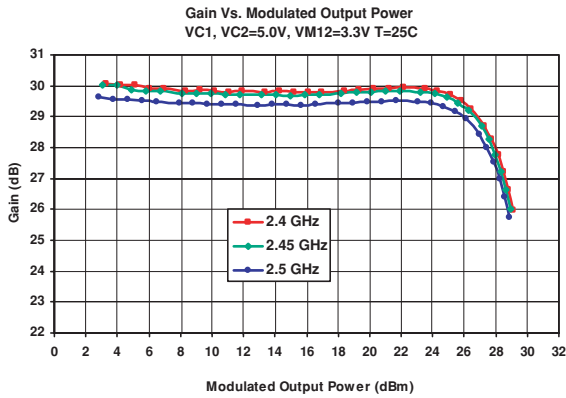
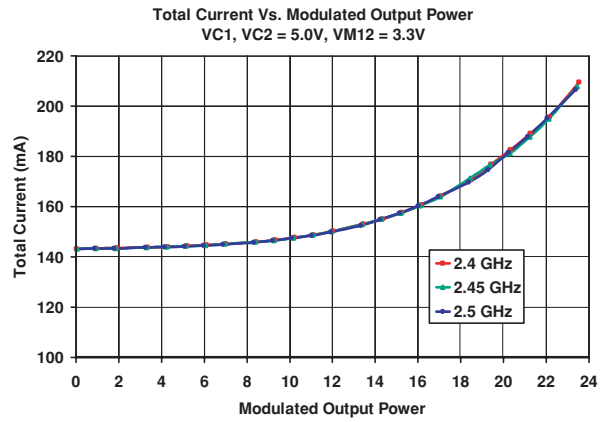
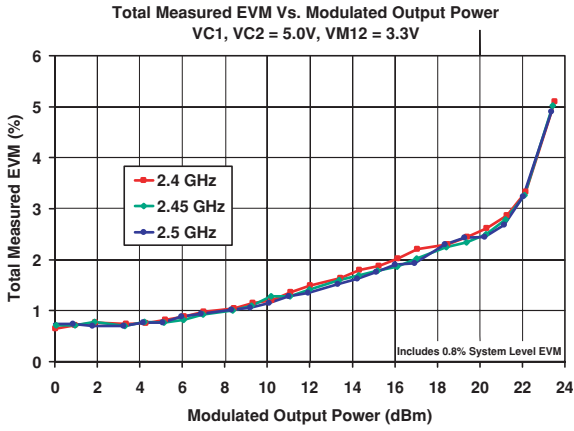
### Functional Block Diagram



| Pin | Description            |
|-----|------------------------|
| 1   | V <sub>L</sub> (logic) |
| 2   | RF IN                  |
| 3   | RF IN                  |
| 4   | N/C                    |
| 5   | VC1                    |
| 6   | N/C                    |
| 7   | N/C                    |
| 8   | N/C                    |
| 9   | N/C                    |
| 10  | RF OUT                 |
| 11  | RF OUT                 |
| 12  | N/C                    |
| 13  | VC2                    |
| 14  | VDET                   |
| 15  | N/C                    |
| 16  | VM12                   |

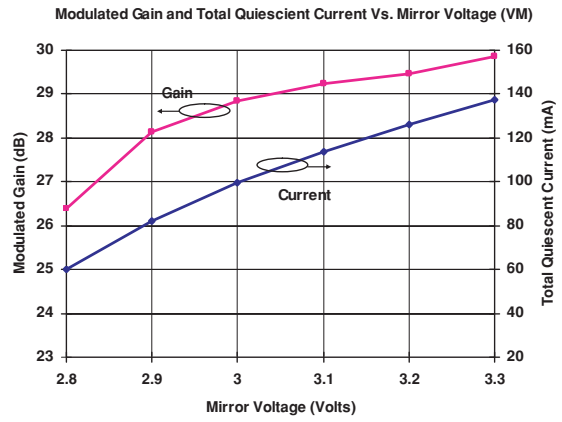
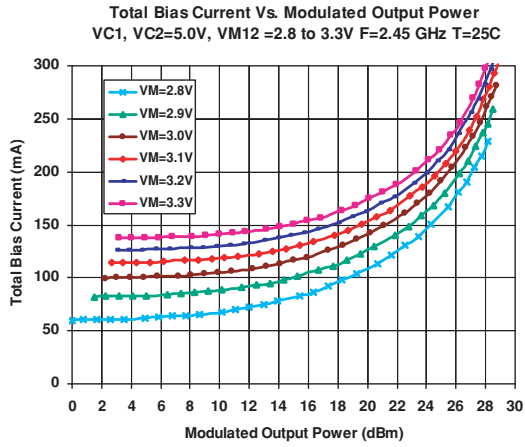
## Performance Data 802.11g OFDM

Modulation (with 176 ms burst time, 100 ms idle time) 54 Mbps Data Rate, 16.7 MHz Bandwidth

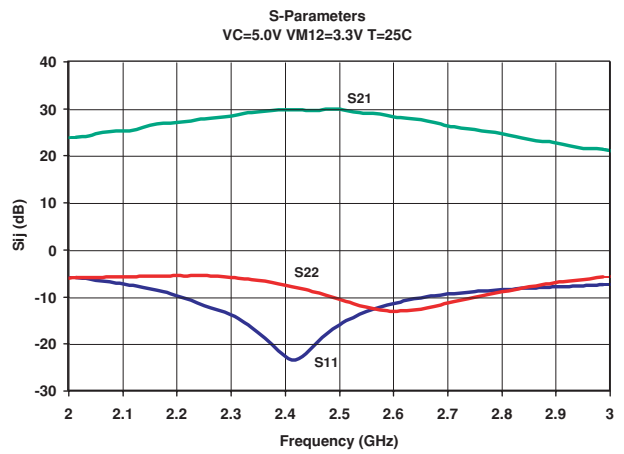
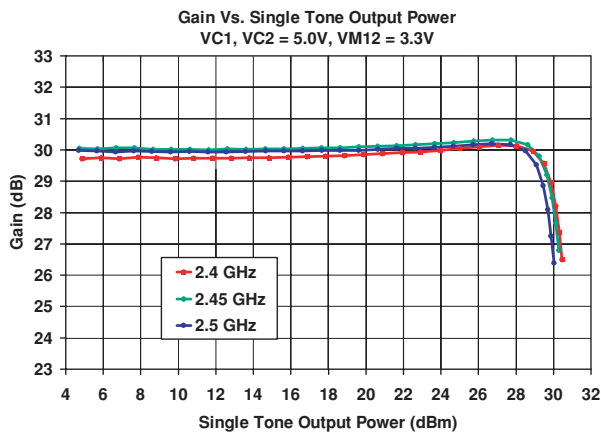


## Performance Data 802.11g OFDM

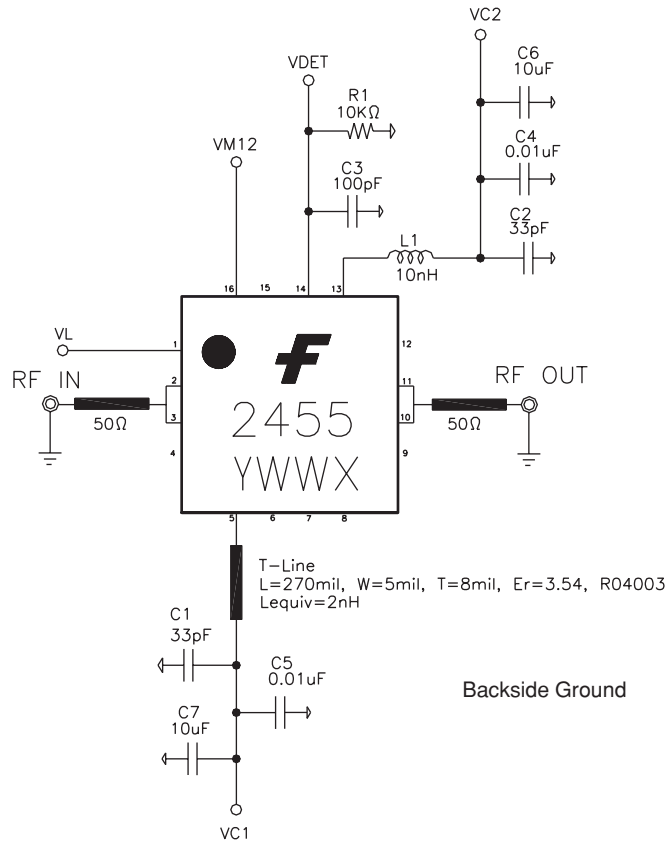
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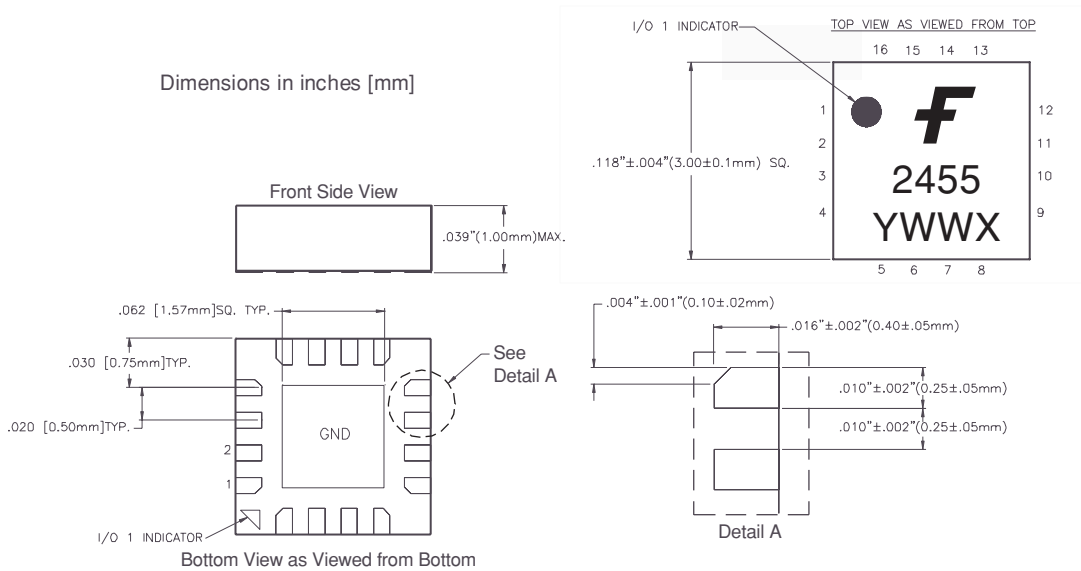
## Single Tone



## Evaluation Board Schematic



## Package Outline



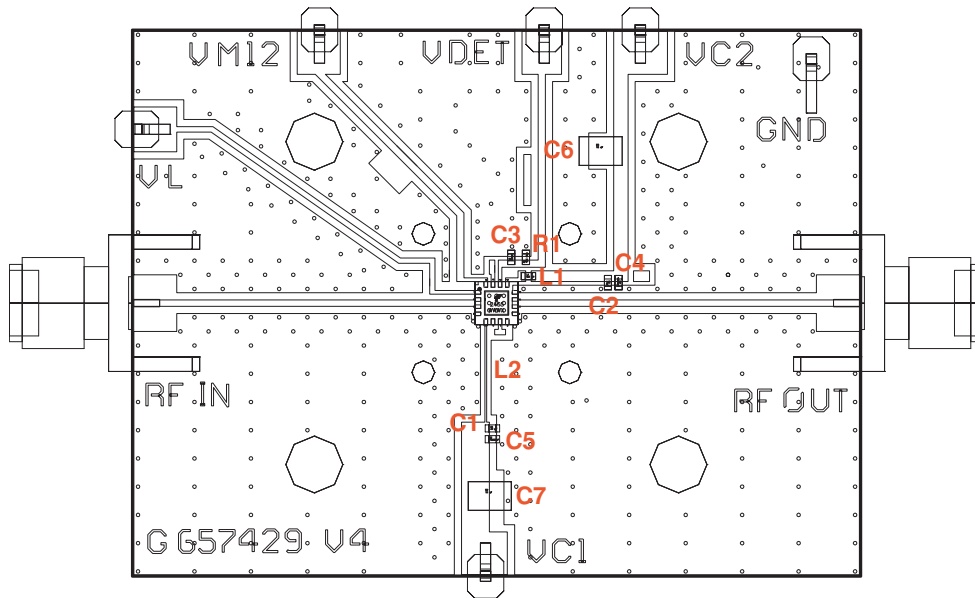
**Note:** Dimensions do not include protrusions or mold flash. These are not to exceed 0.006" (.155mm) on any side.

## Evaluation Board of Materials

### MATERIALS LIST

| QTY | ITEM NO.  | PART NUMBER     | DESCRIPTION            | VENDOR      |
|-----|-----------|-----------------|------------------------|-------------|
| 1   | 1         | G657429         | PC, BOARD              | FAIRCHILD   |
| 2   | 2         | #142-0701-841   | SMA CONNECTOR          | JOHNSON     |
| 6   | 3         | #S1322-XX-ND    | RT ANGLE SGL M HEADER  | DIGIKEY     |
| REF | 4         | F100046         | ASSEMBLY, RMPA2455     | FAIRCHILD   |
| 2   | 5 (C1&C2) | GRM39C0G330J50V | 33 pF CAPACITOR        | MURATA      |
| 1   | 6 (C3)    | GRM36C0G101J50V | 100 pF CAPACITOR       | MURATA      |
| 2   | 7 (C4&C5) | GRM39X7R103K50V | .01 uF CAPACITOR       | MURATA      |
| 2   | 8 (C6&C7) | CC1206JX5R106M  | 10 uF CAPACITOR (6.3V) | TDK         |
| 1   | 9 (L1)    | LLV1005FB10NJ   | 10 nH INDUCTOR         | TDKO        |
| 1   | 10 (R1)   | RCI-0402-1002J  | 10K OHM RESISTOR       | IMS         |
| A/R | 11        | SN63            | SOLDER PASTE           | INDIUM CORP |
| A/R | 12        | SN96            | SOLDER PASTE           | INDIUM CORP |

## Evaluation Board Layout



Actual Board Size = 2.0" X 1.5"

## Evaluation Board Turn-On Sequence<sup>1</sup>

### Recommended turn-on sequence:

- 1) Connect common ground terminal to the Ground (GND) pin on the board.
- 2) Apply low voltage 0.0 to +1.0 V to pin  $V_L$ .
- 3) Apply positive supply voltage VC1 (= 5.0V) to pin VC1 (first stage collector).
- 4) Apply positive supply voltage VC2 (= 5.0V) to pin VC2 (second stage collector).
- 5) Apply positive bias voltage VM12 (= 3.3V) to pin VM12 (bias networks).
- 6) At this point, you should expect to observe the following positive currents flowing into the pins:

| Pin   | Current        |
|-------|----------------|
| VM12  | 15.0 – 20.0 mA |
| VC1   | 45.0 – 65.0 mA |
| VC2   | 60.0 – 80.0 mA |
| $V_L$ | <1 nA          |

7) Apply input RF power to SMA connector pin RFIN. Currents in pins VC1 and VC2 will vary depending on the input drive level.

8) Vary positive voltage  $V_L$  on pin VREG from +0.5V to +2.4V to shut down the amplifier or alter the power level. Shut down current flow into the pins:

| Pin   | Current  |
|-------|----------|
| VM12  | <0.7 mA  |
| VC1   | <1 nA    |
| VC2   | <1 nA    |
| $V_L$ | <0.25 mA |

### Recommended turn-off sequence:

Use reverse order described in the turn-on sequence above.

#### Note:

1. Turn on sequence is not critical and it is not necessary to sequence power supplies in actual system level design.

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