



**THE DATASHEET OF  
MB95F354LWQN-G-SNE1**





**MB95F352E/F352L/F353E/F353L/F354E/F354L**

## **CMOS F<sup>2</sup>MC-8FX MB95350L Series 8-bit Microcontrollers**

MB95350L is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral resources.

### **Features**

#### **F<sup>2</sup>MC-8FX CPU core**

Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

#### **Clock**

- Selectable main clock source

Main OSC clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)

External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)

Main CR clock (1/8/10/12.5 MHz  $\pm$ 2%, maximum machine clock frequency: 12.5 MHz)

- Selectable subclock source

Sub-OSC clock (32.768 kHz)

External clock (32.768 kHz)

Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 200 kHz)

#### **Timer**

- 8/16-bit composite timer  $\times$  2 channels
- Time-base timer  $\times$  1 channel
- Watch prescaler  $\times$  1 channel

**UART/SIO  $\times$  1 channel (The channel can be used either as a UART/SIO channel or as an I<sup>2</sup>C channel.)**

- Alternative selection of UART/SIO
- Full duplex double buffer
- Capable of clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer

**I<sup>2</sup>C  $\times$  2 channels (One of the two channels can be used either as an I<sup>2</sup>C channel or as a UART/SIO channel.)**

- Supports Standard-mode and Fast-mode (400 kHz)
- Built-in wake-up function

#### **LIN-UART**

- Full duplex double buffer
- Capable of clock-synchronous serial data transfer and clock-asynchronous serial data transfer

#### **External interrupt $\times$ 6 channels**

- Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- Can be used to wake up the device from different low power consumption (standby) modes

#### **8/10-bit A/D converter $\times$ 6 channels**

- 8-bit and 10-bit resolution can be chosen.

#### **Low power consumption (standby) modes**

- Stop mode
- Sleep mode
- Watch mode
- Time-base timer mode

#### **I/O port**

- MB95F352L/F353L/F354L (maximum no. of I/O ports: 21)
  - General-purpose I/O ports (N-ch open drain) ..... : 3
  - General-purpose I/O ports (CMOS I/O) ..... : 18
- MB95F352E/F353E/F354E (maximum no. of I/O ports: 22)
  - General-purpose I/O ports (N-ch open drain) ..... : 3
  - General-purpose I/O ports (CMOS I/O) ..... : 18
  - General-purpose input port (CMOS input) ..... : 1

#### **On-chip debug**

- 1-wire serial control
- Serial writing supported (asynchronous mode)

#### **Hardware/software watchdog timer**

- Built-in hardware watchdog timer
- Built-in software watchdog timer

#### **Low-voltage detection reset and interrupt circuit**

- Built-in low-voltage detector

#### **Clock supervisor counter**

- Built-in clock supervisor counter function

**Programmable port input voltage level**

- CMOS input level / hysteresis input level

**Dual operation Flash memory**

- The erase/write operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

**Flash memory security function**

- Protects the content of the Flash memory

## Content

<b>Product Line-up</b> .....	<b>3</b>	Clock Timing .....	29
<b>Packages and Corresponding Products</b> .....	<b>5</b>	Source Clock/Machine Clock .....	31
<b>Differences Among Products and Notes On</b>		External Reset .....	34
<b>Product Selection</b> .....	<b>6</b>	Power-on Reset .....	35
<b>Pin Assignment</b> .....	<b>7</b>	Peripheral Input Timing .....	36
<b>Pin Description (24-pin MCU)</b> .....	<b>8</b>	LIN-UART Timing .....	37
<b>Pin Description (32-pin MCU)</b> .....	<b>10</b>	Low-voltage Detection .....	43
<b>I/O Circuit Type</b> .....	<b>12</b>	I <sup>2</sup> C Timing .....	45
<b>Notes On Device Handling</b> .....	<b>15</b>	UART/SIO, Serial I/O Timing .....	48
<b>Pin Connection</b> .....	<b>15</b>	A/D Converter .....	50
<b>Block Diagram</b> .....	<b>16</b>	A/D Converter Electrical Characteristics .....	50
<b>CPU Core</b> .....	<b>17</b>	Notes on Using the A/D Converter .....	51
<b>I/O Map</b> .....	<b>18</b>	Definitions of A/D Converter Terms .....	52
<b>Interrupt Source Table</b> .....	<b>22</b>	Flash Memory Write/Erase Characteristics .....	54
<b>Electrical Characteristics</b> .....	<b>23</b>	<b>Sample Characteristics</b> .....	<b>55</b>
Absolute Maximum Ratings .....	23	<b>Mask Options</b> .....	<b>61</b>
Recommended Operating Conditions .....	25	<b>Ordering Information</b> .....	<b>62</b>
DC Characteristics .....	26	<b>Package Dimension</b> .....	<b>63</b>
AC Characteristics .....	29	<b>Major Changes</b> .....	<b>66</b>

**1. Product Line-up**

Part number	MB95F352E	MB95F353E	MB95F354E	MB95F352L	MB95F353L	MB95F354L
<b>Parameter</b>						
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Program ROM capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Low-voltage detection reset	Yes			No		
Reset input	Selected through software			Dedicated		
CPU functions	Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8 and 16 bits Minimum instruction execution time : 61.5 ns (with machine clock = 16.25 MHz) Interrupt processing time : 0.6 μs (with machine clock = 16.25 MHz)					
General-purpose I/O	I/O ports (Max): 22 CMOS I/O: 18 N-ch open drain: 3 CMOS input: 1			I/O ports (Max): 21 CMOS I/O: 18 N-ch open drain: 3		
Time-base timer	Interrupt cycle: 0.256 ms to 8.3 s (when external clock = 4 MHz)					
Hardware/software watchdog timer	Reset generation cycle - Main oscillation clock at 10 MHz: 105 ms (Min) The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
LIN-UART	A wide range of communication speeds can be selected by a dedicated reload timer. Clock-synchronous serial data transfer and clock-asynchronous serial data transfer is enabled. The LIN function can be used as a LIN master or a LIN slave.					
8/10-bit A/D converter	6 channels 8-bit resolution and 10-bit resolution can be chosen.					
8/16-bit composite timer	2 channels The timer can be configured as an "8-bit timer x 2 channels" or a "16-bit timer x 1 channel". It has built-in timer function, PWC function, PWM function and input capture function. Count clock: it can be selected from internal clocks (seven types) and external clocks. It can output square wave.					
External interrupt	6 channels Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) It can be used to wake up the device from different standby modes.					
On-chip debug	1-wire serial control It supports serial writing. (asynchronous mode)					

*(Continued)*

(Continued)

Part number	MB95F352E	MB95F353E	MB95F354E	MB95F352L	MB95F353L	MB95F354L
<b>Parameter</b>						
UART/SIO	1 channel (The channel can be used either as a UART/SIO channel or as an I <sup>2</sup> C channel.) Data transfer with UART/SIO is enabled. It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. It uses the NRZ type transfer format. LSB-first data transfer and MSB-first data transfer are available to use. Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
I <sup>2</sup> C	2 channels (One of the two channels can be used either as an I <sup>2</sup> C channel or as a UART/SIO channel.) Master/slave transmission and receiving It has the following functions: <ul style="list-style-type: none"> <li>• bus error function</li> <li>• arbitration function</li> <li>• transmission direction detection function</li> <li>• wake-up function</li> <li>• functions of generating and detecting repeated START conditions.</li> </ul>					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	It supports automatic programming, Embedded Algorithm, write/erase/erase-suspend/erase-resume commands. It has a flag indicating the completion of the operation of Embedded Algorithm. Number of write/erase cycles: 100000 Data retention time: 20 years Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-24P-M34 FPT-24P-M10 LCC-32P-M19					

**2. Packages and Corresponding Products**

<b>Part number</b> <b>Package</b>	<b>MB95F352E</b>	<b>MB95F353E</b>	<b>MB95F354E</b>	<b>MB95F352L</b>	<b>MB95F353L</b>	<b>MB95F354L</b>
FPT-24P-M34	O	O	O	O	O	O
FPT-24P-M10	O	O	O	O	O	O
LCC-32P-M19	O	O	O	O	O	O

O: Available

### 3. Differences Among Products and Notes On Product Selection

#### ■ Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/write.

For details of current consumption, see [“Electrical Characteristics”](#).

#### ■ Package

For details of information on each package, see [“Packages and Corresponding Products”](#) and [“Package Dimension”](#).

#### ■ Operating voltage

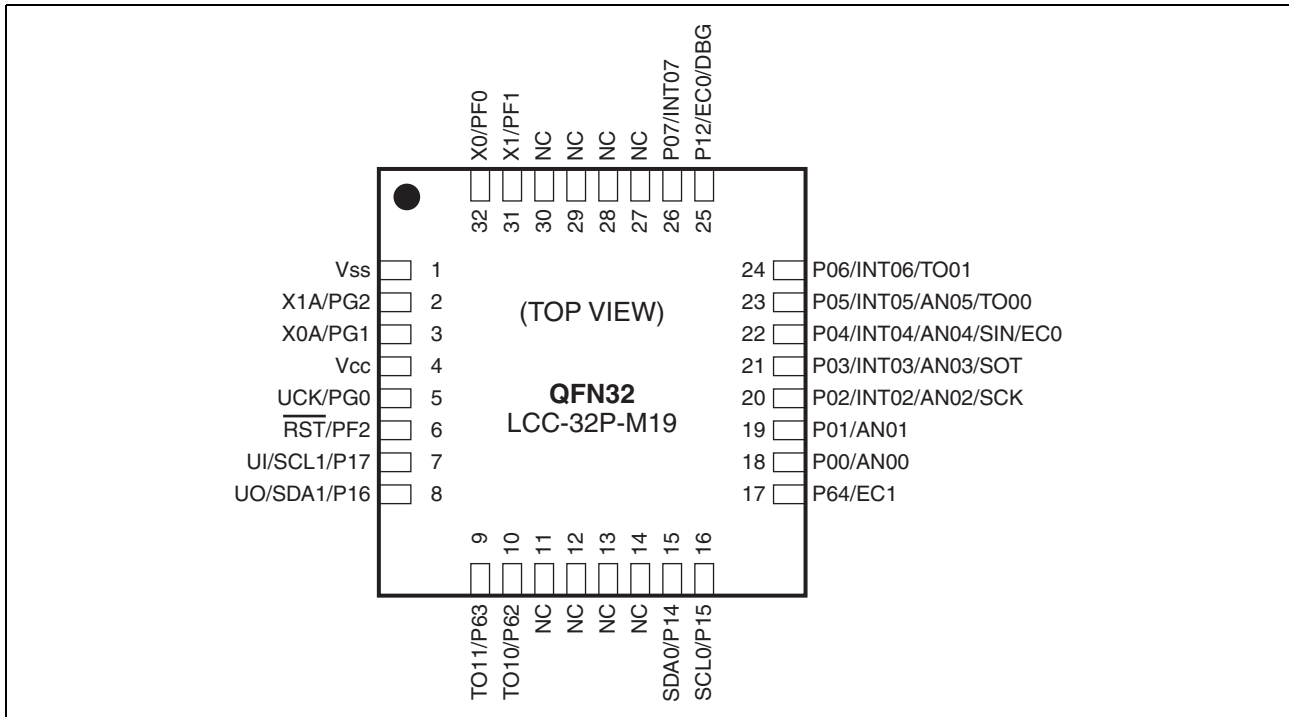
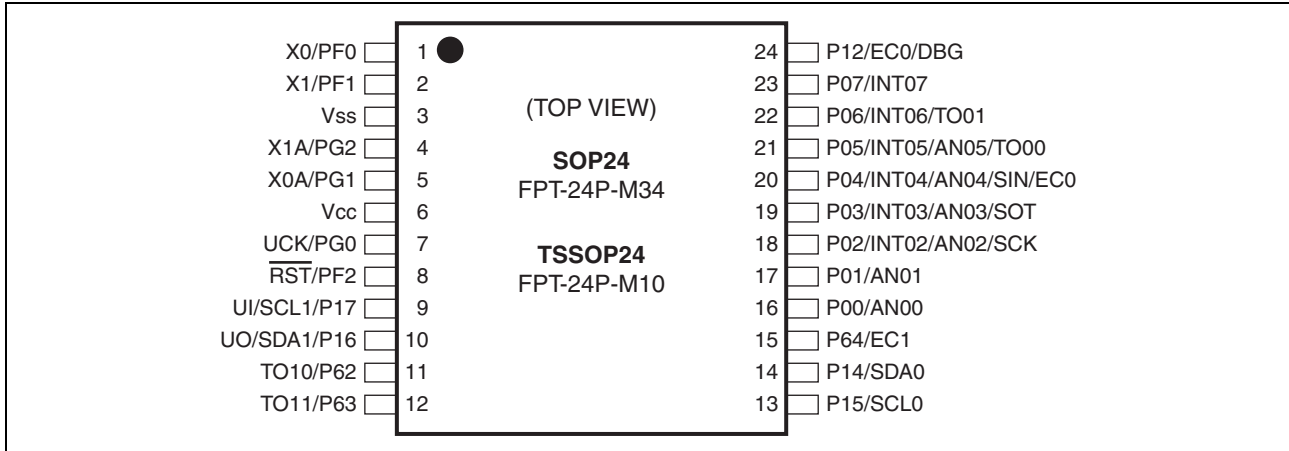
The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see [“Electrical Characteristics”](#)

#### ■ On-chip debug function

The on-chip debug function requires that  $V_{CC}$ ,  $V_{SS}$  and one serial wire be connected to an evaluation tool.

**4. Pin Assignment**



**5. Pin Description (24-pin MCU)**

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
3	V <sub>SS</sub>	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V <sub>CC</sub>	—	Power supply pin
7	PG0	G	General-purpose I/O port
	UCK		UART/SIO clock pin
8	PF2	A	General-purpose input port
	$\overline{\text{RST}}$		Reset pin Dedicated reset pin on MB95F352L/F353L/F354L
9	P17	J	General-purpose I/O port
	SCL1		I <sup>2</sup> C ch. 1 clock I/O pin
	UI		UART/SIO data input pin
10	P16	J	General-purpose I/O port
	SDA1		I <sup>2</sup> C ch. 1 data I/O pin
	UO		UART/SIO data output pin
11	P62	D	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
12	P63	D	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
13	P15	I	General-purpose I/O port
	SCL0		I <sup>2</sup> C ch. 0 clock I/O pin
14	P14	I	General-purpose I/O port
	SDA0		I <sup>2</sup> C ch. 0 data I/O pin
15	P64	D	General-purpose I/O port
	EC1		8/16-bit composite timer ch. 1 clock input pin
16	P00	E	General-purpose I/O port
	AN00		A/D converter analog input pin

*(Continued)*

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
17	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
18	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
19	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
20	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
21	P05	E	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
22	P06	G	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
23	P07	G	General-purpose I/O port
	INT07		External interrupt input pin
24	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

\*: For the I/O circuit types, see "I/O Circuit Type".

**6. Pin Description (32-pin MCU)**

Pin no.	Pin name	I/O circuit type*	Function
1	V <sub>SS</sub>	—	Power supply pin (GND)
2	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
3	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
4	V <sub>CC</sub>	—	Power supply pin
5	PG0	G	General-purpose I/O port
	UCK		UART/SIO clock pin
6	PF2	A	General-purpose input port
	$\overline{\text{RST}}$		Reset pin Dedicated reset pin on MB95F352L/F353L/F354L
7	P17	J	General-purpose I/O port
	SCL1		I <sup>2</sup> C ch. 1 clock I/O pin
	UI		UART/SIO data input pin
8	P16	J	General-purpose I/O port
	SDA1		I <sup>2</sup> C ch. 1 data I/O pin
	UO		UART/SIO data output pin
9	P63	D	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
10	P62	D	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
11	NC	—	It is an internally connected pin. Always leave it unconnected.
12	NC	—	It is an internally connected pin. Always leave it unconnected.
13	NC	—	It is an internally connected pin. Always leave it unconnected.
14	NC	—	It is an internally connected pin. Always leave it unconnected.
15	P14	I	General-purpose I/O port
	SDA0		I <sup>2</sup> C ch. 0 data I/O pin
16	P15	I	General-purpose I/O port
	SCL0		I <sup>2</sup> C ch. 0 clock I/O pin
17	P64	D	General-purpose I/O port
	EC1		8/16-bit composite timer ch. 1 clock input pin
18	P00	E	General-purpose I/O port
	AN00		A/D converter analog input pin


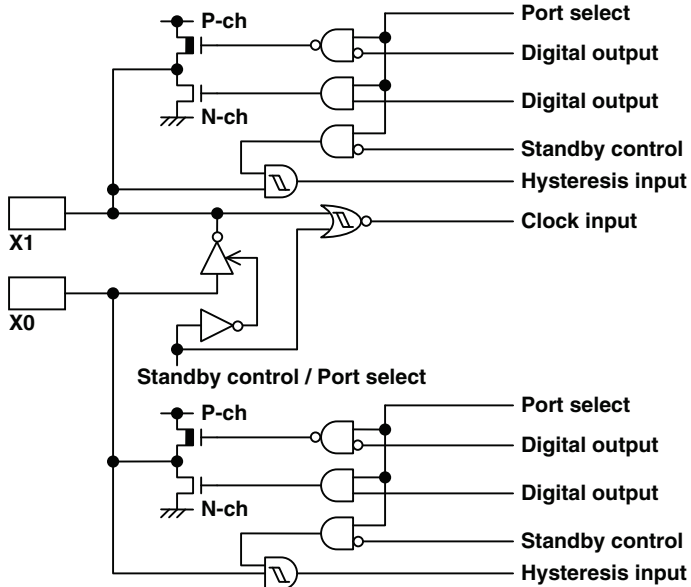
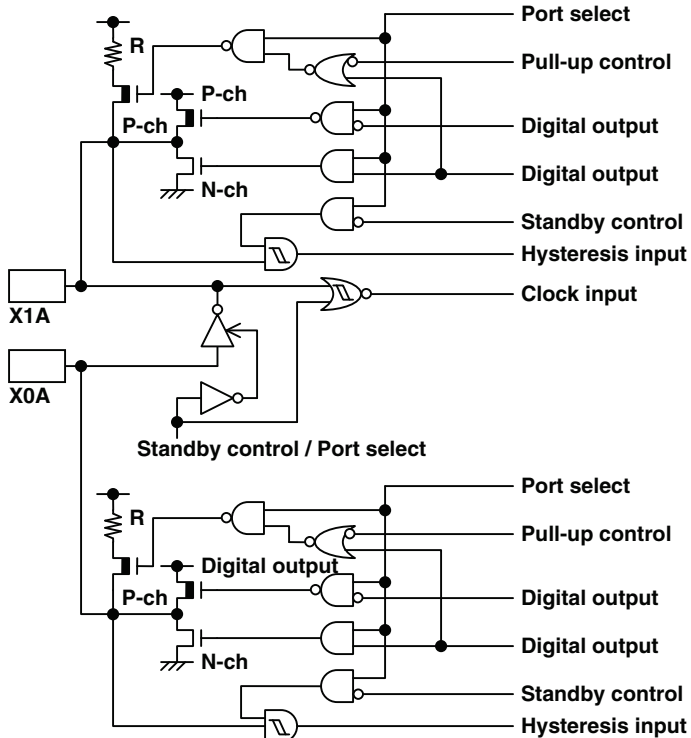
*(Continued)*

(Continued)

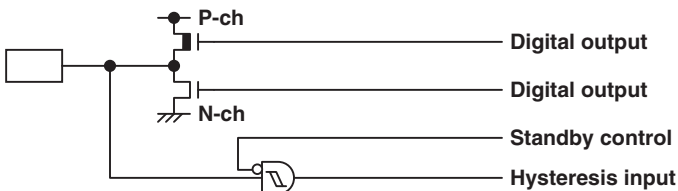
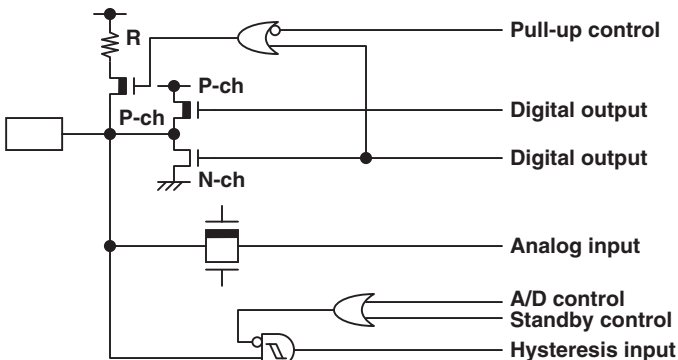
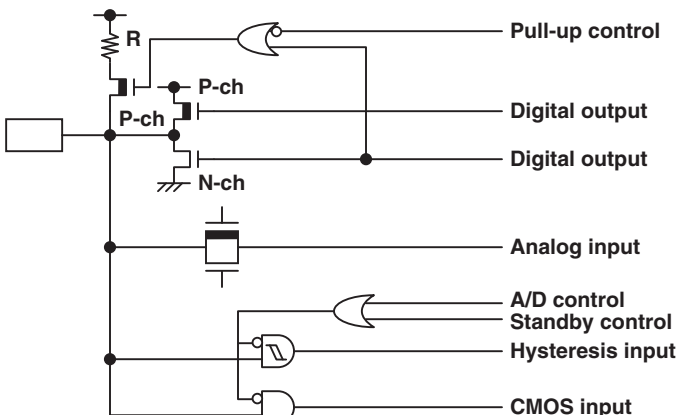
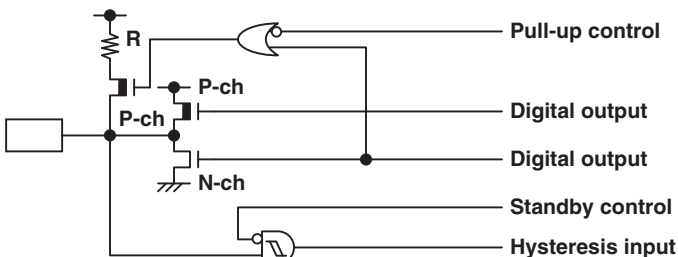
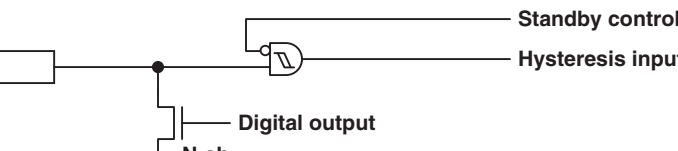
Pin no.	Pin name	I/O circuit type*	Function
19	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
20	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
21	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
22	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
23	P05	E	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
24	P06	G	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
25	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin
26	P07	G	General-purpose I/O port
	INT07		External interrupt input pin
27	NC	—	It is an internally connected pin. Always leave it unconnected.
28	NC	—	It is an internally connected pin. Always leave it unconnected.
29	NC	—	It is an internally connected pin. Always leave it unconnected.
30	NC	—	It is an internally connected pin. Always leave it unconnected.
31	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
32	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin

\*: For the I/O circuit types, see "I/O Circuit Type".

**7. I/O Circuit Type**

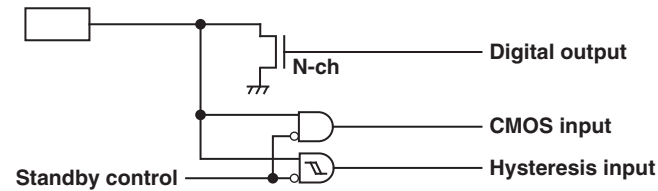
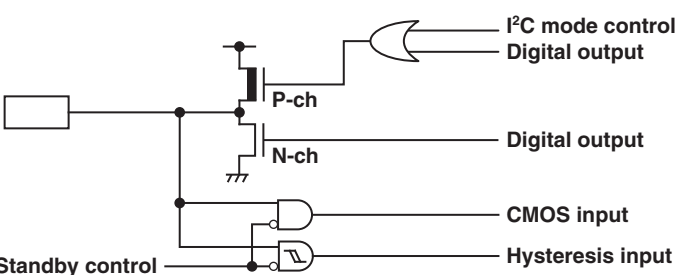
Type	Circuit	Remarks
A		<ul style="list-style-type: none"> <li>■ Hysteresis input</li> <li>■ Reset input</li> </ul>
B		<ul style="list-style-type: none"> <li>■ Oscillation circuit</li> <li>■ High-speed side</li> <li>■ Feedback resistance: approx. 1 MΩ</li> <li>■ CMOS output</li> <li>■ Hysteresis input</li> </ul>
C		<ul style="list-style-type: none"> <li>■ Oscillation circuit</li> <li>■ Low-speed side</li> <li>■ Feedback resistance: approx. 10 MΩ</li> <li>■ CMOS output</li> <li>■ Hysteresis input</li> <li>■ Pull-up control available</li> </ul>

*(Continued)*

Type	Circuit	Remarks
D		<ul style="list-style-type: none"> <li>■ CMOS output</li> <li>■ Hysteresis input</li> </ul>
E		<ul style="list-style-type: none"> <li>■ CMOS output</li> <li>■ Hysteresis input</li> <li>■ Pull-up control available</li> </ul>
F		<ul style="list-style-type: none"> <li>■ CMOS output</li> <li>■ Hysteresis input</li> <li>■ CMOS input</li> <li>■ Pull-up control available</li> </ul>
G		<ul style="list-style-type: none"> <li>■ CMOS output</li> <li>■ Hysteresis input</li> <li>■ Pull-up control available</li> </ul>
H		<ul style="list-style-type: none"> <li>■ N-ch open drain output</li> <li>■ Hysteresis input</li> </ul>

(Continued)

(Continued)

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> <li>■ N-ch open drain output</li> <li>■ Hysteresis input</li> <li>■ CMOS input</li> </ul>
J		<ul style="list-style-type: none"> <li>■ CMOS output</li> <li>■ Hysteresis input</li> <li>■ CMOS input</li> <li>■ N-ch open drain output in I<sup>2</sup>C mode</li> </ul>

## 8. Notes On Device Handling

### ■ Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than  $V_{CC}$  or a voltage lower than  $V_{SS}$  is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "14.1 Absolute Maximum Ratings" of "Electrical Characteristics" is applied to the  $V_{CC}$  pin or the  $V_{SS}$  pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

### ■ Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the  $V_{CC}$  power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in  $V_{CC}$  ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard  $V_{CC}$  value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

### ■ Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

## 9. Pin Connection

### ■ Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 k $\Omega$ . Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

### ■ Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the  $V_{CC}$  pin and the  $V_{SS}$  pin to the power supply and ground outside the device. In addition, connect the current supply source to the  $V_{CC}$  pin and the  $V_{SS}$  pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1  $\mu$ F as a bypass capacitor between the  $V_{CC}$  pin and the  $V_{SS}$  pin at a location close to this device.

### ■ DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the  $V_{CC}$  or  $V_{SS}$  pin when designing the layout of the printed circuit board.

The DBG pin should not stay at "L" level after power-on until the reset is released.

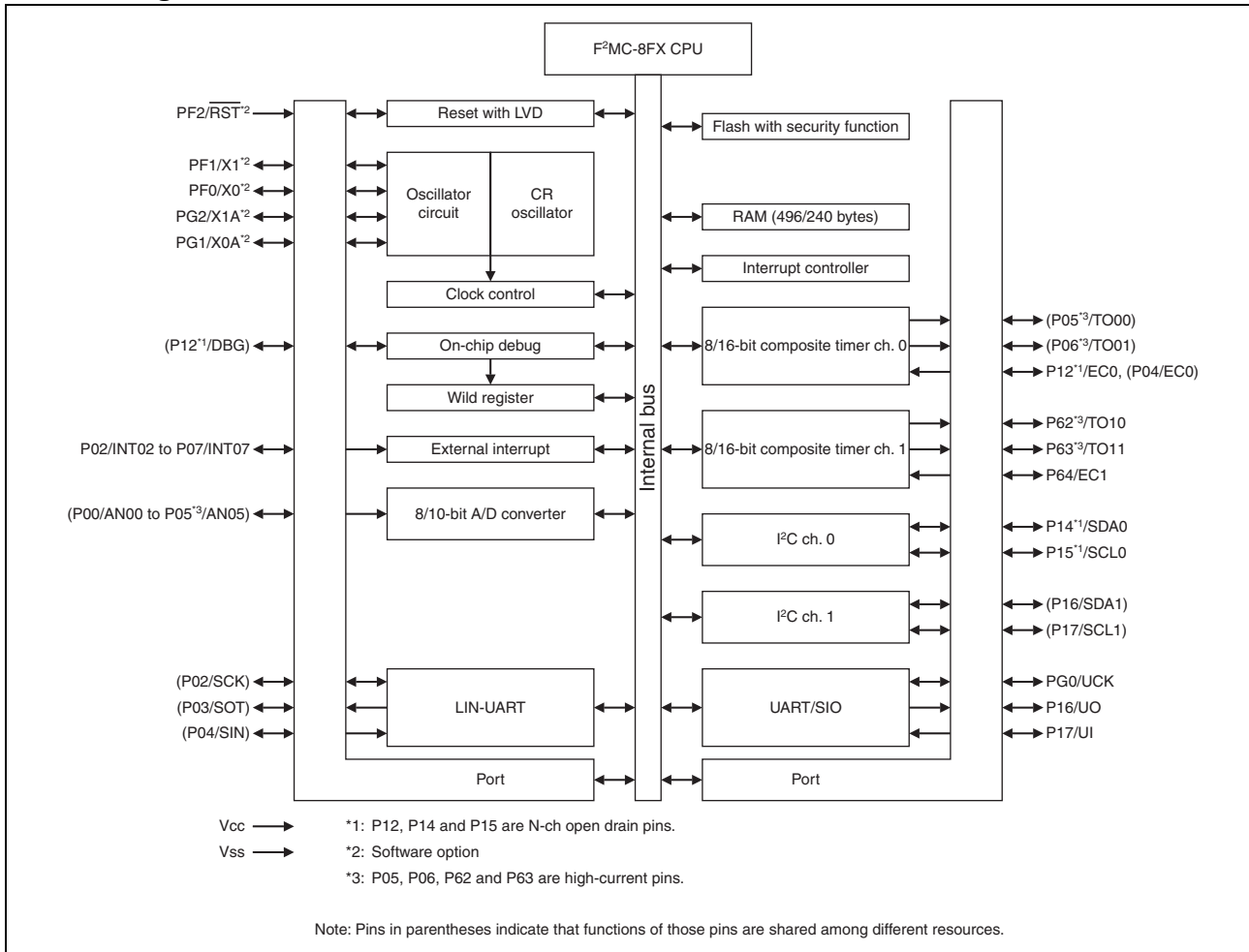
### ■ $\overline{RST}$ pin

Connect the  $\overline{RST}$  pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the  $\overline{RST}$  pin and the  $V_{CC}$  or  $V_{SS}$  pin when designing the layout of the printed circuit board.

The PF2/ $\overline{RST}$  pin functions as the reset input pin after power-on. The RSTEN bit in the SYSC register is used to switch the pin functions, the reset input function and the general-purpose I/O port function, of the PF2/ $\overline{RST}$  pin. However, only on MB95F352E/F353E/F354E can the pin functions be changed.

### 10. Block Diagram

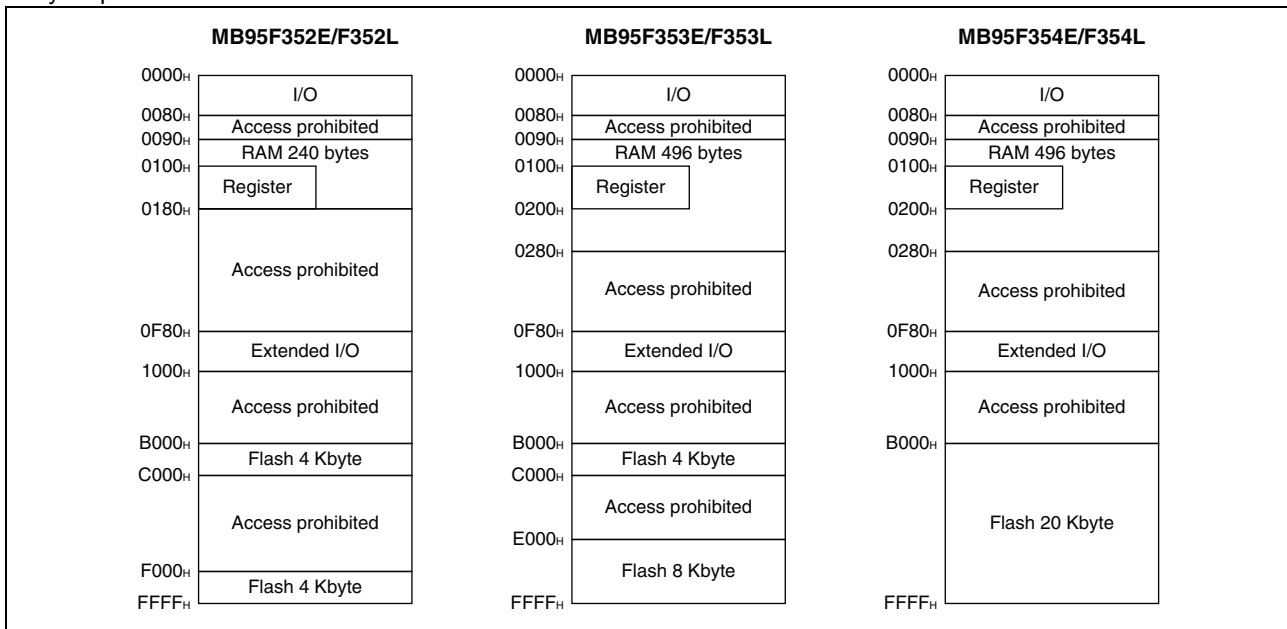


## 11. CPU Core

### ■ Memory Space

The memory space of the MB95350L Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95350L Series are shown below.

### ■ Memory Maps



**12. I/O Map**

Address	Register abbreviation	Register name	R/W	Initial value
0000 <sub>H</sub>	PDR0	Port 0 data register	R/W	00000000 <sub>B</sub>
0001 <sub>H</sub>	DDR0	Port 0 direction register	R/W	00000000 <sub>B</sub>
0002 <sub>H</sub>	PDR1	Port 1 data register	R/W	00000000 <sub>B</sub>
0003 <sub>H</sub>	DDR1	Port 1 direction register	R/W	00000000 <sub>B</sub>
0004 <sub>H</sub>	—	(Disabled)	—	—
0005 <sub>H</sub>	WATR	Oscillation stabilization wait time setting register	R/W	11111111 <sub>B</sub>
0006 <sub>H</sub>	—	(Disabled)	—	—
0007 <sub>H</sub>	SYCC	System clock control register	R/W	0000X011 <sub>B</sub>
0008 <sub>H</sub>	STBC	Standby control register	R/W	0000XXX <sub>B</sub>
0009 <sub>H</sub>	RSRR	Reset source register	R/W	XXXXXXXX <sub>B</sub>
000A <sub>H</sub>	TBTC	Time-base timer control register	R/W	00000000 <sub>B</sub>
000B <sub>H</sub>	WPCR	Watch prescaler control register	R/W	00000000 <sub>B</sub>
000C <sub>H</sub>	WDTC	Watchdog timer control register	R/W	00XX0000 <sub>B</sub>
000D <sub>H</sub>	SYCC2	System clock control register 2	R/W	XX100011 <sub>B</sub>
000E <sub>H</sub> to 0015 <sub>H</sub>	—	(Disabled)	—	—
0016 <sub>H</sub>	PDR6	Port 6 data register	R/W	00000000 <sub>B</sub>
0017 <sub>H</sub>	DDR6	Port 6 direction register	R/W	00000000 <sub>B</sub>
0018 <sub>H</sub> to 0027 <sub>H</sub>	—	(Disabled)	—	—
0028 <sub>H</sub>	PDRF	Port F data register	R/W	00000000 <sub>B</sub>
0029 <sub>H</sub>	DDRF	Port F direction register	R/W	00000000 <sub>B</sub>
002A <sub>H</sub>	PDRG	Port G data register	R/W	00000000 <sub>B</sub>
002B <sub>H</sub>	DDRG	Port G direction register	R/W	00000000 <sub>B</sub>
002C <sub>H</sub>	PUL0	Port 0 pull-up register	R/W	00000000 <sub>B</sub>
002D <sub>H</sub> to 0034 <sub>H</sub>	—	(Disabled)	—	—
0035 <sub>H</sub>	PULG	Port G pull-up register	R/W	00000000 <sub>B</sub>
0036 <sub>H</sub>	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000 <sub>B</sub>
0037 <sub>H</sub>	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000 <sub>B</sub>
0038 <sub>H</sub>	T11CR1	8/16-bit composite timer 11 status control register 1 ch. 1	R/W	00000000 <sub>B</sub>
0039 <sub>H</sub>	T10CR1	8/16-bit composite timer 10 status control register 1 ch. 1	R/W	00000000 <sub>B</sub>
003A <sub>H</sub> to 0048 <sub>H</sub>	—	(Disabled)	—	—
0049 <sub>H</sub>	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000 <sub>B</sub>
004A <sub>H</sub>	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000 <sub>B</sub>
004B <sub>H</sub>	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000 <sub>B</sub>

*(Continued)*

Address	Register abbreviation	Register name	R/W	Initial value
004C <sub>H</sub> , 004D <sub>H</sub>	—	(Disabled)	—	—
004E <sub>H</sub>	LVDR	LVD reset voltage selection ID register	R/W	00000000 <sub>B</sub>
004F <sub>H</sub>	LVDC	LVD interrupt control register	R/W	X000000X <sub>B</sub>
0050 <sub>H</sub>	SCR	LIN-UART serial control register	R/W	00000000 <sub>B</sub>
0051 <sub>H</sub>	SMR	LIN-UART serial mode register	R/W	00000000 <sub>B</sub>
0052 <sub>H</sub>	SSR	LIN-UART serial status register	R/W	00001000 <sub>B</sub>
0053 <sub>H</sub>	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000 <sub>B</sub>
0054 <sub>H</sub>	ESCR	LIN-UART extended status control register	R/W	00000100 <sub>B</sub>
0055 <sub>H</sub>	ECCR	LIN-UART extended communication control register	R/W	000000XX <sub>B</sub>
0056 <sub>H</sub>	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	00000000 <sub>B</sub>
0057 <sub>H</sub>	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	00100000 <sub>B</sub>
0058 <sub>H</sub>	SSR0	UART/SIO serial status and data register ch. 0	R/W	00000001 <sub>B</sub>
0059 <sub>H</sub>	TDR0	UART/SIO serial output data register ch. 0	R/W	00000000 <sub>B</sub>
005A <sub>H</sub>	RDR0	UART/SIO serial input data register ch. 0	R	00000000 <sub>B</sub>
005B <sub>H</sub> to 005F <sub>H</sub>	—	(Disabled)	—	—
0060 <sub>H</sub>	IBCR00	I <sup>2</sup> C bus control register 0 ch. 0	R/W	00000000 <sub>B</sub>
0061 <sub>H</sub>	IBCR10	I <sup>2</sup> C bus control register 1 ch. 0	R/W	00000000 <sub>B</sub>
0062 <sub>H</sub>	IBSR0	I <sup>2</sup> C bus status register ch. 0	R	00000000 <sub>B</sub>
0063 <sub>H</sub>	IDDR0	I <sup>2</sup> C data register ch. 0	R/W	00000000 <sub>B</sub>
0064 <sub>H</sub>	IAAR0	I <sup>2</sup> C address register ch. 0	R/W	00000000 <sub>B</sub>
0065 <sub>H</sub>	ICCR0	I <sup>2</sup> C clock control register ch. 0	R/W	00000000 <sub>B</sub>
0066 <sub>H</sub>	IBCR01	I <sup>2</sup> C bus control register 0 ch. 1	R/W	00000000 <sub>B</sub>
0067 <sub>H</sub>	IBCR11	I <sup>2</sup> C bus control register 1 ch. 1	R/W	00000000 <sub>B</sub>
0068 <sub>H</sub>	IBSR1	I <sup>2</sup> C bus status register ch. 1	R	00000000 <sub>B</sub>
0069 <sub>H</sub>	IDDR1	I <sup>2</sup> C data register ch. 1	R/W	00000000 <sub>B</sub>
006A <sub>H</sub>	IAAR1	I <sup>2</sup> C address register ch. 1	R/W	00000000 <sub>B</sub>
006B <sub>H</sub>	ICCR1	I <sup>2</sup> C clock control register ch. 1	R/W	00000000 <sub>B</sub>
006C <sub>H</sub>	ADC1	8/10-bit A/D converter control register 1	R/W	00000000 <sub>B</sub>
006D <sub>H</sub>	ADC2	8/10-bit A/D converter control register 2	R/W	00000000 <sub>B</sub>
006E <sub>H</sub>	ADDH	8/10-bit A/D converter data register (upper)	R/W	00000000 <sub>B</sub>
006F <sub>H</sub>	ADDL	8/10-bit A/D converter data register (lower)	R/W	00000000 <sub>B</sub>
0070 <sub>H</sub>	—	(Disabled)	—	—
0071 <sub>H</sub>	FSR2	Flash memory status register 2	R/W	00000000 <sub>B</sub>
0072 <sub>H</sub>	FSR	Flash memory status register	R/W	000X0000 <sub>B</sub>
0073 <sub>H</sub>	SWRE0	Flash memory sector write control register 0	R/W	00000000 <sub>B</sub>
0074 <sub>H</sub>	FSR3	Flash memory status register 3	R	00000000 <sub>B</sub>

*(Continued)*

Address	Register abbreviation	Register name	R/W	Initial value
0075 <sub>H</sub>	—	(Disabled)	—	—
0076 <sub>H</sub>	WREN	Wild register address compare enable register	R/W	00000000 <sub>B</sub>
0077 <sub>H</sub>	WROR	Wild register data test setting register	R/W	00000000 <sub>B</sub>
0078 <sub>H</sub>	—	Mirror of register bank pointer (RP) and mirror of direct bank pointer (DP)	—	—
0079 <sub>H</sub>	ILR0	Interrupt level setting register 0	R/W	11111111 <sub>B</sub>
007A <sub>H</sub>	ILR1	Interrupt level setting register 1	R/W	11111111 <sub>B</sub>
007B <sub>H</sub>	ILR2	Interrupt level setting register 2	R/W	11111111 <sub>B</sub>
007C <sub>H</sub>	ILR3	Interrupt level setting register 3	R/W	11111111 <sub>B</sub>
007D <sub>H</sub>	ILR4	Interrupt level setting register 4	R/W	11111111 <sub>B</sub>
007E <sub>H</sub>	ILR5	Interrupt level setting register 5	R/W	11111111 <sub>B</sub>
007F <sub>H</sub>	—	(Disabled)	—	—
0F80 <sub>H</sub>	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000 <sub>B</sub>
0F81 <sub>H</sub>	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000 <sub>B</sub>
0F82 <sub>H</sub>	WRDR0	Wild register data setting register ch. 0	R/W	00000000 <sub>B</sub>
0F83 <sub>H</sub>	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000 <sub>B</sub>
0F84 <sub>H</sub>	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000 <sub>B</sub>
0F85 <sub>H</sub>	WRDR1	Wild register data setting register ch. 1	R/W	00000000 <sub>B</sub>
0F86 <sub>H</sub>	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000 <sub>B</sub>
0F87 <sub>H</sub>	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000 <sub>B</sub>
0F88 <sub>H</sub>	WRDR2	Wild register data setting register ch. 2	R/W	00000000 <sub>B</sub>
0F89 <sub>H</sub> to 0F91 <sub>H</sub>	—	(Disabled)	—	—
0F92 <sub>H</sub>	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000 <sub>B</sub>
0F93 <sub>H</sub>	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000 <sub>B</sub>
0F94 <sub>H</sub>	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000 <sub>B</sub>
0F95 <sub>H</sub>	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000 <sub>B</sub>
0F96 <sub>H</sub>	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000 <sub>B</sub>
0F97 <sub>H</sub>	T11CR0	8/16-bit composite timer 11 status control register 0 ch. 1	R/W	00000000 <sub>B</sub>
0F98 <sub>H</sub>	T10CR0	8/16-bit composite timer 10 status control register 0 ch. 1	R/W	00000000 <sub>B</sub>
0F99 <sub>H</sub>	T11DR	8/16-bit composite timer 11 data register ch. 1	R/W	00000000 <sub>B</sub>
0F9A <sub>H</sub>	T10DR	8/16-bit composite timer 10 data register ch. 1	R/W	00000000 <sub>B</sub>
0F9B <sub>H</sub>	TMCR1	8/16-bit composite timer 10/11 timer mode control register ch. 1	R/W	00000000 <sub>B</sub>
0F9C <sub>H</sub> to 0FBB <sub>H</sub>	—	(Disabled)	—	—

*(Continued)*

*(Continued)*

Address	Register abbreviation	Register name	R/W	Initial value
0FBC <sub>H</sub>	BGR1	LIN-UART baud rate generator register 1	R/W	00000000 <sub>B</sub>
0FBD <sub>H</sub>	BGR0	LIN-UART baud rate generator register 0	R/W	00000000 <sub>B</sub>
0FBE <sub>H</sub>	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	00000000 <sub>B</sub>
0FBF <sub>H</sub>	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	00000000 <sub>B</sub>
0FC0 <sub>H</sub> to 0FC2 <sub>H</sub>	—	(Disabled)	—	—
0FC3 <sub>H</sub>	AIDRL	A/D input disable register (lower)	R/W	00000000 <sub>B</sub>
0FC4 <sub>H</sub> to 0FE3 <sub>H</sub>	—	(Disabled)	—	—
0FE4 <sub>H</sub>	CRT <sub>H</sub>	Main CR clock trimming register (upper)	R/W	0XXXXXXXX <sub>B</sub>
0FE5 <sub>H</sub>	CRT <sub>L</sub>	Main CR clock trimming register (lower)	R/W	00XXXXXXXX <sub>B</sub>
0FE6 <sub>H</sub> , 0FE7 <sub>H</sub>	—	(Disabled)	—	—
0FE8 <sub>H</sub>	SYSC	System configuration register	R/W	11000001 <sub>B</sub>
0FE9 <sub>H</sub>	CMCR	Clock monitoring control register	R/W	00000000 <sub>B</sub>
0FEA <sub>H</sub>	CMDR	Clock monitoring data register	R	00000000 <sub>B</sub>
0FEB <sub>H</sub>	WDTH	Watchdog timer selection ID register (upper)	R	XXXXXXXX <sub>B</sub>
0FEC <sub>H</sub>	WDTL	Watchdog timer selection ID register (lower)	R	XXXXXXXX <sub>B</sub>
0FED <sub>H</sub>	—	(Disabled)	—	—
0FEE <sub>H</sub>	ILSR	Input level select register	R/W	00000000 <sub>B</sub>
0FEF <sub>H</sub> to 0FFF <sub>H</sub>	—	(Disabled)	—	—

**R/W access symbols**



- R/W : Readable / Writable
- R : Read only
- W : Write only

**Initial value symbols**

- 0 : The initial value of this bit is "0".
- 1 : The initial value of this bit is "1".
- X : The initial value of this bit is indeterminate.

**Note:** Do not write to an address that is "(Disabled)". If a "(Disabled)" address is read, an indeterminate value is returned.

**13. Interrupt Source Table**

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	FFFA <sub>H</sub>	FFFB <sub>H</sub>	L00 [1:0]	<div style="text-align: center;">High</div>   <div style="text-align: center;">Low</div>
External interrupt ch. 5	IRQ01	FFF8 <sub>H</sub>	FFF9 <sub>H</sub>	L01 [1:0]	
External interrupt ch. 2	IRQ02	FFF6 <sub>H</sub>	FFF7 <sub>H</sub>	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	FFF4 <sub>H</sub>	FFF5 <sub>H</sub>	L03 [1:0]	
External interrupt ch. 7					
LVD interrupt	IRQ04	FFF2 <sub>H</sub>	FFF3 <sub>H</sub>	L04 [1:0]	
UART/SIO ch. 0					
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0 <sub>H</sub>	FFF1 <sub>H</sub>	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE <sub>H</sub>	FFEF <sub>H</sub>	L06 [1:0]	
LIN-UART (reception)	IRQ07	FFEC <sub>H</sub>	FFED <sub>H</sub>	L07 [1:0]	
LIN-UART (transmission)	IRQ08	FFEA <sub>H</sub>	FFEB <sub>H</sub>	L08 [1:0]	
—	IRQ09	FFE8 <sub>H</sub>	FFE9 <sub>H</sub>	L09 [1:0]	
I <sup>2</sup> C ch. 1	IRQ10	FFE6 <sub>H</sub>	FFE7 <sub>H</sub>	L10 [1:0]	
—	IRQ11	FFE4 <sub>H</sub>	FFE5 <sub>H</sub>	L11 [1:0]	
—	IRQ12	FFE2 <sub>H</sub>	FFE3 <sub>H</sub>	L12 [1:0]	
—	IRQ13	FFE0 <sub>H</sub>	FFE1 <sub>H</sub>	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	FFDE <sub>H</sub>	FFDF <sub>H</sub>	L14 [1:0]	
—	IRQ15	FFDC <sub>H</sub>	FFDD <sub>H</sub>	L15 [1:0]	
I <sup>2</sup> C ch. 0	IRQ16	FFDA <sub>H</sub>	FFDB <sub>H</sub>	L16 [1:0]	
—	IRQ17	FFD8 <sub>H</sub>	FFD9 <sub>H</sub>	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6 <sub>H</sub>	FFD7 <sub>H</sub>	L18 [1:0]	
Time-base timer	IRQ19	FFD4 <sub>H</sub>	FFD5 <sub>H</sub>	L19 [1:0]	
Watch prescaler	IRQ20	FFD2 <sub>H</sub>	FFD3 <sub>H</sub>	L20 [1:0]	
—	IRQ21	FFD0 <sub>H</sub>	FFD1 <sub>H</sub>	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	FFCE <sub>H</sub>	FFCF <sub>H</sub>	L22 [1:0]	
Flash memory	IRQ23	FFCC <sub>H</sub>	FFCD <sub>H</sub>	L23 [1:0]	

## 14. Electrical Characteristics

### 14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage* <sup>1</sup>	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	
Input voltage* <sup>1</sup>	$V_{I1}$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	Other than P14 and P15* <sup>2</sup>
	$V_{I2}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	P14 and P15* <sup>2</sup>
Output voltage* <sup>1</sup>	$V_O$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	* <sup>2</sup>
Maximum clamp current	$I_{CLAMP}$	-2	+2	mA	Applicable to specific pins* <sup>3</sup>
Total maximum clamp current	$\Sigma I_{CLAMP} $	—	20	mA	Applicable to specific pins* <sup>3</sup>
"L" level maximum output current	$I_{OL1}$	—	15	mA	Other than P05, P06, P62 and P63
	$I_{OL2}$	—	15		P05, P06, P62 and P63
"L" level average current	$I_{OLAV1}$	—	4	mA	Other than P05, P06, P62 and P63 Average output current = operating current $\times$ operating ratio (1 pin)
	$I_{OLAV2}$	—	12		P05, P06, P62 and P63 Average output current = operating current $\times$ operating ratio (1 pin)
"L" level total maximum output current	$\Sigma I_{OL}$	—	100	mA	
"L" level total average output current	$\Sigma I_{OLAV}$	—	50	mA	Total average output current = operating current $\times$ operating ratio (Total number of pins)
"H" level maximum output current	$I_{OH1}$	—	-15	mA	Other than P05, P06, P62 and P63
	$I_{OH2}$	—	-15		P05, P06, P62 and P63
"H" level average current	$I_{OHAV1}$	—	-4	mA	Other than P05, P06, P62 and P63 Average output current = operating current $\times$ operating ratio (1 pin)
	$I_{OHAV2}$	—	-8		P05, P06, P62 and P63 Average output current = operating current $\times$ operating ratio (1 pin)
"H" level total maximum output current	$\Sigma I_{OH}$	—	-100	mA	
"H" level total average output current	$\Sigma I_{OHAV}$	—	-50	mA	Total average output current = operating current $\times$ operating ratio (Total number of pins)
Power consumption	$P_d$	—	320	mW	
Operating temperature	$T_A$	-40	+85	°C	
Storage temperature	$T_{stg}$	-55	+150	°C	

*(Continued)*

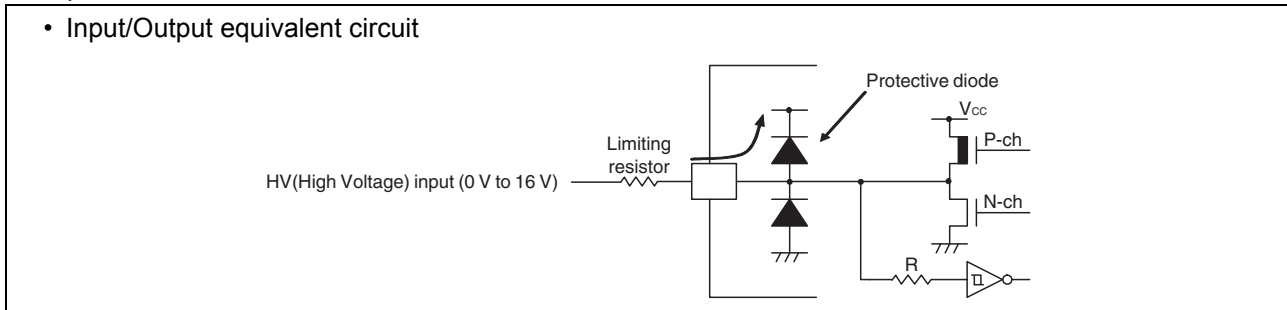
(Continued)

\*1: The parameter is based on  $V_{SS} = 0.0\text{ V}$ .

\*2:  $V_{I1}$ ,  $V_{I2}$  and  $V_O$  must not exceed  $V_{CC} + 0.3\text{ V}$ .  $V_{I1}$  and  $V_{I2}$  must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the  $I_{CLAMP}$  rating is used instead of the  $V_{I1}$  and  $V_{I2}$  ratings.

\*3: Applicable to the following pins: P00 to P07, P15, P16, P62 to P64, PF0, PF1, PG0 to PG2

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the  $V_{CC}$  voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the  $V_{CC}$  pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

**14.2 Recommended Operating Conditions**

 (V<sub>SS</sub> = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V <sub>CC</sub>	1.8*1+2*3	3.6	V	In normal operation, T <sub>A</sub> = -10°C to +85°C	Other than on-chip debug mode
		2.0	3.6		In normal operation, T <sub>A</sub> = -40°C to +85°C	
		1.5	3.6		Hold condition in stop mode	
		2.7	3.6		In normal operation	On-chip debug mode
		1.5	3.6		Hold condition in stop mode	
		Operating temperature	T <sub>A</sub>		-40	+85
+5	+35			On-chip debug mode		

\*1: This value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

\*2: This value is initially 2.03 V when the low-voltage detection reset is used.

\*3: The threshold voltage can be set to 2.03 V, 2.55 V or 3.10 V by using the software.

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

**14.3 DC Characteristics**
 $(V_{CC} = 2.7\text{ V to } 3.6\text{ V}, V_{SS} = 0.0\text{ V}, T_A = -40^\circ\text{C to } +85^\circ\text{C})$ 

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	$V_{IH1}$	P04, P16, P17	*1	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	When CMOS input level is selected
	$V_{IH2}$	P14, P15	*1	$0.7 V_{CC}$	—	$V_{SS} + 5.5$	V	When CMOS input level is selected
	$V_{IHS1}$	P00 to P07, P12, P16, P17, P60 to P64, PF0, PF1, PG0 to PG2	*1	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
	$V_{IHS2}$	P14, P15	*1	$0.8 V_{CC}$	—	$V_{SS} + 5.5$	V	Hysteresis input
	$V_{IHM}$	PF2	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
"L" level input voltage	$V_{IL}$	P04, P14 to P17	*1	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	When CMOS input level is selected
	$V_{ILS}$	P00 to P07, P12, P14 to P17, P62 to P64, PF0, PF1, PG0 to PG2	*1	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Hysteresis input
	$V_{ILM}$	PF2	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	Hysteresis input
Open-drain output application voltage	$V_{D1}$	P12	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$	V	
	$V_{D2}$	P14, P15	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$	V	
	$V_{D3}$	P16, P17	—	$V_{SS} - 0.3$	—	$V_{SS} + 3.6$	V	In I <sup>2</sup> C mode
"H" level output voltage	$V_{OH1}$	Output pins other than P05, P06, P12, P62, P63	$I_{OH} = -4\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
	$V_{OH2}$	P05, P06, P62 and P63	$I_{OH} = -8\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
"L" level output voltage	$V_{OL1}$	Output pins other than P05, P06, P62, P63	$I_{OL} = 4\text{ mA}$	—	—	0.4	V	
	$V_{OL2}$	P05, P06, P62, P63	$I_{OL} = 12\text{ mA}$	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	$I_{LI}$	All input pins	$0.0\text{ V} < V_I < V_{CC}$	-5	—	+5	$\mu\text{A}$	When pull-up resistance is disabled
Pull-up resistance	$R_{PULL}$	P00 to P07, PG1, PG2	$V_I = 0\text{ V}$	25	50	100	$\text{k}\Omega$	When pull-up resistance is enabled
Input capacitance	$C_{IN}$	Other than $V_{CC}$ and $V_{SS}$	$f = 1\text{ MHz}$	—	5	15	pF	

*(Continued)*

$(V_{CC} = 1.8\text{ V to }3.6\text{ V}, V_{SS} = 0.0\text{ V}, T_A = -40^\circ\text{C to }+85^\circ\text{C})$ 

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks		
				Min	Typ <sup>*3</sup>	Max				
Power supply current <sup>*2</sup>	I <sub>CC</sub>	V <sub>CC</sub> (External clock operation)	F <sub>CH</sub> = 32 MHz F <sub>MP</sub> = 16 MHz Main clock mode (divided by 2)	—	11.2	20	mA	Flash memory product (except writing and erasing)		
				—	26.2	38		Flash memory product (at writing and erasing)		
				—	13.3	23.4		At A/D conversion		
	I <sub>CCS</sub>		F <sub>CH</sub> = 32 MHz F <sub>MP</sub> = 16 MHz Main sleep mode (divided by 2)	—	5.2	9.6	μA			
	I <sub>CCL</sub>		F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 16 kHz Subclock mode (divided by 2) T <sub>A</sub> = +25°C	—	15	35				
	I <sub>CCLS</sub>		F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 16 kHz Subsleep mode (divided by 2) T <sub>A</sub> = +25°C	—	5	15				
	I <sub>CCT</sub>		F <sub>CL</sub> = 32 kHz Watch mode Main stop mode T <sub>A</sub> = +25°C	—	1	10	μA			
	I <sub>CCMCR</sub>		V <sub>CC</sub>	F <sub>CRH</sub> = 12.5 MHz F <sub>MP</sub> = 12.5 MHz Main CR clock mode	—	9		15	mA	
	I <sub>CCSCR</sub>			Sub-CR clock mode (divided by 2) T <sub>A</sub> = +25°C	—	77		160		μA
	I <sub>CCTS</sub>		V <sub>CC</sub> (External clock operation)	F <sub>CH</sub> = 32 MHz Time-base timer mode	—	1.1	3	mA		
I <sub>CCH</sub>	Substop mode T <sub>A</sub> = +25°C	—		0.1	5	μA				

*(Continued)*

(Continued)

 $(V_{CC} = 1.8 \text{ V to } 3.6 \text{ V}, V_{SS} = 0.0 \text{ V}, T_A = -40^\circ\text{C to } +85^\circ\text{C})$ 

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ <sup>*3</sup>	Max		
Power supply current <sup>*2</sup>	$I_{LVD}$	$V_{CC}$	Current consumption for low-voltage detection circuit only	—	6.4	32	$\mu\text{A}$	
	$I_{CRH}$		Current consumption for the main CR oscillator	—	0.25	0.6	$\text{mA}$	
	$I_{CRL}$		Current consumption for the sub-CR oscillator oscillating at 100 kHz	—	20	72	$\mu\text{A}$	

\*1: The input levels of P04 and P14 to P17 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

\*2: • The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit ( $I_{LVD}$ ) to one of the value from  $I_{CC}$  to  $I_{CCH}$ . In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators ( $I_{CRH}$ ,  $I_{CRL}$ ) and a specified value. In on-chip debug mode, the CR oscillator ( $I_{CRH}$ ) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.

■ See "AC Characteristics: Clock Timing" for  $F_{CH}$  and  $F_{CL}$ .

■ See "AC Characteristics: Source Clock/Machine Clock" for  $F_{MP}$  and  $F_{MPL}$ .

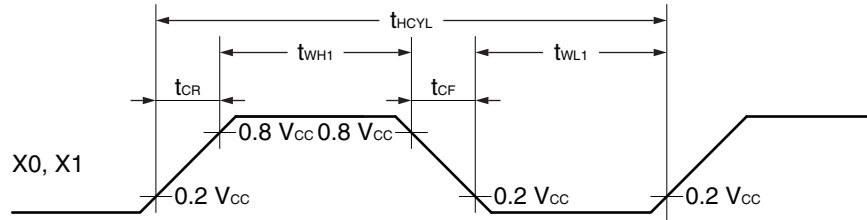
\*3:  $V_{CC} = 3.0 \text{ V}, T_A = +25^\circ\text{C}$

**14.4 AC Characteristics**
**14.4.1 Clock Timing**
 $(V_{CC} = 1.8\text{ V to } 3.6\text{ V}, V_{SS} = 0.0\text{ V}, T_A = -40^\circ\text{C to } +85^\circ\text{C})$ 

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks		
				Min	Typ	Max				
Clock frequency	F <sub>CH</sub>	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used		
		X0	X1: open	1	—	12	MHz	When the main external clock is used		
		X0, X1	*	1	—	32.5	MHz			
	F <sub>CRH</sub>	—	—	—	12.25	12.5	12.75	MHz	When the main CR clock is used T <sub>A</sub> = -10 °C to +85 °C	
					9.8	10	10.2	MHz		
					7.84	8	8.16	MHz		
					0.98	1	1.02	MHz		
		—	—	—	—	12.1875	12.5	12.8125	MHz	When the main CR clock is used T <sub>A</sub> = -40 °C to -10 °C
						9.75	10	10.25	MHz	
						7.8	8	8.2	MHz	
F <sub>CL</sub>	X0A, X1A	—	—	—	32.768	—	kHz	When the sub-oscillation circuit or the sub-external clock is used		
				F <sub>CRL</sub>	—	—	50		100	200
Clock cycle time	t <sub>H CYL</sub>	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used		
		X0	X1: open	83.4	—	1000	ns	When the main external clock is used		
		X0, X1	*	30.8	—	1000	ns			
	t <sub>L CYL</sub>	X0A, X1A	—	—	30.5	—	μs	When the sub-oscillation circuit or the sub-external clock is used		
Input clock pulse width	t <sub>WH1</sub>	X0	X1: open	33.4	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%.		
	t <sub>WL1</sub>	X0, X1	*	12.4	—	—	ns			
	t <sub>WH2</sub>	X0A	—	—	15.2	—	μs			
Input clock rise time and fall time	t <sub>CR</sub>	X0	X1: open	—	—	5	ns	When the external clock is used		
	t <sub>CF</sub>	X0, X1	*	—	—	5	ns			
CR oscillation start time	t <sub>CRHWK</sub>	—	—	—	—	250	μs	When the main CR clock is used		
	t <sub>CRLWK</sub>	—	—	—	—	10	μs	When the sub-CR clock is used		

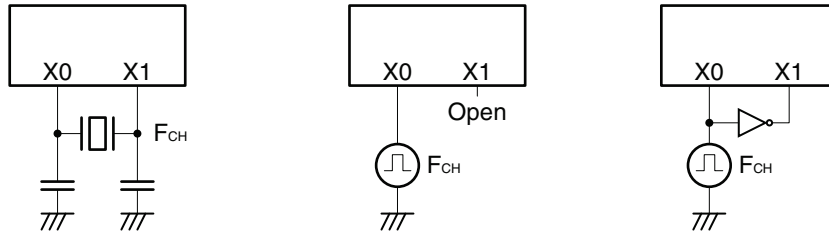
\*: The external clock signal is input to X0 and the inverted external clock signal to X1.

- Input waveform generated when an external clock (main clock) is used

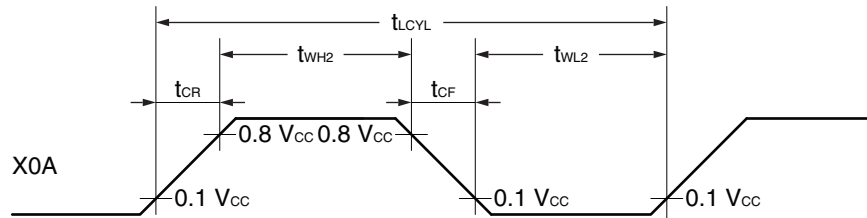


- Figure of main clock input port external connection

When a crystal oscillator or a ceramic oscillator is used      When the external clock is used (X1 is open)      When the external clock is used



- Input waveform generated when an external clock (subclock) is used



- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used      When the external clock is used



**14.4.2 Source Clock/Machine Clock**

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t <sub>SCLK</sub>	—	61.5	—	2000	ns	When the main external clock is used Min: F <sub>CH</sub> = 32.5 MHz, divided by 2 Max: F <sub>CH</sub> = 1 MHz, divided by 2
			80	—	1000	ns	When the main CR clock is used Min: F <sub>CRH</sub> = 12.5 MHz Max: F <sub>CRH</sub> = 1 MHz
			—	61	—	μs	When the sub-oscillation clock is used F <sub>CL</sub> = 32.768 kHz, divided by 2
			—	20	—	μs	When the sub-CR clock is used F <sub>CRL</sub> = 100 kHz, divided by 2
Source clock frequency	F <sub>SP</sub>	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			1	—	12.5	MHz	When the main CR clock is used
	—		16.384	—	kHz	When the sub-oscillation clock is used	
	F <sub>SPL</sub>		—	50	—	kHz	When the sub-CR clock is used F <sub>CRL</sub> = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t <sub>MCLK</sub>	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F <sub>SP</sub> = 16.25 MHz, no division Max: F <sub>SP</sub> = 0.5 MHz, divided by 16
			80	—	16000	ns	When the main CR clock is used Min: F <sub>SP</sub> = 12.5 MHz Max: F <sub>SP</sub> = 1 MHz, divided by 16
			61	—	976.5	μs	When the sub-oscillation clock is used Min: F <sub>SPL</sub> = 16.384 kHz, no division Max: F <sub>SPL</sub> = 16.384 kHz, divided by 16
			20	—	320	μs	When the sub-CR clock is used Min: F <sub>SPL</sub> = 50 kHz, no division Max: F <sub>SPL</sub> = 50 kHz, divided by 16
Machine clock frequency	F <sub>MP</sub>	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	12.5	MHz	When the main CR clock is used
	1.024		—	16.384	kHz	When the sub-oscillation clock is used	
	F <sub>MPL</sub>		3.125	—	50	kHz	When the sub-CR clock is used F <sub>CRL</sub> = 100 kHz

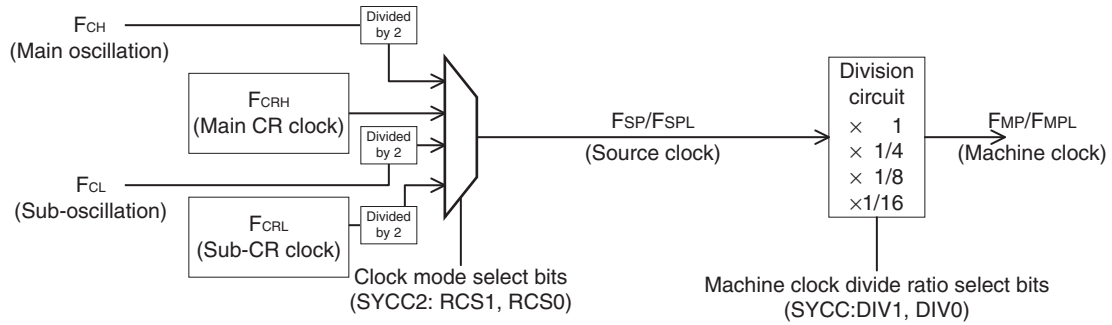
\*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio selection bits (SYCC:DIV1, DIV0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio selection bits (SYCC:DIV1, DIV0]). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

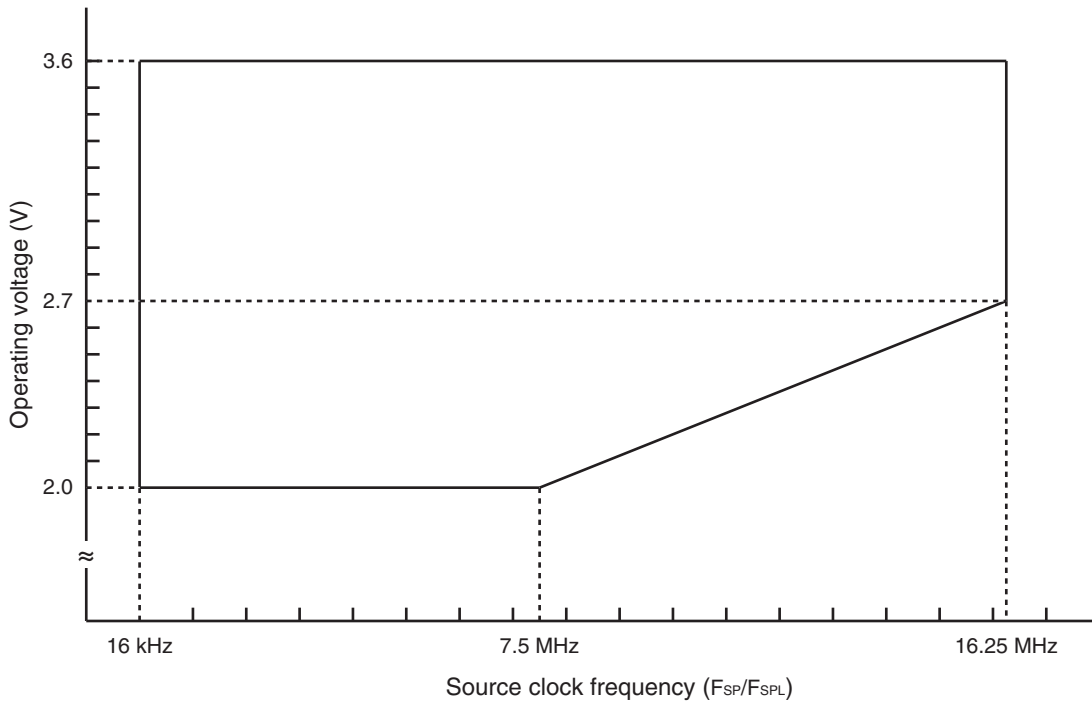
\*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

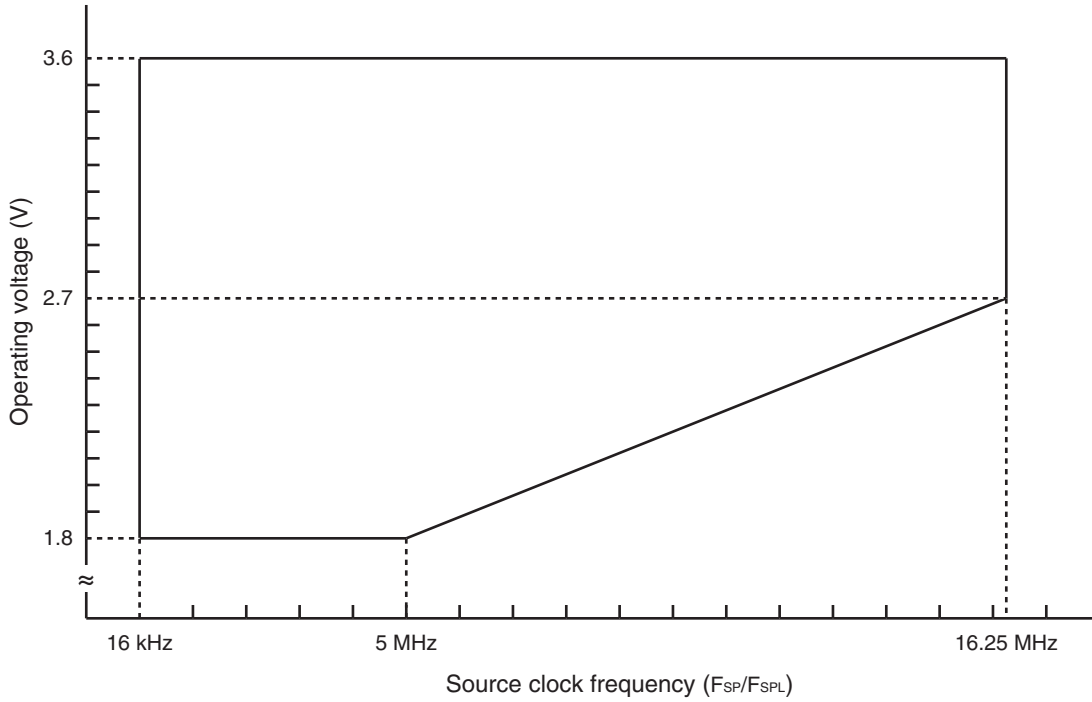
• Schematic diagram of the clock generation block



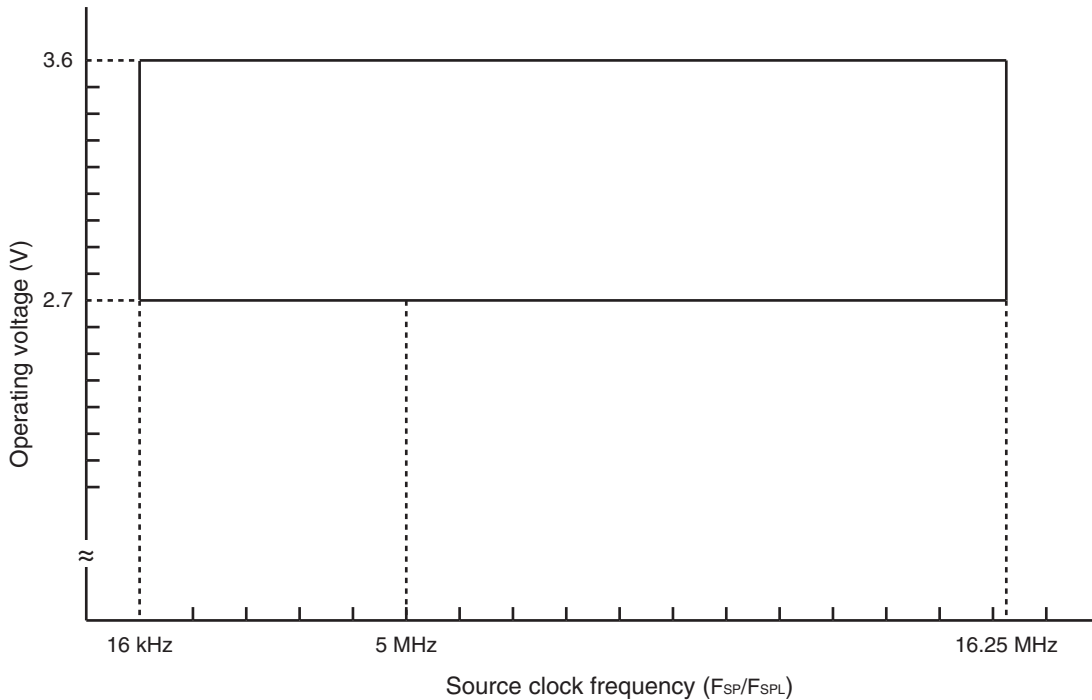
• Operating voltage - Operating frequency (When  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )  
Without the on-chip debug function



- Operating voltage - Operating frequency (When  $T_A = -10^\circ\text{C}$  to  $+85^\circ\text{C}$ )  
Without the on-chip debug function



- Operating voltage - Operating frequency (When  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )  
With the on-chip debug function



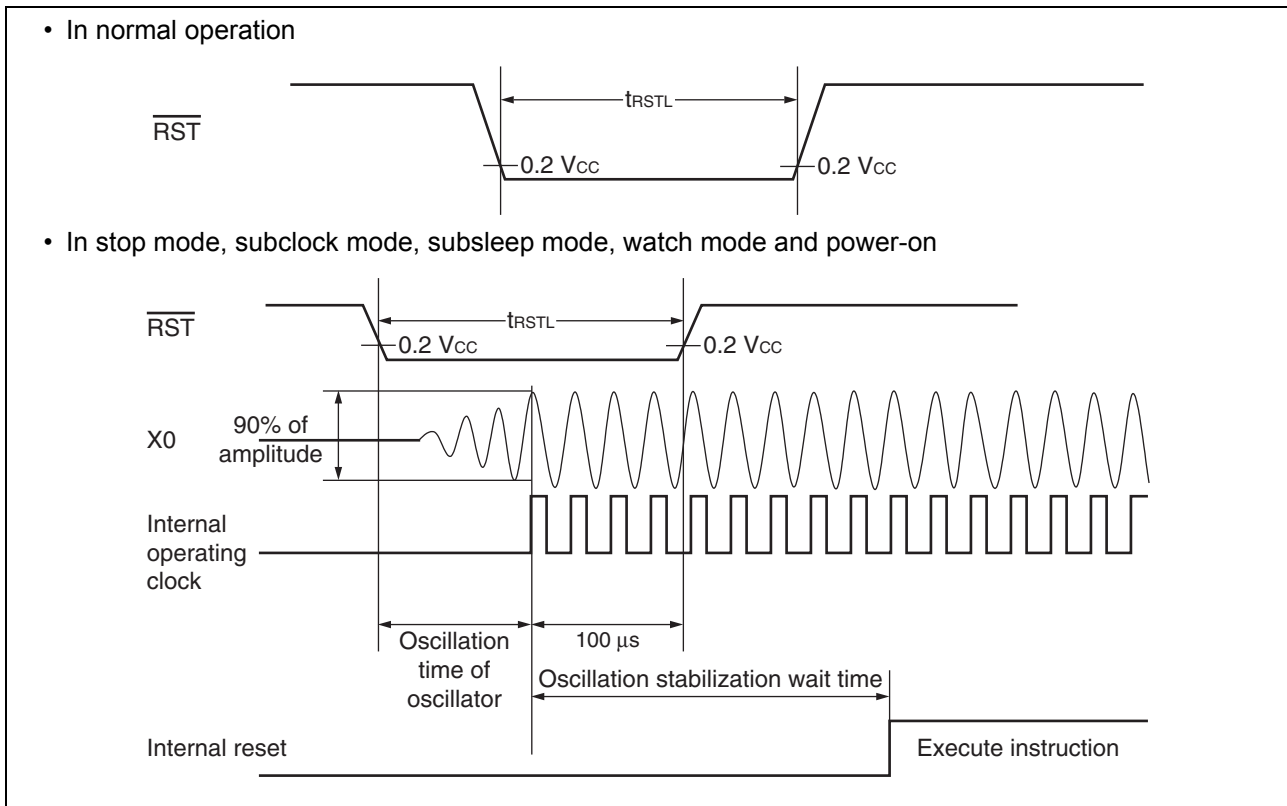
14.4.3 External Reset

( $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{\text{RST}}$ "L" level pulse width	$t_{\text{RSTL}}$	$2 t_{\text{MCLK}}^{*1}$	—	ns	In normal operation
		Oscillation time of the oscillator <sup>*2</sup> + 100	—	$\mu\text{s}$	In stop mode, subclock mode, sub-sleep mode, watch mode, and power-on
		100	—	$\mu\text{s}$	In time-base timer mode

\*1: See "Source Clock/Machine Clock" for  $t_{\text{MCLK}}$ .

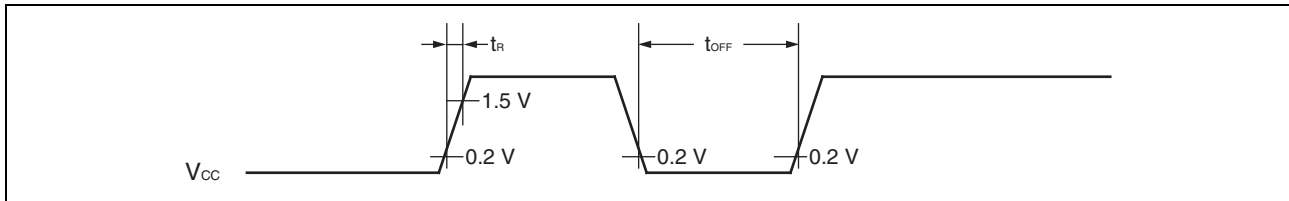
\*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of  $\mu\text{s}$  and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several  $\mu\text{s}$  and several ms.



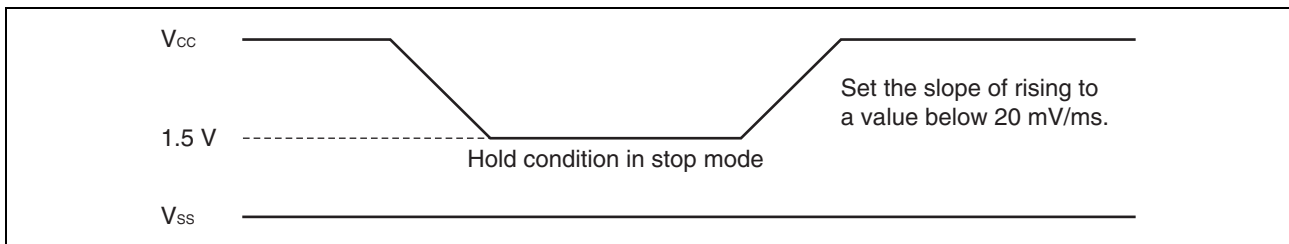
14.4.4 Power-on Reset

( $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	$t_R$	—	—	50	ms	
Power supply cutoff time	$t_{OFF}$	—	1	—	ms	Wait time until power-on



**Note:** A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 20 mV/ms as shown below.

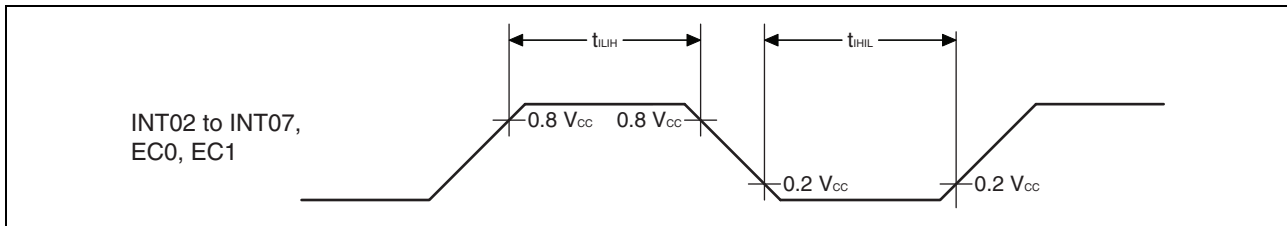


14.4.5 Peripheral Input Timing

( $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input "H" pulse width	$t_{ILIH}$	INT02 to INT07, EC0, EC1	$2 t_{MCLK}^*$	—	ns
Peripheral input "L" pulse width	$t_{IHIL}$		$2 t_{MCLK}^*$	—	ns

\*: See "Source Clock/Machine Clock" for  $t_{MCLK}$ .



**14.4.6 LIN-UART Timing**

Sampling is executed at the rising edge of the sampling clock\*1, and serial clock delay is disabled\*2.  
 (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 0)

( $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ )

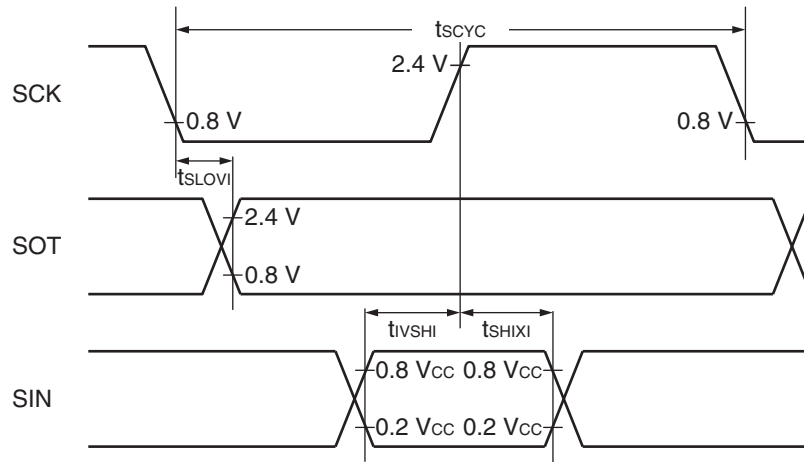
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin: $C_L = 80\text{ pF} + 1\text{ TTL}$	$5 t_{MCLK}^{*3}$	—	ns
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↑	$t_{IVSHI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK ↑ → valid SIN hold time	$t_{SHIXI}$	SCK, SIN		0	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCK	External clock operation output pin: $C_L = 80\text{ pF} + 1\text{ TTL}$	$3 t_{MCLK}^{*3} - t_R$	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCK		$t_{MCLK}^{*3} + 95$	—	ns
SCK ↓ → SOT delay time	$t_{SLOVE}$	SCK, SOT		—	$2 t_{MCLK}^{*3} + 95$	ns
Valid SIN → SCK ↑	$t_{IVSHE}$	SCK, SIN		190	—	ns
SCK ↑ → valid SIN hold time	$t_{SHIXE}$	SCK, SIN		$t_{MCLK}^{*3} + 95$	—	ns
SCK fall time	$t_F$	SCK		—	10	ns
SCK rise time	$t_R$	SCK		—	10	ns

\*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

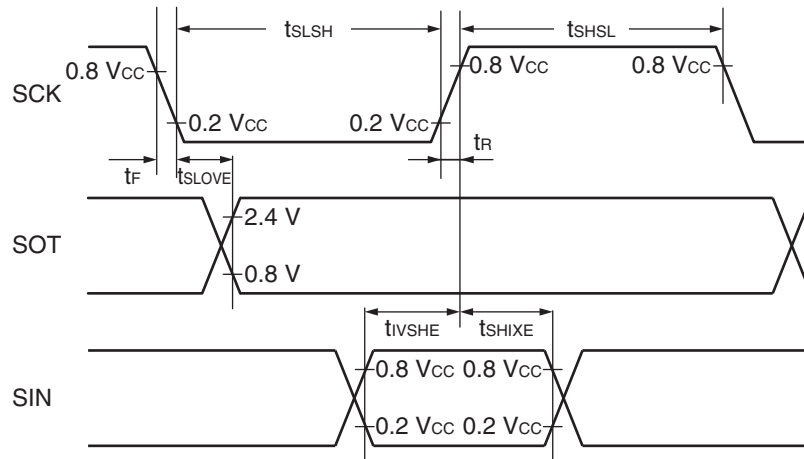
\*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

\*3: See "Source Clock/Machine Clock" for  $t_{MCLK}$ .

• Internal shift clock mode



• External shift clock mode



Sampling is executed at the falling edge of the sampling clock\*1, and serial clock delay is disabled\*2.  
 (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)

( $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ )

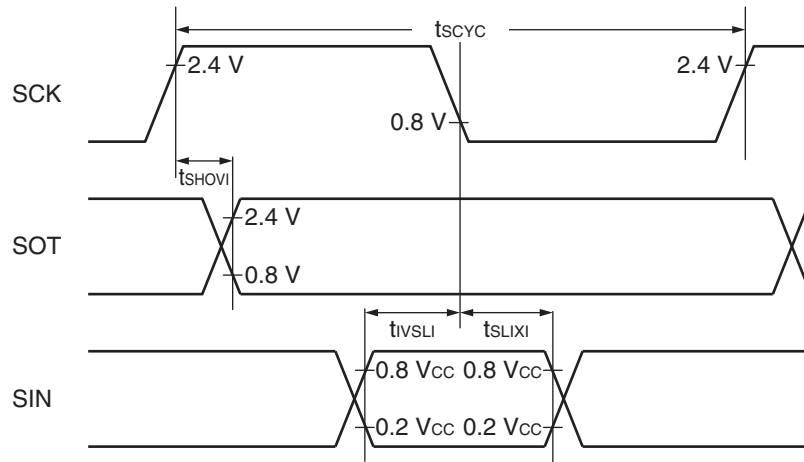
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin: $C_L = 80\text{ pF} + 1\text{ TTL}$	$5 t_{MCLK}^{*3}$	—	ns
SCK $\uparrow$ → SOT delay time	$t_{SHOVI}$	SCK, SOT		-95	+95	ns
Valid SIN → SCK $\downarrow$	$t_{IVSLI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK $\downarrow$ → valid SIN hold time	$t_{SLIXI}$	SCK, SIN		0	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCK	External clock operation output pin: $C_L = 80\text{ pF} + 1\text{ TTL}$	$3 t_{MCLK}^{*3} - t_R$	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCK		$t_{MCLK}^{*3} + 95$	—	ns
SCK $\uparrow$ → SOT delay time	$t_{SHOVE}$	SCK, SOT		—	$2 t_{MCLK}^{*3} + 95$	ns
Valid SIN → SCK $\downarrow$	$t_{IVSLE}$	SCK, SIN		190	—	ns
SCK $\downarrow$ → valid SIN hold time	$t_{SLIXE}$	SCK, SIN		$t_{MCLK}^{*3} + 95$	—	ns
SCK fall time	$t_F$	SCK		—	10	ns
SCK rise time	$t_R$	SCK		—	10	ns

\*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

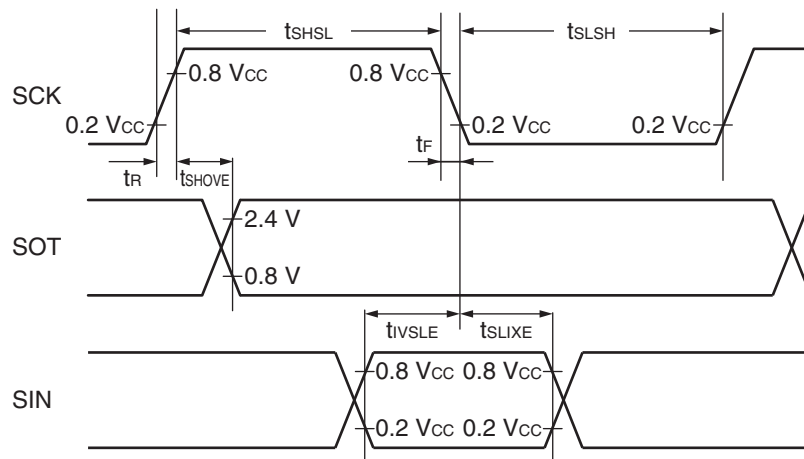
\*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

\*3: See "Source Clock/Machine Clock" for  $t_{MCLK}$ .

• Internal shift clock mode



• External shift clock mode



Sampling is executed at the rising edge of the sampling clock\*1, and serial clock delay is enabled\*2.  
 (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

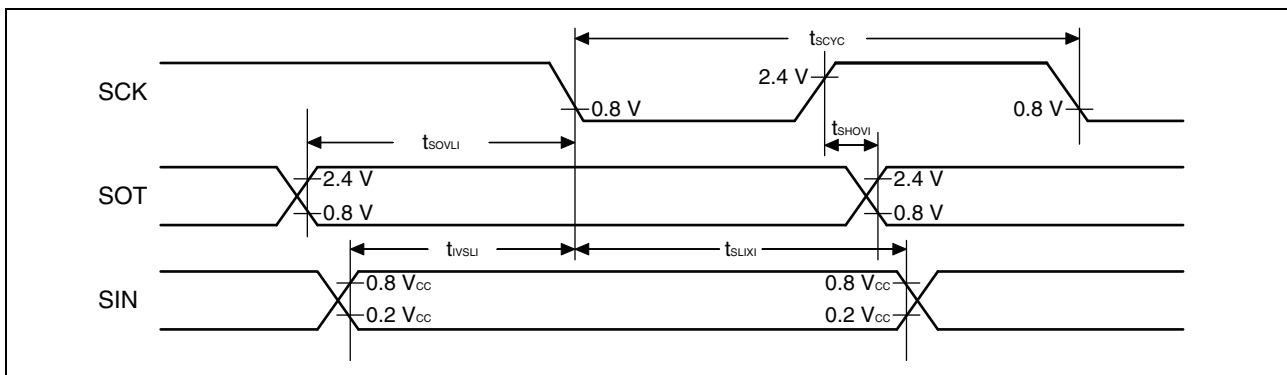
( $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin: $C_L = 80\text{ pF} + 1\text{ TTL}$	$5 t_{MCLK}^{*3}$	—	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVI}$	SCK, SOT		-95	+95	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK $\downarrow$ $\rightarrow$ valid SIN hold time	$t_{SLIXI}$	SCK, SIN		0	—	ns
SOT $\rightarrow$ SCK $\downarrow$ delay time	$t_{SOVLI}$	SCK, SOT		—	$4 t_{MCLK}^{*3}$	ns

\*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

\*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

\*3: See “Source Clock/Machine Clock” for  $t_{MCLK}$ .



Sampling is executed at the falling edge of the sampling clock\*1, and serial clock delay is enabled\*2.  
 (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)

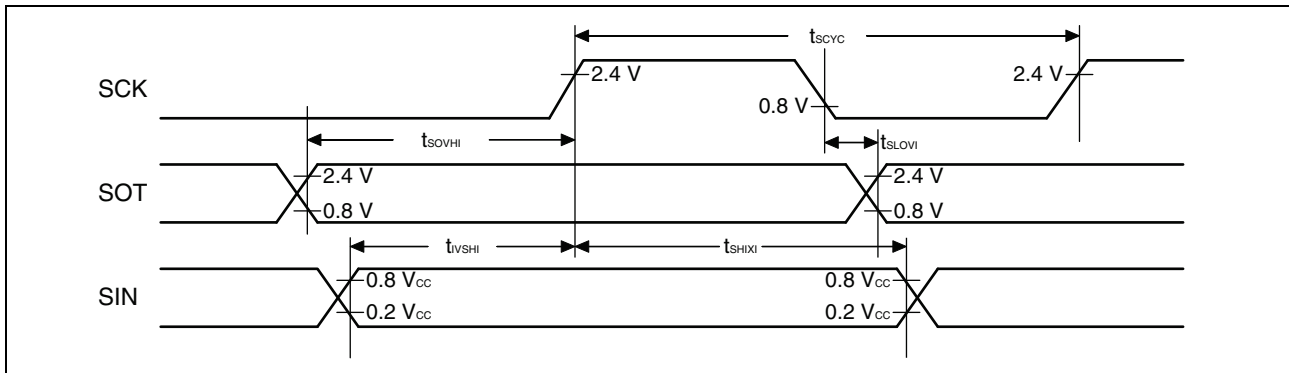
( $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin: $C_L = 80\text{ pF} + 1\text{ TTL}$	$5 t_{MCLK}^{*3}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	$t_{SLOVI}$	SCK, SOT		-95	+95	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	$t_{VSHI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	$t_{SHIXI}$	SCK, SIN		0	—	ns
SOT $\rightarrow$ SCK $\uparrow$ delay time	$t_{SOVHI}$	SCK, SOT		—	$4 t_{MCLK}^{*3}$	ns

\*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

\*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

\*3: See “Source Clock/Machine Clock” for  $t_{MCLK}$ .



**14.4.7 Low-voltage Detection**
 $(V_{SS} = 0.0 \text{ V}, V_{CC} = 1.8 \text{ V to } 3.6 \text{ V}, T_A = -40^\circ\text{C to } +85^\circ\text{C})$ 

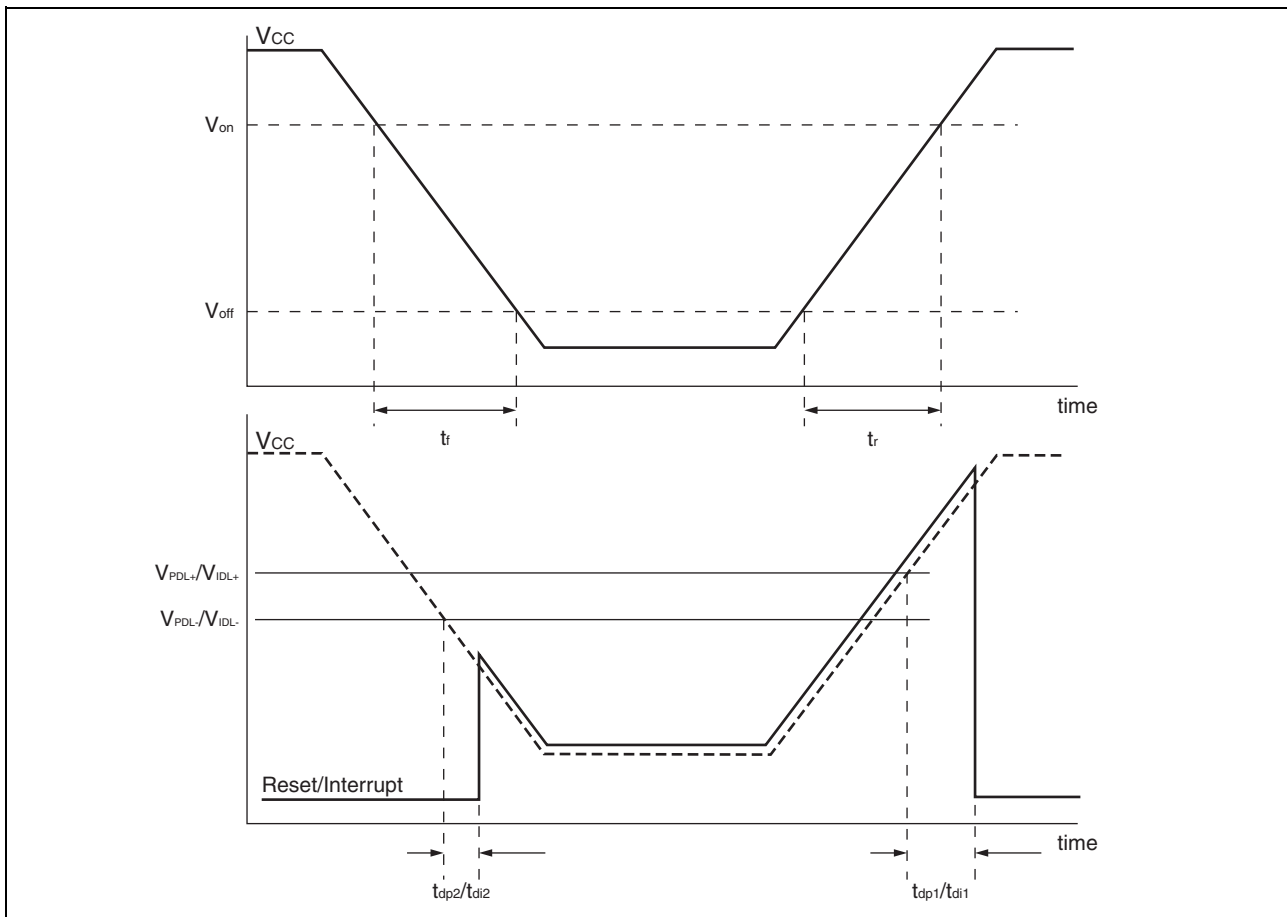
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power release voltage 0	$V_{PDL0+}$	1.83	1.93	2.03	V	At power supply rise
Power detection voltage 0	$V_{PDL0-}$	1.80	1.90	2.00	V	At power supply fall
Power release voltage 1	$V_{PDL1+}$	2.25	2.40	2.55	V	At power supply rise
Power detection voltage 1	$V_{PDL1-}$	2.20	2.35	2.50	V	At power supply fall
Power release voltage 2	$V_{PDL2+}$	2.80	2.95	3.10	V	At power supply rise
Power detection voltage 2	$V_{PDL2-}$	2.70	2.85	3.00	V	At power supply fall
Interrupt release voltage 0	$V_{IDL0+}$	2.03	2.18	2.33	V	At power supply rise
Interrupt detection voltage 0	$V_{IDL0-}$	2.00	2.15	2.30	V	At power supply fall
Interrupt release voltage 1	$V_{IDL1+}$	2.25	2.40	2.55	V	At power supply rise
Interrupt detection voltage 1	$V_{IDL1-}$	2.20	2.35	2.50	V	At power supply fall
Interrupt release voltage 2	$V_{IDL2+}$	2.46	2.61	2.76	V	At power supply rise
Interrupt detection voltage 2	$V_{IDL2-}$	2.40	2.55	2.70	V	At power supply fall
Interrupt release voltage 3	$V_{IDL3+}$	2.67	2.82	2.97	V	At power supply rise
Interrupt detection voltage 3	$V_{IDL3-}$	2.60	2.75	2.90	V	At power supply fall
Interrupt release voltage 4	$V_{IDL4+}$	2.90	3.10	3.30	V	At power supply rise
Interrupt detection voltage 4	$V_{IDL4-}$	2.80	3.00	3.20	V	At power supply fall
Power supply start voltage	$V_{off}$	—	—	1.8	V	
Power supply end voltage	$V_{on}$	3.3	—	—	V	
Power supply voltage change time (at power supply rise)	$t_r$	3000	—	—	$\mu\text{s}$	Slope of power supply that the reset release signal generates within the rating ( $V_{PDL+}/V_{IDL+}$ )

*(Continued)*

(Continued)

( $V_{SS} = 0.0\text{ V}$ ,  $V_{CC} = 1.8\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage change time (at power supply fall)	$t_f$	3000	—	—	$\mu\text{s}$	Slope of power supply that the reset detection signal generates within the rating ( $V_{PDL-}/V_{IDL-}$ )
Power reset release delay time	$t_{dp1}$	10	—	300	$\mu\text{s}$	
Power reset detection delay time	$t_{dp2}$	—	—	150	$\mu\text{s}$	
Interrupt reset release delay time	$t_{di1}$	10	—	200	$\mu\text{s}$	
Interrupt reset detection delay time	$t_{di2}$	—	—	150	$\mu\text{s}$	



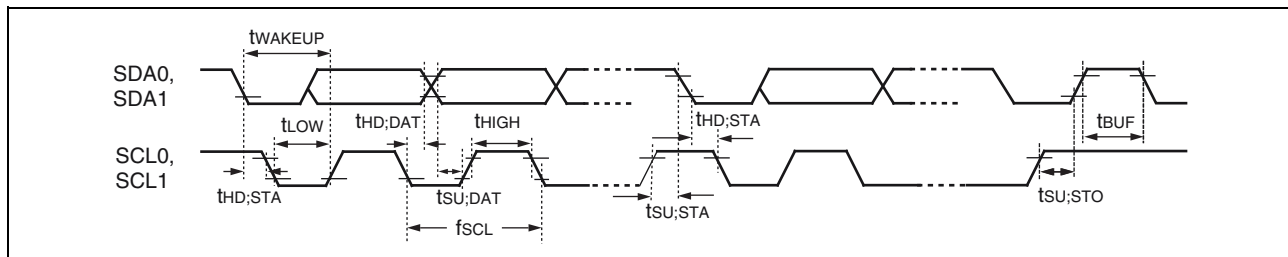
**14.4.8 I<sup>2</sup>C Timing**
 $(V_{CC} = 3.0\text{ V to }3.6\text{ V}, V_{SS} = 0.0\text{ V}, T_A = -40^\circ\text{C to }+85^\circ\text{C})$ 

Parameter	Symbol	Pin name	Condition	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	$f_{SCL}$	SCL0, SCL1	R = 1.7 k $\Omega$ , C = 50 pF*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA $\downarrow \rightarrow$ SCL $\downarrow$	$t_{HD;STA}$	SCL0, SCL1, SDA0, SDA1		4.0	—	0.6	—	$\mu\text{s}$
SCL clock "L" width	$t_{LOW}$	SCL0, SCL1		4.7	—	1.3	—	$\mu\text{s}$
SCL clock "H" width	$t_{HIGH}$	SCL0, SCL1		4.0	—	0.6	—	$\mu\text{s}$
(Repeated) START condition hold time SCL $\uparrow \rightarrow$ SDA $\downarrow$	$t_{SU;STA}$	SCL0, SCL1, SDA0, SDA1		4.7	—	0.6	—	$\mu\text{s}$
Data hold time SCL $\downarrow \rightarrow$ SDA $\uparrow \downarrow$	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		0	3.45*2	0	0.9*3	$\mu\text{s}$
Data setup time SDA $\uparrow \downarrow \rightarrow$ SCL $\uparrow$	$t_{SU;DAT}$	SCL0, SCL1, SDA0, SDA1		0.25	—	0.1	—	$\mu\text{s}$
STOP condition setup time SCL $\uparrow \rightarrow$ SDA $\uparrow$	$t_{SU;STO}$	SCL0, SCL1, SDA0, SDA1		4	—	0.6	—	$\mu\text{s}$
Bus free time between STOP condition and START condition	$t_{BUF}$	SCL0, SCL1, SDA0, SDA1		4.7	—	1.3	—	$\mu\text{s}$

\*1: R represents the pull-up resistor of the SCL0/1 and SDA0/1 lines, and C the load capacitor of the SCL0/1 and SDA0/1 lines.

\*2: The maximum  $t_{HD;DAT}$  in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at "L" ( $t_{LOW}$ ) does not extend.

\*3: A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, provided that the condition of  $t_{SU;DAT} \geq 250\text{ ns}$  is fulfilled.



(Continued)

$(V_{CC} = 3.0\text{ V to }3.6\text{ V}, V_{SS} = 0.0\text{ V}, T_A = -40^\circ\text{C to }+85^\circ\text{C})$ 

Parameter	Sym- bol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock "L" width	$t_{LOW}$	SCL0, SCL1	R = 1.7 k $\Omega$ , C = 50 pF*1	$(2 + nm/2)t_{MCLK} - 20$	—	ns	Master mode
SCL clock "H" width	$t_{HIGH}$	SCL0, SCL1		$(nm/2)t_{MCLK} - 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	$t_{HD;STA}$	SCL0, SCL1, SDA0, SDA1		$(-1 + nm/2)t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	$t_{SU;STO}$	SCL0, SCL1, SDA0, SDA1		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	$t_{SU;STA}$	SCL0, SCL1, SDA0, SDA1		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	$t_{BUF}$	SCL0, SCL1, SDA0, SDA1		$(2nm + 4)t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		$3t_{MCLK} - 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL0, SCL1, SDA0, SDA1		$(-2 + nm/2)t_{MCLK} - 20$	$(-1 + nm/2)t_{MCLK} + 20$	ns	Master mode When assuming that "L" of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL0, SCL1		$(nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Minimum value is applied to interrupt at 9th SCL $\downarrow$ . Maximum value is applied to the interrupt at the 8th SCL $\downarrow$ .

*(Continued)*

(Continued)

( $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ )

Parameter	Sym- bol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock "L" width	$t_{LOW}$	SCL0, SCL1	R = 1.7 k $\Omega$ , C = 50 pF*1	$4 t_{MCLK} - 20$	—	ns	At reception
SCL clock "H" width	$t_{HIGH}$	SCL0, SCL1		$4 t_{MCLK} - 20$	—	ns	At reception
START condition detection	$t_{HD;STA}$	SCL0, SCL1, SDA0, SDA1		$2 t_{MCLK} - 20$	—	ns	Undetected when 1 $t_{MCLK}$ is used at reception
STOP condition detection	$t_{SU;STO}$	SCL0, SCL1, SDA0, SDA1		$2 t_{MCLK} - 20$	—	ns	Undetected when 1 $t_{MCLK}$ is used at reception
RESTART condition detection condition	$t_{SU;STA}$	SCL0, SCL1, SDA0, SDA1		$2 t_{MCLK} - 20$	—	ns	Undetected when 1 $t_{MCLK}$ is used at reception
Bus free time	$t_{BUF}$	SCL0, SCL1, SDA0, SDA1		$2 t_{MCLK} - 20$	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		$2 t_{MCLK} - 20$	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL0, SCL1, SDA0, SDA1		$t_{LOW} - 3 t_{MCLK} - 20$	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL0, SCL1, SDA0, SDA1		$t_{MCLK} - 20$	—	ns	At reception
SDA $\downarrow$ → SCL $\uparrow$ (at wakeup function)	$t_{WAKEUP}$	SCL0, SCL1, SDA0, SDA1		Oscillation stabilization wait time $+2 t_{MCLK} - 20$	—	ns	

\*1: R represents the pull-up resistor of the SCL0/1 and SDA0/1 lines, and C the load capacitor of the SCL0/1 and SDA0/1 lines.

\*2: • See "Source Clock/Machine Clock" for  $t_{MCLK}$ .

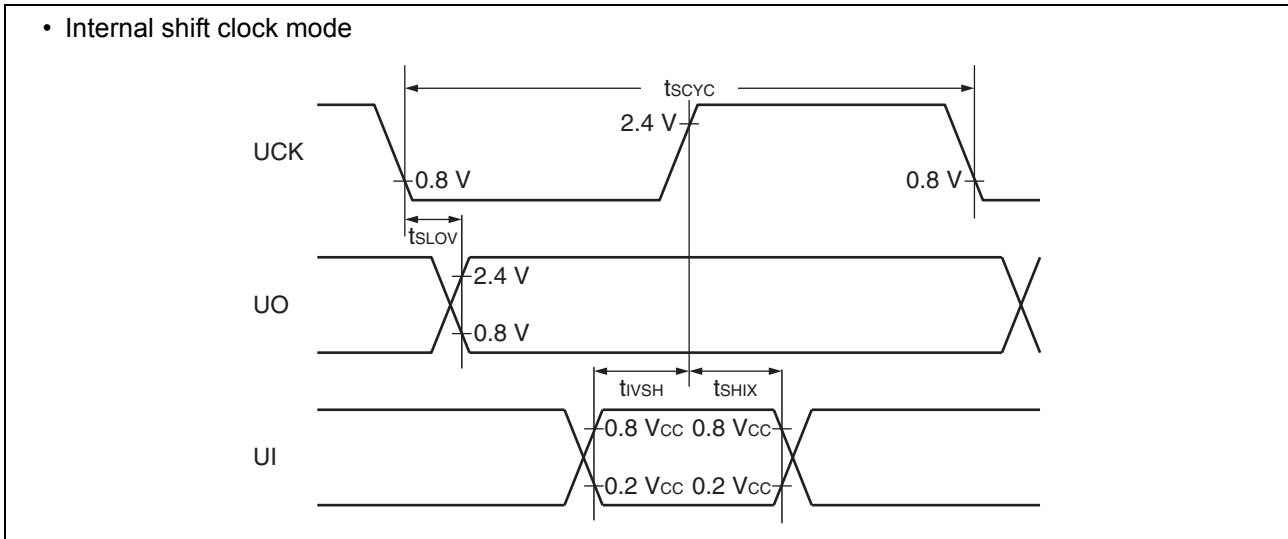
- m represents the CS4 bit and CS3 bit (bit4 and bit3) in the I<sup>2</sup>C clock control register (ICCR0).
- n represents the CS2 bit to CS0 bit (bit2 to bit0) in the I<sup>2</sup>C clock control register (ICCR0).
- The actual timing of I<sup>2</sup>C is determined by the values of m and n set by the machine clock ( $t_{MCLK}$ ) and the CS4 to CS0 bits in the ICCR0 register.
- Standard-mode:
  - m and n can be set to values in the following range:  $0.9\text{ MHz} < t_{MCLK}$  (machine clock)  $< 10\text{ MHz}$ .
  - The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  - (m, n) = (1, 8) :  $0.9\text{ MHz} < t_{MCLK} \leq 1\text{ MHz}$
  - (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) :  $0.9\text{ MHz} < t_{MCLK} \leq 2\text{ MHz}$
  - (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) :  $0.9\text{ MHz} < t_{MCLK} \leq 4\text{ MHz}$
  - (m, n) = (1, 98) :  $0.9\text{ MHz} < t_{MCLK} \leq 10\text{ MHz}$
- Fast-mode:
  - m and n can be set to values in the following range:  $3.3\text{ MHz} < t_{MCLK}$  (machine clock)  $< 10\text{ MHz}$ .
  - The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  - (m, n) = (1, 8) :  $3.3\text{ MHz} < t_{MCLK} \leq 4\text{ MHz}$
  - (m, n) = (1, 22), (5, 4) :  $3.3\text{ MHz} < t_{MCLK} \leq 8\text{ MHz}$
  - (m, n) = (6, 4) :  $3.3\text{ MHz} < t_{MCLK} \leq 10\text{ MHz}$

14.4.9 UART/SIO, Serial I/O Timing

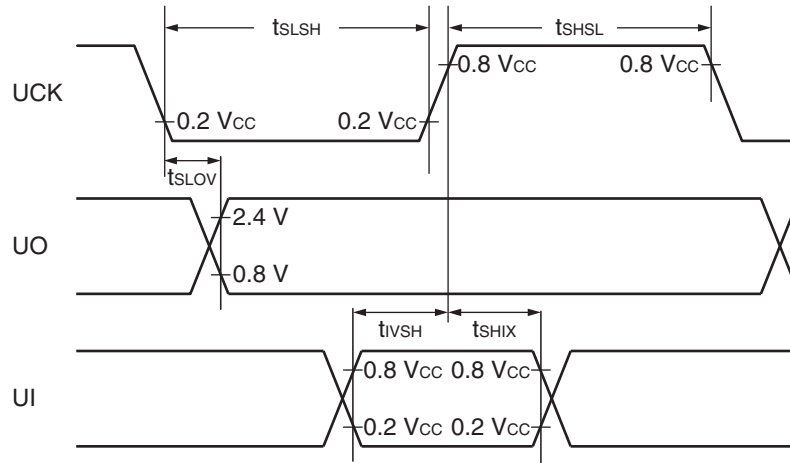
( $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	UCK	Internal clock operation	$4 t_{MCLK}^*$	—	ns
UCK $\downarrow \rightarrow$ UO time	$t_{SLOV}$	UCK, UO		-190	+190	ns
Valid UI $\rightarrow$ UCK $\uparrow$	$t_{IVSH}$	UCK, UI		$2 t_{MCLK}^*$	—	ns
UCK $\uparrow \rightarrow$ valid UI hold time	$t_{SHIX}$	UCK, UI		$2 t_{MCLK}^*$	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	UCK	External clock operation	$4 t_{MCLK}^*$	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	UCK		$4 t_{MCLK}^*$	—	ns
UCK $\downarrow \rightarrow$ UO time	$t_{SLOV}$	UCK, UO		—	190	ns
Valid UI $\rightarrow$ UCK $\uparrow$	$t_{IVSH}$	UCK, UI		$2 t_{MCLK}^*$	—	ns
UCK $\uparrow \rightarrow$ valid UI hold time	$t_{SHIX}$	UCK, UI	$2 t_{MCLK}^*$	—	ns	

\*: See "Source Clock/Machine Clock" for  $t_{MCLK}$ .



• External shift clock mode



**14.5 A/D Converter**
**14.5.1 A/D Converter Electrical Characteristics**
 $(V_{CC} = 1.8\text{ V to } 3.6\text{ V}, V_{SS} = 0.0\text{ V}, T_A = -40^\circ\text{C to } +85^\circ\text{C})$ 

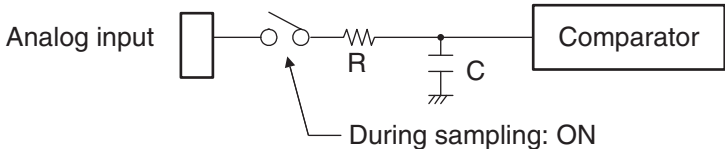
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		-3	—	+3	LSB	
Linearity error		-2.5	—	+2.5	LSB	
Differential linear error		-1.9	—	+1.9	LSB	
Zero transition voltage	$V_{OT}$	$V_{SS} - 1.5\text{ LSB}$	$V_{SS} + 0.5\text{ LSB}$	$V_{SS} + 2.5\text{ LSB}$	V	$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$
		$V_{SS} - 0.5\text{ LSB}$	$V_{SS} + 1.5\text{ LSB}$	$V_{SS} + 3.5\text{ LSB}$	V	$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$
Full-scale transition voltage	$V_{FST}$	$V_{CC} - 3.5\text{ LSB}$	$V_{CC} - 1.5\text{ LSB}$	$V_{CC} + 0.5\text{ LSB}$	V	$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$
		$V_{CC} - 2.5\text{ LSB}$	$V_{CC} - 0.5\text{ LSB}$	$V_{CC} + 1.5\text{ LSB}$	V	$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$
Compare time	—	1.3	—	140	$\mu\text{s}$	$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$
		20	—	140		$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$
Sampling time	—	0.4	—	—	$\mu\text{s}$	$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ , with external impedance $< 1.8\text{ k}\Omega$
		30	—	—	$\mu\text{s}$	$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ , with external impedance $< 14.8\text{ k}\Omega$
Analog input current	$I_{AIN}$	-0.3	—	+0.3	$\mu\text{A}$	
Analog input voltage	$V_{AIN}$	$V_{SS}$	—	$V_{CC}$	V	

14.5.2 Notes on Using the A/D Converter

■ External impedance of analog input and its sampling time

- The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1  $\mu\text{F}$  to the analog input pin.

• Analog input equivalent circuit

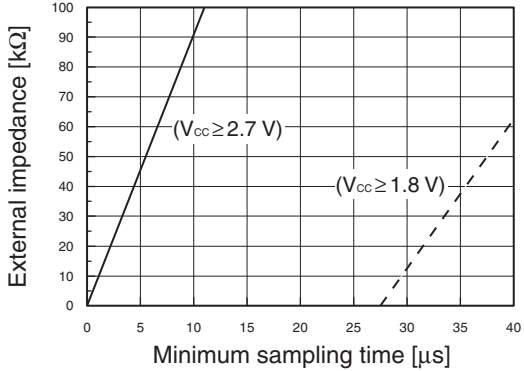


$V_{CC}$	R	C
$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$	1.7 k $\Omega$ (Max)	14.5 pF (Max)
$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	84 k $\Omega$ (Max)	25.2 pF (Max)

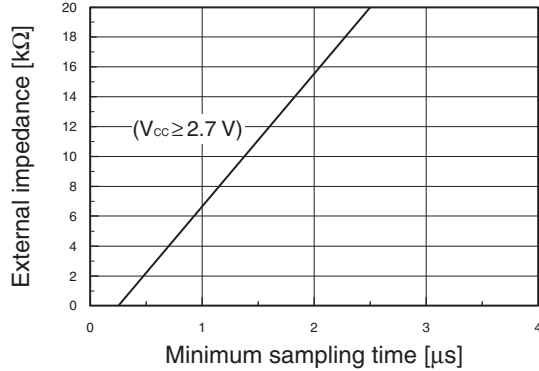
Note: The values are reference values.

• Relationship between external impedance and minimum sampling time

[External impedance = 0 k $\Omega$  to 100 k $\Omega$ ]



[External impedance = 0 k $\Omega$  to 20 k $\Omega$ ]

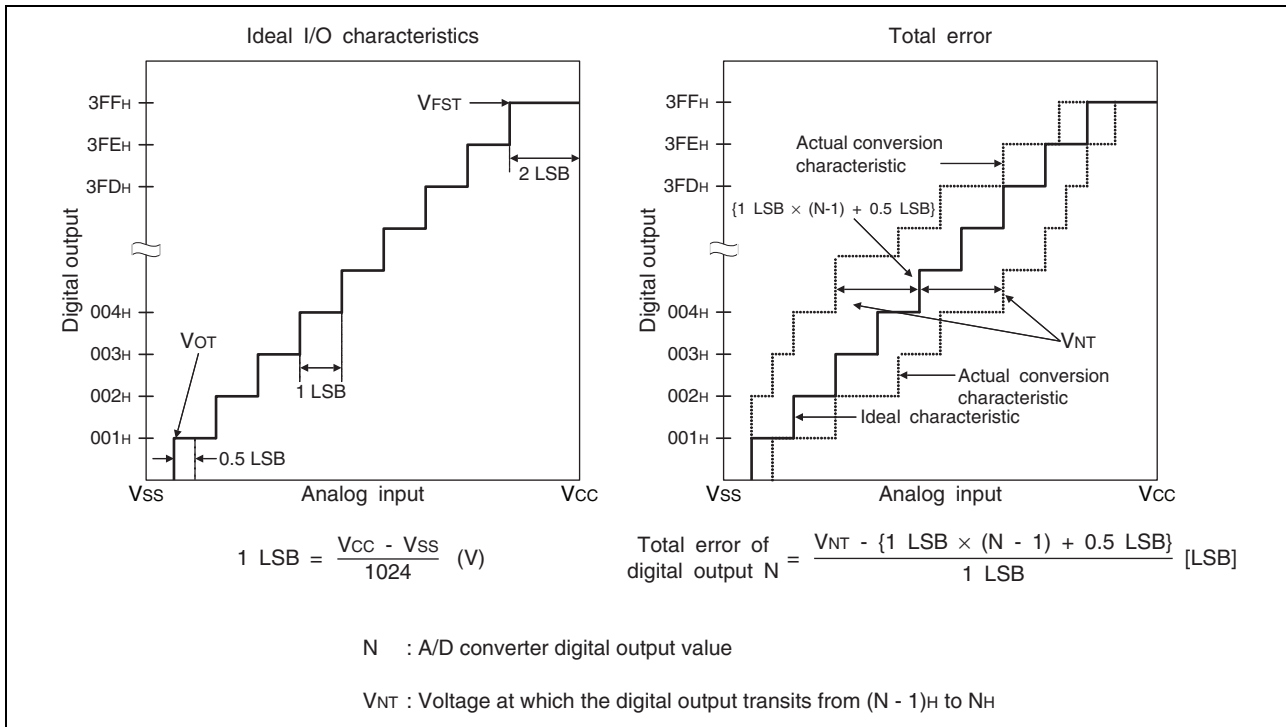


■ A/D conversion error

As  $|V_{CC} - V_{SS}|$  decreases, the A/D conversion error increases proportionately.

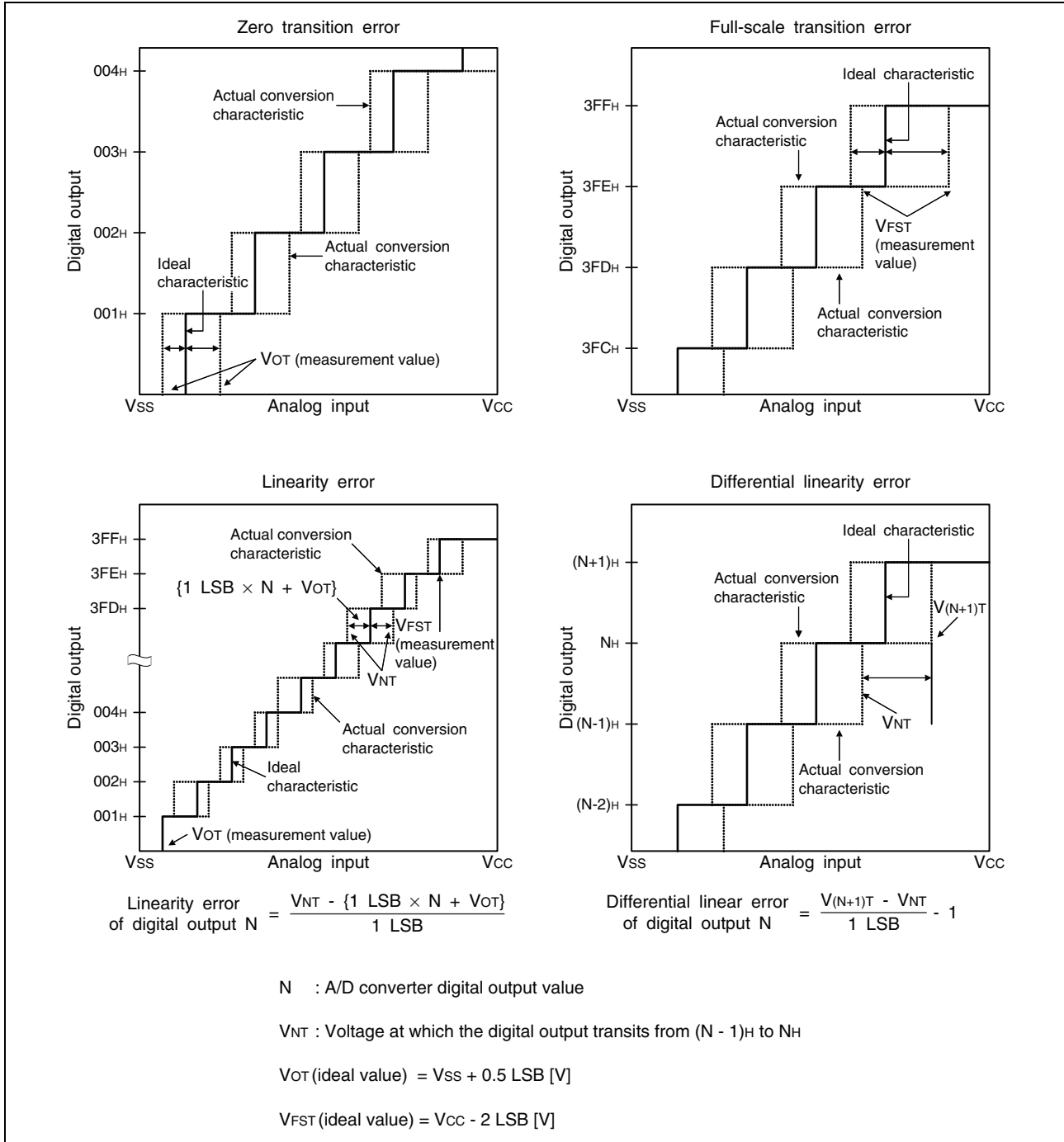
14.5.3 Definitions of A/D Converter Terms

- Resolution  
It indicates the level of analog variation that can be distinguished by the A/D converter. When the number of bits is 10, analog voltage can be divided into  $2^{10} = 1024$ .
- Linearity error (unit: LSB)  
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device to the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) of the same device.
- Differential linear error (unit: LSB)  
It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)  
It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



(Continued)

(Continued)



**14.6 Flash Memory Write/Erase Characteristics**

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.2* <sup>1</sup>	0.5* <sup>2</sup>	s	The time of writing 00 <sub>H</sub> prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.5* <sup>1</sup>	7.5* <sup>2</sup>	s	The time of writing 00 <sub>H</sub> prior to erasure is excluded.
Byte writing time	—	21	6100* <sup>2</sup>	μs	System-level overhead is excluded.
Erase/write cycle	100000	—	—	cycle	
Power supply voltage at erase/write	2.7	3.0	3.6	V	
Flash memory data retention time	20* <sup>3</sup>	—	—	year	Average T <sub>A</sub> = +85°C

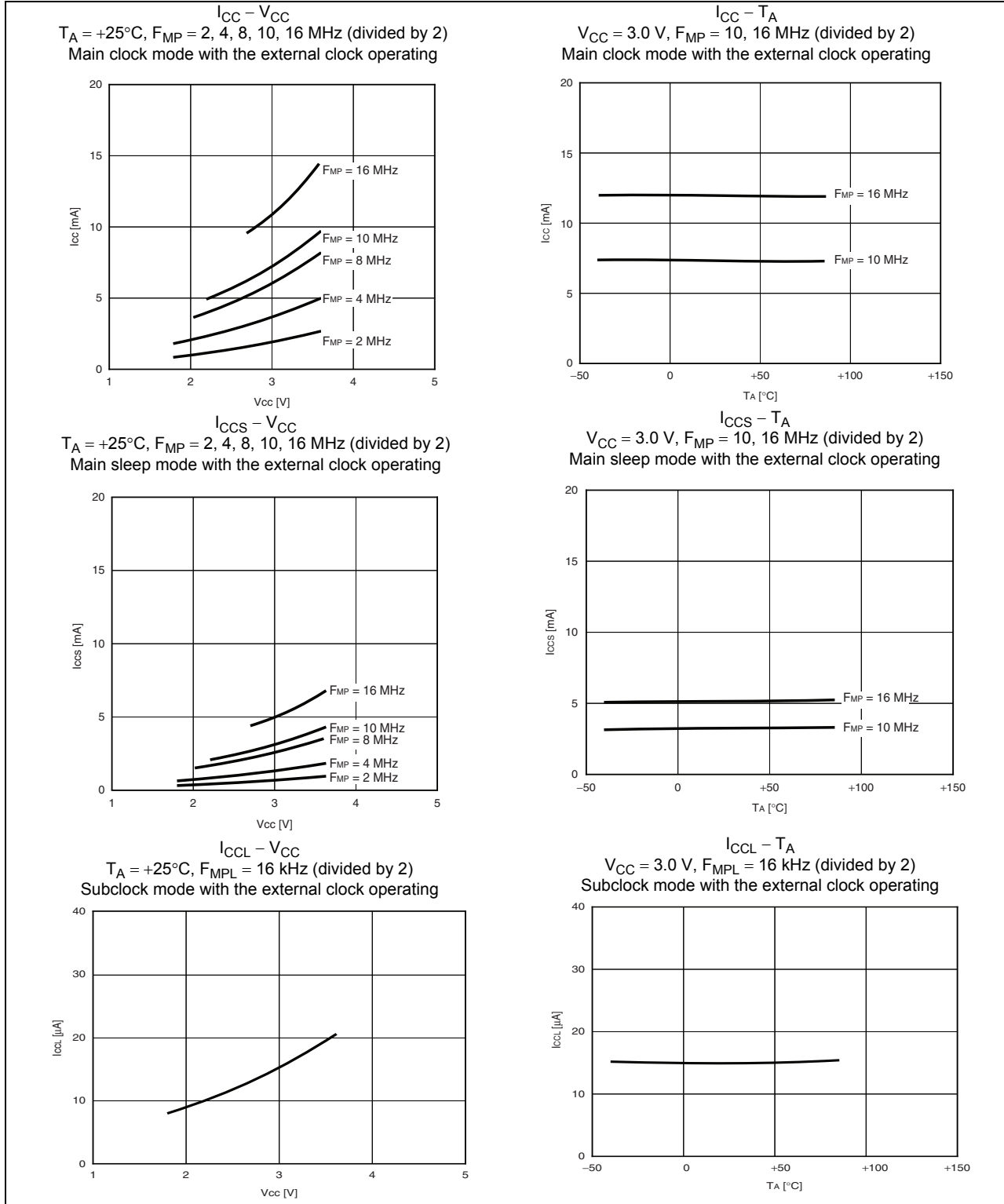
\*1: T<sub>A</sub> = +25°C, V<sub>CC</sub> = 3.0 V, 100000 cycles

\*2: T<sub>A</sub> = +85°C, V<sub>CC</sub> = 2.7 V, 100000 cycles

\*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85°C).

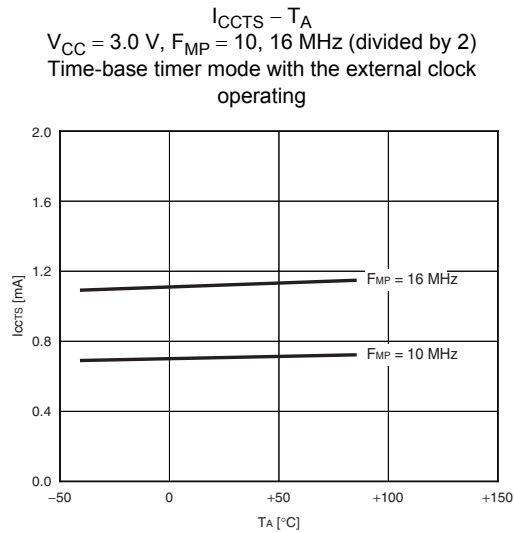
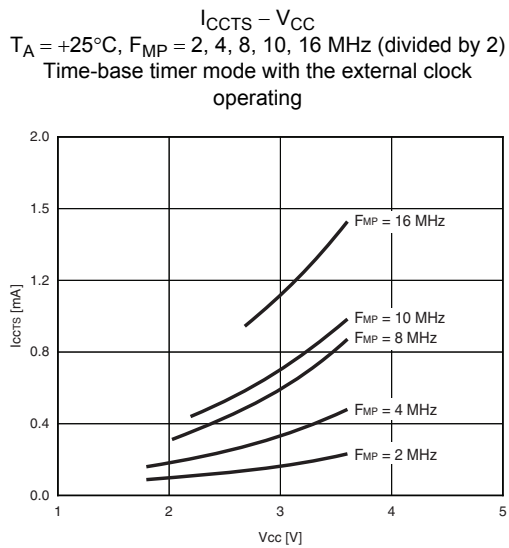
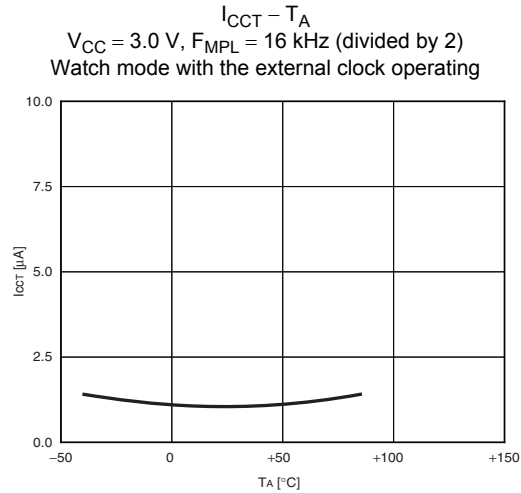
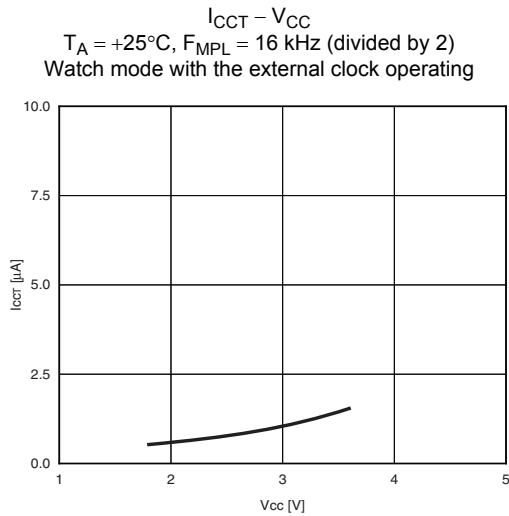
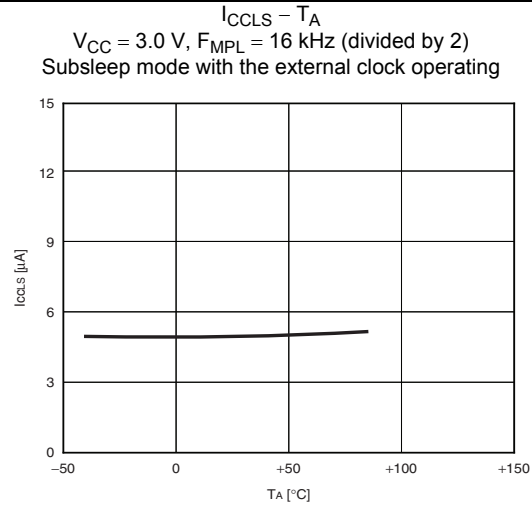
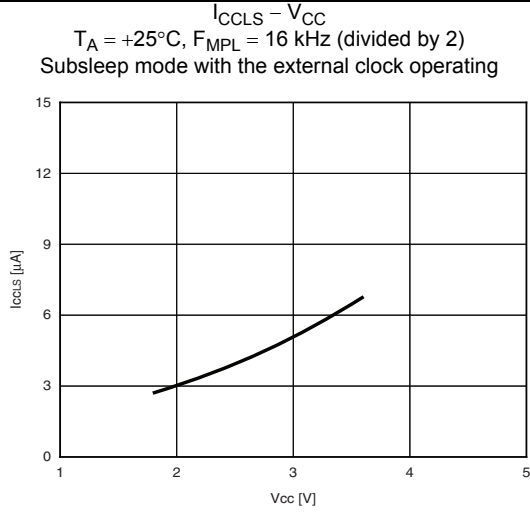
### 15. Sample Characteristics

■ Power supply current temperature characteristics

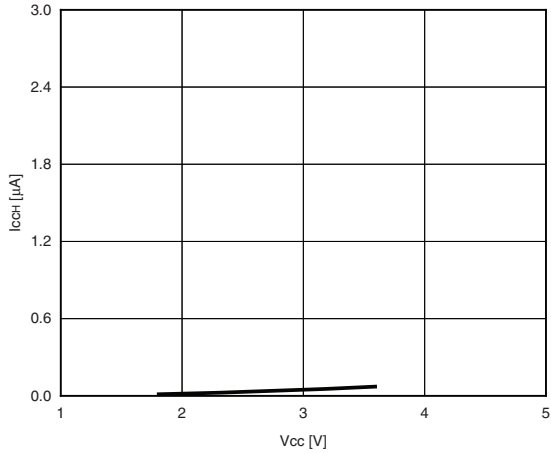


(Continued)

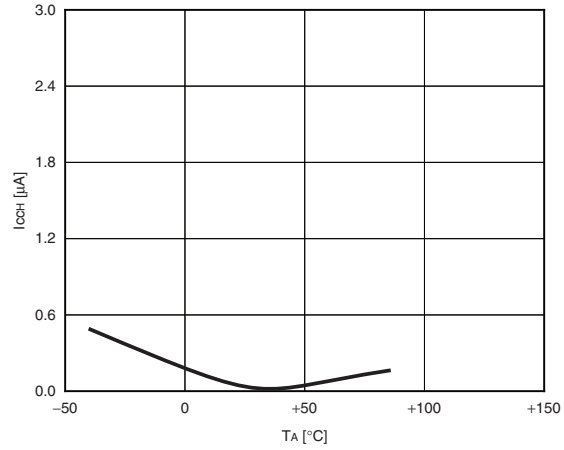
(Continued)



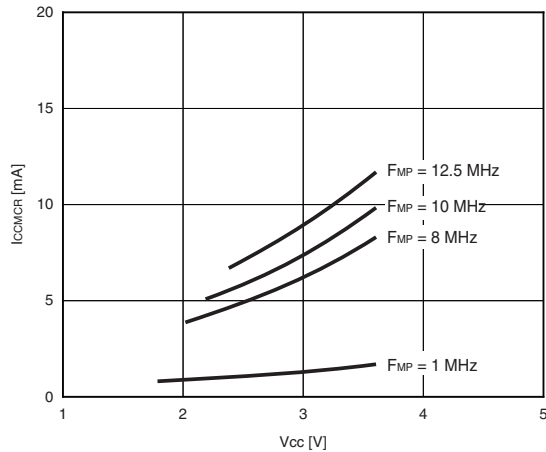
$I_{CCH} - V_{CC}$   
 $T_A = +25^\circ\text{C}, F_{MPL} = (\text{stop})$   
 Substop mode with the external clock stopping



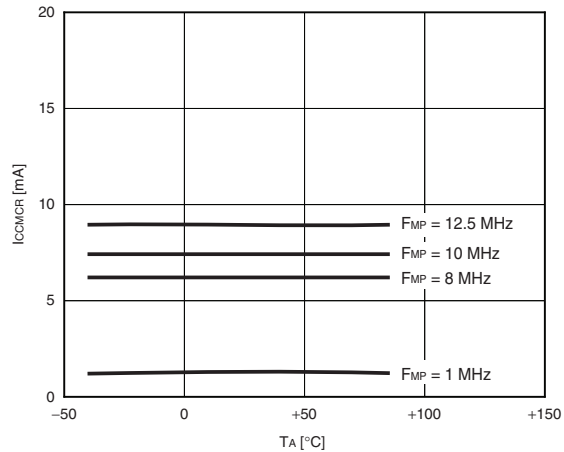
$I_{CCH} - T_A$   
 $V_{CC} = 3.0\text{ V}, F_{MPL} = (\text{stop})$   
 Substop mode with the external clock stopping



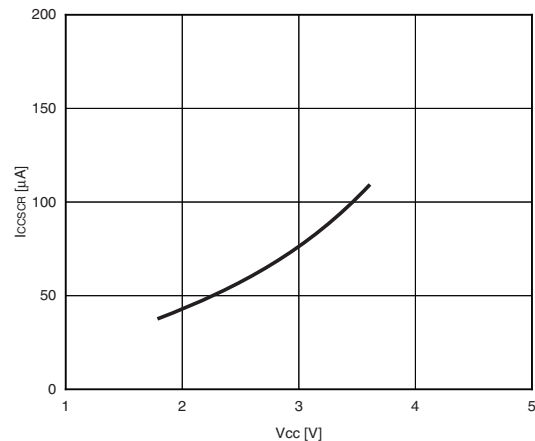
$I_{CCMCR} - V_{CC}$   
 $T_A = +25^\circ\text{C}, F_{MP} = 1, 8, 10, 12.5\text{ MHz (no division)}$   
 Main clock mode with the main CR clock operating



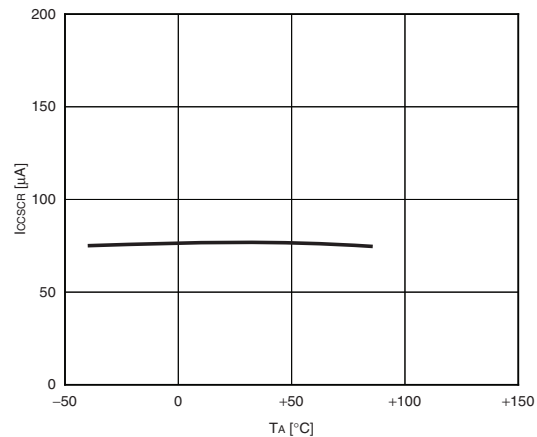
$I_{CCMCR} - T_A$   
 $V_{CC} = 3.0\text{ V}, F_{MP} = 1, 8, 10, 12.5\text{ MHz (no division)}$   
 Main clock mode with the main CR clock operating



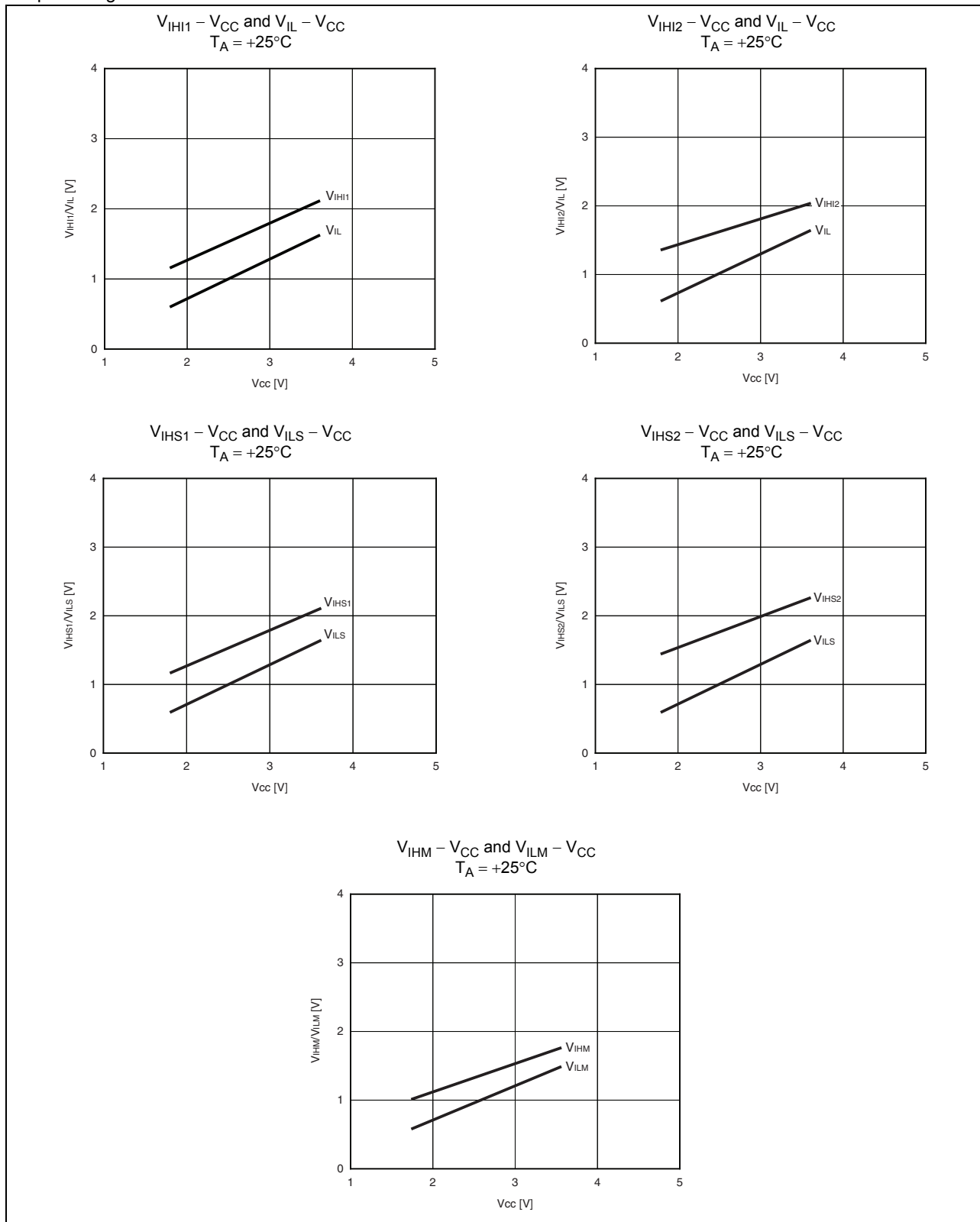
$I_{CCSCR} - V_{CC}$   
 $T_A = +25^\circ\text{C}, F_{MPL} = 50\text{ kHz (divided by 2)}$   
 Subclock mode with the sub-CR clock operating



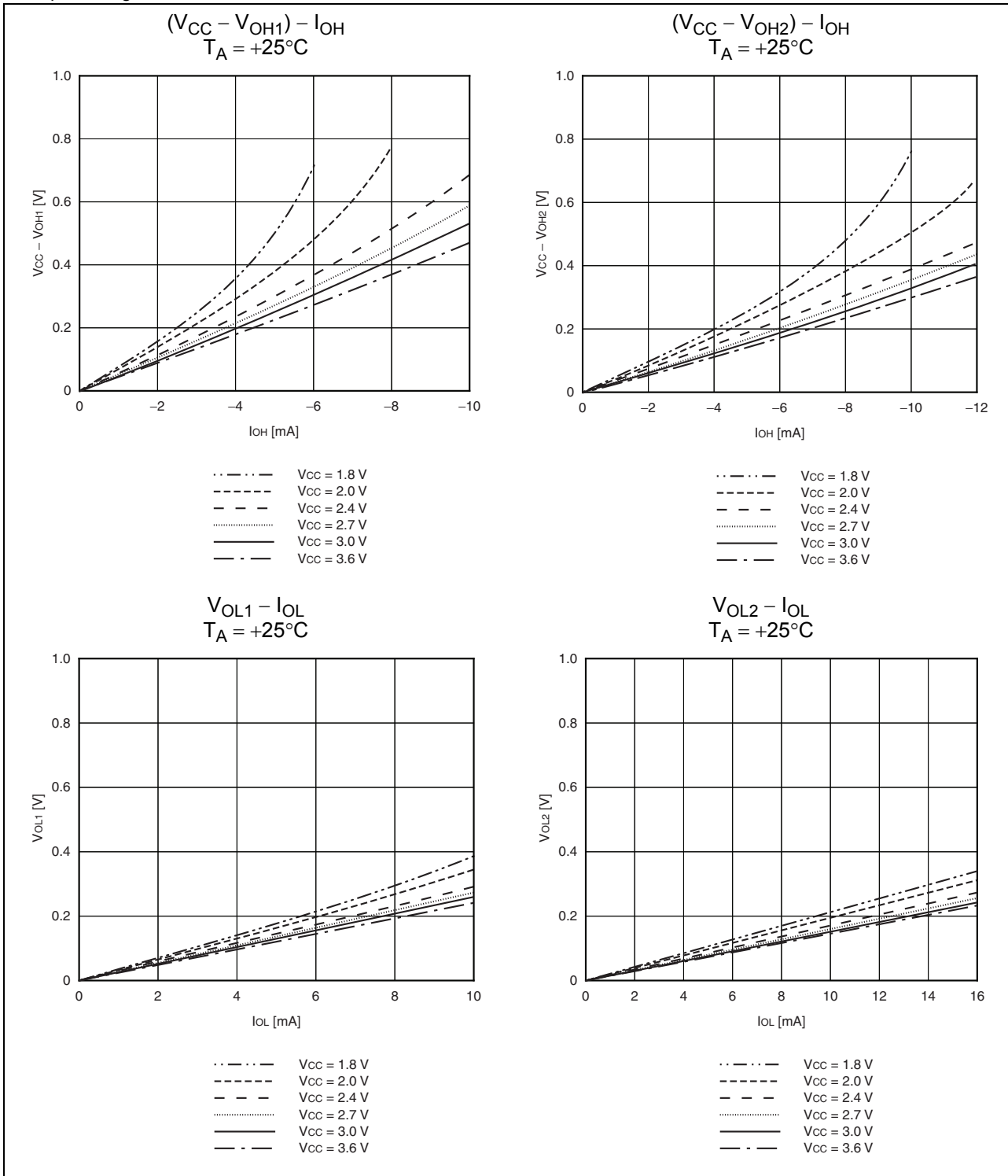
$I_{CCSCR} - T_A$   
 $V_{CC} = 3.0\text{ V}, F_{MPL} = 50\text{ kHz (divided by 2)}$   
 Subclock mode with the sub-CR clock operating



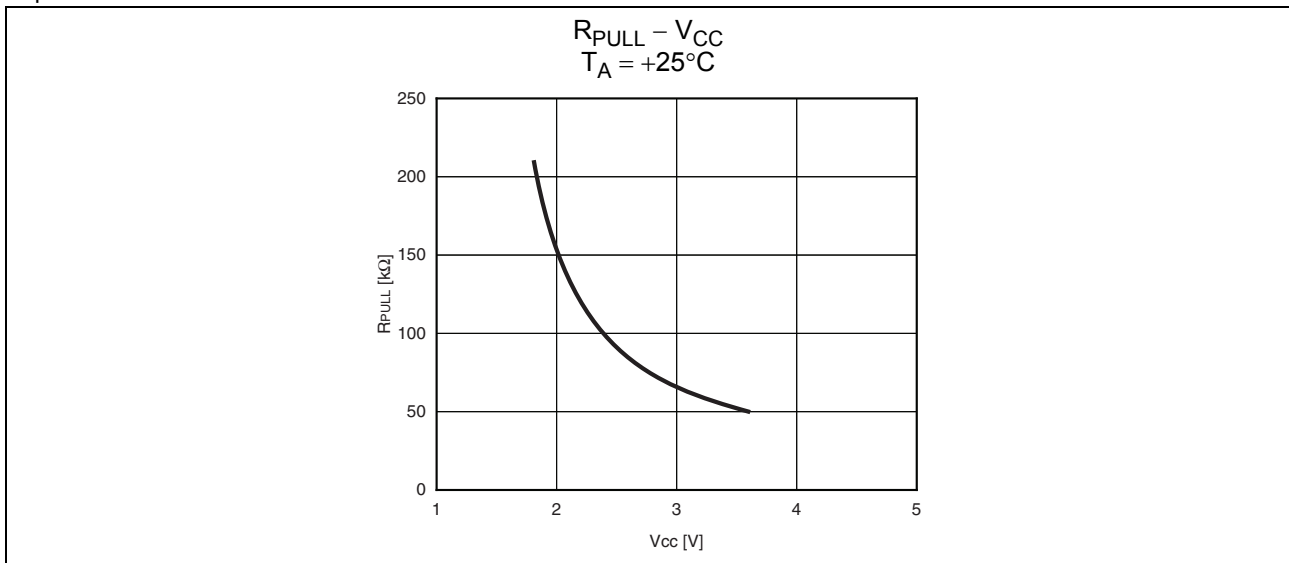
■ Input voltage characteristics



■ Output voltage characteristics



■ Pull-up characteristics



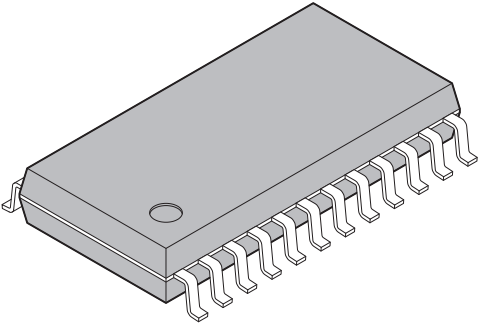
**16. Mask Options**

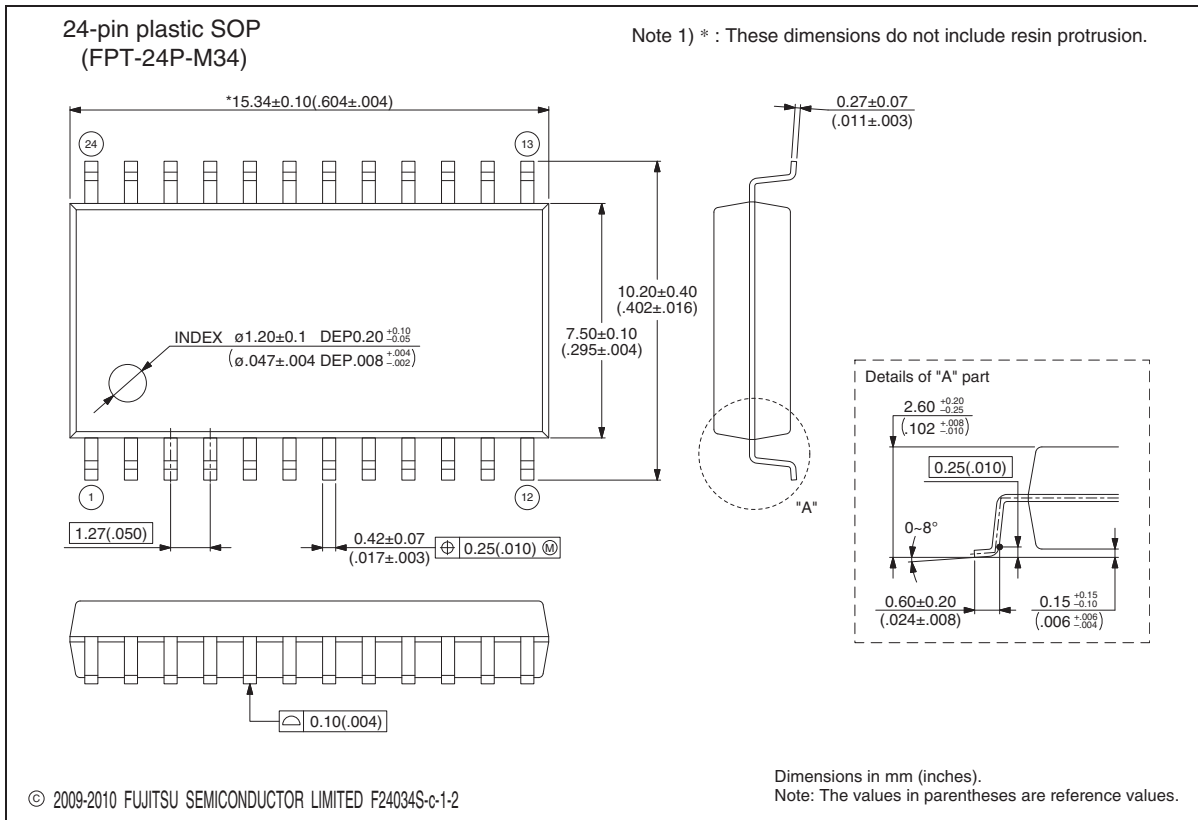
No.	Part Number	MB95F352E MB95F353E MB95F354E	MB95F352L MB95F353L MB95F354L
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	With low-voltage detection reset	Without low-voltage detection reset
2	Reset	Without dedicated reset input	With dedicated reset input

**17. Ordering Information**

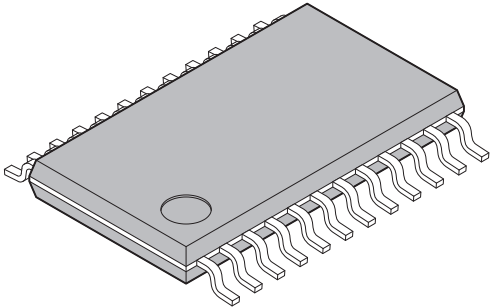
Part Number	Package
MB95F352EPF-G-SNE2 MB95F352LPF-G-SNE2 MB95F353EPF-G-SNE2 MB95F353LPF-G-SNE2 MB95F354EPF-G-SNE2 MB95F354LPF-G-SNE2	24-pin plastic SOP (FPT-24P-M34)
MB95F352EPFT-G-SNE2 MB95F352LPFT-G-SNE2 MB95F353EPFT-G-SNE2 MB95F353LPFT-G-SNE2 MB95F354EPFT-G-SNE2 MB95F354LPFT-G-SNE2	24-pin plastic TSSOP (FPT-24P-M10)
MB95F352EWQN-G-SNE1 MB95F352EWQN-G-SNERE1 MB95F352LWQN-G-SNE1 MB95F352LWQN-G-SNERE1 MB95F353EWQN-G-SNE1 MB95F353EWQN-G-SNERE1 MB95F353LWQN-G-SNE1 MB95F353LWQN-G-SNERE1 MB95F354EWQN-G-SNE1 MB95F354EWQN-G-SNERE1 MB95F354LWQN-G-SNE1 MB95F354LWQN-G-SNERE1	32-pin plastic QFN (LCC-32P-M19)

**18. Package Dimension**

<p>24-pin plastic SOP</p>  <p>(FPT-24P-M34)</p>	Lead pitch	1.27 mm
	Package width × package length	7.50 mm × 15.34 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	2.80 mm MAX
	Weight	0.44 g

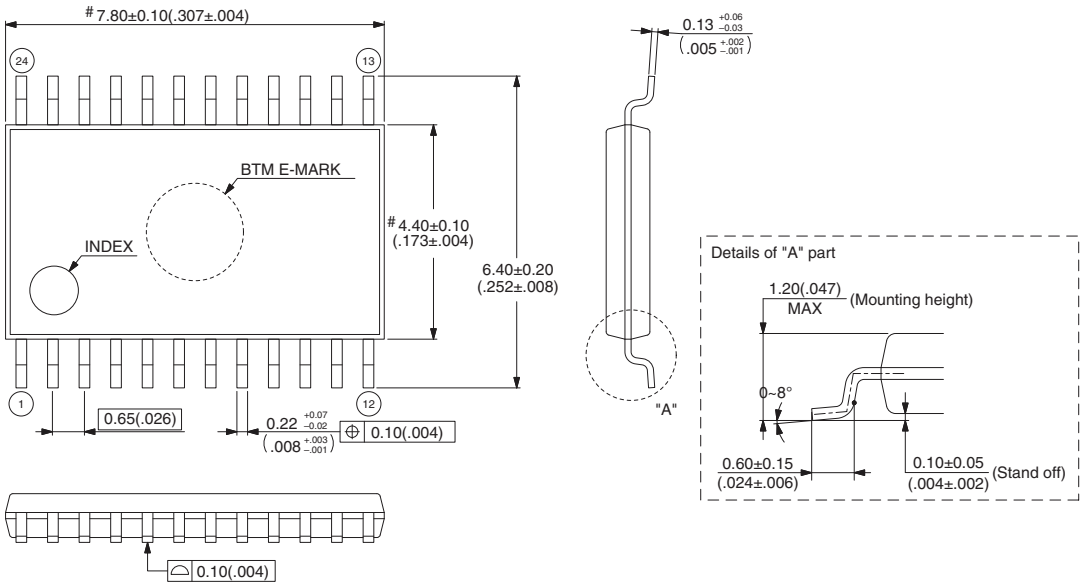


(Continued)

<p>24-pin plastic TSSOP</p>  <p>(FPT-24P-M10)</p>	Lead pitch	0.65 mm
	Package width × package length	4.40 mm × 7.80 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.10 g

24-pin plastic TSSOP (FPT-24P-M10)

Note 1) Pins width and pins thickness include plating thickness.  
 Note 2) Pins width do not include tie bar cutting remainder.  
 Note 3) #: These dimensions do not include resin protrusion.



Top view dimensions:  
 # 7.80±0.10 (.307±.004)  
 # 4.40±0.10 (.173±.004)  
 6.40±0.20 (.252±.008)  
 0.65 (.026)  
 0.22<sup>+0.07</sup>/<sub>-.008</sub> (.008<sup>+0.003</sup>/<sub>-.001</sub>)  
 0.10 (.004)  
 INDEX  
 BTM E-MARK

Side view dimensions:  
 0.13<sup>+0.06</sup>/<sub>-.005</sub> (.005<sup>-.002</sup>/<sub>-.001</sub>)

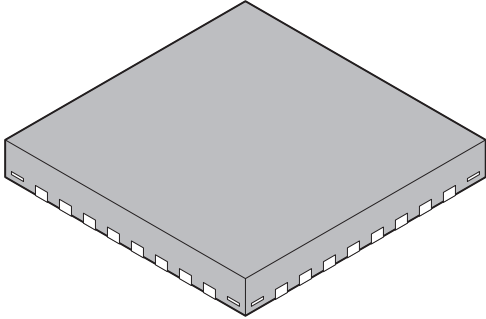
Details of "A" part:  
 1.20 (.047) MAX (Mounting height)  
 0~8°  
 0.60±0.15 (.024±.006)  
 0.10±0.05 (.004±.002) (Stand off)

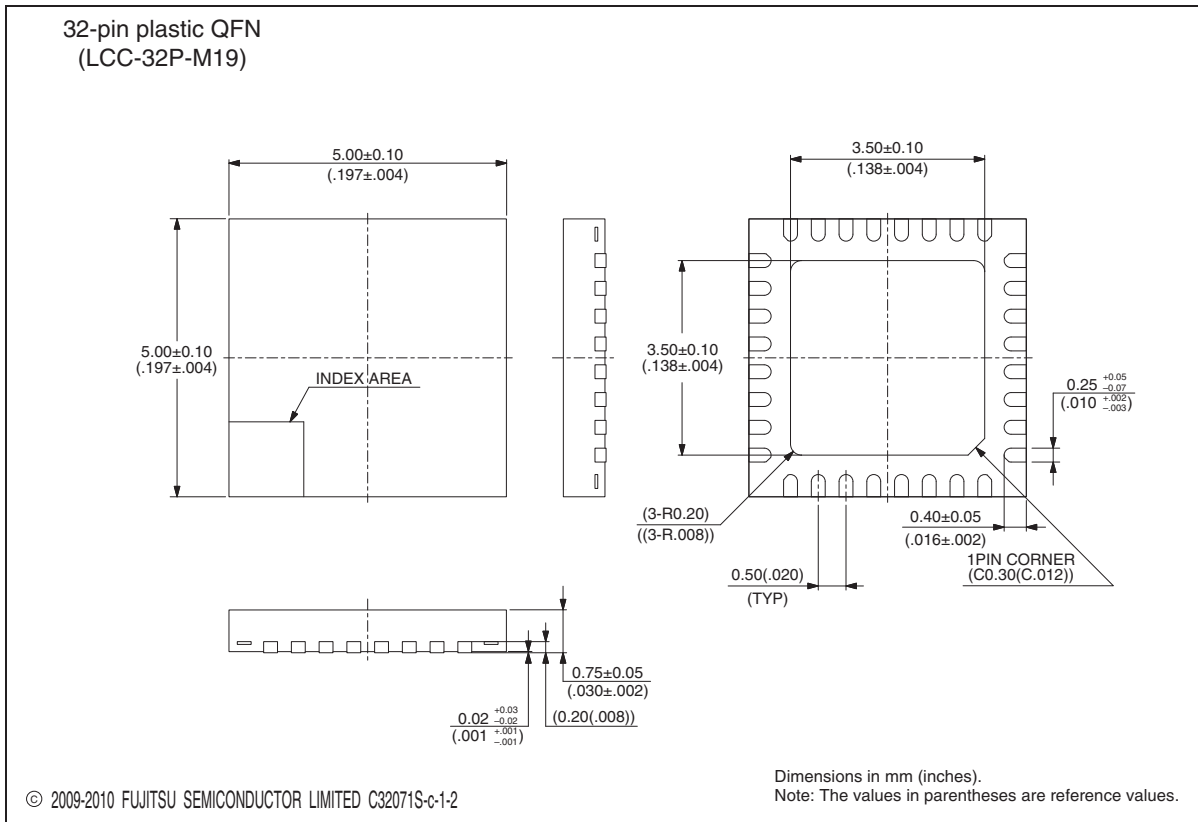
© 2008-2010 FUJITSU SEMICONDUCTOR LIMITED F24033S-c-1-2

Dimensions in mm (inches).  
 Note: The values in parentheses are reference values.

(Continued)

(Continued)

<p style="text-align: center;">32-pin plastic QFN</p>  <p style="text-align: center;">(LCC-32P-M19)</p>	Lead pitch	0.50 mm	
	Package width × package length	5.00 mm × 5.00 mm	
	Sealing method	Plastic mold	
	Mounting height	0.80 mm MAX	
	Weight	0.06 g	



**19. Major Changes**

Page	Section	Details																																														
7	Pin Assignment	Deleted the HCLK1 pin and the HCLK2 pin.																																														
9	Pin Description (24-pin MCU)	Deleted the HCLK1 pin and the HCLK2 pin.																																														
11	Pin Description (32-pin MCU)	Deleted the HCLK1 pin and the HCLK2 pin.																																														
16	Block Diagram	Deleted the HCLK1 pin and the HCLK2 pin.																																														
26	Electrical Characteristics DC Characteristics	Changed the value of $V_{CC}$ in the operating conditions. 3.0 V to 3.6 V → 2.7 V to 3.6 V																																														
27		<p>Changed the value of <math>V_{CC}</math> in the operating conditions. 3.6 V → 1.8 V to 3.6 V</p> <p>Changed the typical (Typ) values and the maximum (Max) values of <math>I_{CC}</math>.</p> <table border="1"> <thead> <tr> <th colspan="3">Value</th> <th rowspan="2">Unit</th> <th rowspan="2">Remarks</th> </tr> <tr> <th>Min</th> <th>Typ</th> <th>Max</th> </tr> </thead> <tbody> <tr> <td>—</td> <td>13.6</td> <td>22.4</td> <td>mA</td> <td>Flash memory product (except writing and erasing)</td> </tr> <tr> <td>—</td> <td>38.1</td> <td>44.9</td> <td>mA</td> <td>Flash memory product (at writing and erasing)</td> </tr> <tr> <td>—</td> <td>15.1</td> <td>24.6</td> <td>mA</td> <td>At A/D conversion</td> </tr> </tbody> </table> <p>→</p> <table border="1"> <thead> <tr> <th colspan="3">Value</th> <th rowspan="2">Unit</th> <th rowspan="2">Remarks</th> </tr> <tr> <th>Min</th> <th>Typ*3</th> <th>Max</th> </tr> </thead> <tbody> <tr> <td>—</td> <td>11.2</td> <td>20</td> <td>mA</td> <td>Flash memory product (except writing and erasing)</td> </tr> <tr> <td>—</td> <td>26.2</td> <td>38</td> <td>mA</td> <td>Flash memory product (at writing and erasing)</td> </tr> <tr> <td>—</td> <td>13.3</td> <td>23.4</td> <td>mA</td> <td>At A/D conversion</td> </tr> </tbody> </table> <p>Changed the Typ value of <math>I_{CCS}</math>. 6.3 → 5.2</p> <p>Changed the Typ value and the Max value of <math>I_{CCL}</math>. Typ : 20 → 15 Max : 45 → 35</p> <p>Changed the Typ value and the Max value of <math>I_{CCLS}</math>. Typ : 6.3 → 5 Max : 30 → 15</p> <p>Changed the Typ value and the Max value of <math>I_{CCT}</math>. Typ : 2 → 1 Max : 22 → 10</p>	Value			Unit	Remarks	Min	Typ	Max	—	13.6	22.4	mA	Flash memory product (except writing and erasing)	—	38.1	44.9	mA	Flash memory product (at writing and erasing)	—	15.1	24.6	mA	At A/D conversion	Value			Unit	Remarks	Min	Typ*3	Max	—	11.2	20	mA	Flash memory product (except writing and erasing)	—	26.2	38	mA	Flash memory product (at writing and erasing)	—	13.3	23.4	mA	At A/D conversion
Value			Unit	Remarks																																												
Min	Typ	Max																																														
—	13.6	22.4	mA	Flash memory product (except writing and erasing)																																												
—	38.1	44.9	mA	Flash memory product (at writing and erasing)																																												
—	15.1	24.6	mA	At A/D conversion																																												
Value			Unit	Remarks																																												
Min	Typ*3	Max																																														
—	11.2	20	mA	Flash memory product (except writing and erasing)																																												
—	26.2	38	mA	Flash memory product (at writing and erasing)																																												
—	13.3	23.4	mA	At A/D conversion																																												

(Continued)

(Continued)

Page	Section	Details
27	Electrical Characteristics DC Characteristics	<p>Changed the Typ value of <math>I_{CCMCR}</math>. 11 → 9</p> <p>Changed the Typ value of <math>I_{CCSCR}</math>. 110 → 77</p> <p>Changed the Typ value of <math>I_{CCTS}</math>. 1.8 → 1.1</p> <p>Changed the Typ value of <math>I_{CCH}</math>. 1 → 0.1</p>
28		<p>Changed the Typ value of <math>I_{LVD}</math>. 8 → 6.4</p> <p>Changed the Typ value of <math>I_{CRH}</math>. 0.5 → 0.25</p> <p>Added the following note: *3: <math>V_{CC} = 3.0\text{ V}</math>, <math>T_A = +25^\circ\text{C}</math></p>
29	Electrical Characteristics AC Characteristics	Deleted all information about the HCLK1 pin and the HCLK2 pin in the table.
30	Clock Timing	<p>Deleted HCLK1 and HCLK2 in the “• Input waveform generated when an external clock (main clock) is used”.</p> <p>Deleted the external connection diagram for the HCLK1 pin and HCLK2 pin in “• Figure of main clock input port external connection”.</p>
43	Electrical Characteristics AC Characteristics Low-voltage Detection	Deleted the following parameters: Power hysteresis width 0, Power hysteresis width 1, Power hysteresis width 2, Interrupt hysteresis width 0, Interrupt hysteresis width 1, Interrupt hysteresis width 2, Interrupt hysteresis width 3, Interrupt hysteresis width 4
44		Deleted $V_{PHYS}/V_{IHYS}$ from the diagram.
54 to 59	Sample Characteristics	Added diagrams showing sample characteristics.
61	Ordering Information	<p>Added the following part numbers for the 32-pin plastic QFN package (LCC-32P-M19):</p> <p>MB95F352EWQN-G-SNE1            MB95F352LWQN-G-SNE1            MB95F353EWQN-G-SNE1            MB95F353LWQN-G-SNE1            MB95F354EWQN-G-SNE1            MB95F354LWQN-G-SNE1</p>

**Document History**

Document Title: MB95F352E/F352L/F353E/F353L/F354E/F354L CMOS F <sup>2</sup> MC-8FX MB95350L Series 8-bit Microcontrollers				
Document Number: 002-07527				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	AKIH	04/13/2010	Migrated to Cypress and assigned document number 002-07527. No change to document contents or format.
*A	5183750	AKIH	03/31/2016	Updated to Cypress template

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

#### Products

ARM® Cortex® Microcontrollers	<a href="http://cypress.com/arm">cypress.com/arm</a>
Automotive	<a href="http://cypress.com/automotive">cypress.com/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/clocks">cypress.com/clocks</a>
Interface	<a href="http://cypress.com/interface">cypress.com/interface</a>
Lighting & Power Control	<a href="http://cypress.com/powerpsoc">cypress.com/powerpsoc</a>
Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
USB Controllers	<a href="http://cypress.com/usb">cypress.com/usb</a>
Wireless/RF	<a href="http://cypress.com/wireless">cypress.com/wireless</a>

#### PSoC® Solutions

[cypress.com/psoc](http://cypress.com/psoc)  
PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

#### Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

#### Technical Support

[cypress.com/support](http://cypress.com/support)

© Cypress Semiconductor Corporation 2010 - 2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you under its copyright rights in the Software, a personal, non-exclusive, nontransferable license (without the right to sublicense) (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units. Cypress also grants you a personal, non-exclusive, nontransferable, license (without the right to sublicense) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely to the minimum extent that is necessary for you to exercise your rights under the copyright license granted in the previous sentence. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and Company shall and hereby does release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. Company shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View MB95F354LWQN-G-SNE1 on WIN SOURCE](#)
- ⊖ [Infineon Technologies](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management