



**THE DATASHEET OF  
LMP7712MME/NOPB**



## Single and Dual Precision, 17 MHz, Low Noise, CMOS Input Amplifiers

Check for Samples: [LMP7711](#)

### FEATURES

- Unless Otherwise Noted, Typical Values at  $V_S = 5V$ .
- Input Offset Voltage  $\pm 150 \mu V$  (Max)
- Input Bias Current 100 fA
- Input Voltage Noise 5.8 nV/ $\sqrt{Hz}$
- Gain Bandwidth Product 17 MHz
- Supply Current (LMP7711) 1.15 mA
- Supply Current (LMP7712) 1.30 mA
- Supply Voltage Range 1.8V to 5.5V
- THD+N @  $f = 1 \text{ kHz}$  0.001%
- Operating Temperature Range  $-40^\circ C$  to  $125^\circ C$
- Rail-to-rail Output Swing
- Space Saving SOT Package (LMP7711)
- 10-pin VSSOP Package (LMP7712)

### APPLICATIONS

- Active Filters and Buffers
- Sensor Interface Applications
- Transimpedance Amplifiers

### DESCRIPTION

The LMP7711/LMP7712 are single and dual low noise, low offset, CMOS input, rail-to-rail output precision amplifiers with a high gain bandwidth product and an enable pin. The LMP7711/LMP7712 are part of the LMP™ precision amplifier family and are ideal for a variety of instrumentation applications.

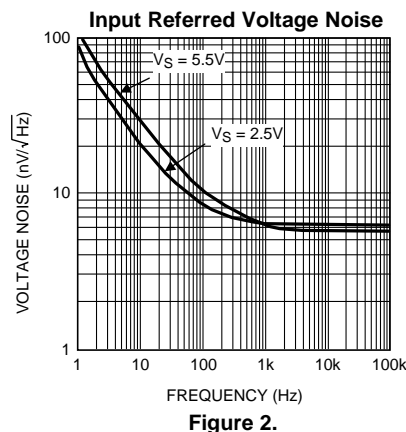
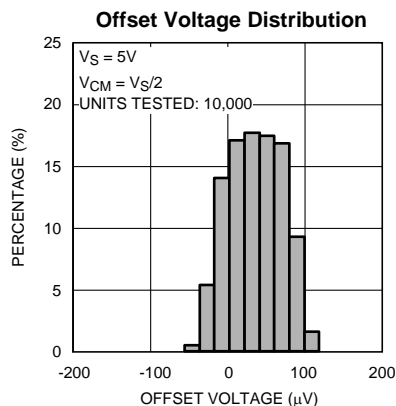
Utilizing a CMOS input stage, the LMP7711/LMP7712 achieve an input bias current of 100 fA, an input referred voltage noise of 5.8 nV/ $\sqrt{Hz}$ , and an input offset voltage of less than  $\pm 150 \mu V$ . These features make the LMP7711/LMP7712 superior choices for precision applications.

Consuming only 1.15 mA of supply current, the LMP7711 offers a high gain bandwidth product of 17 MHz, enabling accurate amplification at high closed loop gains.

The LMP7711/LMP7712 have a supply voltage range of 1.8V to 5.5V, which makes these ideal choices for portable low power applications with low supply voltage requirements. In order to reduce the already low power consumption the LMP7711/LMP7712 have an enable function. Once in shutdown, the LMP7711/LMP7712 draw only 140 nA of supply current.

The LMP7711/LMP7712 are built with TI's advanced VIP50 process technology. The LMP7711 is offered in a 6-pin SOT package and the LMP7712 is offered in a 10-pin VSSOP.

### TYPICAL PERFORMANCE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LMP is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>

ESD Tolerance <sup>(3)</sup>	Human Body Model	2000V
	Machine Model	200V
	Charge-Device Model	1000V
$V_{IN}$ Differential		±0.3V
Supply Voltage ( $V_S = V^+ - V^-$ )		6.0V
Voltage on Input/Output Pins		$V^+ +0.3V, V^- -0.3V$
Storage Temperature Range		-65°C to 150°C
Junction Temperature <sup>(4)</sup>		+150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temp. (10 sec)	260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
- (4) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$ . All numbers apply for packages soldered directly onto a PC Board.

### OPERATING RATINGS<sup>(1)</sup>

Temperature Range <sup>(2)</sup>		-40°C to 125°C
Supply Voltage ( $V_S = V^+ - V^-$ )	$0^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	1.8V to 5.5V
	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	2.0V to 5.5V
Package Thermal Resistance ( $\theta_{JA}$ ) <sup>(2)</sup>	6-Pin SOT	170°C/W
	10-Pin VSSOP	236°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (2) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$ . All numbers apply for packages soldered directly onto a PC Board.

## 2.5V ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all limits are ensured for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 2.5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_O = V_{CM} = V^+/2$ ,  $V_{EN} = V^+$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ <sup>(2)</sup>	Max <sup>(1)</sup>	Units
$V_{OS}$	Input Offset Voltage			±20	±180 ±480	μV
TC $V_{OS}$	Input Offset Voltage Temperature Drift <sup>(3)(4)</sup>	LMP7711	-1.75	-1	±4	μV/°C
		LMP7712				
$I_B$	Input Bias Current	$V_{CM} = 1.0\text{V}^{(5)(4)}$	-40°C ≤ $T_A$ ≤ 85°C	0.05	1 <b>25</b>	pA
			-40°C ≤ $T_A$ ≤ 125°C		0.05	
$I_{OS}$	Input Offset Current	$V_{CM} = 1.0\text{V}^{(4)}$		0.006	0.5 <b>50</b>	pA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 1.4\text{V}$	83 <b>80</b>	100		dB
PSRR	Power Supply Rejection Ratio	$2.0\text{V} \leq V^+ \leq 5.5\text{V}$ $V^- = 0\text{V}$ , $V_{CM} = 0$	85 <b>80</b>	100		dB
		$1.8\text{V} \leq V^+ \leq 5.5\text{V}$ $V^- = 0\text{V}$ , $V_{CM} = 0$	85	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB	-0.3 <b>-0.3</b>		1.5 <b>1.5</b>	V
$A_{VOL}$	Open Loop Voltage Gain	LMP7711, $V_O = 0.15$ to $2.2\text{V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$	88 <b>82</b>	98		dB
		LMP7712, $V_O = 0.15$ to $2.2\text{V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$	84 <b>80</b>	92		
		LMP7711, $V_O = 0.15$ to $2.2\text{V}$ $R_L = 10\text{ k}\Omega$ to $V^+/2$	92 <b>88</b>	114		
		LMP7712, $V_O = 0.15$ to $2.2\text{V}$ $R_L = 10\text{ k}\Omega$ to $V^+/2$	90 <b>86</b>	95		
$V_{OUT}$	Output Voltage Swing High	$R_L = 2\text{ k}\Omega$ to $V^+/2$		25	70 <b>77</b>	mV from either rail
		$R_L = 10\text{ k}\Omega$ to $V^+/2$		20	60 <b>66</b>	
	Output Voltage Swing Low	$R_L = 2\text{ k}\Omega$ to $V^+/2$		30	70 <b>73</b>	
		$R_L = 10\text{ k}\Omega$ to $V^+/2$		15	60 <b>62</b>	
$I_{OUT}$	Output Current	Sourcing to $V^-$ $V_{IN} = 200\text{ mV}^{(6)}$	36 <b>30</b>	52		mA
		Sinking to $V^+$ $V_{IN} = -200\text{ mV}^{(6)}$	7.5 <b>5.0</b>	15		
$I_S$	Supply Current	LMP7711 Enable Mode $V_{EN} \geq 2.1$		0.95	1.30 <b>1.65</b>	mA
		LMP7712 (per channel) Enable Mode $V_{EN} \geq 2.1$		1.10	1.50 <b>1.85</b>	
		Shutdown Mode (per channel) $V_{EN} \leq 0.4$		0.03	1 <b>4</b>	μA
SR	Slew Rate	$A_V = +1$ , Rising (10% to 90%)		8.3		V/μs
		$A_V = +1$ , Falling (90% to 10%)		10.3		

- (1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
- (3) Offset voltage average drift is determined by dividing the change in  $V_{OS}$  at the temperature extremes by the total temperature change.
- (4) This parameter is specified by design and/or characterization and is not tested in production.
- (5) Positive current corresponds to current flowing into the device.
- (6) The short circuit test is a momentary open loop test.

## 2.5V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted, all limits are ensured for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 2.5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_O = V_{\text{CM}} = V^+/2$ ,  $V_{\text{EN}} = V^+$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ <sup>(2)</sup>	Max <sup>(1)</sup>	Units
GBW	Gain Bandwidth			14		MHz
$e_n$	Input Referred Voltage Noise Density	$f = 400\text{ Hz}$		6.8		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		5.8		
$i_n$	Input Referred Current Noise Density	$f = 1\text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$
$t_{\text{on}}$	Turn-on Time			140		ns
$t_{\text{off}}$	Turn-off Time			1000		ns
$V_{\text{EN}}$	Enable Pin Voltage Range	Enable Mode	2.1	2 - 2.5		V
		Shutdown Mode		0 - 0.5	0.4	
$I_{\text{EN}}$	Enable Pin Input Current	$V_{\text{EN}} = 2.5\text{V}^{(5)}$		1.5	3.0	$\mu\text{A}$
		$V_{\text{EN}} = 0\text{V}^{(5)}$		0.003	0.1	
THD+N	Total Harmonic Distortion + Noise	$f = 1\text{ kHz}$ , $A_V = 1$ , $R_L = 100\text{ k}\Omega$ $V_O = 0.9\text{ V}_{\text{PP}}$		0.003		%
		$f = 1\text{ kHz}$ , $A_V = 1$ , $R_L = 600\Omega$ $V_O = 0.9\text{ V}_{\text{PP}}$		0.004		

## 5V ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all limits are ensured for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2$ ,  $V_{\text{EN}} = V^+$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ <sup>(2)</sup>	Max <sup>(1)</sup>	Units
$V_{\text{OS}}$	Input Offset Voltage			$\pm 10$	$\pm 150$ <b><math>\pm 450</math></b>	$\mu\text{V}$
TC $V_{\text{OS}}$	Input Offset Voltage Temperature Drift <sup>(3)(4)</sup>	LMP7711	-1.75	-1	$\pm 4$	$\mu\text{V}/^\circ\text{C}$
		LMP7712				
$I_{\text{B}}$	Input Bias Current	$V_{\text{CM}} = 2.0\text{V}^{(5)(4)}$	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0.1	1 <b>25</b>	$\text{pA}$
			$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	0.1	1 <b>100</b>	
$I_{\text{OS}}$	Input Offset Current	$V_{\text{CM}} = 2.0\text{V}^{(4)}$		0.01	0.5 <b>50</b>	$\text{pA}$
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 3.7\text{V}$	85 <b>82</b>	100		dB
PSRR	Power Supply Rejection Ratio	$2.0\text{V} \leq V^+ \leq 5.5\text{V}$ $V^- = 0\text{V}$ , $V_{\text{CM}} = 0$	85 <b>80</b>	100		dB
		$1.8\text{V} \leq V^+ \leq 5.5\text{V}$ $V^- = 0\text{V}$ , $V_{\text{CM}} = 0$	85	98		
CMVR	Common Mode Voltage Range	CMRR $\geq 80\text{ dB}$ CMRR $\geq 78\text{ dB}$	-0.3 <b>-0.3</b>		4 <b>4</b>	V

- (1) Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
- (3) Offset voltage average drift is determined by dividing the change in  $V_{\text{OS}}$  at the temperature extremes by the total temperature change.
- (4) This parameter is specified by design and/or characterization and is not tested in production.
- (5) Positive current corresponds to current flowing into the device.

**5V ELECTRICAL CHARACTERISTICS (continued)**

Unless otherwise noted, all limits are ensured for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2$ ,  $V_{\text{EN}} = V^+$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ <sup>(2)</sup>	Max <sup>(1)</sup>	Units
A <sub>VOL</sub>	Open Loop Voltage Gain	LMP7711, $V_O = 0.3$ to $4.7\text{V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$	88 <b>82</b>	107		dB
		LMP7712, $V_O = 0.3$ to $4.7\text{V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$	84 <b>80</b>	90		
		LMP7711, $V_O = 0.3$ to $4.7\text{V}$ $R_L = 10\text{ k}\Omega$ to $V^+/2$	92 <b>88</b>	114		
		LMP7712, $V_O = 0.3$ to $4.7\text{V}$ $R_L = 10\text{ k}\Omega$ to $V^+/2$	90 <b>86</b>	95		
V <sub>OUT</sub>	Output Voltage Swing High	$R_L = 2\text{ k}\Omega$ to $V^+/2$		32	70 <b>77</b>	mV from either rail
		$R_L = 10\text{ k}\Omega$ to $V^+/2$		22	60 <b>66</b>	
	Output Voltage Swing Low	$R_L = 2\text{ k}\Omega$ to $V^+/2$ (LMP7711)		42	70 <b>73</b>	
		$R_L = 2\text{ k}\Omega$ to $V^+/2$ (LMP7712)		50	75 <b>78</b>	
	$R_L = 10\text{ k}\Omega$ to $V^+/2$		20	60 <b>62</b>		
I <sub>OUT</sub>	Output Current	Sourcing to $V^-$ $V_{\text{IN}} = 200\text{ mV}^{(6)}$	46 <b>38</b>	66		mA
		Sinking to $V^+$ $V_{\text{IN}} = -200\text{ mV}^{(6)}$	10.5 <b>6.5</b>	23		
I <sub>S</sub>	Supply Current	LMP7711 Enable Mode $V_{\text{EN}} \geq 4.6$		1.15	1.40 <b>1.75</b>	mA
		LMP7712 (per channel) Enable Mode $V_{\text{EN}} \geq 4.6$		1.30	1.70 <b>2.05</b>	
		Shutdown Mode $V_{\text{EN}} \leq 0.4$ (per channel)		0.14	1 <b>4</b>	$\mu\text{A}$
SR	Slew Rate	$A_V = +1$ , Rising (10% to 90%)	6.0	9.5		$\text{V}/\mu\text{s}$
		$A_V = +1$ , Falling (90% to 10%)	7.5	11.5		
GBW	Gain Bandwidth			17		MHz
e <sub>n</sub>	Input Referred Voltage Noise Density	$f = 400\text{ Hz}$		7.0		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		5.8		
i <sub>n</sub>	Input Referred Current Noise Density	$f = 1\text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$
t <sub>on</sub>	Turn-on Time			114		ns
t <sub>off</sub>	Turn-off Time			800		ns
V <sub>EN</sub>	Enable Pin Voltage Range	Enable Mode	4.6	4.5 – 5		V
		Shutdown Mode		0 – 0.5	0.4	
I <sub>EN</sub>	Enable Pin Input Current	$V_{\text{EN}} = 5\text{V}^{(7)}$		5.6	10	$\mu\text{A}$
		$V_{\text{EN}} = 0\text{V}^{(7)}$		0.005	0.2	
THD+N	Total Harmonic Distortion + Noise	$f = 1\text{ kHz}$ , $A_V = 1$ , $R_L = 100\text{ k}\Omega$ $V_O = 4\text{ V}_{\text{PP}}$		0.001		%
		$f = 1\text{ kHz}$ , $A_V = 1$ , $R_L = 600\Omega$ $V_O = 4\text{ V}_{\text{PP}}$		0.004		

(6) The short circuit test is a momentary open loop test.

(7) Positive current corresponds to current flowing into the device.

CONNECTION DIAGRAM

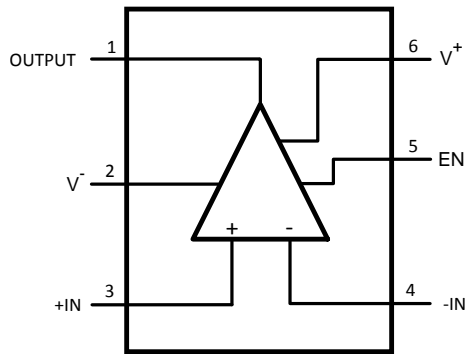


Figure 3. 6-Pin SOT - Top View  
See Package Number DDC

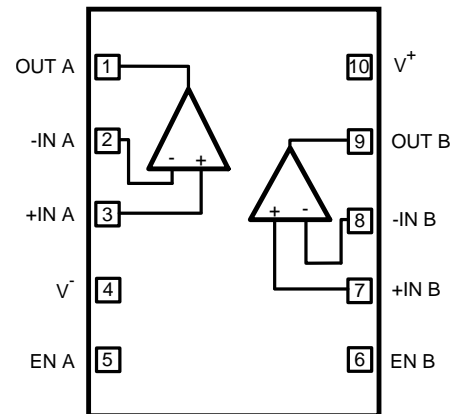


Figure 4. 10-Pin VSSOP-Top View  
See Package Number DGS

**TYPICAL PERFORMANCE CHARACTERISTICS**

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{CM} = V_S/2$ ,  $V_{EN} = V^+$ .

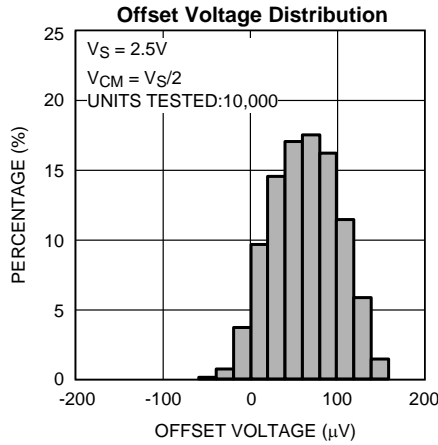


Figure 5.

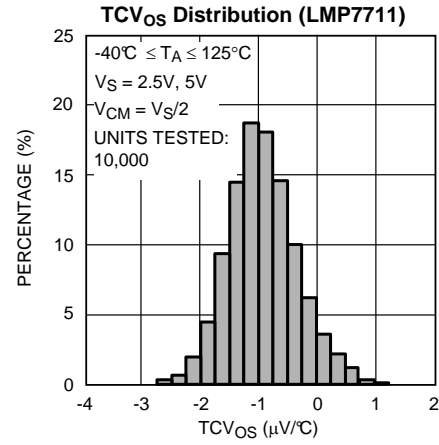


Figure 6.

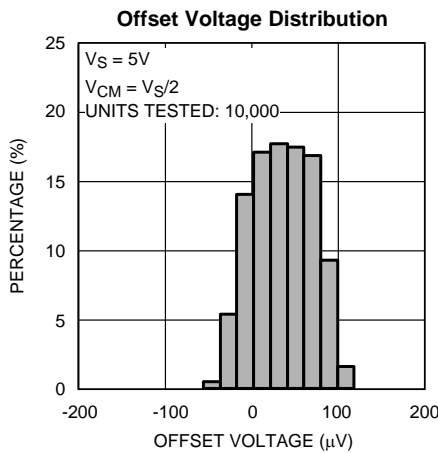


Figure 7.

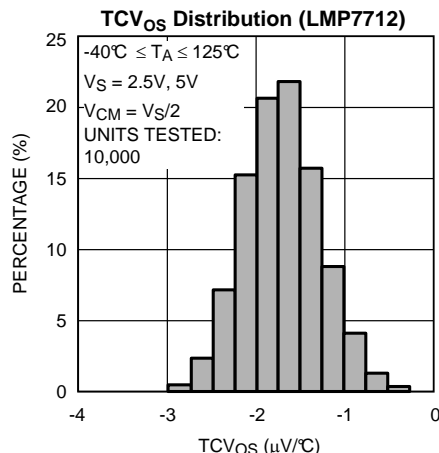


Figure 8.

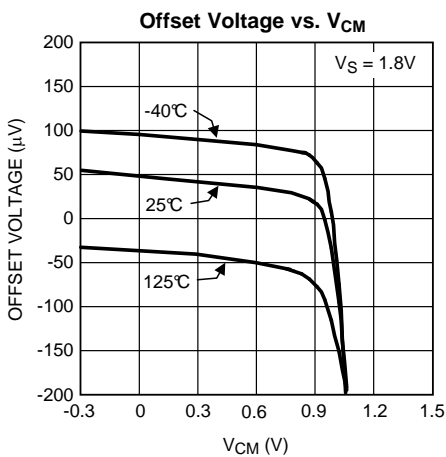


Figure 9.

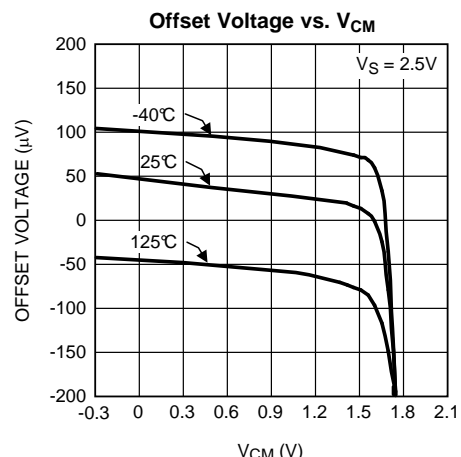


Figure 10.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{CM} = V_S/2$ ,  $V_{EN} = V^+$ .

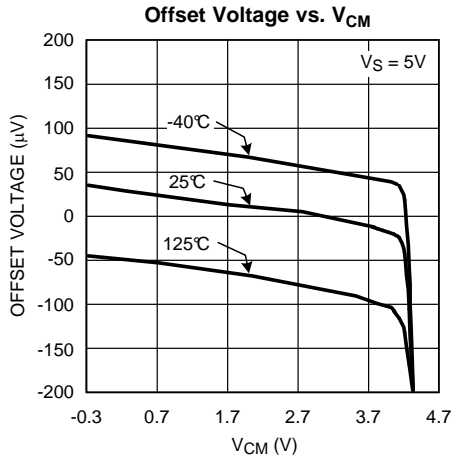


Figure 11.

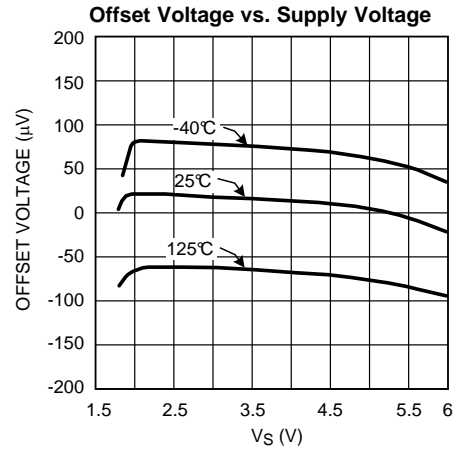


Figure 12.

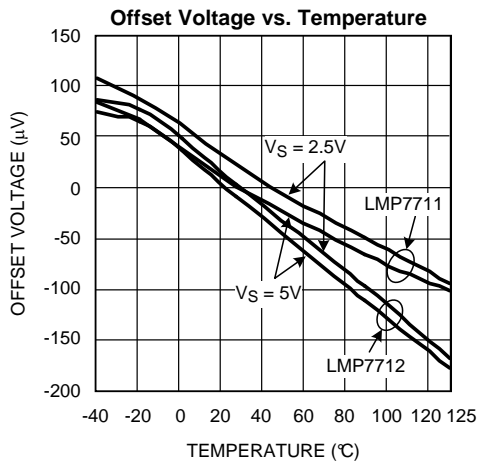


Figure 13.

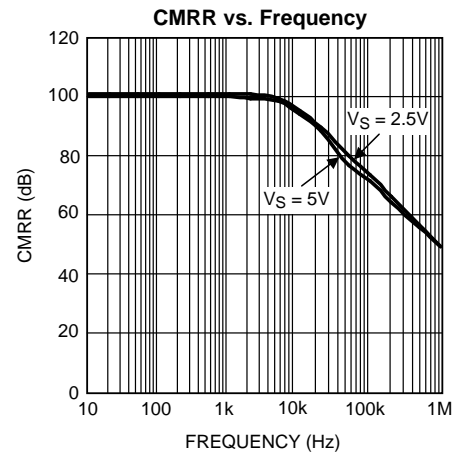


Figure 14.

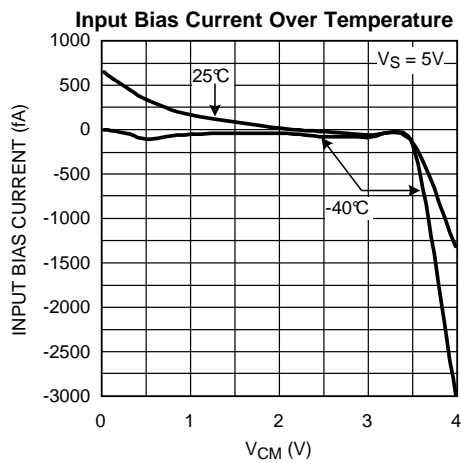


Figure 15.

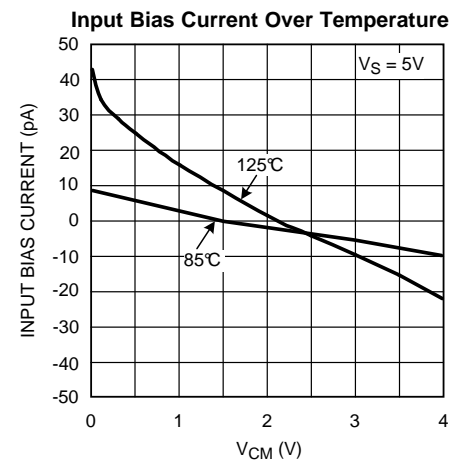


Figure 16.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{CM} = V_S/2$ ,  $V_{EN} = V^+$ .

**Supply Current vs. Supply Voltage (LMP7711)**

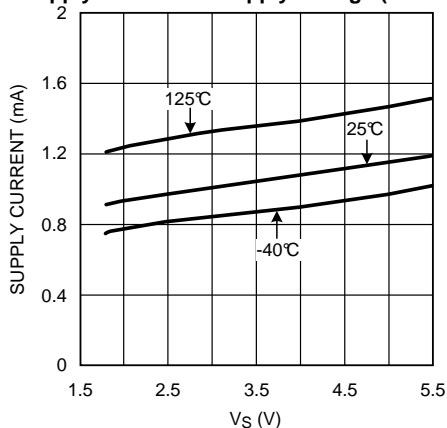


Figure 17.

**Supply Current vs. Supply Voltage (LMP7712)**

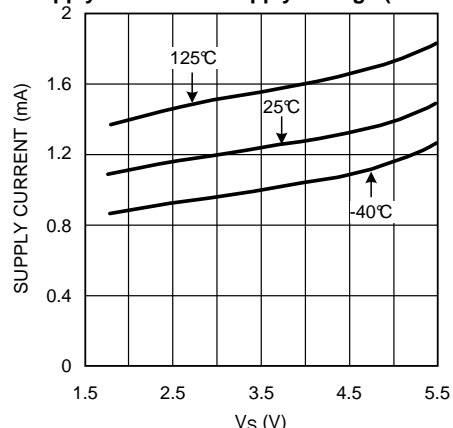


Figure 18.

**Supply Current vs. Supply Voltage (Shutdown)**

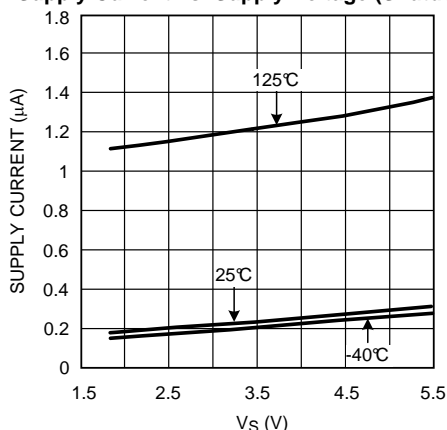


Figure 19.

**Crosstalk Rejection Ratio (LMP7712)**

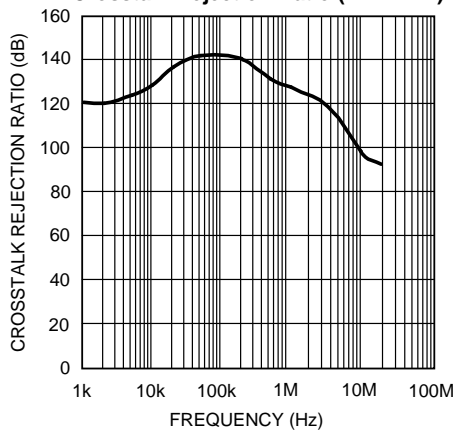


Figure 20.

**Supply Current vs. Enable Pin Voltage (LMP7711)**

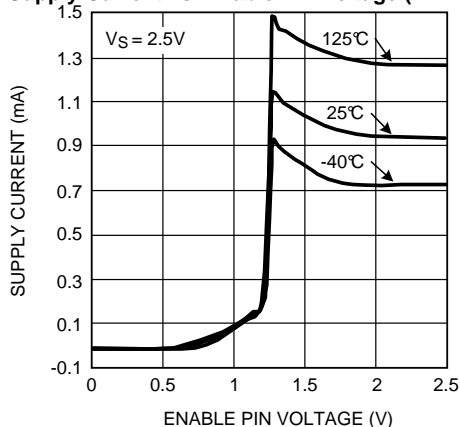


Figure 21.

**Supply Current vs. Enable Pin Voltage (LMP7711)**

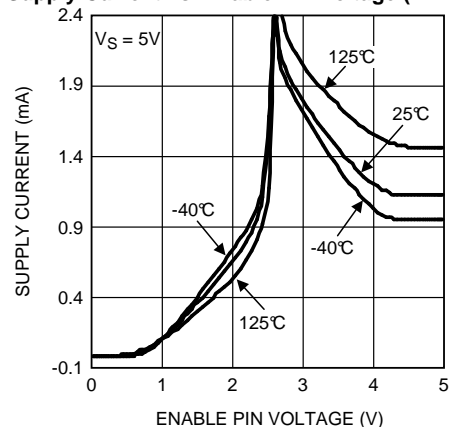
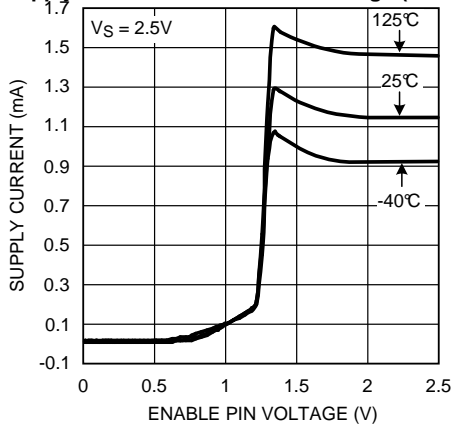


Figure 22.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

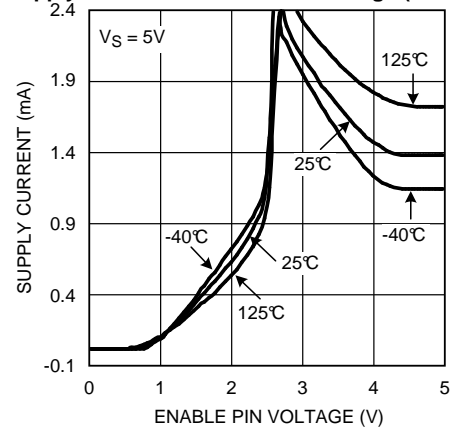
Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{CM} = V_S/2$ ,  $V_{EN} = V^+$ .

**Supply Current vs. Enable Pin Voltage (LMP7712)**



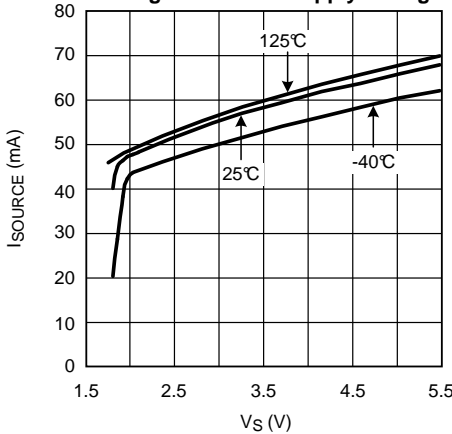
**Figure 23.**

**Supply Current vs. Enable Pin Voltage (LMP7712)**



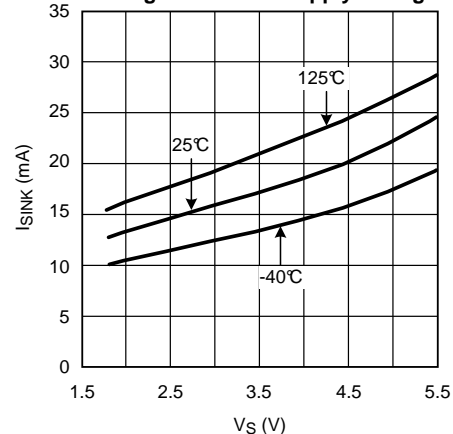
**Figure 24.**

**Sourcing Current vs. Supply Voltage**



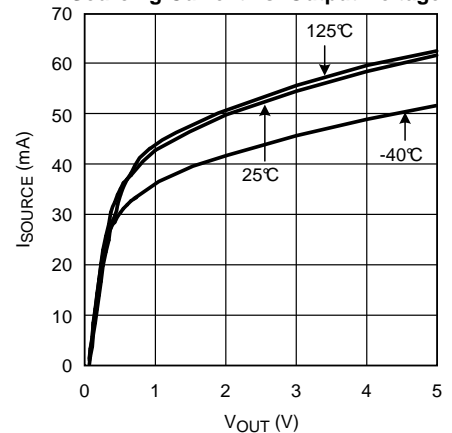
**Figure 25.**

**Sinking Current vs. Supply Voltage**



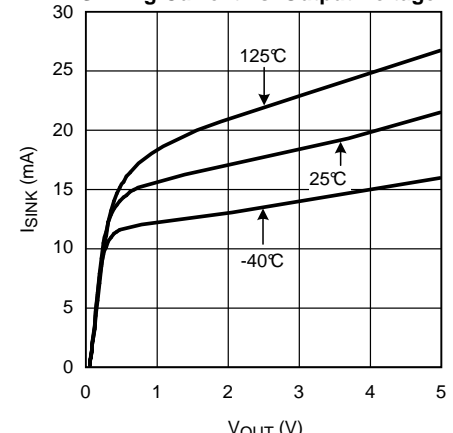
**Figure 26.**

**Sourcing Current vs. Output Voltage**



**Figure 27.**

**Sinking Current vs. Output Voltage**



**Figure 28.**

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{CM} = V_S/2$ ,  $V_{EN} = V^+$ .

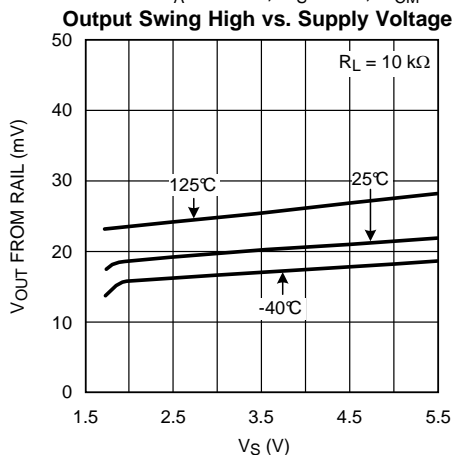


Figure 29.

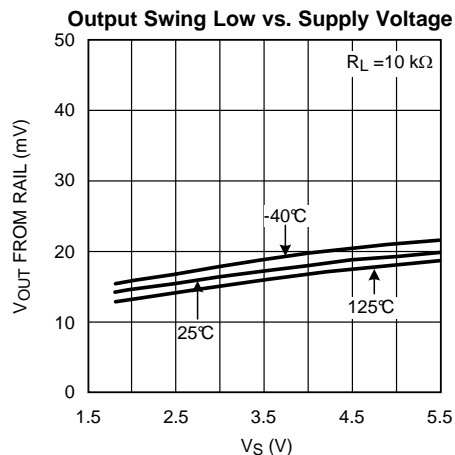


Figure 30.

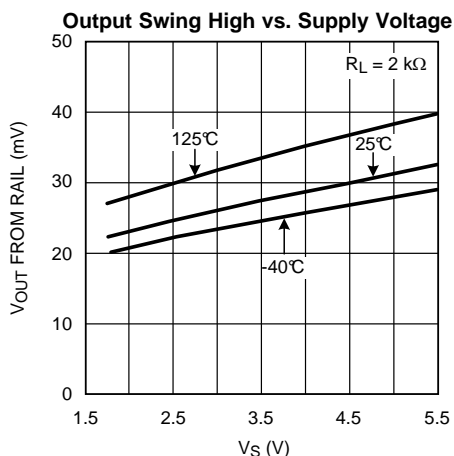


Figure 31.

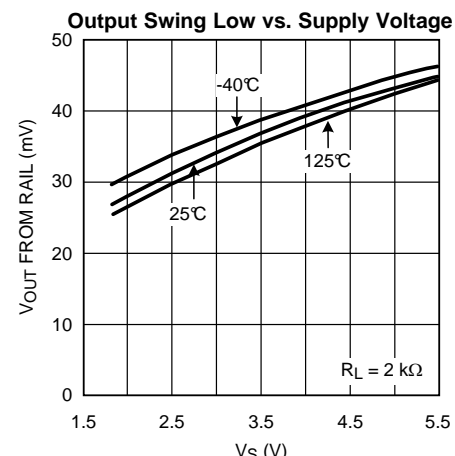


Figure 32.

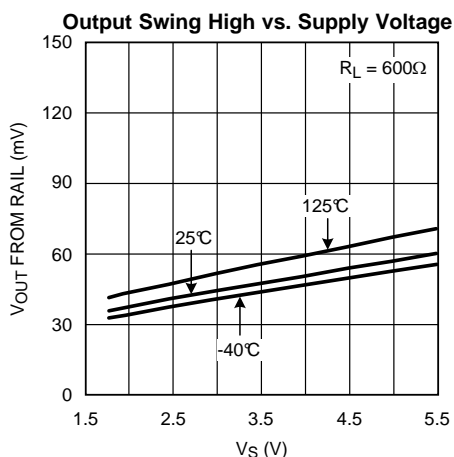


Figure 33.

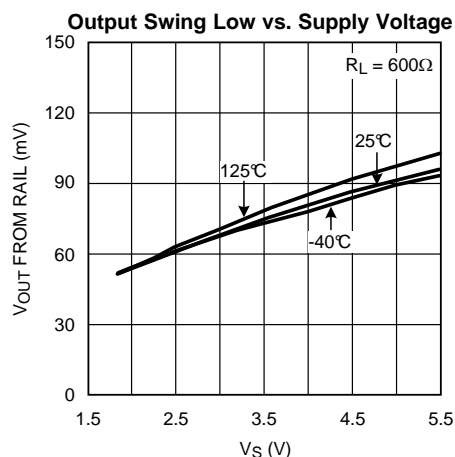


Figure 34.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{CM} = V_S/2$ ,  $V_{EN} = V^+$ .

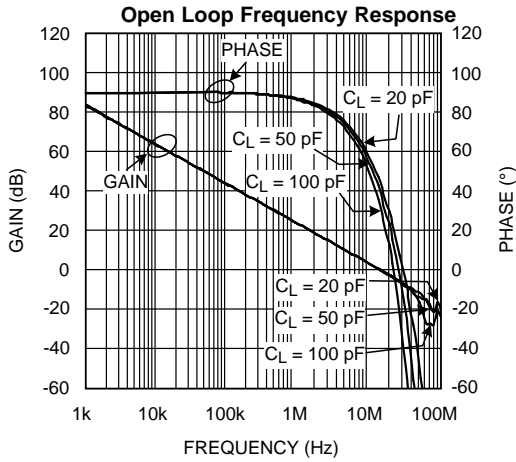


Figure 35.

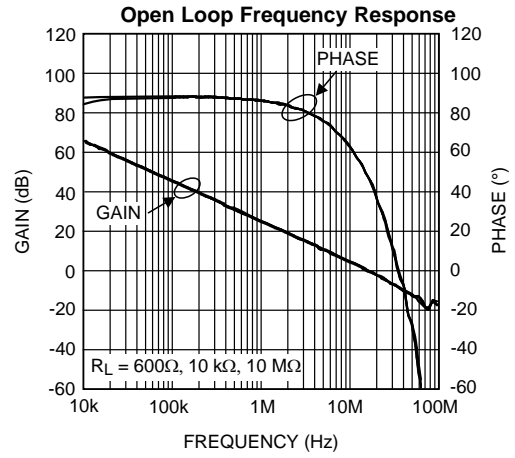


Figure 36.

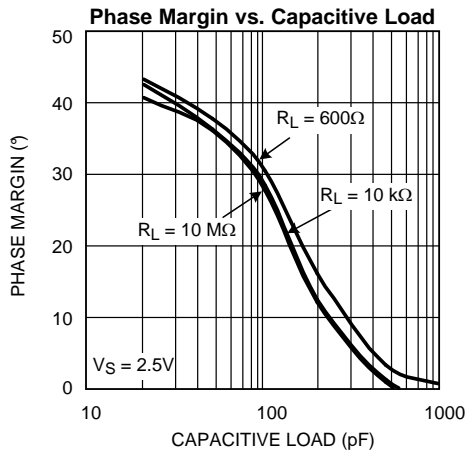


Figure 37.

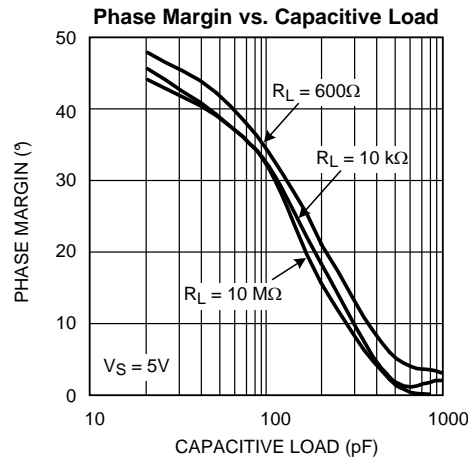


Figure 38.

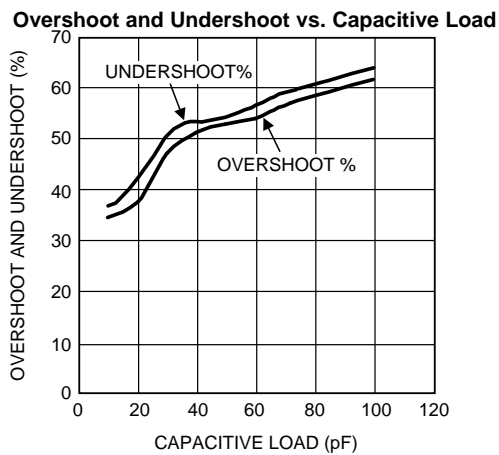


Figure 39.

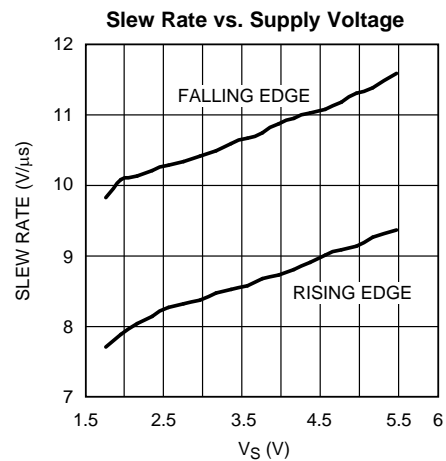
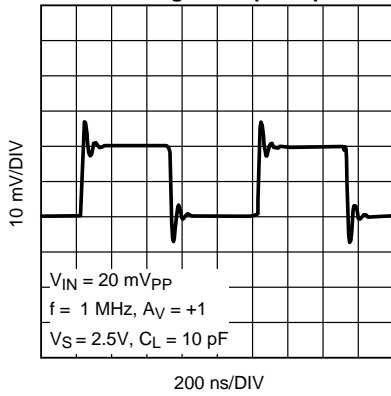


Figure 40.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

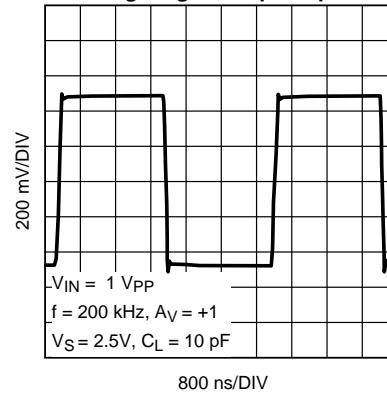
Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{CM} = V_S/2$ ,  $V_{EN} = V^+$ .

**Small Signal Step Response**



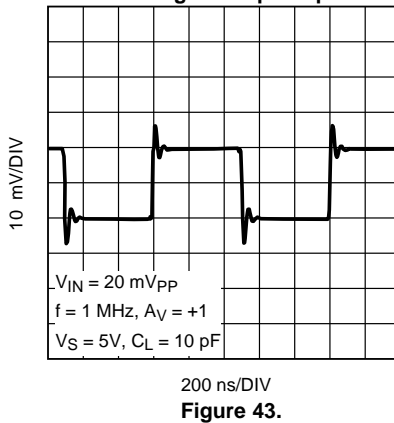
**Figure 41.**

**Large Signal Step Response**



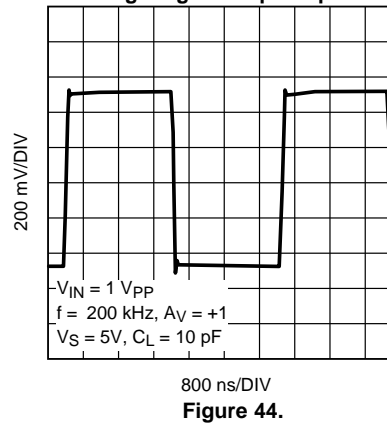
**Figure 42.**

**Small Signal Step Response**



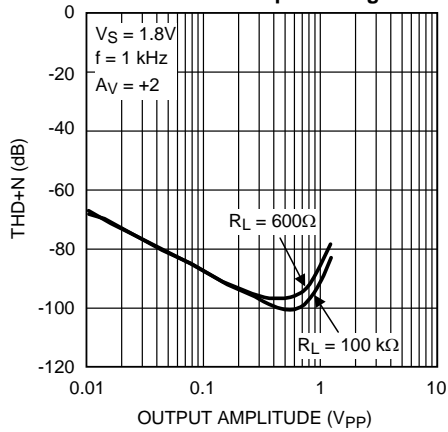
**Figure 43.**

**Large Signal Step Response**



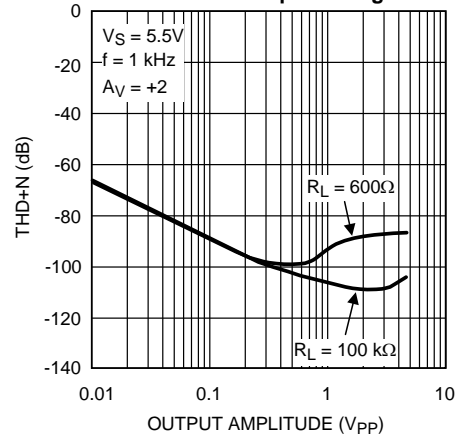
**Figure 44.**

**THD+N vs. Output Voltage**



**Figure 45.**

**THD+N vs. Output Voltage**



**Figure 46.**

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{CM} = V_S/2$ ,  $V_{EN} = V^+$ .

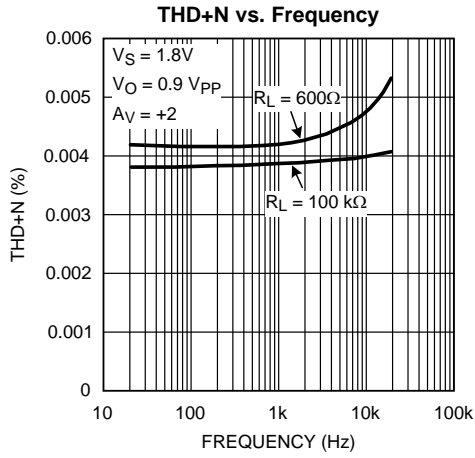


Figure 47.

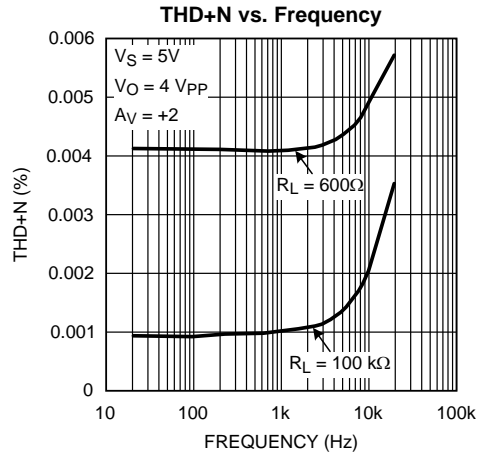


Figure 48.

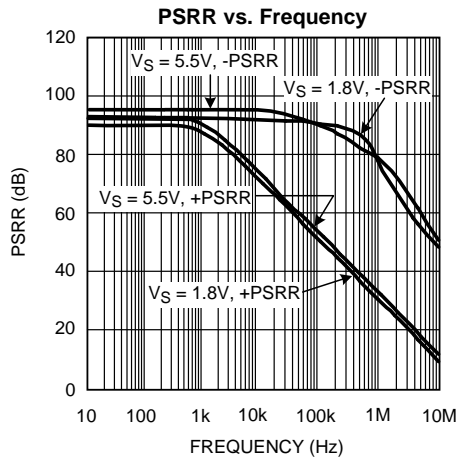


Figure 49.

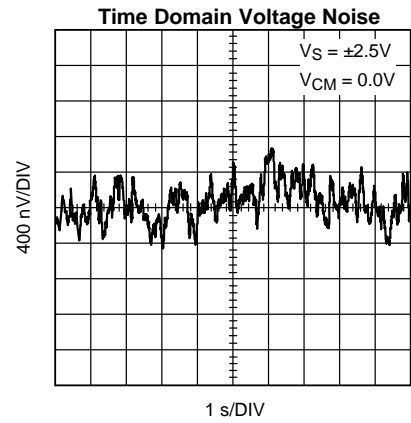


Figure 50.

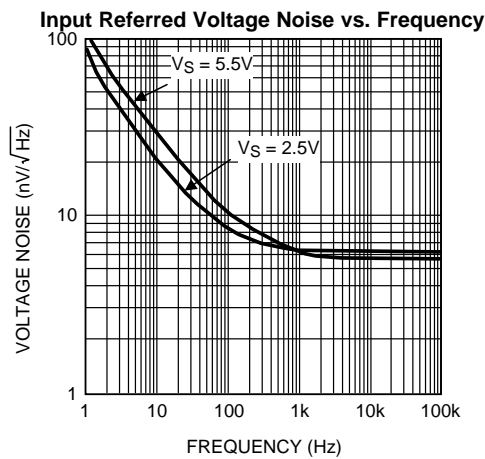


Figure 51.

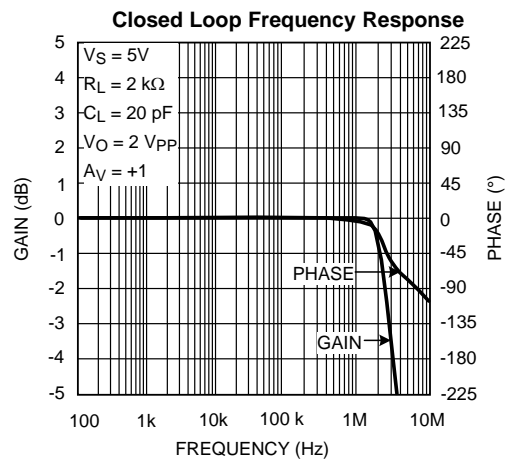
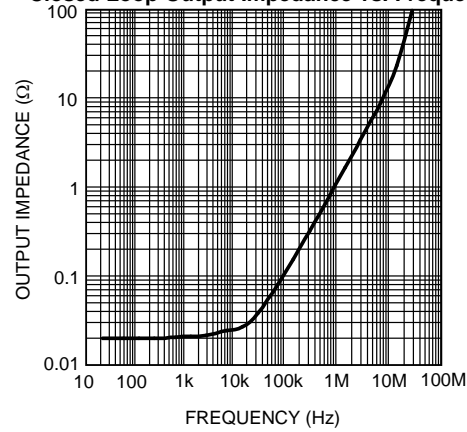


Figure 52.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise noted:  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $V_{CM} = V_S/2$ ,  $V_{EN} = V^+$ .

**Closed Loop Output Impedance vs. Frequency**



**Figure 53.**

## APPLICATION NOTES

### LMP7711/LMP7712

The LMP7711/LMP7712 are single and dual, low noise, low offset, rail-to-rail output precision amplifiers with a wide gain bandwidth product of 17 MHz and low supply current. The wide bandwidth makes the LMP7711/LMP7712 ideal choices for wide-band amplification in portable applications. The low supply current along with the enable feature that is built-in on the LMP7711/LMP7712 allows for even more power efficient designs by turning the device off when not in use.

The LMP7711/LMP7712 are superior for sensor applications. The very low input referred voltage noise of only 5.8 nV/√Hz at 1 kHz and very low input referred current noise of only 10 fA/√Hz mean more signal fidelity and higher signal-to-noise ratio.

The LMP7711/LMP7712 have a supply voltage range of 1.8V to 5.5V over a wide temperature range of 0°C to 125°C. This is optimal for low voltage commercial applications. For applications where the ambient temperature might be less than 0°C, the LMP7711/LMP7712 are fully operational at supply voltages of 2.0V to 5.5V over the temperature range of -40°C to 125°C.

The outputs of the LMP7711/LMP7712 swing within 25 mV of either rail providing maximum dynamic range in applications requiring low supply voltage. The input common mode range of the LMP7711/LMP7712 extends to 300 mV below ground. This feature enables users to utilize this device in single supply applications.

The use of a very innovative feedback topology has enhanced the current drive capability of the LMP7711/LMP7712, resulting in sourcing currents as much as 47 mA with a supply voltage of only 1.8V.

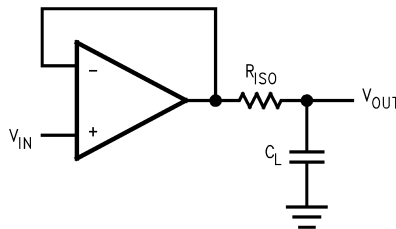
The LMP7711 is offered in the space saving SOT package and the LMP7712 is offered in a 10-pin VSSOP. These small packages are ideal solutions for applications requiring minimum PC board footprint.

Texas Instruments is heavily committed to precision amplifiers and the market segments they serves. Technical support and extensive characterization data is available for sensitive applications or applications with a constrained error budget.

### CAPACITIVE LOAD

The unity gain follower is the most sensitive configuration to capacitive loading. The combination of a capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag which in turn reduces the phase margin of the amplifier. If phase margin is significantly reduced, the response will be either underdamped or the amplifier will oscillate.

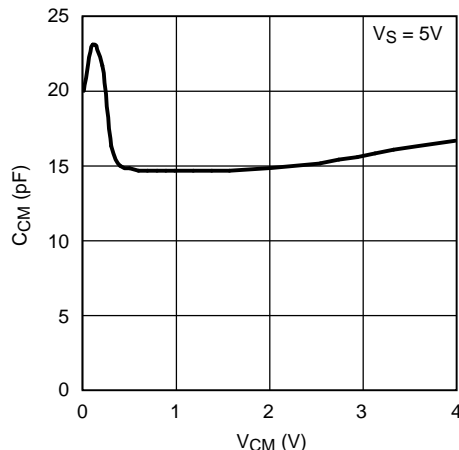
The LMP7711/LMP7712 can directly drive capacitive loads of up to 120 pF without oscillating. To drive heavier capacitive loads, an isolation resistor,  $R_{ISO}$  in [Figure 54](#), should be used. This resistor and  $C_L$  form a pole and hence delay the phase lag or increase the phase margin of the overall system. The larger the value of  $R_{ISO}$ , the more stable the output voltage will be. However, larger values of  $R_{ISO}$  result in reduced output swing and reduced output current drive.



**Figure 54. Isolating Capacitive Load**

### INPUT CAPACITANCE

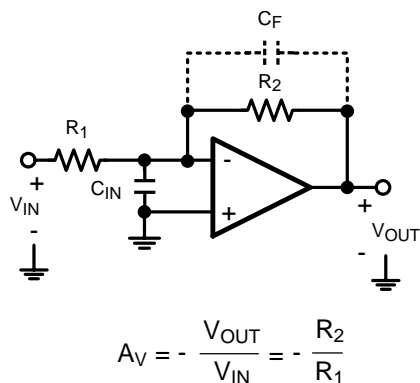
CMOS input stages inherently have low input bias current and higher input referred voltage noise. The LMP7711/LMP7712 enhance this performance by having the low input bias current of only 50 fA, as well as, a very low input referred voltage noise of 5.8 nV/√Hz. In order to achieve this a larger input stage has been used. This larger input stage increases the input capacitance of the LMP7711/LMP7712. [Figure 55](#) shows typical input common mode input capacitance of the LMP7711/LMP7712.



**Figure 55. Input Common Mode Capacitance**

This input capacitance will interact with other impedances such as gain and feedback resistors, which are seen on the inputs of the amplifier to form a pole. This pole will have little or no effect on the output of the amplifier at low frequencies and under DC conditions, but will play a bigger role as the frequency increases. At higher frequencies, the presence of this pole will decrease phase margin and also causes gain peaking. In order to compensate for the input capacitance, care must be taken in choosing feedback resistors. In addition to being selective in picking values for the feedback resistor, a capacitor can be added to the feedback path to increase stability.

The DC gain of the circuit shown in [Figure 56](#) is simply  $-R_2/R_1$ .



**Figure 56. Compensating for Input Capacitance**

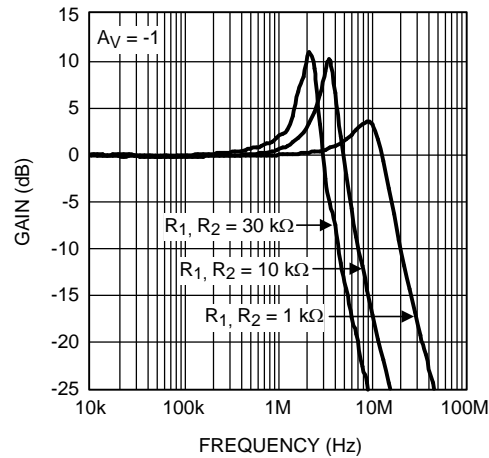
For the time being, ignore  $C_F$ . The AC gain of the circuit in [Figure 56](#) can be calculated as follows:

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}} \quad (1)$$

This equation is rearranged to find the location of the two poles:

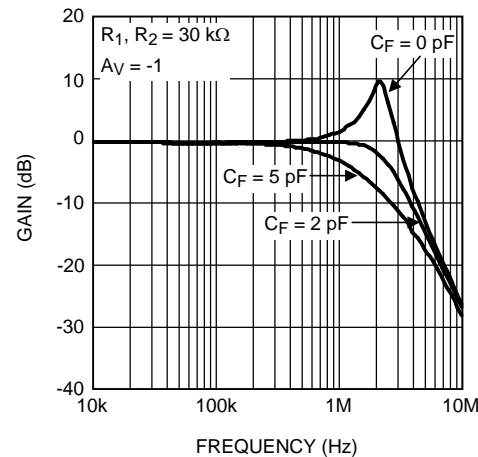
$$P_{1,2} = \frac{-1}{2C_{IN}} \left[ \frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4 A_0 C_{IN}}{R_2}} \right] \quad (2)$$

As shown in Equation 2, as the values of  $R_1$  and  $R_2$  are increased, the magnitude of the poles are reduced, which in turn decreases the bandwidth of the amplifier. Figure 57 shows the frequency response with different value resistors for  $R_1$  and  $R_2$ . Whenever possible, it is best to choose smaller feedback resistors.



**Figure 57. Closed Loop Frequency Response**

As mentioned before, adding a capacitor to the feedback path will decrease the peaking. This is because  $C_F$  will form yet another pole in the system and will prevent pairs of poles, or complex conjugates from forming. It is the presence of pairs of poles that cause the peaking of gain. Figure 58 shows the frequency response of the schematic presented in Figure 56 with different values of  $C_F$ . As can be seen, using a small value capacitor significantly reduces or eliminates the peaking.



**Figure 58. Closed Loop Frequency Response**

## TRANSIMPEDANCE AMPLIFIER

In many applications, the signal of interest is a very small amount of current that needs to be detected. Current that is transmitted through a photodiode is a good example. Barcode scanners, light meters, fiber optic receivers, and industrial sensors are some typical applications utilizing photodiodes for current detection. This current needs to be amplified before it can be further processed. This amplification is performed using a current-to-voltage converter configuration or transimpedance amplifier. The signal of interest is fed to the inverting input of an op amp with a feedback resistor in the current path. The voltage at the output of this amplifier will be equal to the negative of the input current times the value of the feedback resistor. Figure 59 shows a transimpedance amplifier configuration.  $C_D$  represents the photodiode parasitic capacitance and  $C_{CM}$  denotes the common-mode capacitance of the amplifier. The presence of all of these capacitances at higher frequencies might lead to less stable topologies at higher frequencies. Care must be taken when designing a transimpedance amplifier to prevent the circuit from oscillating.

With a wide gain bandwidth product, low input bias current and low input voltage and current noise, the LMP7711/LMP7712 are ideal for wideband transimpedance applications.

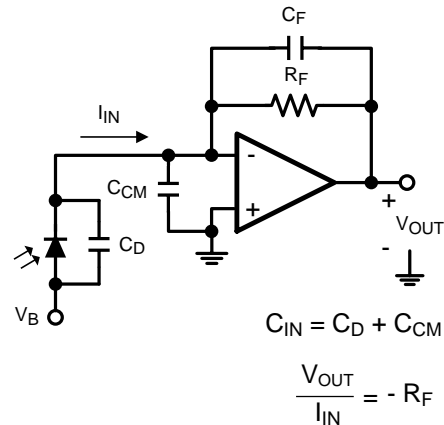


Figure 59. Transimpedance Amplifier

A feedback capacitance  $C_F$  is usually added in parallel with  $R_F$  to maintain circuit stability and to control the frequency response. To achieve a maximally flat, 2<sup>nd</sup> order response,  $R_F$  and  $C_F$  should be chosen by using Equation 3

$$C_F = \sqrt{\frac{C_{IN}}{GBWP * 2 \pi R_F}} \quad (3)$$

Calculating  $C_F$  from Equation 3 can sometimes result in capacitor values which are less than 2 pF. This is especially the case for high speed applications. In these instances, it is often more practical to use the circuit shown in Figure 60 in order to allow more sensible choices for  $C_F$ . The new feedback capacitor,  $C'_F$ , is  $(1 + R_B/R_A) C_F$ . This relationship holds as long as  $R_A \ll R_F$ .

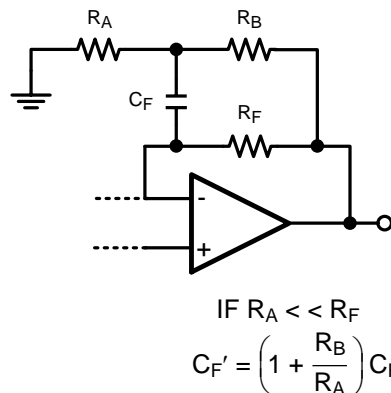
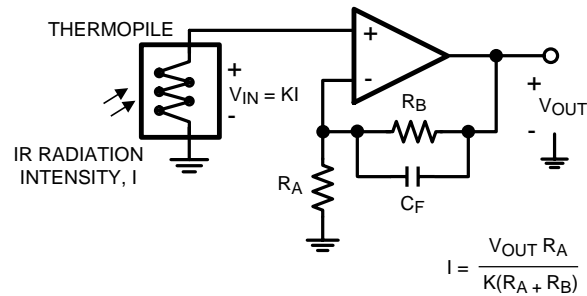


Figure 60. Modified Transimpedance Amplifier

## SENSOR INTERFACE

The LMP7711/LMP7712 have low input bias current and low input referred noise, which make them ideal choices for sensor interfaces such as thermopiles, Infra Red (IR) thermometry, thermocouple amplifiers, and pH electrode buffers.

Thermopiles generate voltage in response to receiving radiation. These voltages are often only a few microvolts. As a result, the operational amplifier used for this application needs to have low offset voltage, low input voltage noise, and low input bias current. Figure 61 shows a thermopile application where the sensor detects radiation from a distance and generates a voltage that is proportional to the intensity of the radiation. The two resistors,  $R_A$  and  $R_B$ , are selected to provide high gain to amplify this signal, while  $C_F$  removes the high frequency noise.

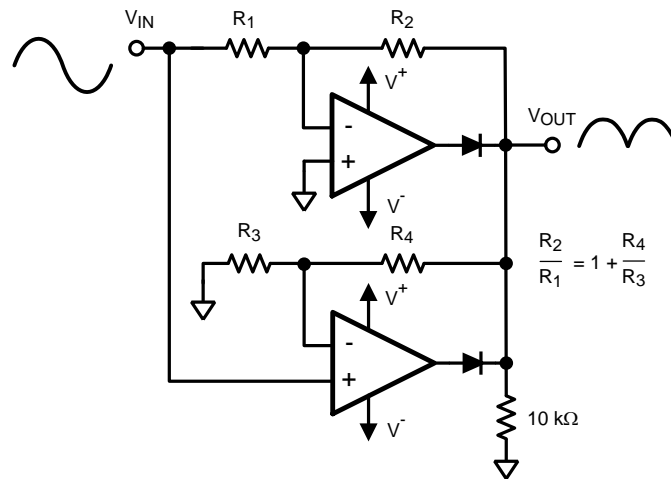


**Figure 61. Thermopile Sensor Interface**

## PRECISION RECTIFIER

Rectifiers are electrical circuits used for converting AC signals to DC signals. Figure 62 shows a full-wave precision rectifier. Each operational amplifier used in this circuit has a diode on its output. This means for the diodes to conduct, the output of the amplifier needs to be positive with respect to ground. If  $V_{IN}$  is in its positive half cycle then only the output of the bottom amplifier will be positive. As a result, the diode on the output of the bottom amplifier will conduct and the signal will show at the output of the circuit. If  $V_{IN}$  is in its negative half cycle then the output of the top amplifier will be positive, resulting in the diode on the output of the top amplifier conducting and, delivering the signal on the amplifier's output to the circuit's output.

For  $R_2/R_1 \geq 2$ , the resistor values can be found by using the equation shown in Figure 62. If  $R_2/R_1 = 1$ , then  $R_3$  should be left open, no resistor needed, and  $R_4$  should simply be shorted.



**Figure 62. Precision Rectifier**

---

**REVISION HISTORY**

<b>Changes from Revision E (May 2013) to Revision F</b>	<b>Page</b>
<hr/> <ul style="list-style-type: none"><li>• Changed layout of National Data Sheet to TI format. ....</li></ul>	<hr/> <a href="#">20</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP7711MK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AC3A	<a href="#">Samples</a>
LMP7711MKE/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AC3A	<a href="#">Samples</a>
LMP7711MKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AC3A	<a href="#">Samples</a>
LMP7712MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AD3A	<a href="#">Samples</a>
LMP7712MME/NOPB	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AD3A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7711MK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7711MKE/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7711MKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7712MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7712MME/NOPB	VSSOP	DGS	10	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7711MK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LMP7711MKE/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMP7711MKX/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMP7712MM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LMP7712MME/NOPB	VSSOP	DGS	10	250	210.0	185.0	35.0

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View LMP7712MME/NOPB on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management