THE DATASHEET OF

BQ24130RHLT

www.win-source.net 0086-755-83957316

600-kHz Synchronous Switch-Mode Host-Controlled Battery/Supercapacitor Charger With 4-A Integrated MOSFETs

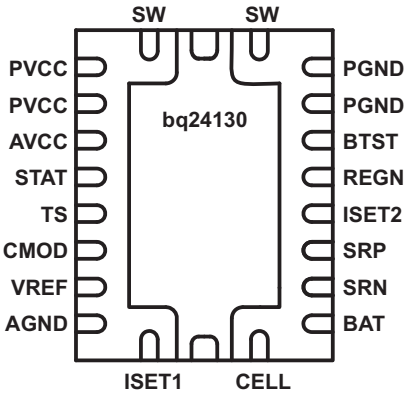
Check for Samples: bq24130

FEATURES

- 600kHz Synchronous Switch-mode Charger with 4 A Integrated N-MOSFETs
- Up to 96% Efficiency
- 30 V Input Rating with 18V Overvoltage Protection
  - 4.5 V to 17 V Input Operating Range
- Battery Charge Voltage
  - 1, 2,or 3-Cell With 4.2V/Cell
- Constant Current Super Capacitor Charging
- High Integration
  - Integrated 20-V Switching MOSFETs
  - Integrated Bootstrap Diode
  - Internal Loop Compensation
  - Internal Digital Soft Start
- Safety
  - Thermal Regulation Loop Throttles Back Current to Limit T_J = 120°C
  - Thermal Shutdown
  - Battery Thermistor Sense Hot/Cold Charge Suspend
  - Input Overvoltage Protection
  - Cycle by Cycle Current Limit
- Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±4% Charge Current Regulation
- Less than 15 µA Battery Current with Adapter Removed
- Small QFN Package
  - 3.5 mm x 4.5 mm QFN-20 pin

APPLICATIONS

- Tablet PC
- Netbook and Ultra-Mobile Computers
- Portable Data Capture Terminals
- Portable Printers
- Medical Diagnostics Equipment
- Battery Bay Chargers
- Back-Up Systems
- Li-Ion/Li-Polymer Battery and Super Capacitor Applications



DESCRIPTION

The bq24130 is an integrated host-controlled Li-ion and Li-polymer switch-mode battery charge controllers with two integrated N-channel power MOSFETs. It offers a constant-frequency synchronous PWM controller with high accuracy regulation of charge current and voltage. The fast charge and precharge current can be either hardwired with resistors or programmed by system power management microcontroller using a DAC or GPIOs. Battery remote sensing provides accurate charge voltage regulation.

The bq24130 monitors the battery pack temperature to allow charger only in a preset temperature window. The thermal regulation loop reduces the charge current to maintain the junction temperature of 120ºC during operation.

The bq24130 automatically enters a low-quiescent current sleep mode when the input voltage falls below the battery voltage. The bq24130 charges one, two or three cell (selected by CELL pin), supporting up to 4 A charge current. The bq24130 is available in a 20-pin, 3.5 x 4.5 mm^2 thin QFN package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN FUNCTIONS

PIN	NAME	TYPE	FUNCTION DESCRIPTION
1, 20	SW	P	Switching node, charge current output inductor connection. Connect the 0.47-µF bootstrap capacitor from SW to BTST.
2, 3	PVCC	P	Charger input voltage. Connect at least 10-µF ceramic capacitor from PVCC to PGND and place it as close as possible to IC.
4	AVCC	P	IC power positive supply. Place a 1-µF ceramic capacitor from AVCC to AGND and place it as close as possible to IC. Place a 10 ohm resistor from input side to AVCC pin to filter the noise. For 5 V input, a 5-Ω resistor is recommended.
5	STAT	O	Open-drain charge status pin with 10-kΩ pull up to power rail. The STAT pin can be used to drive LED or communicate with the host processor. It indicates various charger operations: LOW when charge in process, HIGH when charge complete or SLEEP mode. Blinking when fault occurs, such as charge suspend, and input overvoltage.
6	TS	I	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program the hot and cold temperature window with a resistor divider from VREF to TS to AGND. The temperature qualification window can be set to 5-40ºC or wider. The 103AT thermister is recommended.
7	CMOD	I	Charge mode selection: low (pull down to AGND) for pre-charge current as set by ISET2 pin and high (pull up to VREF) for fast charge current as set by ISET1 pin. If the battery voltage reaches the voltage regulation set point, IC changes to voltage regulation mode regardless of CMOD pin input.
8	VREF	P	3.3 V reference voltage output. Place a 1-µF ceramic capacitor from VREF to AGND pin close to the IC. This voltage could be used for programming charge current regulation on ISET1 and ISET2 pins, programming the threshold of TS pin, and the pull-up rail of STAT pin and CELL pin.
9	AGND	P	Analog ground. Ground connection for low-current sensitive analog and digital signals. On PCB layout, connect to the analog ground plane, and only connect to PGND through the PowerPad underneath the IC.
10	ISET1	I	Fast charge current set point. Use a voltage divider from VREF to AGND to set this value. $I_{(CHG)} = \frac{V_{(ISET1)}}{20 \times R_{(SR)}}$ The charger is disabled when ISET1 pin voltage is below 50mV and is enabled when ISET1 pin voltage is above 100mV.
11	CELL	I	Cell selection pin. Set CELL pin LO for 1-cell, Float for 2-cell, and HI for 3-cell with a fixed 4.2 V per cell.
12	BAT	I	Battery voltage remote sense. Directly connect a kelvin sense trace from the battery pack positive terminal to the BAT pin to accurately sense the battery pack voltage. Place a 0.1-µF capacitor from BAT to AGND close to the IC to filter high frequency noise.
13	SRN	I	Charge current sense resistor, negative input. A 0.1-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from SRN pin to AGND for common-mode filtering.
14	SRP	P/I	Charge current sense resistor, positive input. A 0.1-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from SRP pin to AGND for common-mode filtering.
15	ISET2	I	Pre-charge current set point. Use a voltage divider from VREF to AGND to set this value. $I_{(PRECHG)} = \frac{V_{(ISET2)}}{100 \times R_{(SR)}}$
16	REGN	P	PWM low side driver positive 6V supply output. Connect a 1-µF ceramic capacitor from REGN to PGND pin, close to the IC. Use for low side driver and high-side driver bootstrap voltage by integrated diode from REGN to BTST.
17	BTST	P	PWM high side driver positive supply. Connect the 47 nF bootstrap capacitor from SW to BTST.
18, 19	PGND		Power ground. Ground connection for high-current power converter node. On PCB layout, connect directly to source of low-side power MOSFET, to ground connection of in put and output capacitors of the charger. Only connect to AGND through the PowerPAD underneath the IC.
PowerPAD™	Pad	Pad	Exposed pad beneath the IC. Always solder PowerPAD to the board, and have vias on the PowerPAD plane star-connecting to AGND and ground plane for high-current power converter. It also serves as a thermal pad to dissipate the heat.

ORDERING INFORMATION(1)

PART NUMBER	MARKING	PACKAGE	ORDERING NUMBER	QUANTITY
bq24130	bq24130	20-pin 3.5 x 4.5mm^2 QFN	bq24130RHLR	3000
			bq24130RHLT	250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage (with respect to AGND and PGND)	PVCC	–0.3	20	V
	AVCC, STAT	–0.3	30	V
	SRP, SRN, BAT	–0.3	20	V
	SW	–2	20	V
	REGN, TS, CELL, CMOD	–0.3	7	V
	BTST	–0.3	26	V
	VREF, ISET1, ISET2	–0.3	3.6	V
Maximum difference voltage	SRP–SRN	–0.5	0.5	V
Junction temperature, T_J		–40	155	°C
Storage temperature, T_{stg}		–55	155	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal, if not specified. Consult Packaging Section of the data sheet for thermal limitations and considerations of packages.

THERMAL INFORMATION

THERMAL METRIC(1) (2)		bq24130	UNITS
		RHL (20 PIN)	
θ_{JA}	Junction-to-ambient thermal resistance	35	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	N/A	
θ_{JB}	Junction-to-board thermal resistance	N/A	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	9.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Input voltage	VIN	4.5	17	V
Output voltage	BAT		13.5	V
Output current	I_{OUT}	0.6	4	A
Maximum difference voltage	SRP-SRN	–200	200	mV
Operating junction temperature range	T_J	–40	125	°C

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ELECTRICAL CHARACTERISTICS

4.5 V ≤ $V_{(PVCC,\ AVCC)}$ ≤ 17 V, -40°C < T_J < 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS						
$V_{(AVCC)}$	AVCC Input Voltage Operating Range		4.5		17	V
QUIESCENT CURRENTS						
$I_{(BAT)}$	Battery Discharge Current (sum of currents into AVCC, BTST, SW, SRP, SRN, BAT)	$V_{(AVCC)}$ < $V_{(UVLO)}$, 0°C - 85°C			15	µA
		$V_{(AVCC)}$ > $V_{(UVLO)}$ $V_{(SRN)}$ > $V_{(AVCC)}$ (SLEEP)			15	
		$V_{(AVCC)}$ > $V_{(UVLO)}$, $V_{(AVCC)}$ > $V_{(SRN)}$ ISET1 < 40 mV (Charge disabled)			25	
		$V_{(AVCC)}$ > $V_{(UVLO)}$, $V_{(AVCC)}$ > $V_{(SRN)}$ ISET1 > 120 mV (Charge enabled), Charge done			25	
$I_{(AC)}$	Adapter Supply Current (sum of currents into AVCC)	$V_{(AVCC)}$ > $V_{(UVLO)}$, $V_{(AVCC)}$ > $V_{(BAT)}$ ISET1 < 40 mV (Charge disabled)		1	1.5	mA
		$V_{(AVCC)}$ > $V_{(UVLO)}$, $V_{(AVCC)}$ > $V_{(BAT)}$ ISET1 > 120 mV (Charge enabled), no switching		2	5	
		$V_{(AVCC)}$ > $V_{(UVLO)}$, $V_{(AVCC)}$ > $V_{(BAT)}$ ISET1 > 120 mV (Charge enabled), switching		15		
CHARGE VOLTAGE REGULATION						
$V_{(BAT_REG)}$	BAT Regulation Voltage	bq24130, CELL to AGND		4.2		V
		bq24130, CELL floating		8.4		
		bq24130, CELL to VREF		12.6		
	Charge Voltage Regulation Accuracy	T_J = 0 to 85°C	–0.5%		0.5%	
		T_J = -40 to 125°C	–0.7%		0.7%	
$R_{(BAT)}$	BAT pin resistance(1)		614	717	820	kΩ
CURRENT REGULATION (FAST CHARGE)						
$V_{(ISET1)}$	ISET1 Voltage Range		0.12		0.8	V
$K_{(ISET1)}$	Charge Current Set Factor (Amps of Charge Current per Volt on ISET1 pin)	R_{SENSE} = 10 mΩ		5		A/V
	Charge Current Regulation Accuracy (With Schottky Diode on SW)	$V_{(IREG_CHG)}$ = 40 mV	–4%		4%	
		$V_{(IREG_CHG)}$ = 20 mV	-7%		7%	
		$V_{(IREG)}$ = 5 mV	–25%		25%	
$V_{(ISET1_CE)}$	ISET1 Rising Threshold to Enable Charge	ISET1 rising		100	120	mV
	ISET1 Falling to Disable Charge	ISET1 falling	40	50		mV
I_{Lkg}	Leakage Current into ISET1 pin	$V_{(ISET1)}$ = 2 V			100	nA
CURRENT REGULATION – PRECHARGE						
$V_{(ISET2)}$	ISET2 Voltage Range		0		2	V
$I_{(IREG_PRECHG)}$	Precharge current range	R_{SENSE} = 10 mΩ	0.125		2	A
$K_{(ISET2)}$	Precharge Current Set Factor (Amps of precharge Current per Volt on ISET2 pin)	R_{SENSE} = 10 mΩ		1		A/V
	Precharge Current Regulation Accuracy	$V_{(IREG_CHG)}$ = 10 mV, $V_{(SRP)}$ = 4 V	–10%		10%	
		$V_{(IREG_CHG)}$ = 10 mV, $V_{(SRP)}$ = 2.6 V	–15%		15%	
		$V_{(IREG_CHG)}$ = 4 mV	–25%		25%	
		$V_{(IREG_CHG)}$ = 2 mV	-40%		40%	
I_{Lkg}	Leakage Current into ISET2 pin	$V_{(ISET2)}$ = 2V		100		nA
INPUT UNDERVOLTAGE LOCK-OUT COMPARATOR (UVLO)						
UVLO	AC Undervoltage Rising Threshold	Measure on AVCC	3.4	3.6	3.8	V
	AC Undervoltage Hysteresis, falling			340		mV
SLEEP COMPARATOR (REVERSE DISCHARGING PROTECTION)						
$V_{(SLEEP)}$	SLEEP Falling Threshold	$V_{(AVCC)}$ – $V_{(SRN)}$ to enter SLEEP	50	90	150	mV
	SLEEP Hysteresis			200		mV
	SLEEP Rising Shutdown Deglitch	AVCC falling below SRN		100		ms
	SLEEP Falling Power-up Deglitch	AVCC rising above SRN		30		ms

(1) Specified by Design

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V ≤ $V_{(PVCC,\ AVCC)}$ ≤ 17 V, -40°C < T_J < 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BAT OVERVOLTAGE COMPARATOR						
$V_{(OV_RISE)}$	Overvoltage Rising Threshold	As percentage of VBAT		104%		
$V_{(OV_FALL)}$	Overvoltage Falling Threshold	As percentage of VBAT		102%		
t_{OV}	Overvoltage Deglitch Time to Disable Charge			30		ms
INPUT OVERVOLTAGE COMPARATOR (ACOV)						
$V_{(ACOV)}$	AC Overvoltage Rising Threshold	Measure on AVCC	17	18	19	V
	AC Overvoltage Falling Hysteresis	Measured on AVCC		540		mV
	AC Overvoltage Rising Deglitch			1		ms
	AC Overvoltage Falling Deglitch			1		ms
THERMAL REGULATION						
T_J	Junction Temperature Regulation Accuracy	ISET1 > 120 mV, Charging		120		°C
THERMAL SHUTDOWN COMPARATOR						
$T_{(SHUT)}$	Thermal Shutdown Rising Temperature	Temperature Increasing		150		°C
	Thermal Shutdown Hysteresis			20		°C
	Thermal Shutdown Rising Deglitch	Temperature Increasing Delay		100		µs
	Thermal Shutdown Falling Deglitch	Temperature Decreasing Delay		10		ms
THERMISTOR COMPARATOR						
$V_{(LTF)}$	Cold Temperature Threshold, TS pin Voltage Rising Threshold	Charger suspends charge as Percentage to VREF	73%	73.5%	74%	
$V_{(LTF_HYS)}$	Cold Temperature Hysteresis, TS pin Voltage Falling	As Percentage to VREF	0.2%	0.4%	0.6%	
$V_{(HTF)}$	Hot Temperature TS pin voltage falling Threshold	As Percentage to VREF	46.6%	47.2%	47.8%	
$V_{(TCO)}$	Cut-off Temperature TS pin voltage falling Threshold	As Percentage to VREF	44.2%	44.7%	45.2%	
	Deglitch time for Temperature Out of Range Detection	$V_{(TS)} > V_{(LTF)}$, or $V_{(TS)} < V_{(TCO)}$, or $V_{(TS)} < V_{(HTF)}$		400		ms
	Deglitch time for Temperature in Valid Range Detection	$V_{(TS)} < V_{(LTF)} - V_{(LTF_HYS)}$ or $V_{(TS)} > V_{(TCO)}$, or $V_{(TS)} > V_{(HTF)}$		20		ms
CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
$V_{(OC)}$	Charge Overvurrent Rising Threshold, $V_{(SRP)}$ > 2.2V	Current as percentage of $V_{(IREG_CHG)}$		160%		
	Charge Overvurrent Rising Threshold, $V_{(SRP)}$ < 2.2V			45		mV
	Charge Overvurrent Limit Range, $V_{(SRP)}$ > 2.2V			75		mV
$I_{(OCP)}$	Charge OCP using high side sense FET		8	11.5		A
CHARGE UNDERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
$V_{(UCP)}$	Charge Undercurrent Falling Threshold	Switch from Sync mode to Non-Sync mode, measure on $V_{(SRP-SRN)}$	1	5	9	mV
BAT SHORT COMPARATOR (BATSHORT)						
$V_{(BATSHT)}$	Battery Short Falling Threshold	Measure on BAT		2		V
	Battery Short Rising Hysteresis			200		mV
	Deglitch on Both Edge			1		µs
LOW CHARGE CURRENT COMPARATOR						
$V_{(LC)}$	Low Charge Current Falling Threshold	Measure on $V_{(SRP-SRN)}$		1.25		mV
	Low Charge Current Rising Hysteresis			1.25		mV
	Deglitch on Both Edge			1		µs
VREF REGULATOR						
$V_{(VREF_REG)}$	VREF Regulator Voltage	$V_{(AVCC)}$ > UVLO	3.267	3.3	3.333	V
$I_{(VREF_LIM)}$	VREF Current Limit	$V_{(VREF)}$ = 0V, $V_{(AVCC)}$ > UVLO	35		120	mA

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V ≤ $V_{(PVCC,\ AVCC)}$ ≤ 17 V, -40°C < T_J < 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REGN REGULATOR						
$V_{(REGN_REG)}$	REGN Regulator Voltage	$V_{(AVCC)}$ > 10 V, 0mA - 40 mA, ISET1 > 100 mV	5.7	6	6.3	V
$I_{(REGN_LIM)}$	REGN Current Limit	$V_{(REGN)}$ = 0 V, $V_{(AVCC)}$ > UVLO	40		120	mA
INTERNAL PWM						
	PWM Switching Frequency		500	600	700	kHz
	Driver Dead Time	Dead time when switching between LSD and HSD, no load		30		ns
$R_{(DS_HI)}$	High Side MOSFET On Resistance	$V_{(BTST)}$ – $V_{(SW)}$ = 5.5 V		25	45	mΩ
$R_{(DS_LO)}$	Low Side MOSFET On Resistance			60	110	mΩ
$V_{(BTST)}$	Bootstrap Refresh Comparator Threshold Voltage	$V_{(BTST)}$ – $V_{(SW)}$ when low side refresh pulse is requested, $V_{(VCC)}$ = 4.5 V	3			V
		$V_{(BTST)}$ – $V_{(SW)}$ when low side refresh pulse is requested, $V_{(VCC)}$ > 6 V	4			V
INTERNAL SOFT START (8 steps to regulation current $I_{(CHG)}$)						
	Soft Start Steps			8		step
	Soft Start Step Time			1.6	3	ms
CHARGER SECTION POWER-UP SEQUENCING						
	Charge-Enable Delay after Power-up (2)	Delay from ISET1 above 120 mV to start charging the battery		2	5	ms
INTEGRATED BTST DIODE						
V_F	Forward Bias Voltage	I_F = 120 mA at 25°C		0.85		V
V_R	Reverse breakdown voltage	I_R = 2 µA at 25°C			20	V
LOGIC IO PIN CHARACTERISTICS						
$V_{(OUT_LO)}$	STAT Output Low Saturation Voltage	Sink Current = 5 mA			0.5	V
$V_{(CELL_LO)}$	CELL pin input low threshold, 1 cell	CELL pin voltage falling edge			0.5	V
$V_{(CELL_MID)}$	CELL pin input mid threshold, 2 cells	CELL pin voltage rising for MIN, falling for MAX	0.8		1.8	V
$V_{(CELL_HI)}$	CELL pin input high threshold, 3 cells	CELL pin voltage rising edge	2.5			V
$R_{(CELL_GND)}$	Resistance between CELL to ground to keep CELL LOW [1]				120	kΩ
V_{IL}	CMOD Low-level input voltage threshold	I_{IL} = 5 µA			0.8	V
V_{IH}	CMOD High-level input voltage threshold	I_{IL} = 20 µA	2.1			V

(2) Specified by Design

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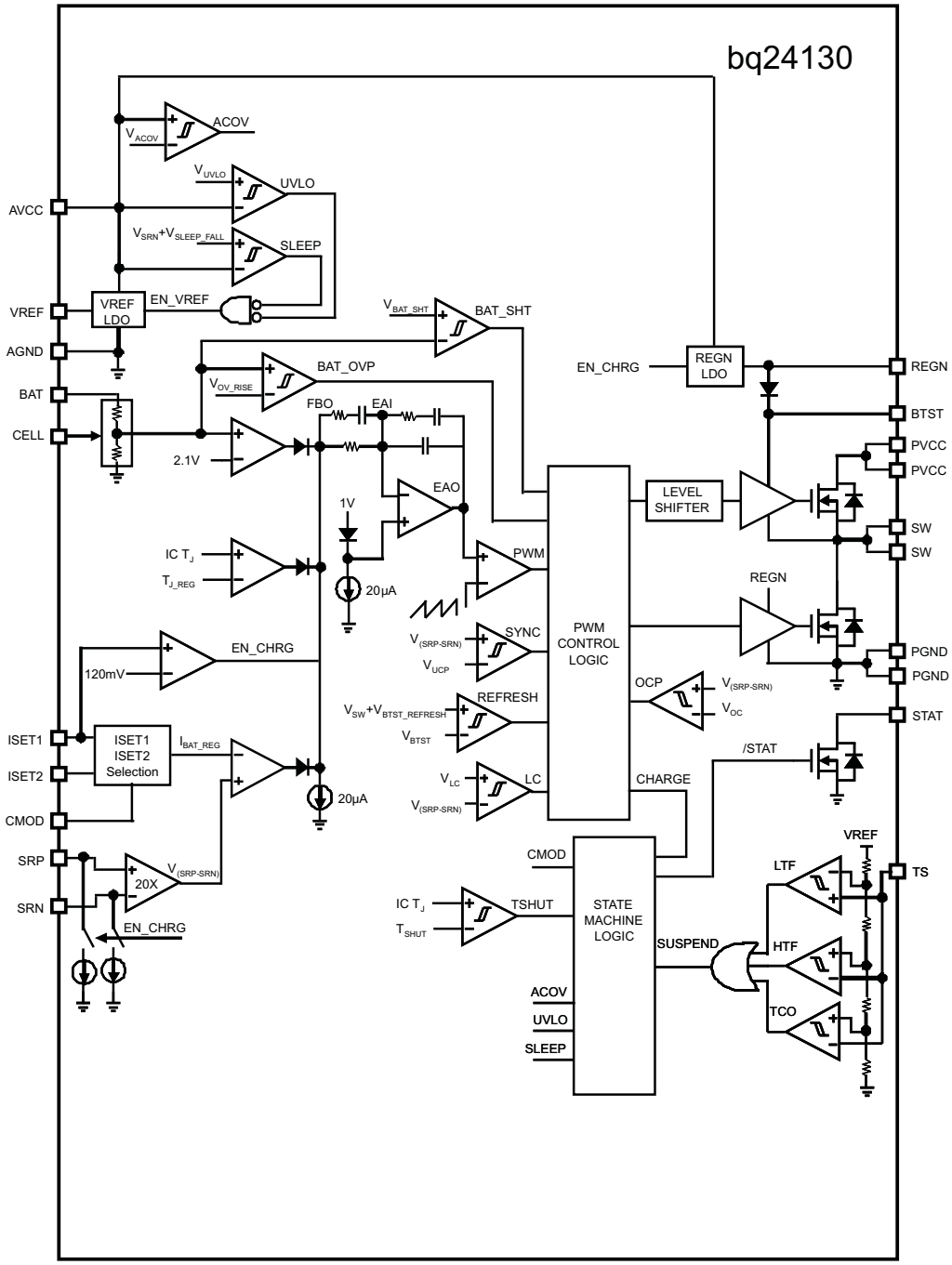
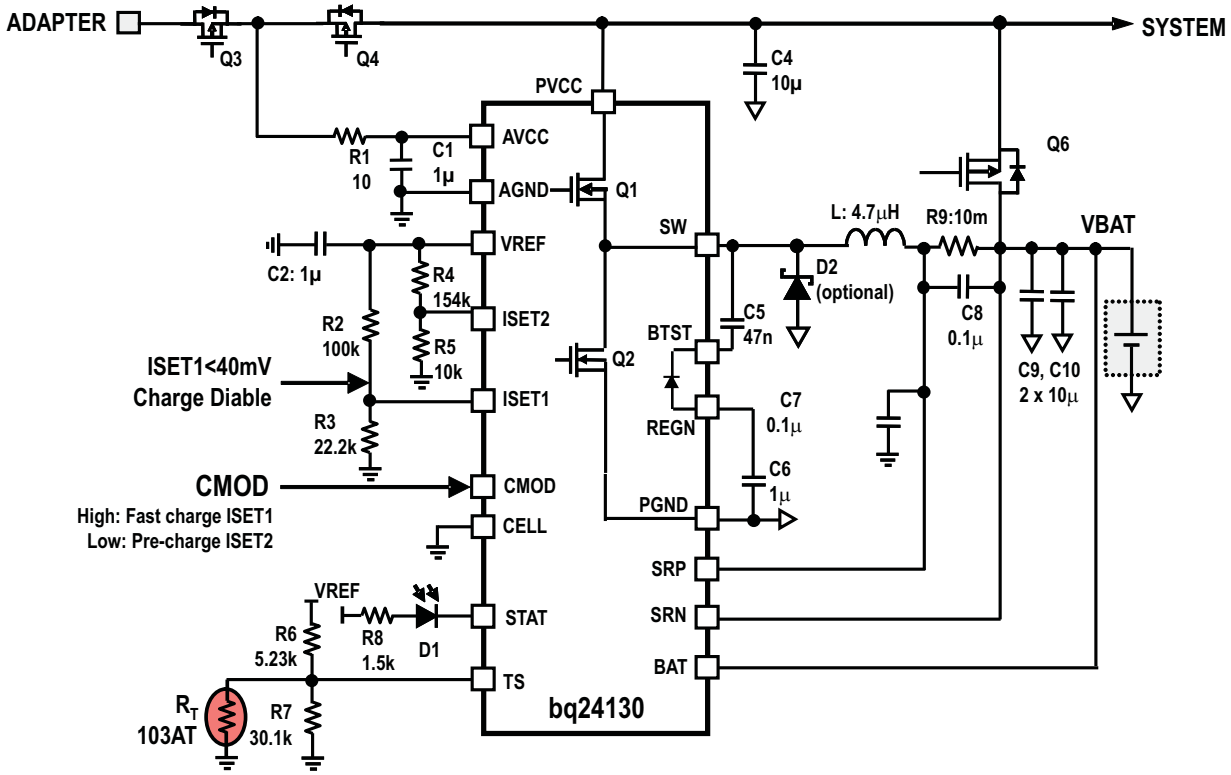
BLOCK DIAGRAM



TYPICAL APPLICATION



12 V input, 1 Cell, 3 A Charge Current, 0.2 A Pre-charge Current, 0°C - 45°C TS

Figure 1. Typical Battery Charging Application Schematic

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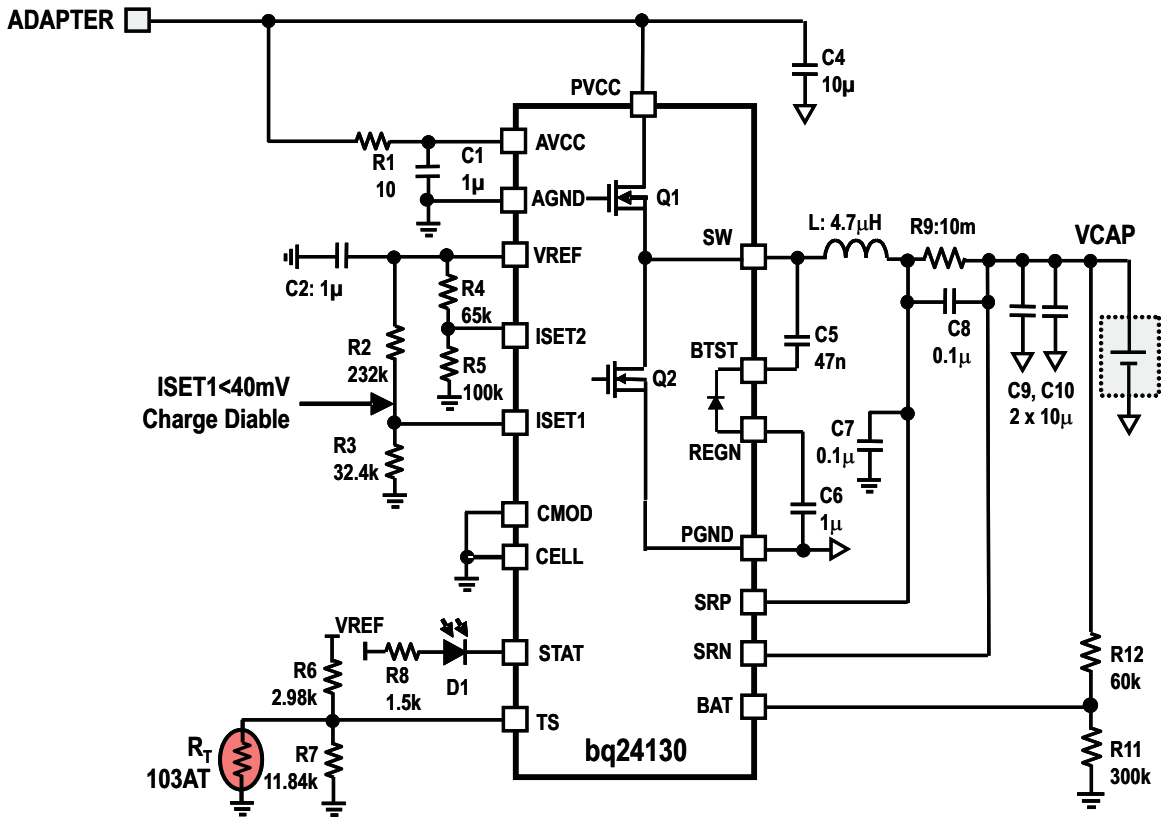
TYPICAL APPLICATION (continued)



12 V input, 5.4 V Output, 2 A Charge Current, 0°C - 60°C TS

Figure 2. Typical Super Capacitor Charging Application Schematic

TYPICAL CHARACTERISTICS

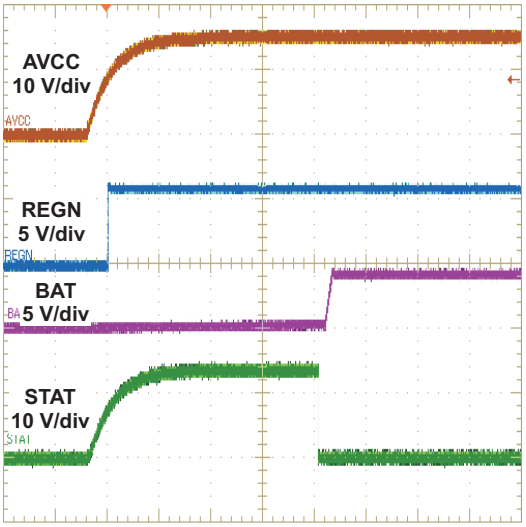


Figure 3. Power Up (BAT, STAT)

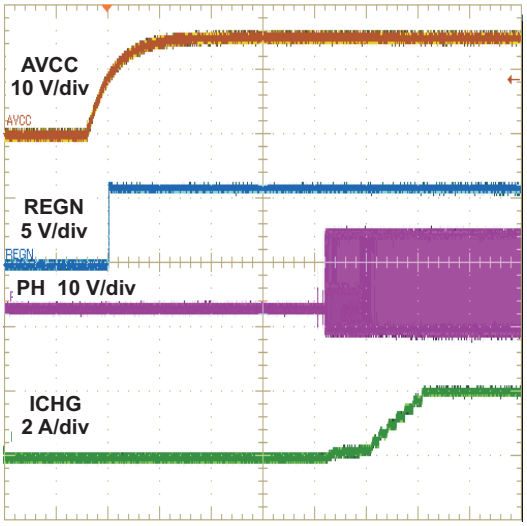


Figure 4. Power Up (PH, ICHG)

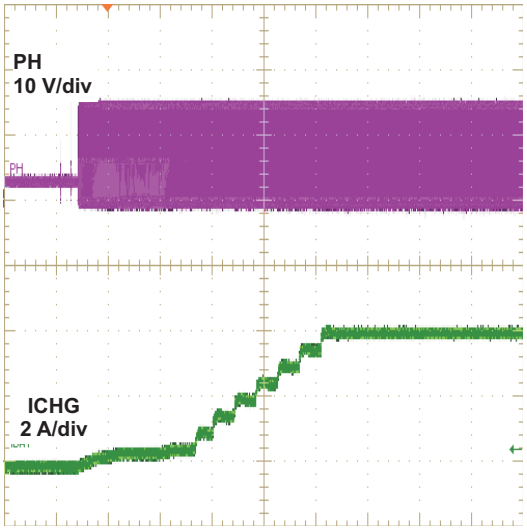


Figure 5. Current Soft Start

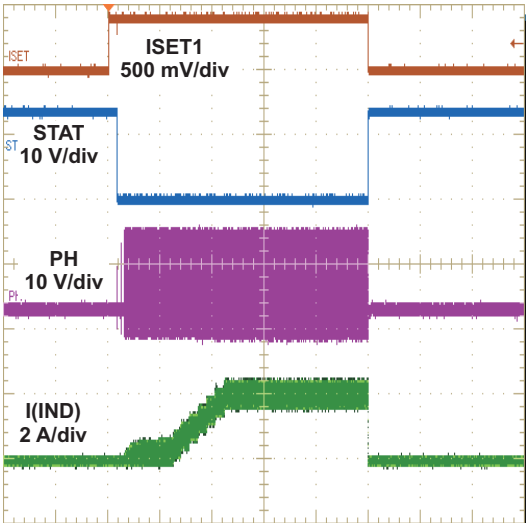


Figure 6. ISET1 Enable and Disable Charge

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TYPICAL CHARACTERISTICS (continued)

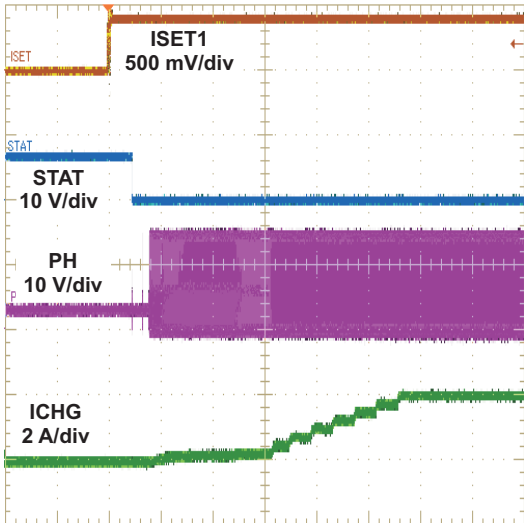

Figure 7. Charge Enable

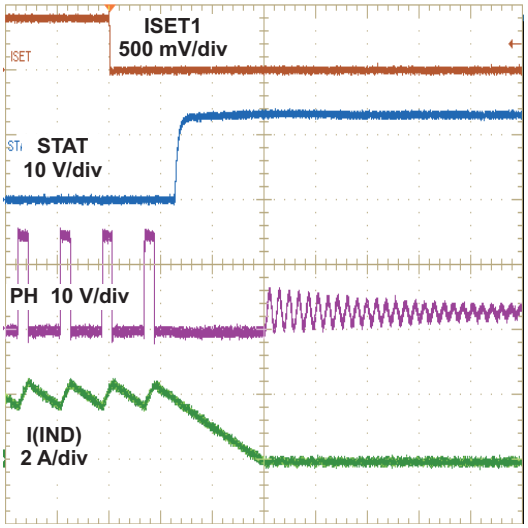

Figure 8. Charge Disable

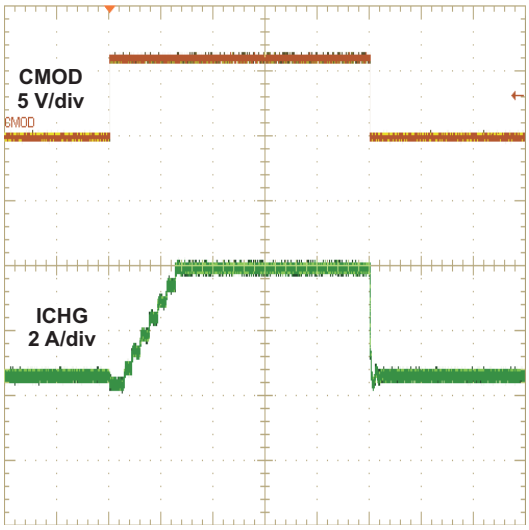

Figure 9. CMOD Select Charge Current (ISET1 2A, ISET2 0.4A)

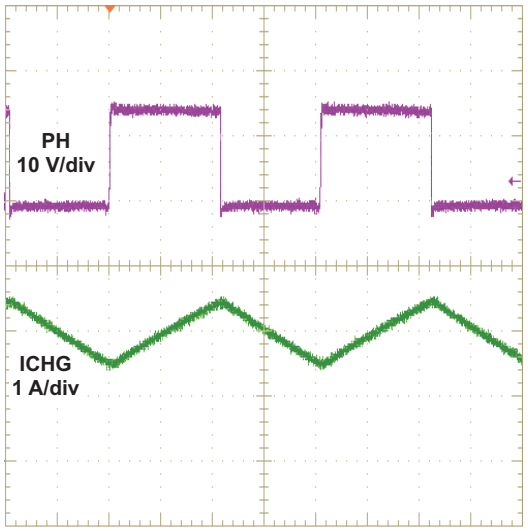

Figure 10. Switching (CCM)

TYPICAL CHARACTERISTICS (continued)

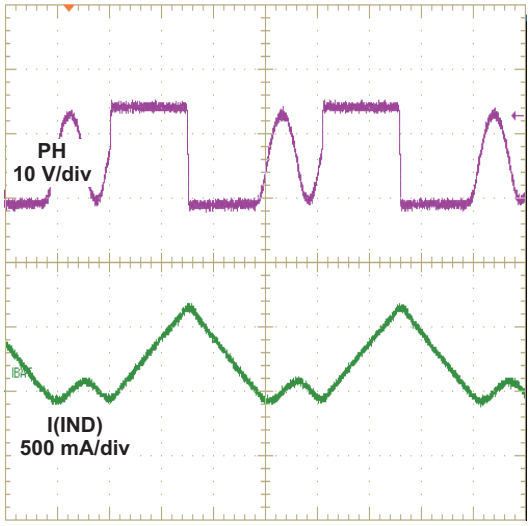

Figure 11. Switching (DCM)

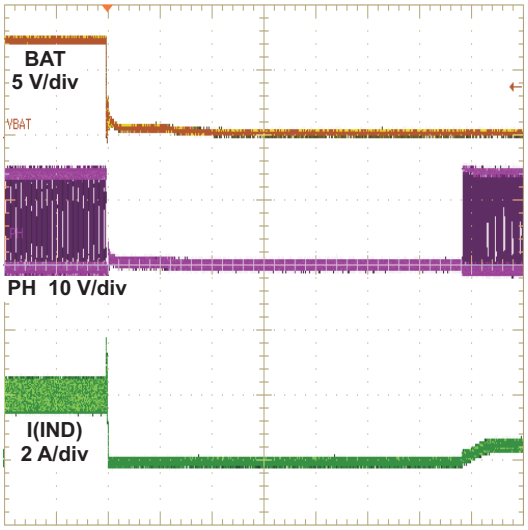

Figure 12. Short Battery

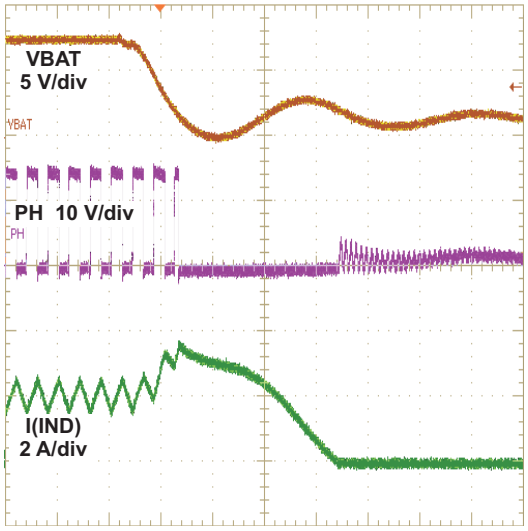

Figure 13. Short Battery (zoom-in)

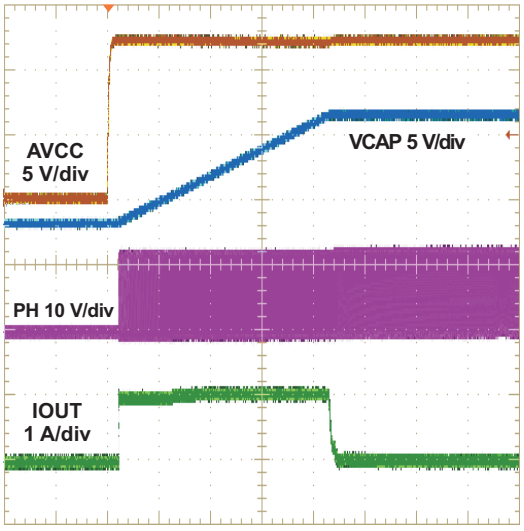

Figure 14. SuperCap Charge Cycle

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TYPICAL CHARACTERISTICS (continued)

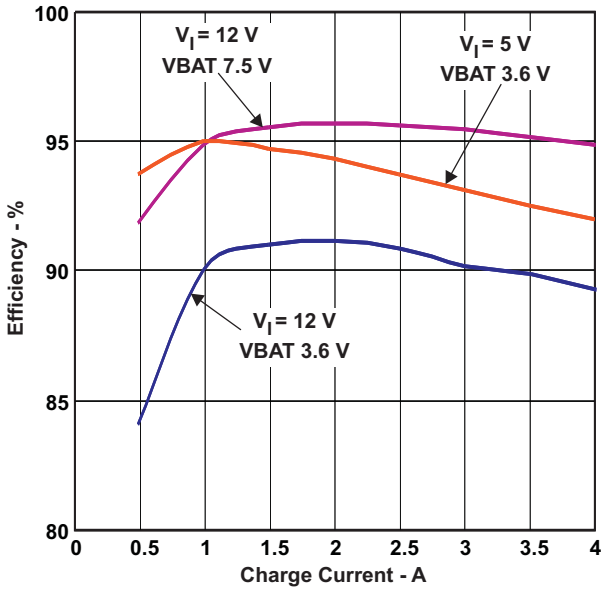

Figure 15. Efficiency

DETAILED DESCRIPTION

Battery Voltage Regulation

Internally, the BAT pin has 717 kΩ to AGND. For output voltage above 4.2 V, but not 8.4 V or 12 V, the user can use an external resistor divider from output to VBAT pin to AGND.

The bq24130 offers a high accuracy voltage regulation on charge voltage. The bq24130 uses CELL pin to select number of cells with a fixed 4.2 V/cell. CELL pin adjusts internal resistor voltage divider from BAT pin to AGND pin for voltage feedback and regulate to internal 2.1 V voltage reference.

Table 1.

CELL Pin	Voltage Regulation
AGND	4.2V
Floating	8.4V
VREF	12.6V

Internally, the BAT pin has 717 kΩ to AGND. For output voltage above 4.2 V, but not 8.4 V or 12 V, the user can use an external resistor divider from output to the VBAT pin to AGND.

Battery Current Regulation

The bq24130 has two current setting inputs, ISET1 and ISET2.

A low-level signal on the CMOD pin forces the IC to charge at the pre-charge rate set on the ISET2 pin. A high-level signal forces charge at fast-charge rate as set by the ISET1 pin. The CMOD pin cannot float.

The ISET1 input sets the maximum charging current. Battery current is sensed by current sensing resistor RSR connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is 40 mV max. The equation for charge current is:

$$I_{(CHARGE)} = \frac{V_{(ISET1)}}{20 \times R_{(SR)}} \quad (1)$$

The valid input voltage range of ISET1 is up to 0.8 V. With 10 mΩ sense resistor, the maximum output current is 4 A. With 20 mΩ sense resistor, the maximum output current is 2 A.

The ISET2 input sets the pre-charge current up to 2 A on a 10 mΩ sense resistor.

$$I_{(PRECHARGE)} = \frac{V_{(ISET2)}}{100 \times R_{(SR)}} \quad (2)$$

The charger is disabled when ISET1 pin voltage is below 40 mV and is enabled when ISET1 pin voltage is above 120 mV. For 10 mΩ current sensing resistor, the minimum fast charge current must higher than 600 mA.

Under high ambient temperature, the charge current will fold back to keep IC temperature not exceeding 120°C

Power Up

The charger uses a SLEEP comparator to determine the source of power on the AVCC pin, since AVCC can be supplied either from the battery or the adapter. If the AVCC voltage is greater than the SRN voltage, charger exits SLEEP mode. If all conditions are met for charging, charger will then attempt to charge the battery (See the Enable and Disable Charging section). If the SRN voltage is greater than AVCC, charger enters a low quiescent current 15 µA) SLEEP mode to minimize current drain from the battery. During the SLEEP mode, the VREF output turns off and the STAT pin goes to high impedance.

If AVCC is below the UVLO threshold, the device is disabled.

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Enable and Disable Charging

The following conditions have to be valid before charge is enabled:

- ISET1 pin above 120 mV
- The device is not in Under Voltage Lockout (UVLO) mode (i.e. $V_{(AVCC)}$ > UVLO)
- The device is not in SLEEP mode (i.e. $V_{(AVCC)} > V_{(SRN)}$)
- The AVCC voltage is lower than the AC over-voltage threshold (i.e. $V_{(AVCC)} < V_{(ACOV)}$)
- 50 ms delay is complete after initial power-up
- The REGN and VREF LDO voltages are at the correct levels
- Thermal Shut down (T_{SHUT}) is not valid
- No T_S fault is detected

One of the following conditions will stop on-going charging:

- ISET1 pin voltage is below 40mV;
- The device is in UVLO mode;
- Adapter is removed, causing the device to enter SLEEP mode;
- AVCC voltage is over voltage
- The REGN or VREF LDO voltage is overloaded;
- T_{SHUT} temperature threshold is reached.
- T_S voltage goes out of range indicating the battery temperature is too hot or too cold

Automatic Internal Soft-Start Charger Current

The charger automatically soft-starts the charger regulation current every time the charger goes into fast-charge to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft-start consists of stepping-up the charge regulation current into 8 evenly divided steps up to the programmed charge current. Each step lasts around 1.6 ms, for a typical rise time of 12.8 ms. No external components are needed for this function.

Converter Operation

The bq24130 employs a 600kHz constant-frequency step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design and keeping it out of the audible noise region.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal saw-tooth ramp is compared to the internal error control signals to vary the duty-cycle of the converter. The ramp height is proportional to the AVCC voltage to cancel out any loop gain variation due to a change in input voltage, and simplifies loop compensation. Internal gate drive logic allows achieving 97% duty cycle before pulse skipping starts.

Charge Undercurrent Protection

When the voltage between BTST and SW falls below 4 V, the low-side FET turns on to provide refresh charge up the bootstrap capacitor. After the recharge, if the SRP-SRN voltage decreases below 5 mV, the low side FET will be turned off for the remainder of the switching cycle (i.e. non-synchronous operation). This is important to prevent negative inductor current from causing any boost effect in which the input voltage increases as power is transferred from the battery to the input capacitors. This can lead to an overvoltage on the AVCC node and potentially cause damage to the system.

When the IC senses SRP-SRN average voltage drops below 1.25 mV (0.125 A of inductor current for a 10 mΩ sense resistor) or the battery voltage is less than 2 V, the charger will enter non-synchronous mode and the low-side n-channel power MOSFET will stay off and rely on the body diode to make converter as a standard buck. This prevents the battery discharge current when battery is almost fully charged and current tapers down to a lower level. The low-side n-channel power MOSFET will turn on when a bootstrap capacitor refresh pulse is needed.

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Charge Overcurrent Protection

The charger monitors top side MOSFET current by high side sense FET. When peak current is higher than over-current threshold, it will turn off the top side MOSFET and keep it off until the next cycle. The charger has a secondary cycle-to-cycle over-current protection. It monitors the charge current, and prevents the current from exceeding 160% of the programmed charge current. The high-side gate drive turns off when the overcurrent is detected, and automatically resumes when the current falls below the over-current threshold.

Battery Overvoltage Protection

The converter will not allow the high-side FET to turn-on until the battery voltage goes below 102% of the regulation voltage. This allows one-cycle response to an over-voltage condition – such as occurs when the load is removed or the battery is disconnected. An 8 mA current sink from SRP/SRN to AGND is on only during charge and allows discharging the stored output inductor energy that is transferred to the output capacitors. If battery overvoltage condition lasts for more than 30 ms, charge is disabled.

Battery Short Protection

When SRN pin voltage is lower than 2 V it is considered as battery short condition during charging period. The charger will shut down immediately, then soft start back to the charging current 1.25 A max. This prevents high current may build in output inductor and cause inductor saturation when battery terminal is shorted during charging. The converter works in non-synchronous mode during battery short.

Input Overvoltage Protection (ACOV)

ACOV provides protection to prevent system damage due to high input voltage. In bq24130, once the voltage on AVCC reaches the 18 V ACOV threshold, charge is disabled.

Input Under Voltage Lock Out (UVLO)

The system must have a minimum 3.85 V AVCC voltage to allow proper operation. This AVCC voltage could come from either input adapter or battery, since a conduction path exists from the battery to AVCC through the high side NMOS body diode. When AVCC is below the 3.85 V UVLO threshold, all circuits on the IC are disabled.

Thermal Regulation and Shutdown Protection

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. The internal thermal regulation loop will adjust the charge current to maintain the junction temperature around 120°C.

As added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the T_{SHUT} threshold of 150°C. The charger stays off until the junction temperature falls below 130°C.

Temperature Qualification

The controller continuously monitors battery temperature by measuring the voltage between the TS pin and AGND. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The controller compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the $V_{(LTF)}$ to $V_{(HTF)}$ thresholds. If battery temperature is outside of this range, the controller suspends charge and waits until the battery temperature is within the $V_{(LTF)}$ to $V_{(HTF)}$ range. During the charge cycle the battery temperature must be within the $V_{(LTF)}$ to $V_{(TCO)}$ thresholds. If battery temperature is outside of this range, the controller suspends charge and waits until the battery temperature is within the $V_{(LTF)}$ to $V_{(HTF)}$ range. The controller suspends charge by turning off the PWM charge MOSFETs. Figure 16 summarizes the operation.

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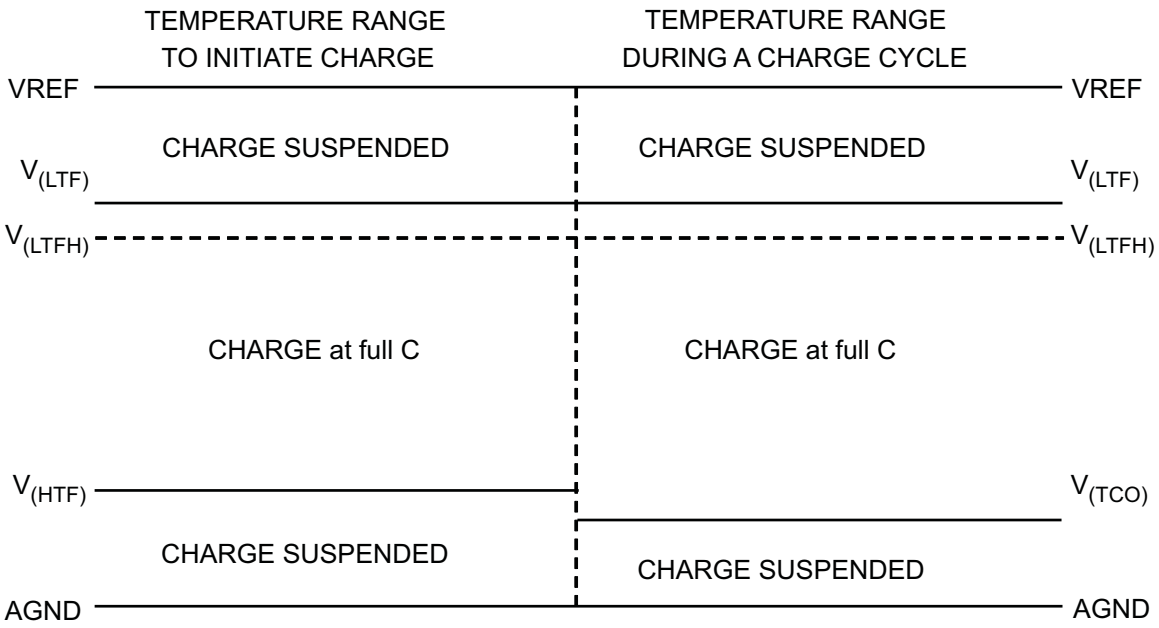

Figure 16. TS pin, Thermistor Sense Thresholds

Assuming a 103AT NTC thermistor on the battery pack as shown in Figure 1, the value RT1 and RT2 can be determined by using Equation 4 and Equation 4:

$$RT2 = \frac{V_{(VREF)} \times RTH_{(COLD)} \times RTH_{(HOT)} \times \left(\frac{1}{V_{(LTF)}} - \frac{1}{V_{(TCO)}} \right)}{RTH_{(HOT)} \times \left(\frac{V_{(VREF)}}{V_{(TCO)}} - 1 \right) - RTH_{(COLD)} \times \left(\frac{V_{(VREF)}}{V_{(LTF)}} - 1 \right)} \quad (3)$$

$$RT1 = \frac{\frac{V_{(VREF)}}{V_{(LTF)}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{(COLD)}}} \quad (4)$$

Select 0°C to 45°C range for Li-ion or Li-polymer battery.

- $RTH_{(COLD)}$ = 27.28 KΩ
- $RTH_{(HOT)}$ = 4.911 KΩ
- RT1 = 5.253 kΩ, Select Resistor 5.23k
- RT2 = 31.318 kΩ, Select Resistor 30.9k

After select closest standard resistor value, by calculating the thermistor resistance at temperature threshold, the final temperature range can be determined from thermistor data sheet temperature-resistance.

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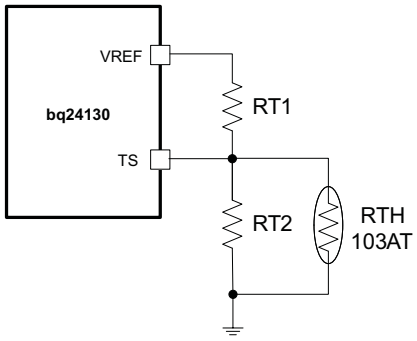

Figure 17. TS Resistor Network

Inductor, Capacitor, and Sense Resistor Selection Guidelines

The IC provides internal loop compensation. With this scheme, best stability occurs when the LC resonant frequency, f_o, is approximately 12 kHz – 17 kHz for IC per Equation 5:

$$f_o = \frac{1}{2\pi\sqrt{LC}} \quad (5)$$

Charge Status Outputs

The open-drain STAT outputs indicate various charger operations as shown in . These status pins can be used to drive LED or communicate with the host processor. Note that OFF indicates that the open-drain transistor is turned off.

Table 2. STAT Pin Defination

Charge State	STAT
Charge in progress	On
Sleep mode, Charge Disabled	OFF
Chagre suspended. Input overvoltage, Battery overvoltage	BLINK

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APPLICATION INFORMATION

Inductor Selection

The bq24130 has 600 kHz switching frequency to allow the use of small inductor and capacitor values. The Inductor saturation current should be higher than the charging current ($I_{(CHG)}$) plus half the ripple current ($I_{(RIPPLE)}$):

$$I_{(SAT)} \geq I_{(CHG)} + (1/2)\ I_{(RIPPLE)} \quad (6)$$

The inductor ripple current depends on input voltage (V_{IN}), duty cycle ($D = V_{OUT}/V_{IN}$), switching frequency (fs) and inductance (L):

$$I_{(RIPPLE)} = \frac{V_{IN} \times D \times (1-D)}{fs \times L} \quad (7)$$

Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current $I_{(CIN)}$ occurs where the duty cycle is closest to 50% and can be estimated by Equation 8:

$$I_{(CIN)} = I_{(CHG)} \times \sqrt{D \times (1-D)} \quad (8)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25 V rating or higher capacitor is preferred for 15 V input voltage. 20 µF capacitance is suggested for typical of 3 A - 4 A charging current.

Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current $I_{(COUT)}$ is given:

$$I_{(COUT)} = \frac{I_{(RIPPLE)}}{2 \times \sqrt{3}} \approx 0.29 \times I_{(RIPPLE)} \quad (9)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The bq24130 has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 12 kHz and 17 kHz. The preferred ceramic capacitor is 25 V or higher rating, X7R or X5R

Input Filter Design

During adapter hot plug-in, the parasitic inductance and input capacitor from the adapter cable form a second order system. The voltage spike at AVCC/PVCC pin may be beyond IC maximum voltage rating and damage IC. The input filter must be carefully designed and tested to prevent overvoltage event on AVCC/PVCC pin.

There are several methods to damping or limit the overvoltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the overvoltage spike well below the IC maximum pin voltage rating. A high current capability TVS Zener diode can also limit the over voltage level to an IC safe level. However, these two solutions may not have low cost or small size.

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A cost effective and small size solution is shown in Figure 18. The R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result the overvoltage spike is limited to a safe level. D1 is used for reverse voltage protection for AVCC pin. C2 is AVCC pin decoupling capacitor and it should be place to AVCC pin as close as possible. The R2 and C2 form a damping RC network to further protect the IC from high dv/dt and high voltage spike. C2 value should be less than C1 value so R1 can dominant the equivalent ESR value to get enough damping effect for hot plug-in. R1 and R2 package must be sized enough to handle inrush current power loss according to resistor manufacturer's data sheet. The filter components value always need to be verified with real application and minor adjustments may need to fit in the real application circuit.

If the input is 5 V (USB host or USB adapter), the D1 can be saved. R2 has to be 5 Ω or higher to limit the current if the input is reversely inserted.

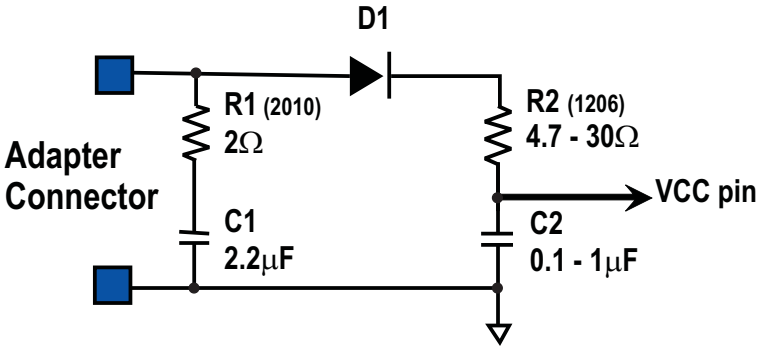

Figure 18. Input Filter

PCB LAYOUT

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 19) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential

1. Place input capacitor as close as possible to PVCC supply and ground connections and use shortest copper trace connection. These parts should be placed on the same layer of PCB instead of on different layers and using vias to make this connection.
2. Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. The charging current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see Figure 20 for Kelvin connection for best current accuracy). Place decoupling capacitor on these traces next to the IC.
4. Place output capacitor next to the sensing resistor output and ground.
5. Output capacitor ground connections need to be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
6. Route analog ground separately from power ground and use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling. Use thermal pad as the single ground connection point to connect analog ground and power ground together. Or using a 0 Ω resistor to tie analog ground to power ground (thermal pad should tie to analog ground). A star-connection under thermal pad is highly recommended.
7. It is critical that the exposed thermal pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.

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9. All via size and number should be enough for a given current path.

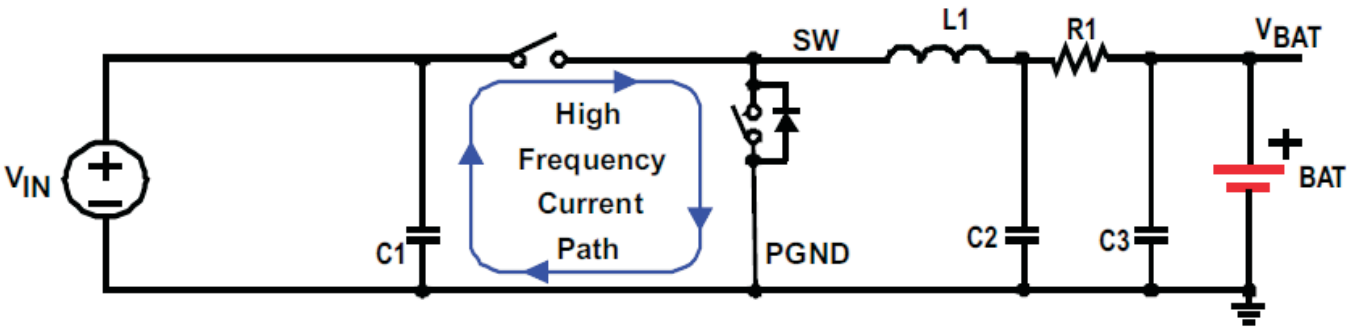

Figure 19. High Frequency Current Path

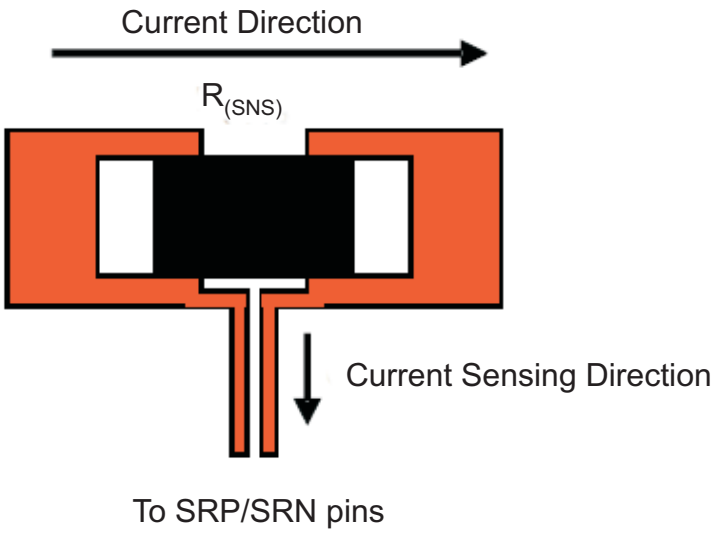

Figure 20. Sensing Resistor PCB Layout

REVISION HISTORY

Changes from Original (July 2011) to Revision A **Page**

- Added the Li-Ion/Li-Polymer battery Application 1
- Changed pin BTST Description From: Connect the 0.1 µF bootstrap capacitor. To: Connect the 47 nF bootstrap capacitor 2
- Changed the Min and Max values for Voltage in the ABS Max Ratings Table 3
- Changed the RECOMMENDED OPERATING CONDITIONS table 3
- Changed the ELECT CHARACTERISTICS conditions statement From: 4.5 V ≤ $V_{(PVCC,\ AVCC)}$ ≤ 18 V To: 4.5 V ≤ $V_{(PVCC,\ AVCC)}$ ≤ 17 V 4
- Changed the Electrical Characteristics table 4
- Added Figure 2 9
- Added the TYPICAL CHARACTERISTICS section 10
- Changed the Battery Voltage Regulation section 14
- Changed the Charge Overcurrent Protection section 16

Changes from Revision A (August 2011) to Revision B **Page**

- Added Features Bullet: Constant Current Super Capacitor Charging 1
- Changed the Thermal Information Table 3
- Changed Figure 1 8
- Changed Figure 2 9
- Changed Figure 14 12

Changes from Revision B (August 2011) to Revision C **Page**

- Changed the value of RT1 From: RT1 = 31.23 KΩ To: RT1 = 5.253 kΩ, Select Resistor 5.23k 17
- Changed the value of RT2 From: RT2 = 5.25 KΩ To: RT2 = 31.318 kΩ, Select Resistor 30.9k 17

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24130RHLR	ACTIVE	VQFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ24130	Samples
BQ24130RHLT	ACTIVE	VQFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ24130	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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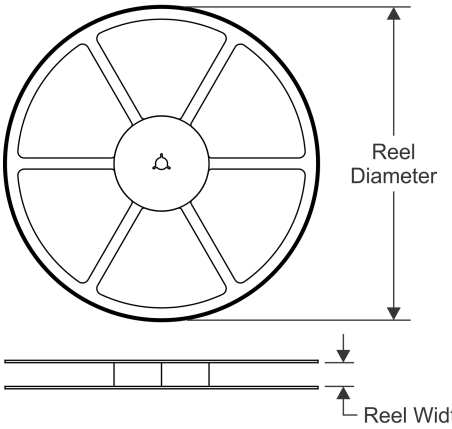
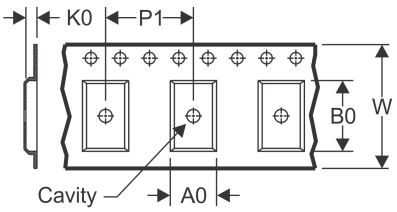
TAPE AND REEL INFORMATION

REEL DIMENSIONS

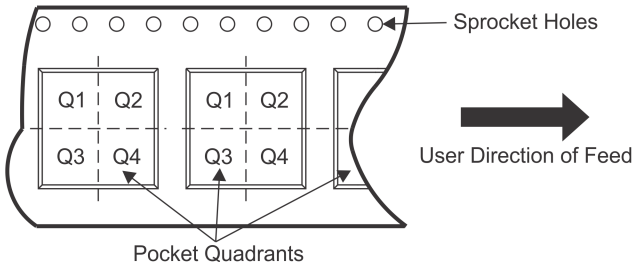


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

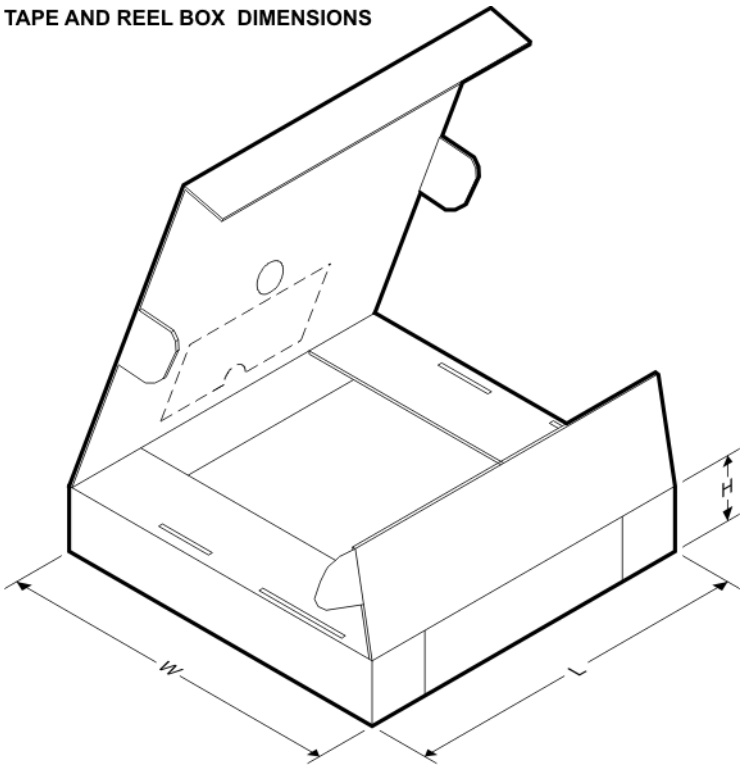
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24130RHLR	VQFN	RHL	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ24130RHLT	VQFN	RHL	20	250	180.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

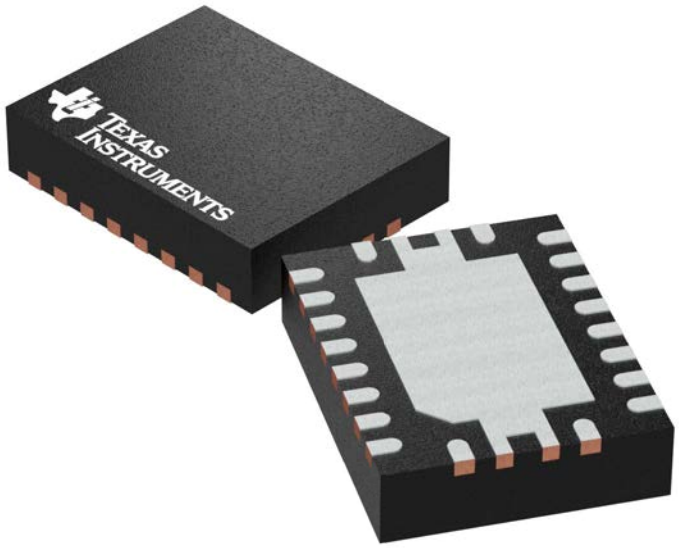
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24130RHLR	VQFN	RHL	20	3000	367.0	367.0	35.0
BQ24130RHLT	VQFN	RHL	20	250	210.0	185.0	35.0

RHL 20

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

3.5 x 4.5 mm, 0.5 mm pitch



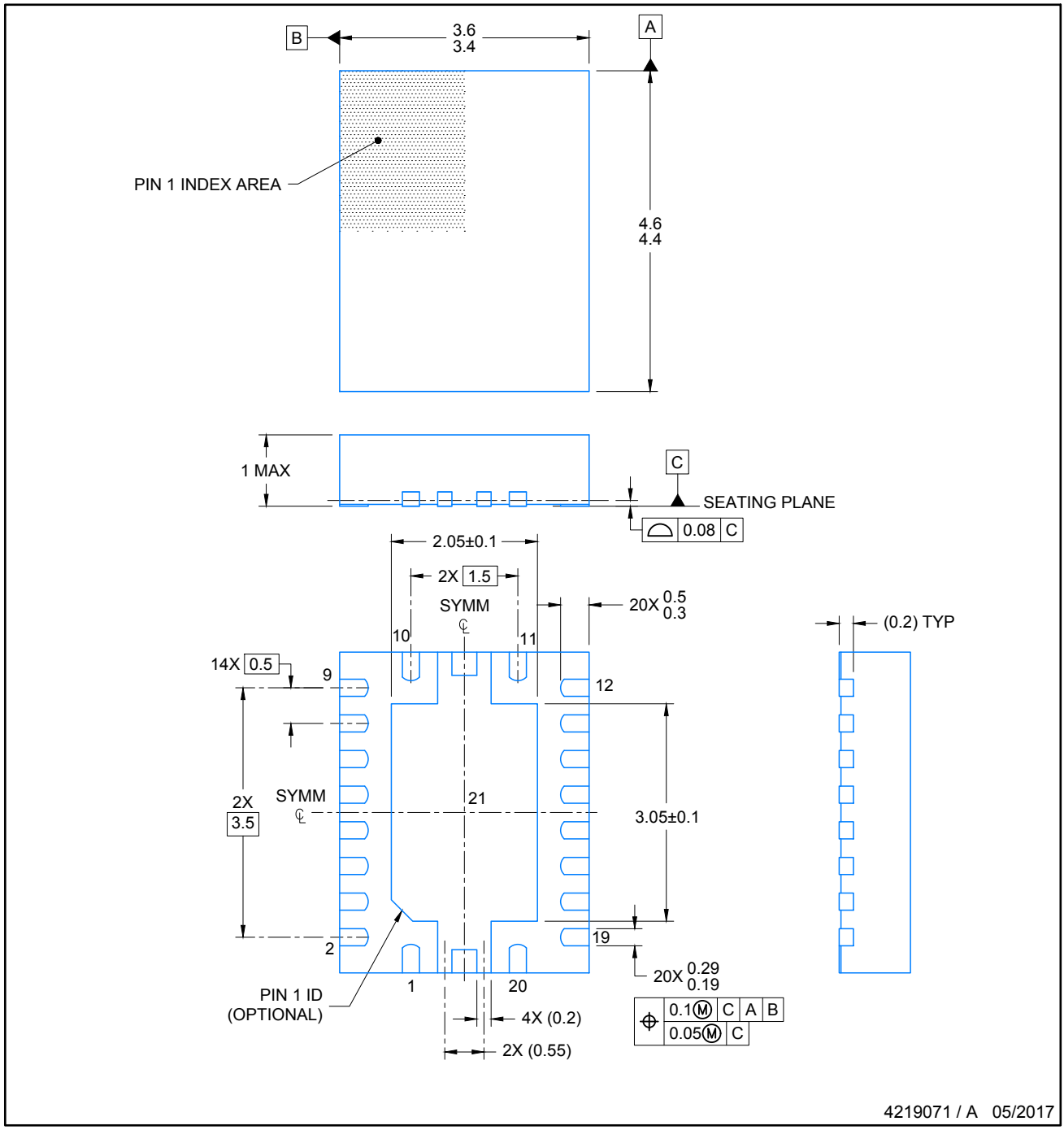
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RHL0020A

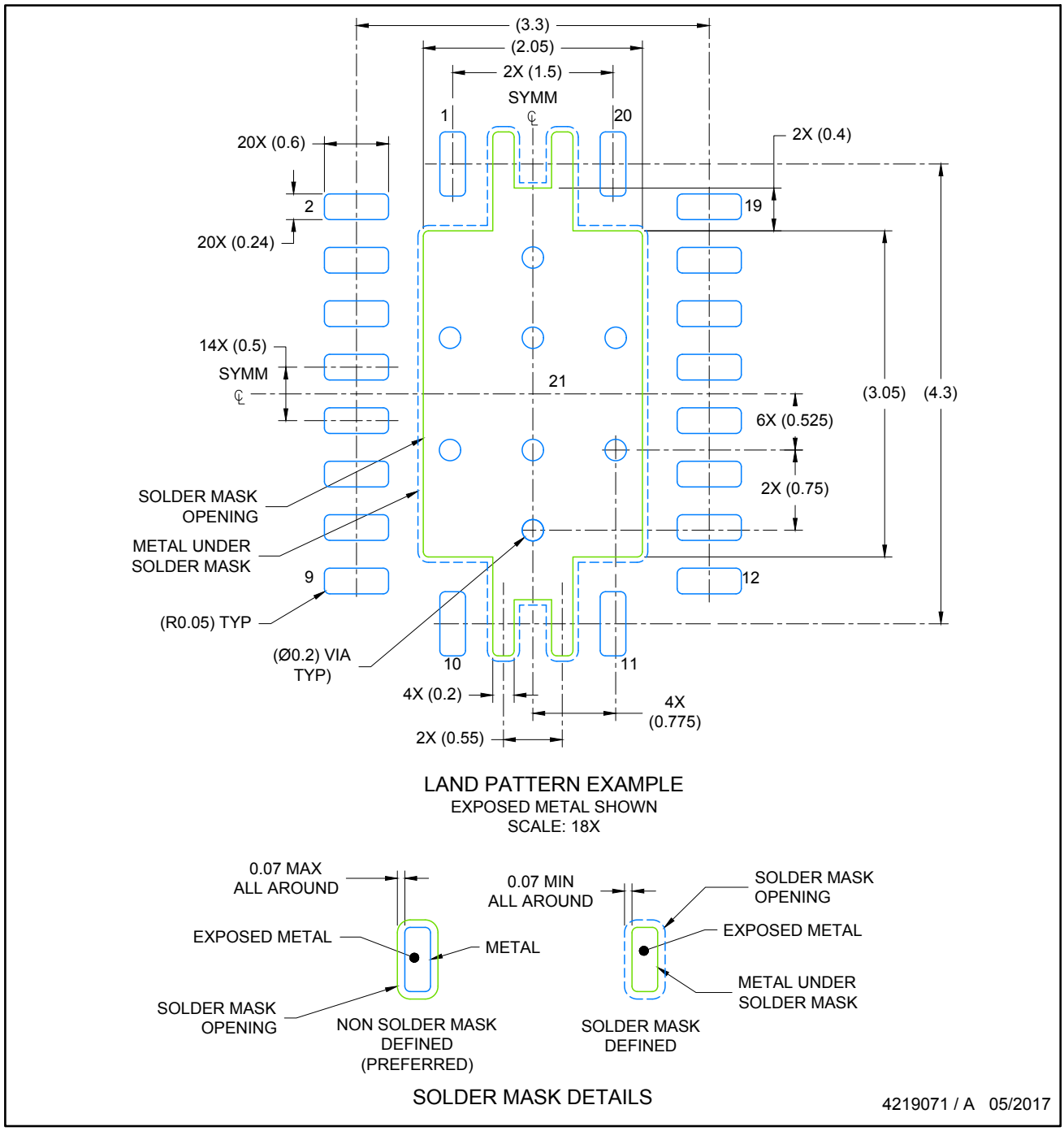
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

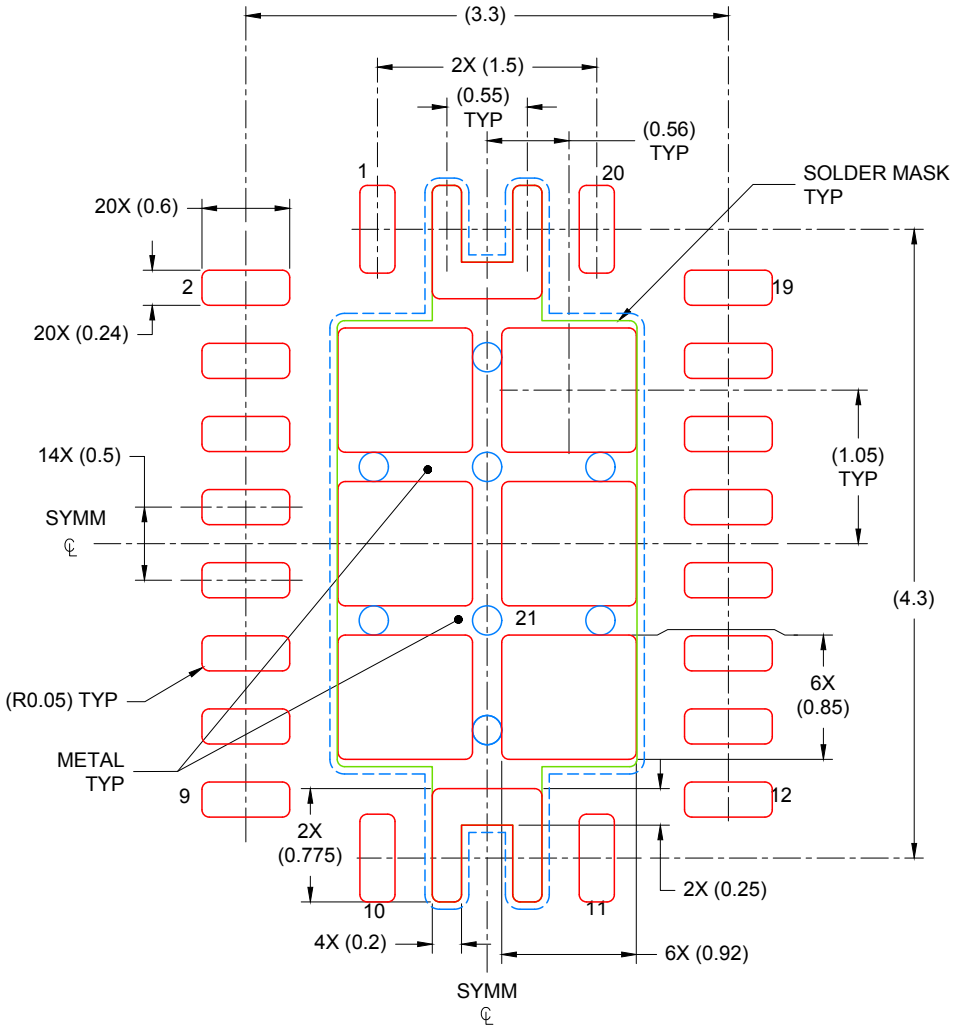


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to theri locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 20X

4219071 / A 05/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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