THE DATASHEET OF

ADS7846IRGVTG4

SBAS125H – SEPTEMBER 1999 – REVISED JANUARY 2005

TOUCH SCREEN CONTROLLER

FEATURES

- SAME PINOUT AS ADS7843
- 2.2V TO 5.25V OPERATION
- INTERNAL 2.5V REFERENCE
- DIRECT BATTERY MEASUREMENT (0V to 6V)
- ON-CHIP TEMPERATURE MEASUREMENT
- TOUCH-PRESSURE MEASUREMENT
- QSPI™/SPI™ 3-WIRE INTERFACE
- AUTO POWER-DOWN
- TSSOP-16, SSOP-16, QFN-16, AND VFBGA-48 PACKAGES

APPLICATIONS

- PERSONAL DIGITAL ASSISTANTS
- PORTABLE INSTRUMENTS
- POINT-OF-SALE TERMINALS
- PAGERS
- TOUCH SCREEN MONITORS
- CELLULAR PHONES

US Patent No. 6246394

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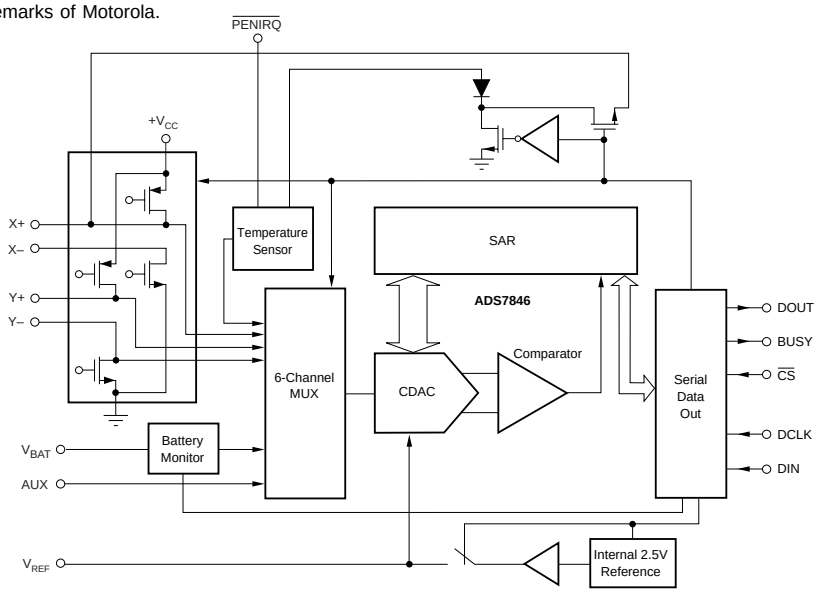
DESCRIPTION

The ADS7846 is a next-generation version to the industry standard ADS7843 4-wire touch screen controller. The ADS7846 is 100% pin-compatible with the existing ADS7843, and drops into the same socket. This allows for easy upgrade of current applications to the new version. Only software changes are required to take advantage of the added features of direct battery measurement, temperature measurement, and touch-pressure measurement. The ADS7846 also has an on-chip 2.5V reference that can be used for the auxiliary input, battery monitor, and temperature measurement modes. The reference can also be powered down when not used to conserve power. The internal reference operates down to 2.7V supply voltage while monitoring the battery voltage from 0V to 6V.

The low-power consumption of < 0.75mW (typ at 2.7V, reference off), high speed (up to 125kHz clock rate), and on-chip drivers make the ADS7846 an ideal choice for battery-operated systems such as personal digital assistants (PDAs) with resistive touch screens, pagers, cellular phones, and other portable equipment. The ADS7846 is available in the small TSSOP-16, SSOP-16, QFN-16, and VFBGA-48 packages and is specified over the –40°C to +85°C temperature range.



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ABSOLUTE MAXIMUM RATINGS[1]

$+V_{CC}$ to GND	–0.3V to +6V
Analog Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Digital Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings can cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER
ADS7846E	±2	SSOP-16	DBQ	–40°C to +85°C	ADS7846E	ADS7846E
"	"	"	"	"	"	ADS7846E/2K5
ADS7846N	±2	TSSOP-16	PW	–40°C to +85°C	ADS7846N	ADS7846N
"	"	"	"	"	"	ADS7846N/2K5
"	"	"	"	"	"	ADS7846N/2K5G4
ADS7846I	±2	VFBGA-48	GQC	–40°C to +85°C	ADS7846	ADS7846IGQCR
ADS7846I	±2	QFN-16	RGV	–40°C to +85°C	ADS7846	ADS7846IRGVT
"	"	"	"	"	"	ADS7846IRGVR

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

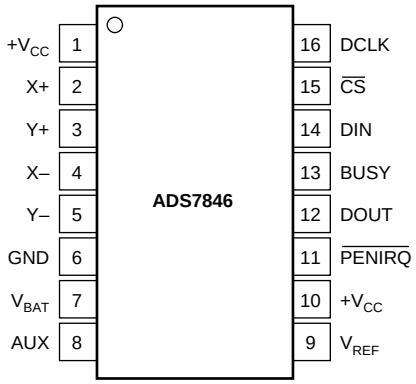
At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = 2.5V internal voltage, f_{SAMPLE} = 125kHz, f_{CLK} = 16 • f_{SAMPLE} = 2MHz, 12-bit mode, and digital inputs = GND or $+V_{CC}$, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7846E MIN	ADS7846E TYP	ADS7846E MAX	UNITS
ANALOG INPUT					
Full-Scale Input Span	Positive Input-Negative Input	0		V_{REF}	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ + 0.2	V
	Negative Input	–0.2		+0.2	V
Capacitance			25		pF
Leakage Current			0.1		µA
SYSTEM PERFORMANCE					
Resolution			12		Bits
No Missing Codes		11			Bits
Integral Linearity Error				±2	LSB(1)
Offset Error				±6	LSB
Gain Error	External V_{REF}			±4	LSB
Noise	Including Internal V_{REF}		70		µVrms
Power-Supply Rejection			70		dB
SAMPLING DYNAMICS					
Conversion Time				12	CLK Cycles
Acquisition Time		3			CLK Cycles
Throughput Rate				125	kHz
Multiplexer Settling Time			500		ns
Aperture Delay			30		ns
Aperture Jitter			100		ps
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 50kHz		100		dB
SWITCH DRIVERS					
On-Resistance					
Y+, X+			5		Ω
Y–, X–			6		Ω
Drive Current(2)	Duration 100ms			50	mA
REFERENCE OUTPUT					
Internal Reference Voltage		2.45	2.50	2.55	V
Internal Reference Drift			15		ppm/°C
Quiescent Current			500		µA
REFERENCE INPUT					
Range		1.0		$+V_{CC}$	V
Input Impedance	SER/$\overline{DFR}$ = 0, PD1 = 0,		1		GΩ
	Internal Reference Off				
	Internal Reference On		250		Ω
BATTERY MONITOR					
Input Voltage Range		0.5		6.0	V
Input Impedance					
Sampling Battery			10		kΩ
Battery Monitor Off			1		GΩ
Accuracy	External V_{REF} = 2.5V	–2		+2	%
	Internal Reference	–3		+3	%
TEMPERATURE MEASUREMENT					
Temperature Range		–40		+85	°C
Resolution	Differential Method(3)		1.6		°C
	TEMP0(4)		0.3		°C
Accuracy	Differential Method(3)		±2		°C
	TEMP0(4)		±3		°C
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Logic Levels, Except $\overline{PENIRQ}$					
V_{IH}	| I_{IH} | ≤ +5µA	$+V_{CC}$ • 0.7		$+V_{CC}$ + 0.3	
V_{IL}	| I_{IL} | ≤ +5µA	–0.3		+0.8	V
V_{OH}	I_{OH} = –250µA	$+V_{CC}$ • 0.8			V
V_{OL}	I_{OL} = 250µA			0.4	V
$\overline{PENIRQ}$					
V_{OL}	T_A = 0°C to +85°C, 50kΩ Pull-Up			0.8	V
Data Format			Straight Binary		
POWER-SUPPLY REQUIREMENTS					
$+V_{CC}$(5)	Specified Performance	2.7		3.6	V
	Operating Range	2.2		5.25	V
Quiescent Current	Internal Reference Off		280	650	µA
	Internal Reference On		780		µA
	f_{SAMPLE} = 12.5kHz		220		µA
	Power-Down Mode with $\overline{CS}$ = DCLK = DIN = $+V_{CC}$			3	µA
Power Dissipation	$+V_{CC}$ = +2.7V			1.8	mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C

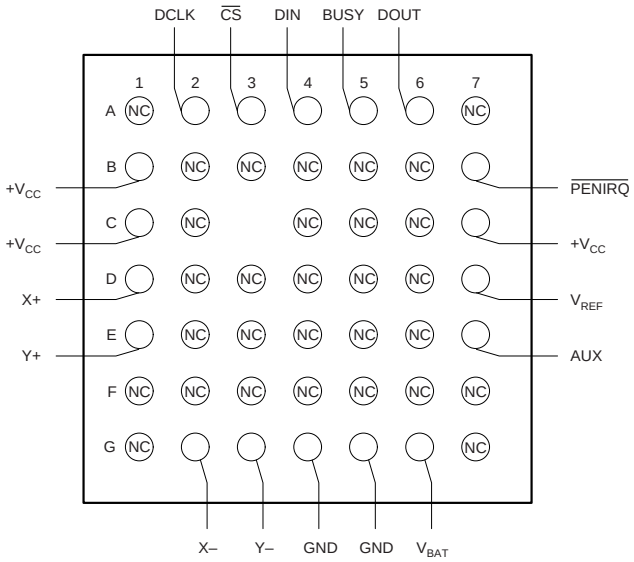
NOTES: (1) LSB means least significant bit. With V_{REF} equal to +2.5V, one LSB is 610µV. (2) Ensured by design, but not tested. Exceeding 50mA source current may result in device degradation. (3) Difference between TEMP0 and TEMP1 measurement. No calibration necessary. (4) Temperature drift is –2.1mV/°C. (5) ADS7846 operates down to 2.2V.

PIN CONFIGURATION

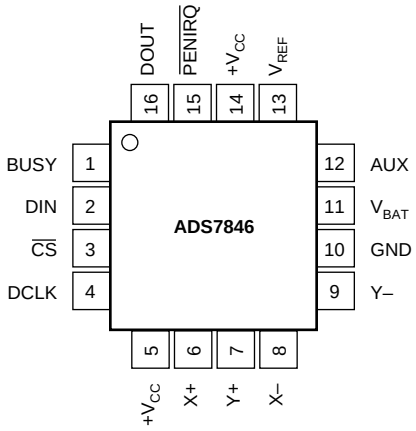
Top View **SSOP, TSSOP**



Top View **VFBGA**



Top View **QFN**



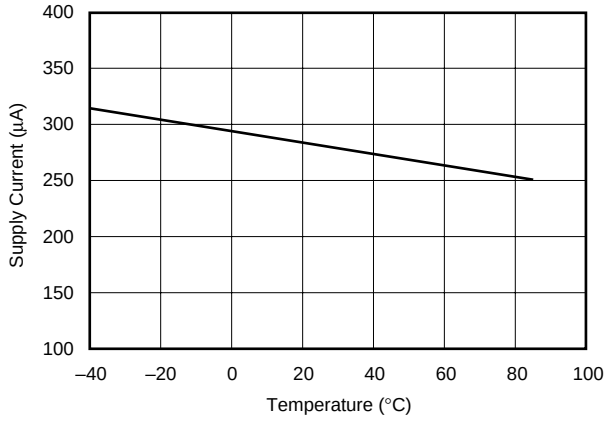
PIN DESCRIPTION

SSOP AND TSSOP PIN #	VFBGA PIN #	QFN PIN #	NAME	DESCRIPTION
1	B1 and C1	5	$+V_{CC}$	Power Supply
2	D1	6	X+	X+ Position Input
3	E1	7	Y+	Y+ Position Input
4	G2	8	X–	X– Position Input
5	G3	9	Y–	Y– Position Input
6	G4 and G5	10	GND	Ground
7	G6	11	V_{BAT}	Battery Monitor Input
8	E7	12	AUX	Auxiliary Input to ADC
9	D7	13	V_{REF}	Voltage Reference Input/Output
10	C7	14	$+V_{CC}$	Digital I/O Power Supply
11	B7	15	$\overline{\text{PENIRQ}}$	Pen Interrupt. Open anode output (requires 10kΩ to 100kΩ pull-up resistor externally).
12	A6	16	DOUT	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{\text{CS}}$ is high.
13	A5	1	BUSY	Busy Output. This output is high impedance when $\overline{\text{CS}}$ is high.
14	A4	2	DIN	Serial Data Input. If $\overline{\text{CS}}$ is low, data is latched on rising edge of DCLK.
15	A3	3	$\overline{\text{CS}}$	Chip Select Input. Controls conversion timing and enables the serial input/output register. $\overline{\text{CS}}$ high = power-down mode (ADC only).
16	A2	4	DCLK	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.

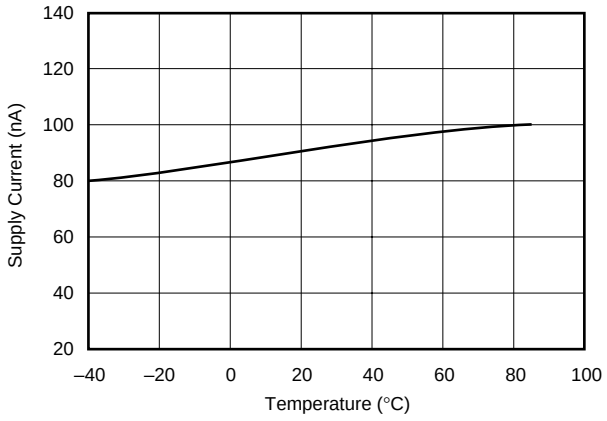
TYPICAL CHARACTERISTICS

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = External +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

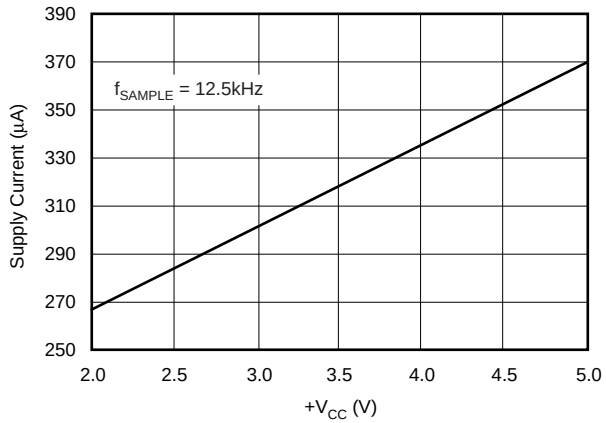
SUPPLY CURRENT vs TEMPERATURE



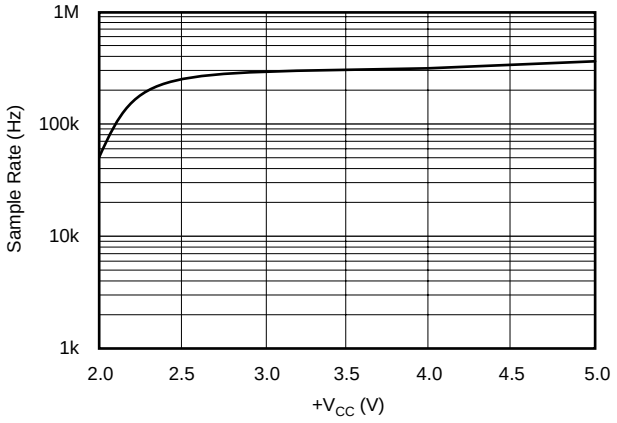
POWER-DOWN SUPPLY CURRENT vs TEMPERATURE



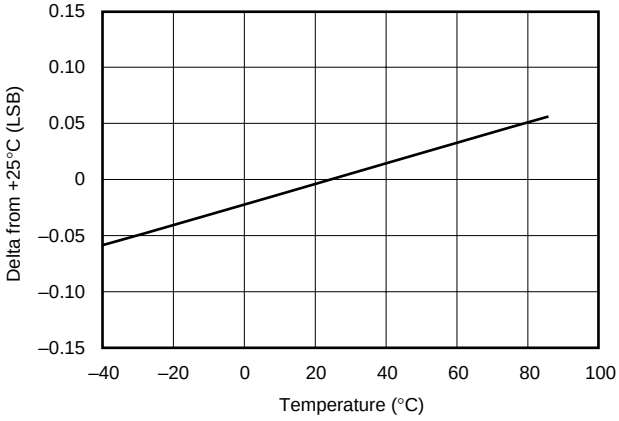
SUPPLY CURRENT vs $+V_{CC}$



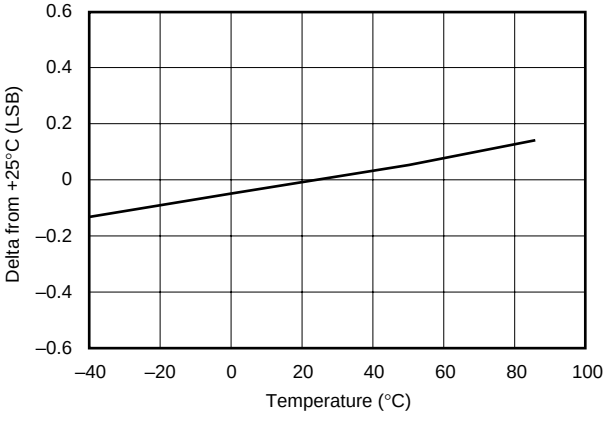
MAXIMUM SAMPLE RATE vs $+V_{CC}$



CHANGE IN GAIN vs TEMPERATURE



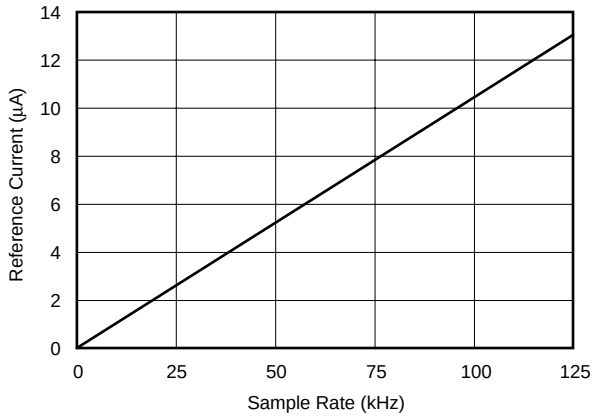
CHANGE IN OFFSET vs TEMPERATURE



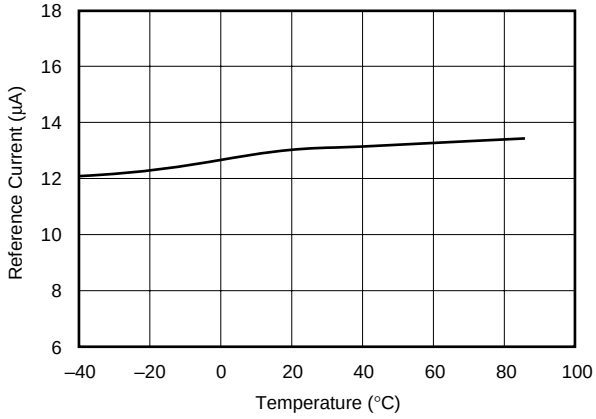
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = External +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

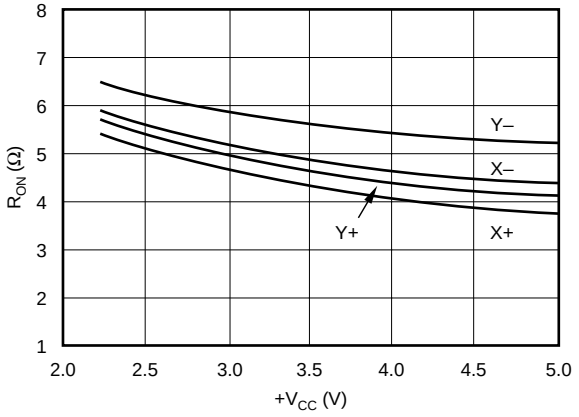
REFERENCE CURRENT vs SAMPLE RATE



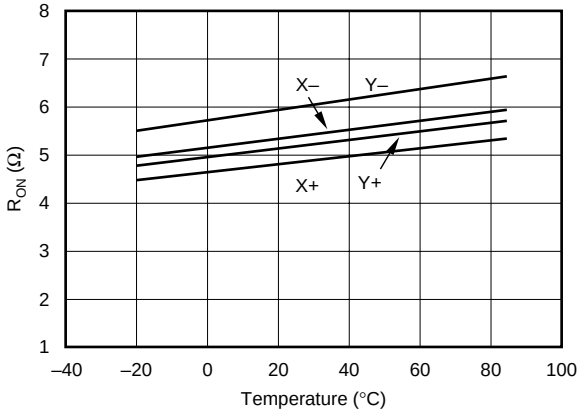
REFERENCE CURRENT vs TEMPERATURE



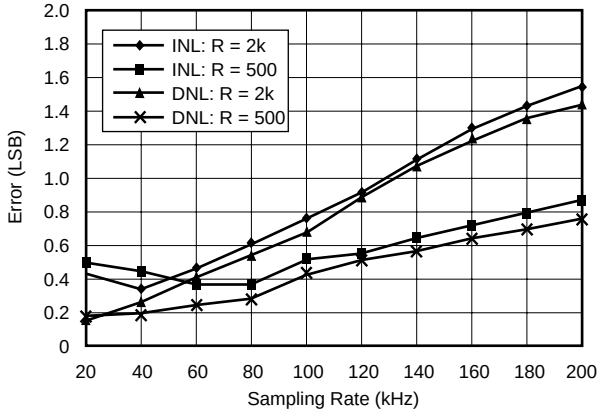
SWITCH-ON RESISTANCE vs $+V_{CC}$
(X+, Y+: $+V_{CC}$ to Pin; X–, Y–: Pin to GND)



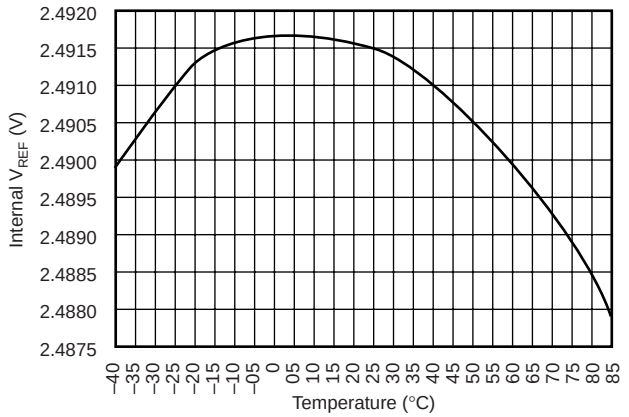
SWITCH-ON RESISTANCE vs TEMPERATURE
(X+, Y+: $+V_{CC}$ to Pin; X–, Y–: Pin to GND)



MAXIMUM SAMPLING RATE vs R_{IN}



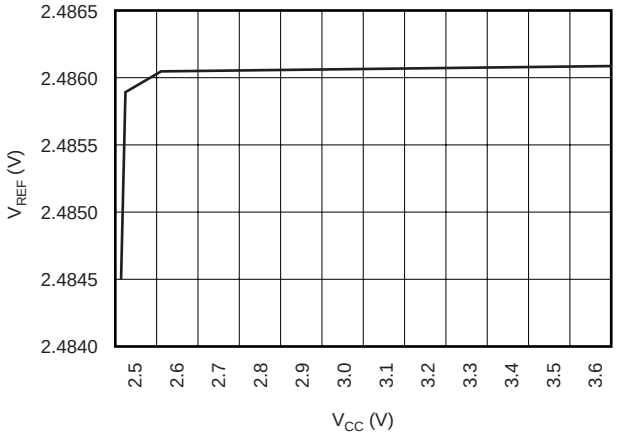
INTERNAL V_{REF} vs TEMPERATURE



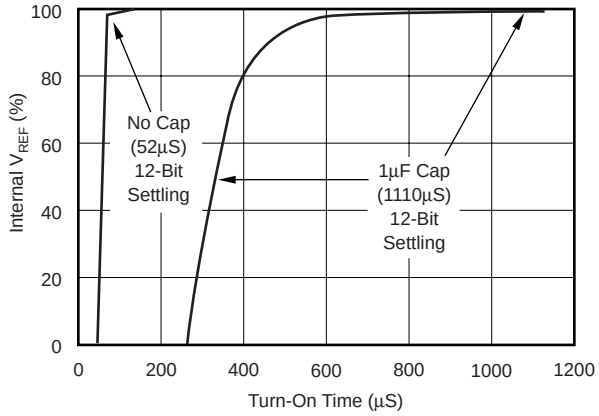
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = External +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

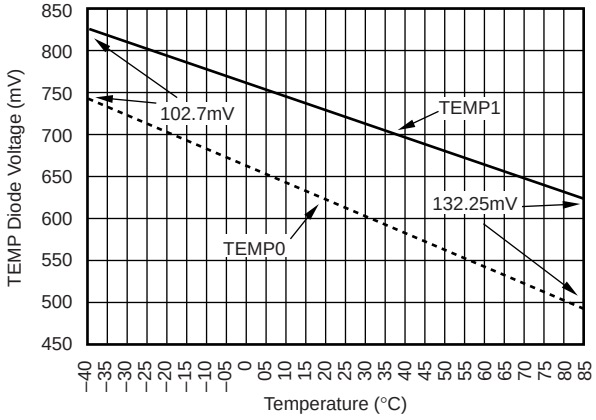
INTERNAL V_{REF} vs V_{CC}



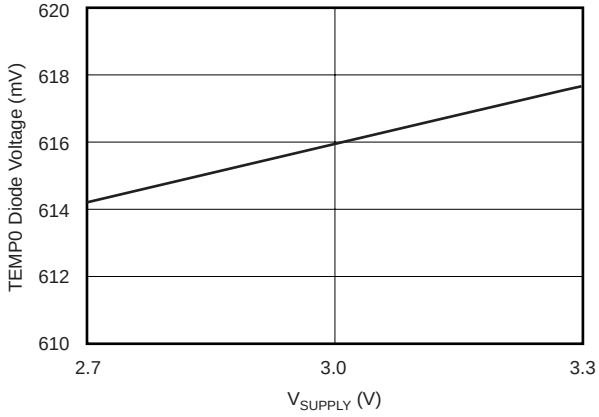
INTERNAL V_{REF} vs TURN-ON TIME



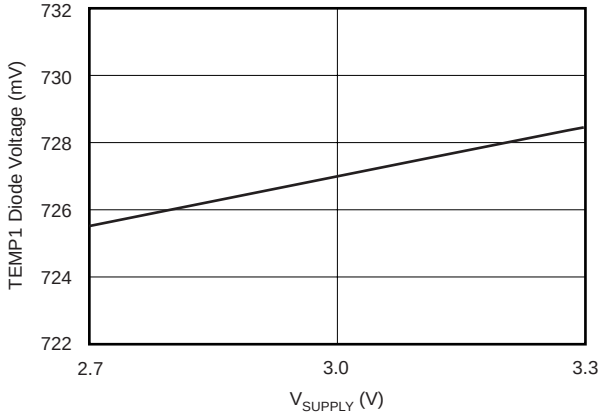
TEMP DIODE VOLTAGE
vs TEMPERATURE (2.7V SUPPLY)



TEMP0 DIODE VOLTAGE vs V_{SUPPLY} (25°C)



TEMP1 DIODE VOLTAGE vs V_{SUPPLY} (25°C)



THEORY OF OPERATION

The ADS7846 is a classic successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µm CMOS process.

The basic operation of the ADS7846 is shown in Figure 1. The device features an internal 2.5V reference and an external clock. Operation is maintained from a single supply of 2.7V to 5.25V. The internal reference can be overdriven with an external, low impedance source between 1V and $+V_{CC}$. The value of the reference voltage directly sets the input range of the converter.

The analog input (X-, Y-, and Z-position coordinates, auxiliary input, battery voltage, and chip temperature) to the converter is provided via a multiplexer. A unique configuration of low on-resistance touch panel driver switches allows an unselected ADC input channel to provide power and its accompanying pin to provide ground for an external device, such as a touch screen. By maintaining a differential input to the converter and a differential reference architecture, it is possible to negate the error from each touch panel driver switch's on-resistance (if this is a source of error for the particular measurement).

ANALOG INPUT

See Figure 2 for a block diagram of the input multiplexer on the ADS7846, the differential input of the ADC, and the differential reference of the converter. Table I and Table II show the relationship between the A2, A1, A0, and SER/$\overline{\text{DFR}}$ control bits and the configuration of the ADS7846. The control bits are provided serially via the DIN pin—see the Digital Interface section of this data sheet for more details.

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs (see Figure 2) is captured on the internal capacitor array. The input current into the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

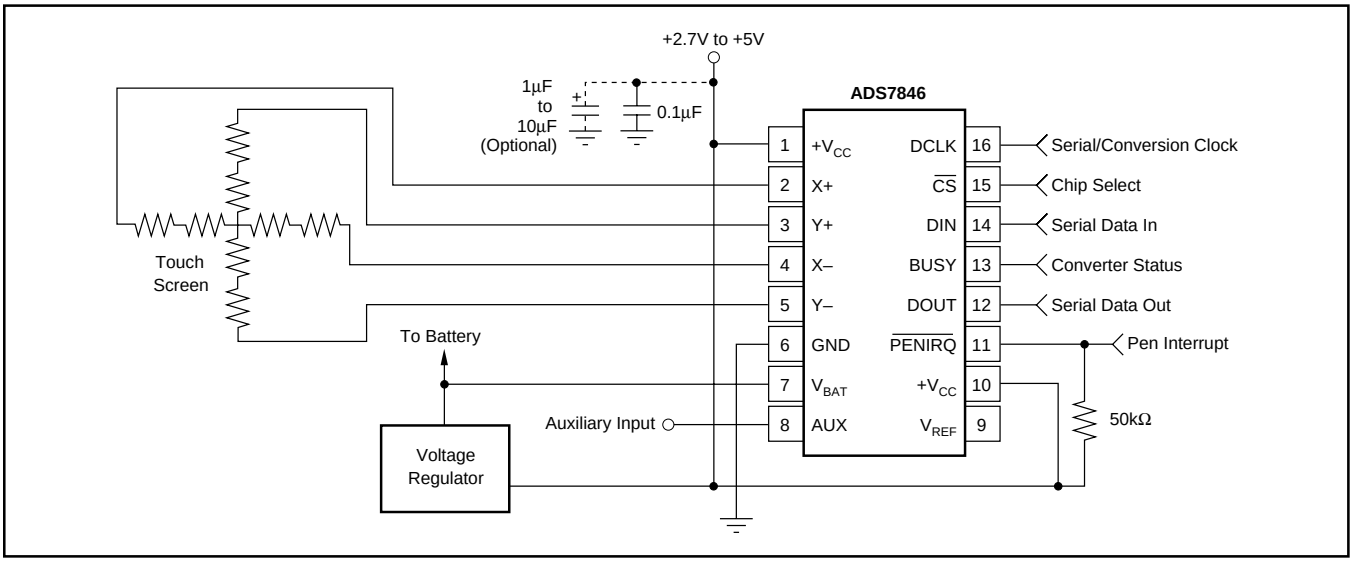


FIGURE 1. Basic Operation of the ADS7846.

A2	A1	A0	V_{BAT}	AUX_{IN}	TEMP	Y–	X+	Y+	Y-POSITION	X-POSITION	Z_1-POSITION	Z_2-POSITION	X-DRIVERS	Y-DRIVERS
0	0	0			+IN (TEMP0)								Off	Off
0	0	1					+IN		Measure				Off	On
0	1	0	+IN										Off	Off
0	1	1					+IN				Measure		X–, On	Y+, On
1	0	0				+IN						Measure	X–, On	Y+, On
1	0	1						+IN		Measure			On	Off
1	1	0		+IN									Off	Off
1	1	1			+IN (TEMP1)								Off	Off

TABLE I. Input Configuration (DIN), Single-Ended Reference Mode (SER/$\overline{\text{DFR}}$ high).

A2	A1	A0	+REF	–REF	Y–	X+	Y+	Y-POSITION	X-POSITION	Z_1-POSITION	Z_2-POSITION	DRIVERS ON
0	0	1	Y+	Y–		+IN		Measure				Y+, Y–
0	1	1	Y+	X–		+IN				Measure		Y+, X–
1	0	0	Y+	X–	+IN						Measure	Y+, X–
1	0	1	X+	X–			+IN		Measure			X+, X–

TABLE II. Input Configuration (DIN), Differential Reference Mode (SER/$\overline{\text{DFR}}$ low).

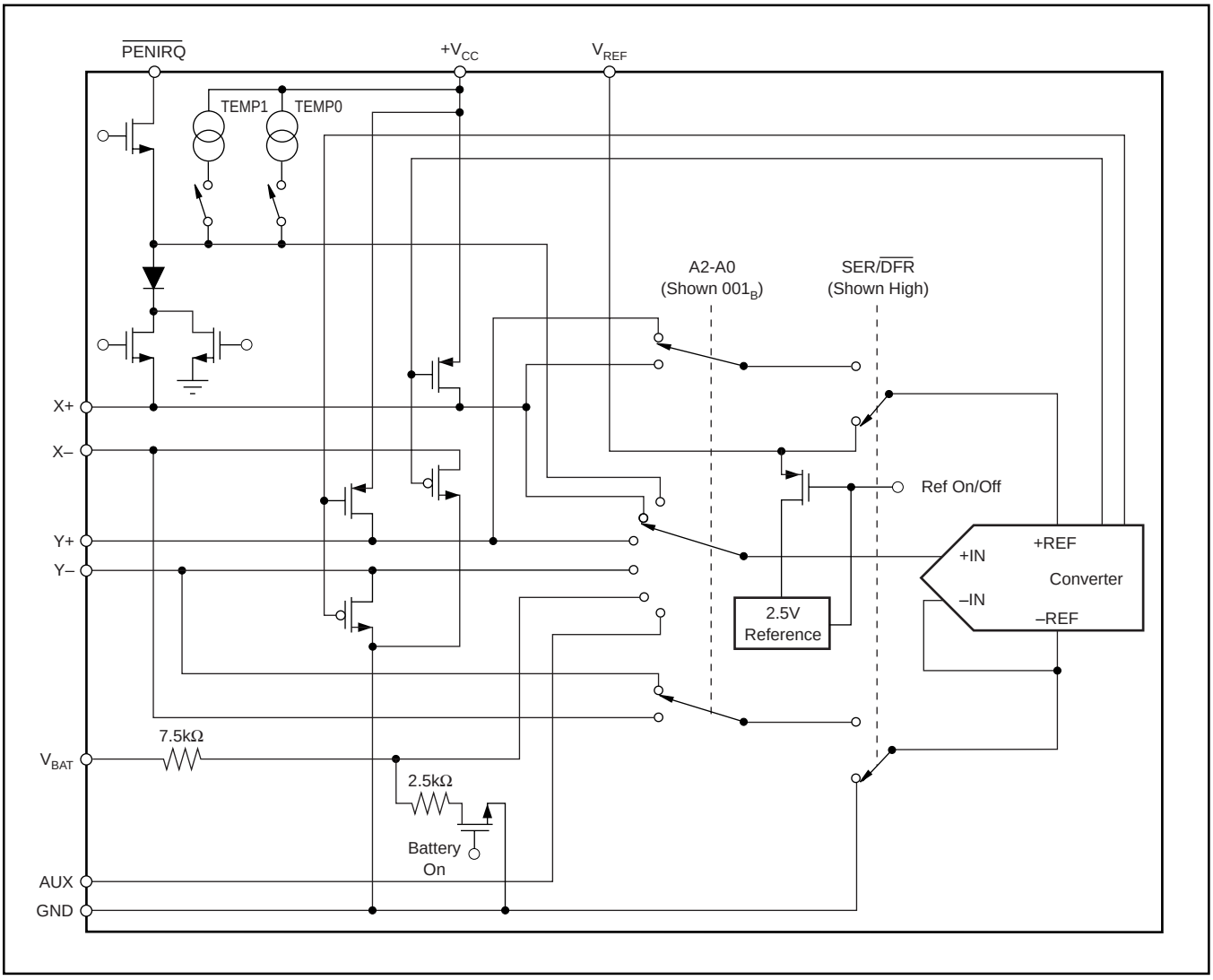


FIGURE 2. Simplified Diagram of Analog Input.

INTERNAL REFERENCE

The ADS7846 has an internal 2.5V voltage reference that can be turned on or off with the control bit, PD1 = 1 (see Table V and Figure 3). Typically, the internal reference voltage is only used in the single-ended mode for battery monitoring, temperature measurement, and for using the auxiliary input. Optimal touch screen performance is achieved when using the differential mode. The internal reference voltage of the ADS7846 must be commanded to be off to maintain compatibility with the ADS7843. Therefore, after power-up, a write of PD1 = 0 is required to insure the reference is off (see the Typical Characteristics for power-up time of the reference from power-down).

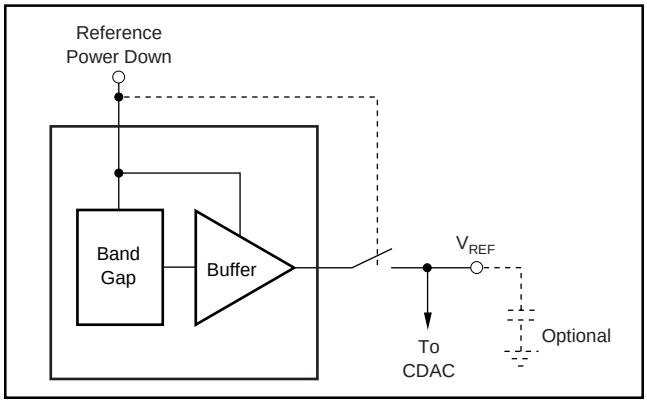


FIGURE 3. Simplified Diagram of the Internal Reference.

REFERENCE INPUT

The voltage difference between +REF and –REF (shown in Figure 2) sets the analog input range. The ADS7846 operates with a reference in the range of 1V to $+V_{CC}$. There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096 in 12-bit mode. Any offset or gain error inherent in the ADC appears to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2LSBs with a 2.5V reference, it is typically 5LSBs with a 1V reference. In each case, the actual offset of the device is the same, 1.22mV. With a lower reference

voltage, more care must be taken to provide a clean layout including adequate bypassing, a clean (low-noise, low-ripple) power supply, a low-noise reference (if an external reference is used), and a low-noise input signal.

The voltage into the V_{REF} input directly drives the capacitor digital-to-analog converter (CDAC) portion of the ADS7846. Therefore, the input current is very low (typically < 13μA).

There is also a critical item regarding the reference when making measurements where the switch drivers are on. For this discussion, it is useful to consider the basic operation of the ADS7846 (see Figure 1). This particular application shows the device being used to digitize a resistive touch screen. A measurement of the current Y position of the pointing device is made by connecting the X+ input to the ADC, turning on the Y+ and Y– drivers, and digitizing the voltage on X+ (Figure 4 shows a block diagram). For this measurement, the resistance in the X+ lead does not affect the conversion (it does affect the settling time, but the resistance is usually small enough that this is not a concern). However, since the resistance between Y+ and Y– is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it is not possible to achieve a 0V input or a full-scale input regardless of where the pointing device is on the touch screen, because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error.

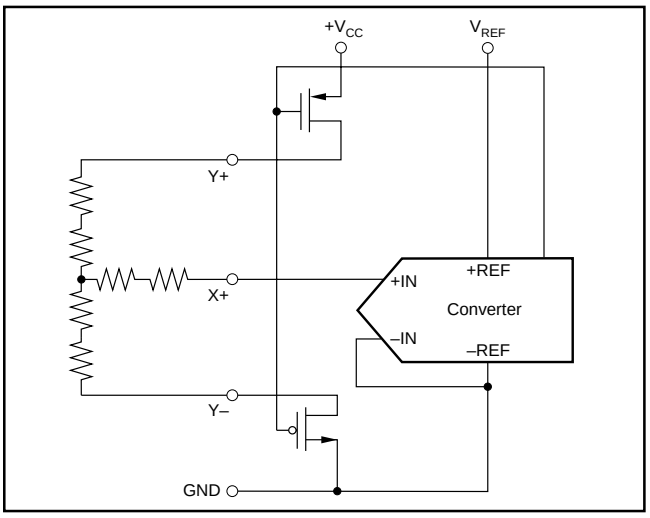


FIGURE 4. Simplified Diagram of Single-Ended Reference (SER/$\overline{DFR}$ High, Y Switches Enabled, X+ is Analog Input).

This situation can be remedied as shown in Figure 5. By setting the SER/$\overline{DFR}$ bit low, the +REF and –REF inputs are connected directly to Y+ and Y–, respectively, which makes the analog-to-digital conversion ratiometric. The result of the conversion is always a percentage of the external resistance, regardless of how it changes in relation to the on-resistance of the internal switches. Note that there is an important consideration regarding power dissipation when using the ratiometric mode of operation (see the Power Dissipation section for more details).

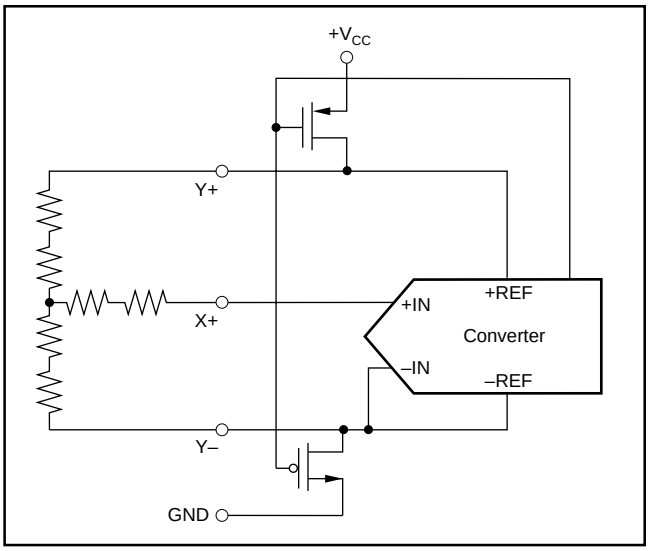


FIGURE 5. Simplified Diagram of Differential Reference (SER/$\overline{DFR}$ Low, Y Switches Enabled, X+ is Analog Input).

As a final note about the differential reference mode, it must be used with $+V_{CC}$ as the source of the +REF voltage and cannot be used with V_{REF}. It is possible to use a high precision reference on V_{REF} and single-ended reference mode for measurements which do not need to be ratiometric. In some cases, it is possible to power the converter directly from a precision reference. Most references can provide enough power for the ADS7846, but might not be able to supply enough current for the external load (such as a resistive touch screen).

TOUCH SCREEN SETTLING

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (for example, noise generated by the LCD panel or backlight circuitry). These capacitors provide a low-pass filter to reduce the noise, but cause a settling time requirement when the panel is touched that typically shows up as a gain error. The problem is that the input and/or reference has not settled to the final steady-state value prior to the ADC sampling the input(s) and providing the digital output. Additionally, the reference voltage may still be changing during the measurement cycle. There are several methods for minimizing or eliminating this issue. Option 1 is to stop or slow down the ADS7846 DCLK for the required touch screen settling time. This allows the input and reference to have stable values for the Acquire period (3 clock cycles of the ADS7846; see Figure 9). This works for both the single-ended and the differential modes. Option 2 is to operate the ADS7846 in the differential mode only for the touch screen measurements and command the ADS7846 to remain on (touch screen drivers on) and not go into power-down (PD0 = 1). Several conversions are made depending on the settling time required and the ADS7846 data rate. Once the required number of conversions have been made, the processor commands the ADS7846 to go into the power-down state on the last measurement. This process is

required for X-position, Y-position, and Z-position measurements. Option 3 is to operate in the 15 Clock-per-Conversion mode which overlaps the analog-to-digital conversions and maintains the touch screen drivers on until commanded to stop by the processor (see Figure 12).

TEMPERATURE MEASUREMENT

In some applications, such as battery recharging, a measurement of ambient temperature is required. The temperature measurement technique used in the ADS7846 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (V_{BE}) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the 25°C value of the V_{BE} voltage and then monitoring the delta of that voltage as the temperature changes. The ADS7846 offers two modes of operation. The first mode requires calibration at a known temperature, but only requires a single reading to predict the ambient temperature. The $\overline{\text{PENIRQ}}$ diode is used (turned on) during this measurement cycle. The voltage across the diode is connected through the MUX for digitizing the forward bias voltage by the ADC with an address of A2 = 0, A1 = 0, and A0 = 0 (see Table I and Figure 6 for details). This voltage is typically 600mV at +25°C with a 20µA current through the diode. The absolute value of this diode voltage can vary a few millivolts. However, the TC of this voltage is very consistent at –2.1mV/°C. During the final test of the end product, the diode voltage would be stored at a known room temperature, in memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of 0.3°C/LSB (in 12-bit mode).

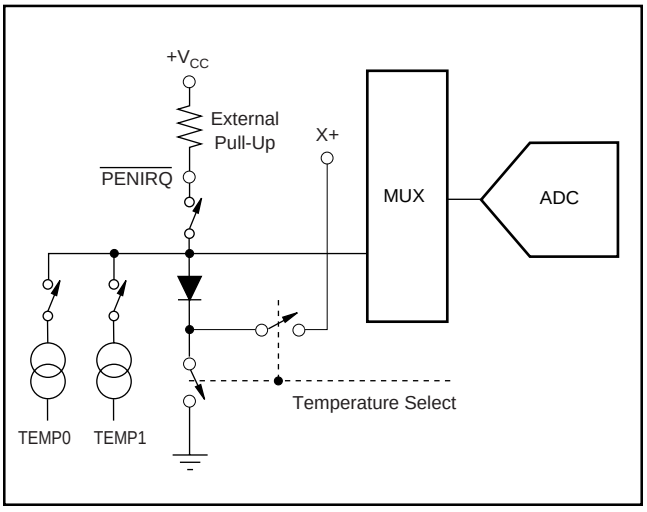


FIGURE 6. Functional Block Diagram of Temperature Measurement Mode.

The second mode does not require a test temperature calibration, but uses a two-measurement method to eliminate the need for absolute temperature calibration and for achieving 2°C accuracy. This mode requires a second conversion with an address of A2 = 1, A1 = 1, and A0 = 1, with a 91 times larger current. The voltage difference between the first and second conversion using 91 times the bias current is represented by kT/q • ln (N), where N is the current ratio = 91, k = Boltzmann's constant ($1.38054 \cdot 10^{-23}$ electron volts/degrees Kelvin), q = the electron charge ($1.602189 \cdot 10^{-19}$ C), and T = the temperature in degrees Kelvin. This method can provide improved absolute temperature measurement over the first mode at the cost of less resolution (1.6°C/LSB). The equation for solving for °K is:

$$°K = q \cdot \Delta V/(k \cdot \ln (N)) \quad (1)$$

where, $\Delta V = V(I_{91}) - V(I_1)$ (in mV)

$$\therefore °K = 2.573°K/mV \cdot \Delta V$$

$$°C = 2.573 \cdot \Delta V(mV) - 273°K$$

NOTE: The bias current for each diode temperature measurement is only on for 3 clock cycles (during the acquisition mode). Therefore, it does not add any noticeable increase in power, especially if the temperature measurement only occurs occasionally.

BATTERY MEASUREMENT

An added feature of the ADS7846 is the ability to monitor the battery voltage on the other side of the voltage regulator (DC/DC converter), as shown in Figure 7. The battery voltage can vary from 0.5V to 6V, while maintaining the voltage to the ADS7846 at 2.7V, 3.3V, etc. The input voltage (V_{BAT}) is divided down by 4 so that a 6.0V battery voltage is represented as 1.5V to the ADC. This simplifies the multiplexer and control logic. In order to minimize the power consumption, the divider is only on during the sampling period when A2 = 0, A1 = 1, and A0 = 0 (see Table I for the relationship between the control bits and configuration of the ADS7846).

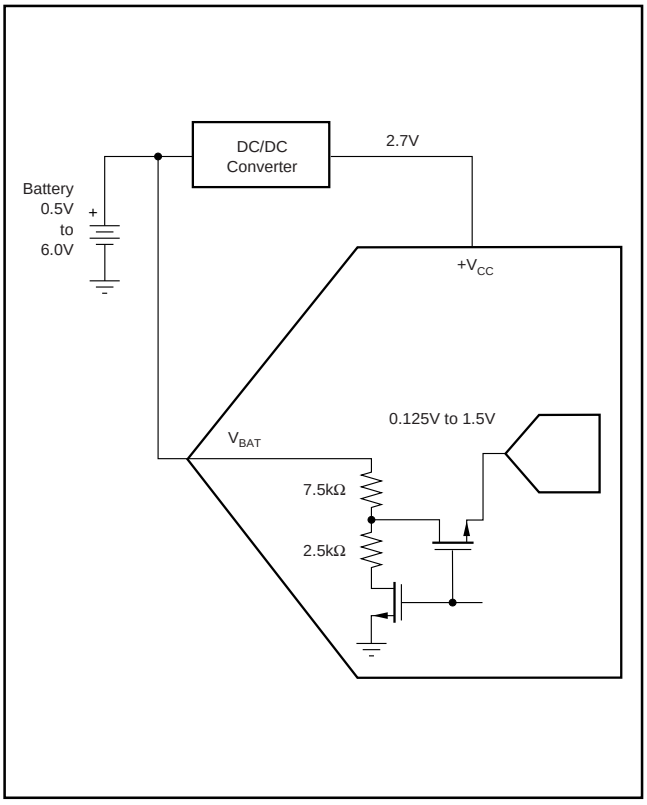


FIGURE 7. Battery Measurement Functional Block Diagram.

PRESSURE MEASUREMENT

Measuring touch pressure can also be done with the ADS7846. To determine pen or finger touch, the pressure of the touch needs to be determined. Generally, it is not necessary to have very high performance for this test; therefore, the 8-bit resolution mode is recommended (however, calculations will be shown here are in 12-bit resolution mode). There are several different ways of performing this measurement. The ADS7846 supports two methods. The first method requires knowing the X-plate resistance, measurement of the X-Position, and two additional cross-panel measurements (Z_1 and Z_2) of the touch screen, as shown in Figure 8. Using Equation 2 calculates the touch resistance:

$$R_{TOUCH} = R_{X-plate} \bullet \frac{X-Position}{4096} \left(\frac{Z_2}{Z_1} - 1 \right) \qquad (2)$$

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-Position and Y-Position, and Z_1. Using Equation 3 also calculates the touch resistance:

$$R_{TOUCH} = \frac{R_{X-plate} \bullet X-Position}{4096} \left(\frac{4096}{Z_1} - 1 \right) - R_{Y-plate} \bullet \left(1 - \frac{Y\ Position}{4096} \right) \qquad (3)$$

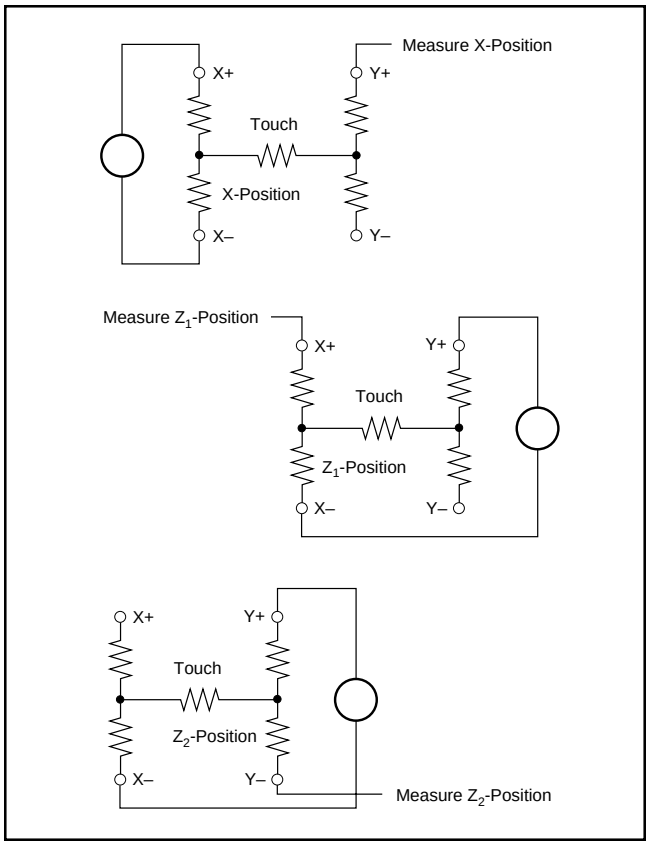
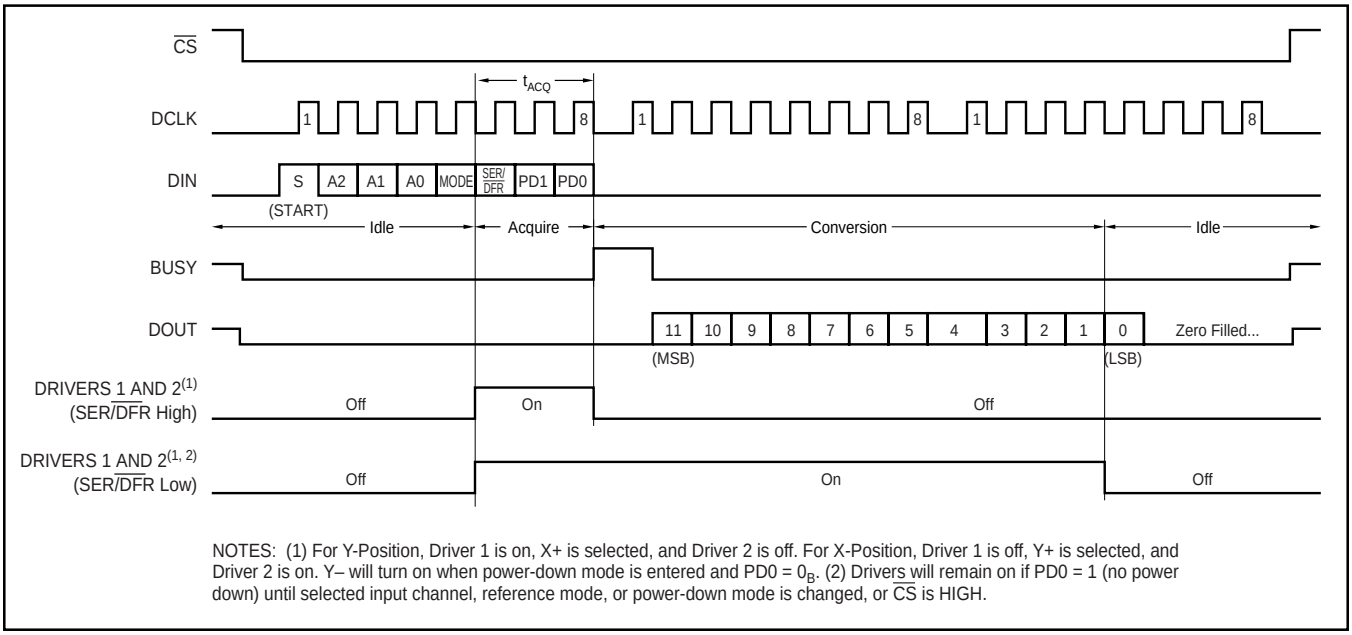


FIGURE 8. Pressure Measurement Block Diagrams.

DIGITAL INTERFACE

Figure 9 shows the typical operation of the ADS7846 digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface. Each communication between the processor and the converter, such as SPI/SSI or Microwire™ synchronous serial interface, consists of eight clock cycles. One complete conversion can be accomplished with three serial communications for a total of 24 clock cycles on the DCLK input.

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer and reference inputs appropriately, the converter enters the acquisition (sample) mode and, if needed, the touch panel drivers are turned on. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input



NOTES: (1) For Y-Position, Driver 1 is on, X+ is selected, and Driver 2 is off. For X-Position, Driver 1 is off, Y+ is selected, and Driver 2 is on. Y– will turn on when power-down mode is entered and PD0 = 0_B. (2) Drivers will remain on if PD0 = 1 (no power down) until selected input channel, reference mode, or power-down mode is changed, or $\overline{CS}$ is HIGH.

FIGURE 9. Conversion Timing, 24 Clocks-per-Conversion, 8-bit Bus Interface. No DCLK delay required with dedicated serial port.

sample-and-hold goes into the hold mode and the touch panel drivers turn off (in single-ended mode). The next 12 clock cycles accomplish the actual analog-to-digital conversion. If the conversion is ratiometric (SER/$\overline{\text{DFR}}$ = 0), the drivers are on during the conversion and a 13th clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be low), which are ignored by the converter.

Control Byte

The control byte (on DIN), as shown in Table III, provides the start conversion, addressing, ADC resolution, configuration, and power-down of the ADS7846. Figure 9 and Tables III and IV give detailed information regarding the order and description of these control bits within the control byte.

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	MODE	SER/$\overline{\text{DFR}}$	PD1	PD0

TABLE III. Order of the Control Bits in the Control Byte.

BIT	NAME	DESCRIPTION
7	S	Start Bit. Control byte starts with first high bit on DIN. A new control byte can start every 15th clock cycle in 12-bit conversion mode or every 11th clock cycle in 8-bit conversion mode (see Figure 12).
6-4	A2-A0	Channel Select Bits. Along with the SER/$\overline{\text{DFR}}$ bit, these bits control the setting of the multiplexer input, touch driver switches, and reference inputs (see Tables I and II).
3	MODE	12-Bit/8-Bit Conversion Select Bit. This bit controls the number of bits for the next conversion: 12-bits (low) or 8-bits (high).
2	SER/$\overline{\text{DFR}}$	Single-Ended/Differential Reference Select Bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input, touch driver switches, and reference inputs (see Tables I and I).
1-0	PD1-PD0	Power-Down Mode Select Bits. See Table V for details.

TABLE IV. Descriptions of the Control Bits within the Control Byte.

Initiate START—The first bit, the S bit, must always be high and initiates the start of the control byte. The ADS7846 ignores inputs on the DIN pin until the start bit is detected.

Addressing—The next three bits (A2, A1, and A0) select the active input channel(s) of the input multiplexer (see Tables I, II, and Figure 2), touch screen drivers, and the reference inputs.

MODE—The mode bit sets the resolution of the ADC. With this bit low, the next conversion has 12 bits of resolution; with this bit high, the next conversion has 8 bits of resolution.

SER/$\overline{\text{DFR}}$—The SER/$\overline{\text{DFR}}$ bit controls the reference mode, either single-ended (high) or differential (low). The differential mode is also referred to as the ratiometric conversion mode and is preferred for X-Position, Y-Position, and Pressure-Touch measurements for optimum performance. The reference is derived from the voltage at the switch drivers, which is almost the same as the voltage to the touch screen. In this case a reference voltage is not needed, as the reference voltage to the ADC is the voltage across the touch screen. In the single-ended mode, the converter reference voltage is always the difference between the V_{REF} and GND pins (see Tables I and II, and Figures 2 through 5 for further information).

If X-Position, Y-Position, and Pressure-Touch are measured in the single-ended mode, an external reference voltage is needed. The ADS7846 should also be powered from the external reference. Caution must be observed when using the single-ended mode such that the input voltage to the ADC does not exceed the internal reference voltage, especially if the supply voltage is greater than 2.7V.

NOTE: The differential mode can only be used for X-Position, Y-Position, and Pressure-Touch measurements. All other measurements require the single-ended mode.

PD0 and PD1—Table V describes the power-down and the internal reference voltage configurations. The internal reference voltage can be turned on or off independently of the ADC. This can allow extra time for the internal reference voltage to settle to the final value prior to making a conversion. Make sure to also allow this extra wake-up time if the internal reference is powered down. The ADC requires no wake-up time and can be instantaneously used. Also note that the status of the internal reference power-down is latched into the part (internally) with BUSY going high. Therefore, in order to turn the reference off, an additional write to the ADS7846 is required after the channel is converted.

PD1	PD0	$\overline{\text{PENIRQ}}$	DESCRIPTION
0	0	Enabled	Power-Down Between Conversions. When each conversion is finished, the converter enters a low-power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid. The Y– switch is on when in power-down.
0	1	Disabled	Reference is off and ADC is on.
1	0	Enabled	Reference is on and ADC is off.
1	1	Disabled	Device is always powered. Reference is on and ADC is on.

TABLE V. Power-Down and Internal Reference Selection.

16 Clocks-per-Conversion

The control bits for conversion n + 1 can be overlapped with conversion n to allow for a conversion every 16 clock cycles, as shown in Figure 10. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer from the processor to the converter. This is possible provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that is captured on the input sample-and-hold may droop enough to affect the conversion result. Note that the ADS7846 is fully powered while other serial communications are taking place during a conversion.

Digital Timing

Figures 9, 11, and Table VI provide detailed timing for the digital interface of the ADS7846.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	1.5			µs
t_{DS}	DIN Valid Prior to DCLK Rising	100			ns
t_{DH}	DIN Hold After DCLK High	10			ns
t_{DO}	DCLK Falling to DOUT Valid			200	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			200	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			200	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	100			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK High	200			ns
t_{CL}	DCLK Low	200			ns
t_{BD}	DCLK Falling to BUSY Rising			200	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			200	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			200	ns

TABLE VI. Timing Specifications ($+V_{CC}$ = +2.7V and Above, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

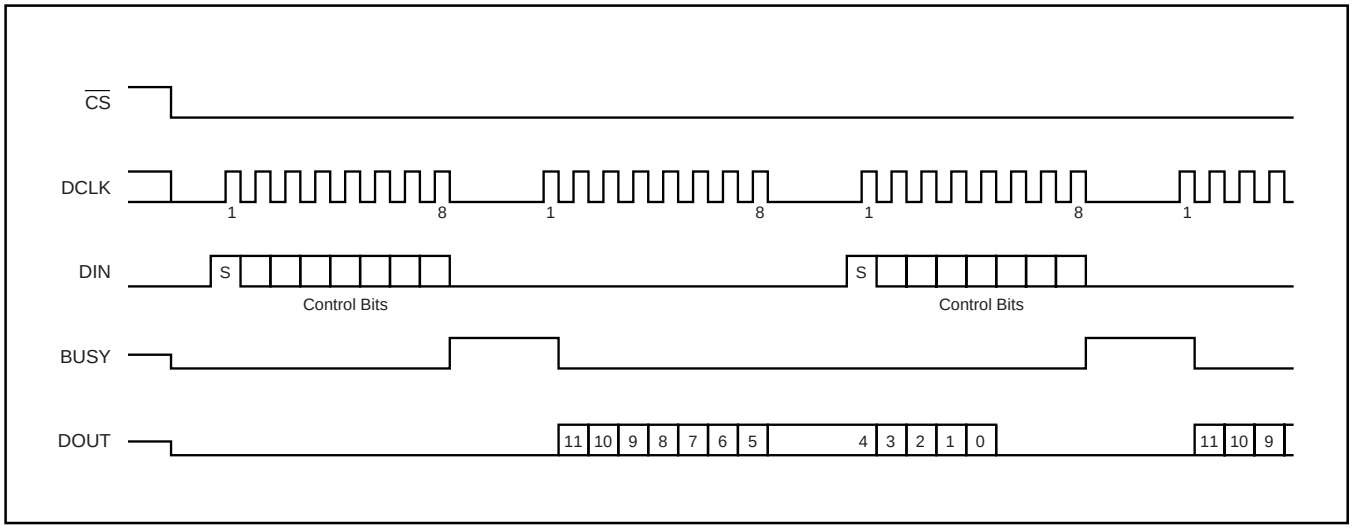


FIGURE 10. Conversion Timing, 16 Clocks-per-Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

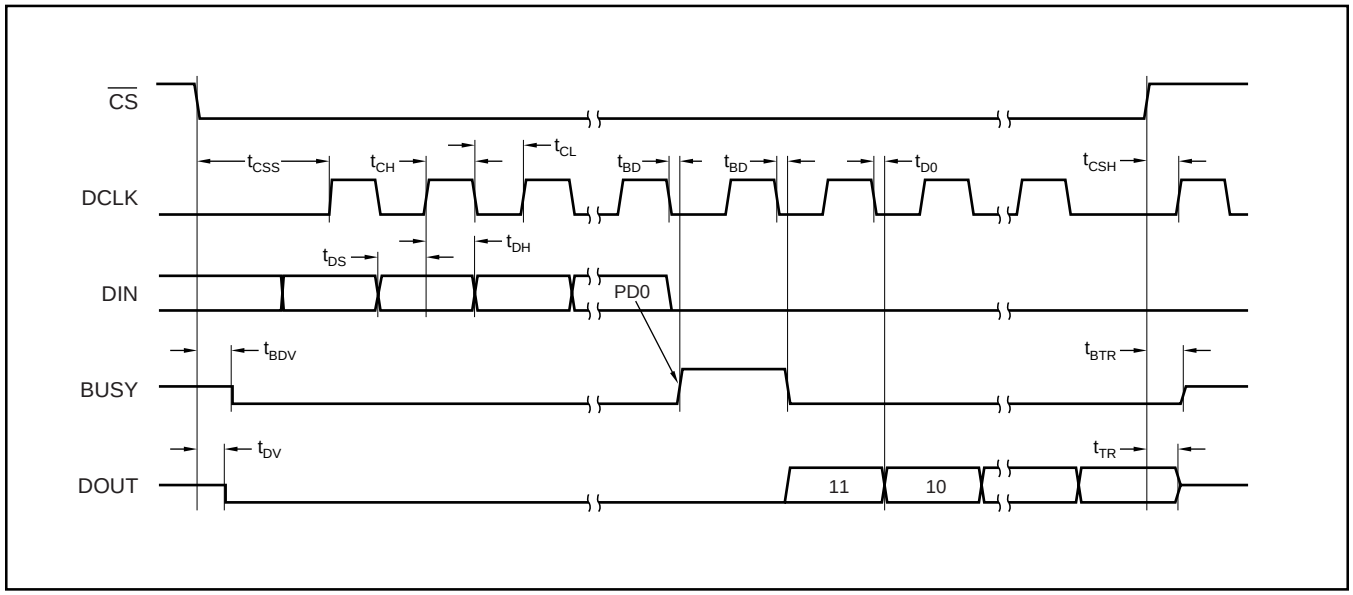


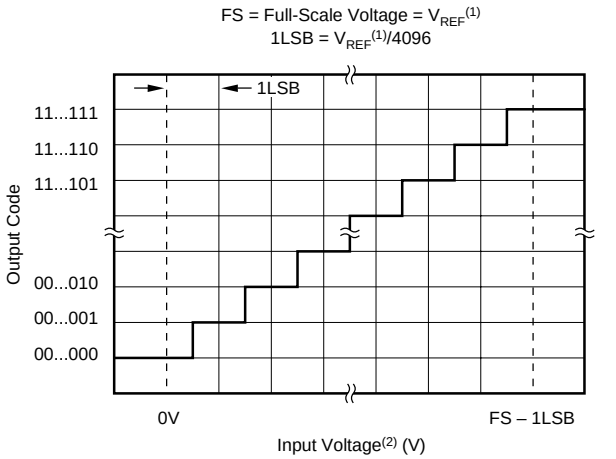
FIGURE 11. Detailed Timing Diagram.

15 Clocks-per-Conversion

Figure 12 provides the fastest way to clock the ADS7846. This method does not work with the serial interface of most microcontrollers and digital signal processors, as they are generally not capable of providing 15 clock cycles per serial transfer. However, this method can be used with field programmable gate arrays (FPGAs) or application specific integrated circuits (ASICs). Note that this effectively increases the maximum conversion rate of the converter beyond the values given in the specification tables, which assume 16 clock cycles per conversion.

Data Format

The ADS7846 output data is in Straight Binary format as shown in Figure 13. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



NOTES: (1) Reference voltage at converter: +REF – (–REF), see Figure 2.
(2) Input voltage at converter, after multiplexer: +IN – (–IN), see Figure 2.

FIGURE 13. Ideal Input Voltages and Output Codes.

8-Bit Conversion

The ADS7846 provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at a faster clock rate. This is because the internal settling time of the ADS7846 is not as critical—settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.

POWER DISSIPATION

There are two major power modes for the ADS7846: full power (PD0 = 1_B) and auto power-down (PD0 = 0_B). When operating at full speed and 16 clocks-per-conversion (see Figure 10), the ADS7846 spends most of the time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Therefore, the difference between full-power mode and auto power-down is negligible. If the conversion rate is decreased by slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion but conversions are done less often, the difference between the two modes is dramatic.

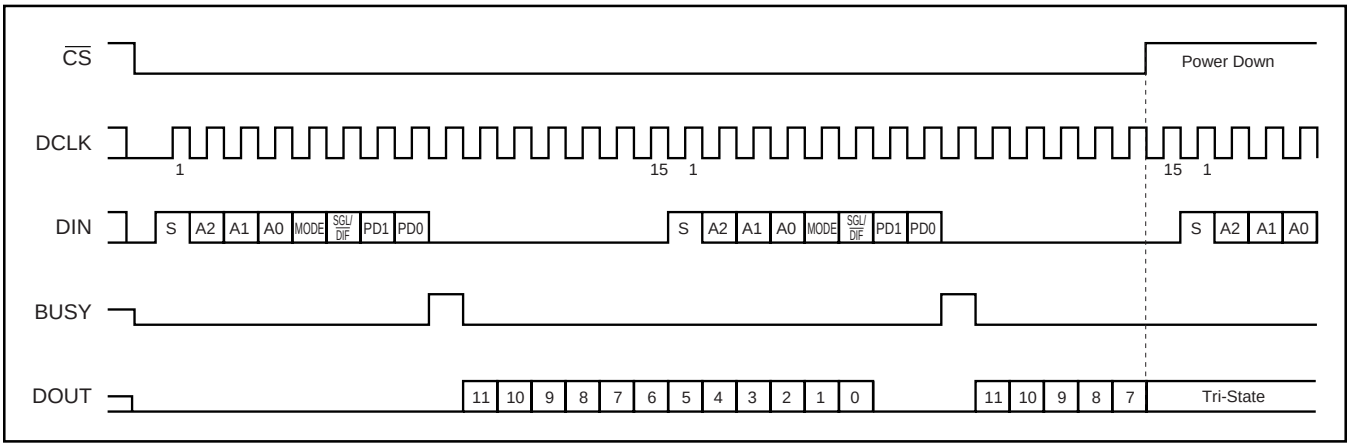


FIGURE 12. Maximum Conversion Rate, 15 Clocks-per-Conversion.

Figure 14 shows the difference between reducing the DCLK frequency (scaling DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversions per second. In the latter case, the converter spends an increasing percentage of time in power-down mode (assuming the auto power-down mode is active).

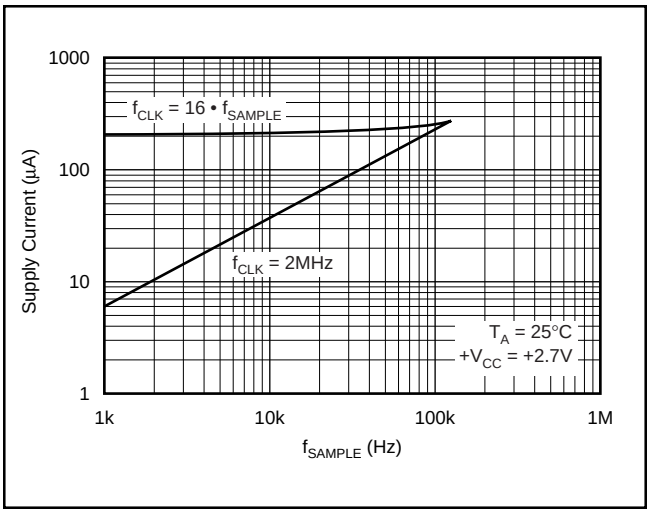


FIGURE 14. Supply Current versus Directly Scaling the Frequency of DCLK with Sample Rate or Maintaining DCLK at the Maximum Possible Frequency.

Another important consideration for power dissipation is the reference mode of the converter. In the single-ended reference mode, the touch panel drivers are on only when the analog input voltage is being acquired (see Figure 9 and Table I). Therefore, the external device (e.g., a resistive touch screen) is only powered during the acquisition period. In the differential reference mode, the external device must be powered throughout the acquisition and conversion periods (see Figure 9). If the conversion rate is high, this could substantially increase power dissipation.

$\overline{CS}$ also puts the ADS7846 into power-down mode. When $\overline{CS}$ goes high, the ADS7846 immediately goes into power-down and does not complete the current conversion. However, the internal reference does not turn off with $\overline{CS}$ going high. To turn the reference off, an additional write is required before $\overline{CS}$ goes high (PD1 = 0).

LAYOUT

The following layout suggestions provide the most optimum performance from the ADS7846. However, many portable applications have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly clean power and grounds because most of the internal components are very low power. This situation means less bypassing for the converter power and less concern regarding grounding. Still, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care must be taken with the physical layout of the ADS7846 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an n-bit SAR converter, there are n 'windows' in which large external transient voltages can easily affect the conversion result. Such glitches can originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS7846 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. A 1µF to 10µF capacitor may also be needed if the impedance of the connection between +V_{CC} and the power supply is high. Low-leakage capacitors should be used to minimize power dissipation through the bypass capacitors when the ADS7846 is in power-down mode.

A bypass capacitor is generally not needed on the V_{REF} pin because the internal reference is buffered by an internal op amp. If an external reference voltage originates from an op amp, make sure that it can drive any bypass capacitor that is used without oscillation.

The ADS7846 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. Whereas high-frequency noise can be filtered out, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin must be connected to a clean ground point. In many cases, this is the analog ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery-connection point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Although resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Longer connections are a source of error, much like the on-resistance of the internal switches. Likewise, loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch screen applications (for example, applications that require a backlit LCD panel). This EMI noise can be coupled through the LCD panel to the touch screen and cause “flickering” of the converted data. Several things can be done to reduce this error, such as using a touch screen with a bottom-side metal layer connected to ground to shunt the majority of noise to ground. Additionally, filtering capacitors, from Y+, Y–, X+, and X– pins to ground can also help. Caution should be observed under these circumstances for settling time of the touch screen, especially operating in the single-ended mode and at high data rates.

$\overline{\text{PENIRQ}}$ OUTPUT

The pen-interrupt output function is shown in Figure 15. While in power-down mode with PD0 = 0, the Y– driver is on and connects the Y-plane of the touch screen to GND. The $\overline{\text{PENIRQ}}$ output is connected to the X+ input through two transmission gates. When the screen is touched, the X+ input is pulled to ground through the touch screen. The $\overline{\text{PENIRQ}}$ output goes low due to the current path through the touch screen to ground, which initiates an interrupt to the processor. During the measurement cycle for X-, Y-, and Z-Position, the X+ input is disconnected from the external pull-up resistor. This is done to eliminate any leakage current from the external pull-up resistor through the touch screen, thus causing no errors.

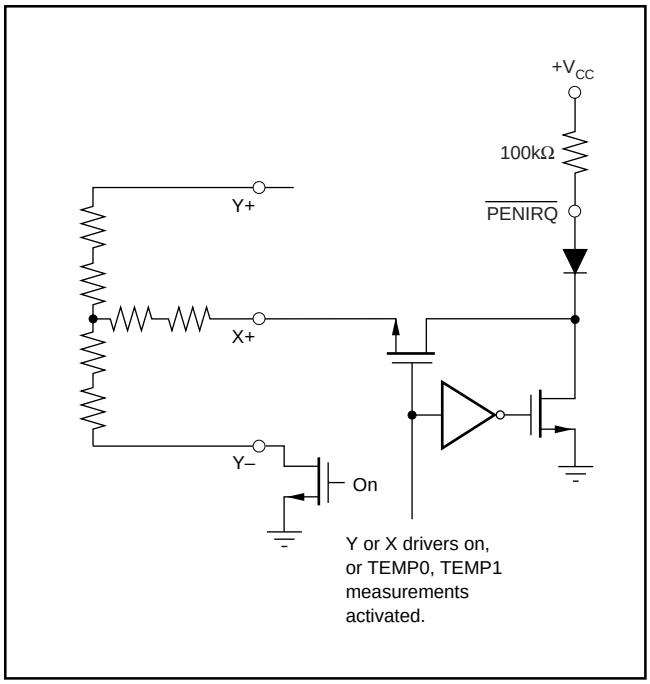


FIGURE 15. ADS7846 $\overline{\text{PENIRQ}}$ Functional Block Diagram.

Furthermore, the $\overline{\text{PENIRQ}}$ output is disabled and low during the measurement cycle for X-, Y-, and Z-Position. The $\overline{\text{PENIRQ}}$ output is disabled and high during the measurement cycle for battery monitor, auxiliary input, and chip temperature. If the last control byte written to the ADS7846 contains PD0 = 1, the pen-interrupt output function is disabled and is not able to detect when the screen is touched. In order to re-enable the pen-interrupt output function under these circumstances, a control byte needs to be written to the ADS7846 with PD0 = 0. If the last control byte written to the ADS7846 contains PD0 = 0, the pen-interrupt output function is enabled at the end of the conversion. The end of the conversion occurs on the falling edge of DCLK after bit 1 of the converted data is clocked out of the ADS7846.

It is recommended that the processor mask the interrupt $\overline{\text{PENIRQ}}$ is associated with whenever the processor sends a control byte to the ADS7846. This prevents false triggering of interrupts when the $\overline{\text{PENIRQ}}$ output is disabled, as in the cases discussed in this section.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7846E	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7846E	Samples
ADS7846E/2K5	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7846E	Samples
ADS7846EG4	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7846E	Samples
ADS7846IRGVT	ACTIVE	VQFN	RGV	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7846	Samples
ADS7846N	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7846N	Samples
ADS7846N/2K5	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7846N	Samples
ADS7846N/2K5G4	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7846N	Samples
ADS7846NG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7846N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

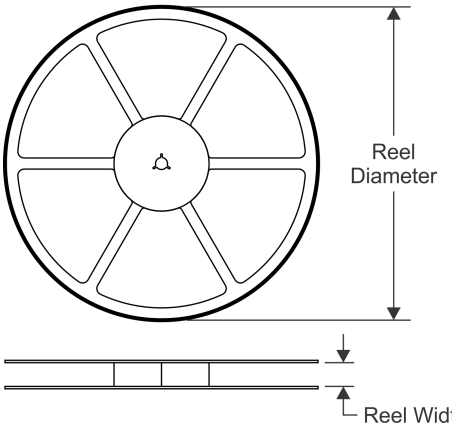
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

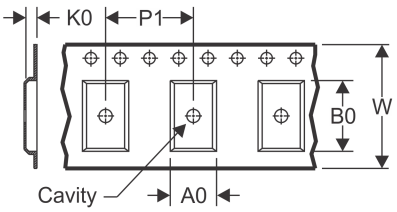
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

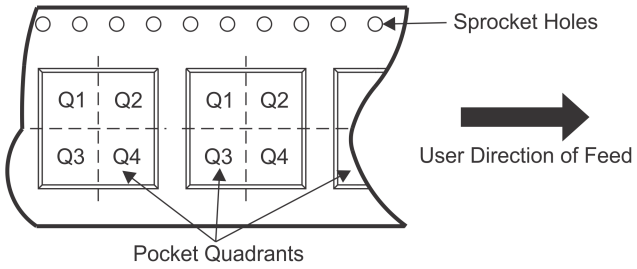


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

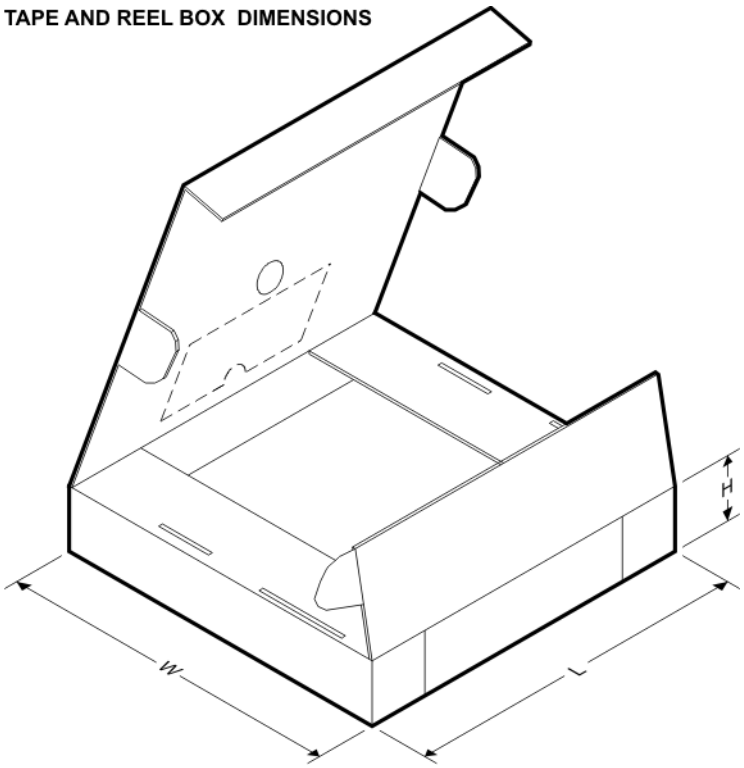
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7846E/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ADS7846IRGVT	VQFN	RGV	16	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
ADS7846N/2K5	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

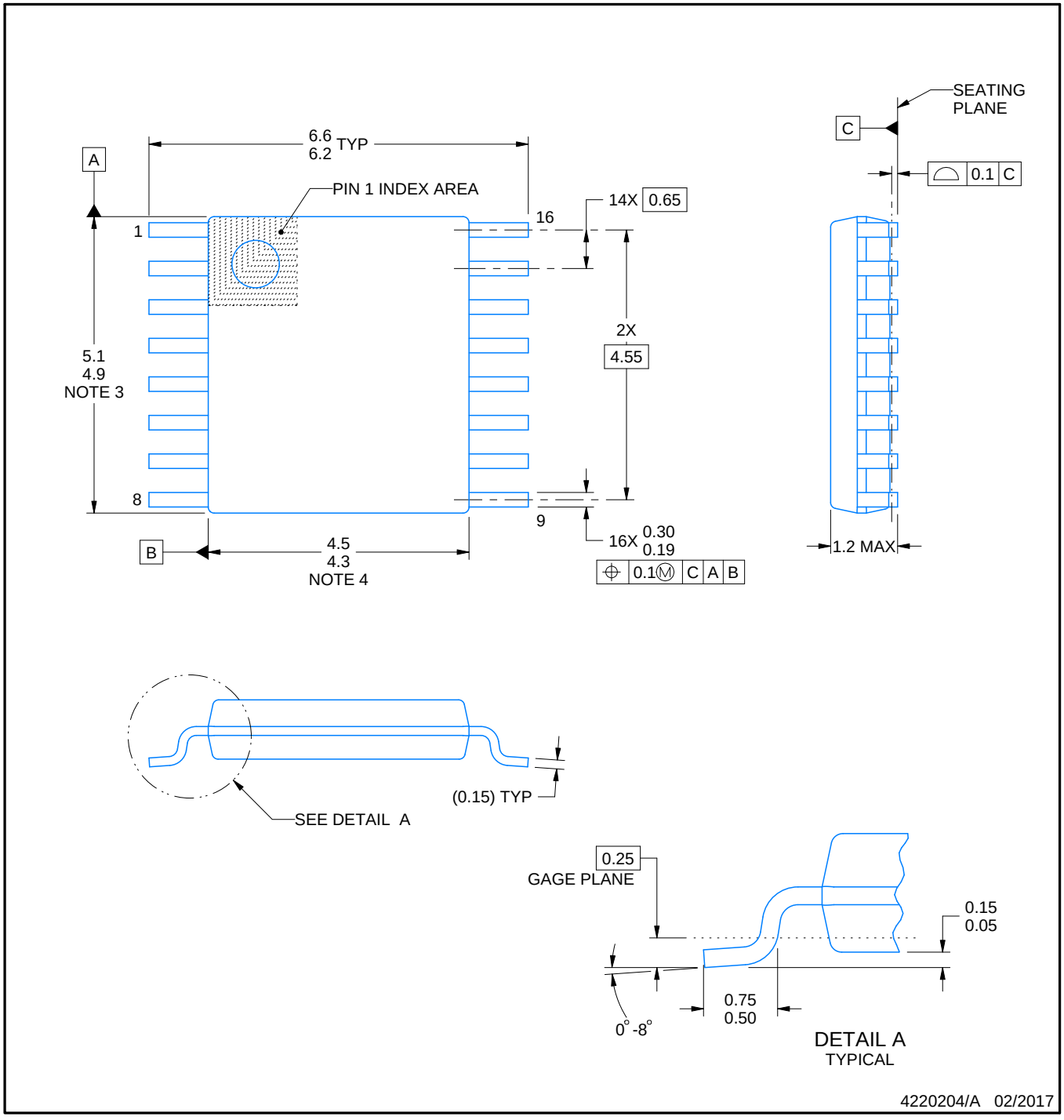
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7846E/2K5	SSOP	DBQ	16	2500	367.0	367.0	35.0
ADS7846IRGVT	VQFN	RGV	16	250	210.0	185.0	35.0
ADS7846N/2K5	TSSOP	PW	16	2500	367.0	367.0	35.0

PACKAGE OUTLINE

PW0016A

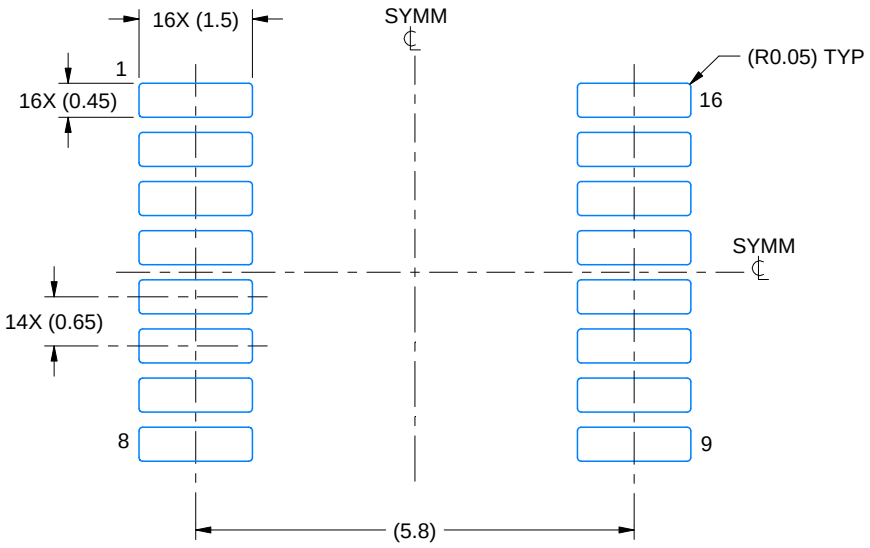
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

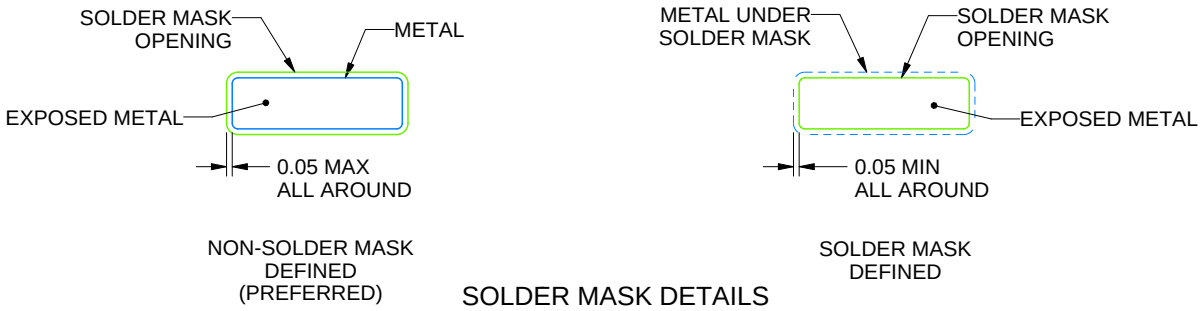


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

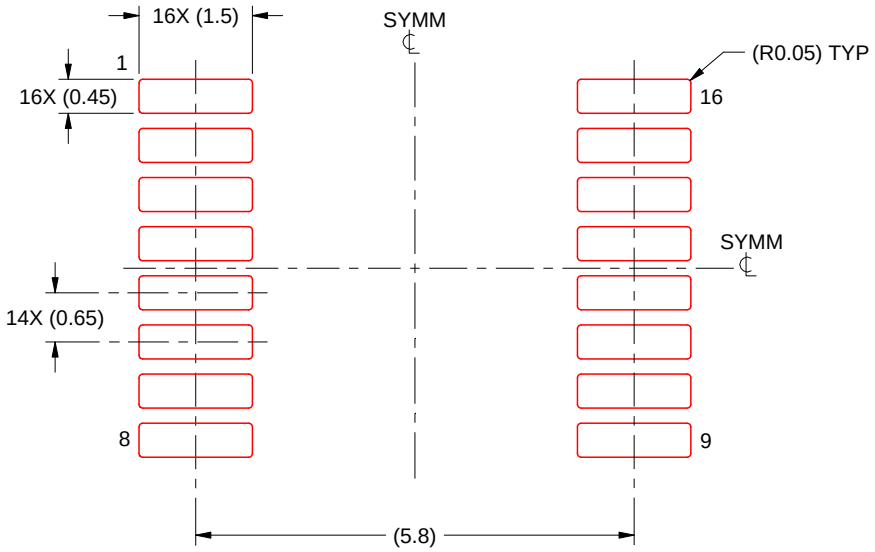


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



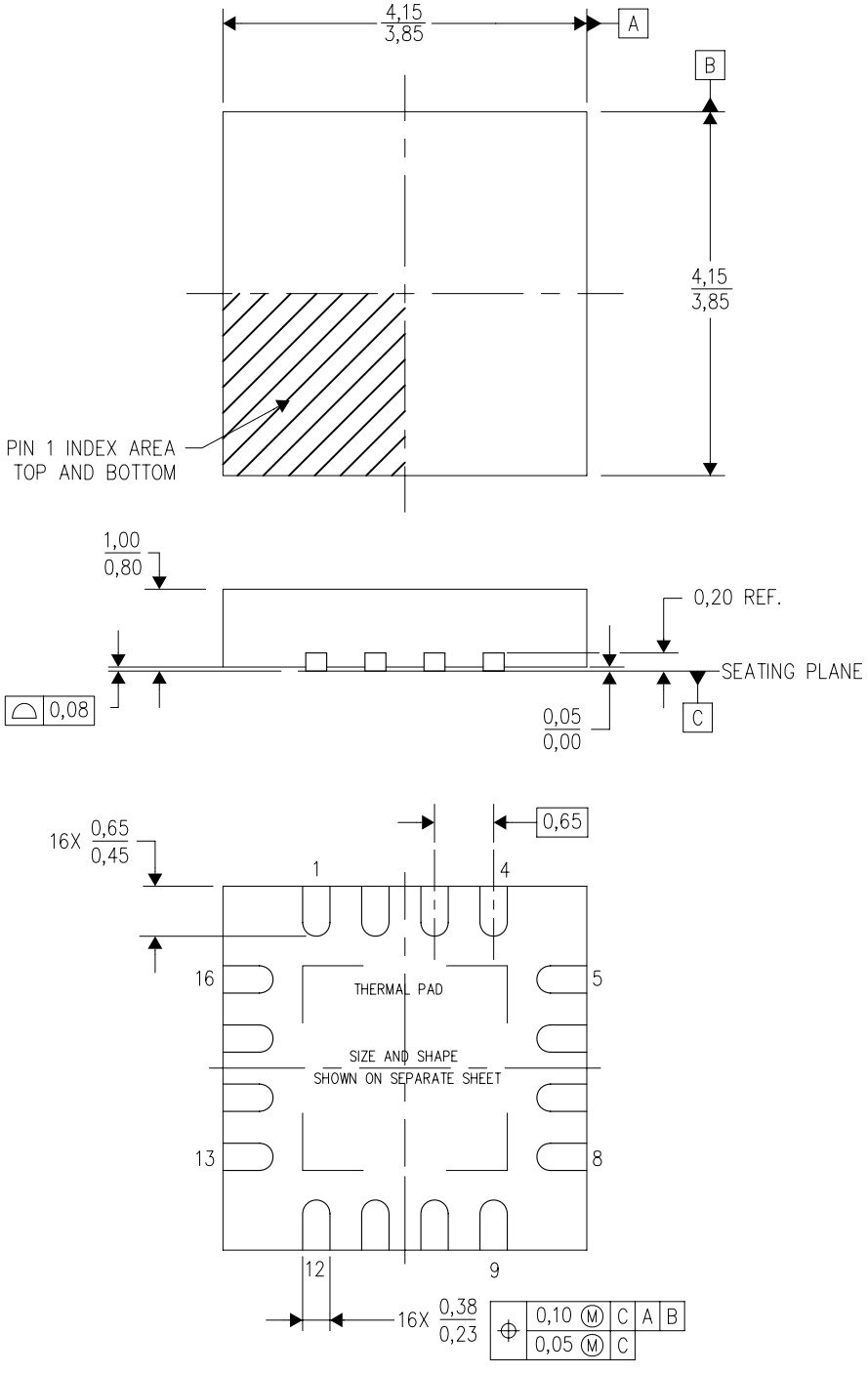
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

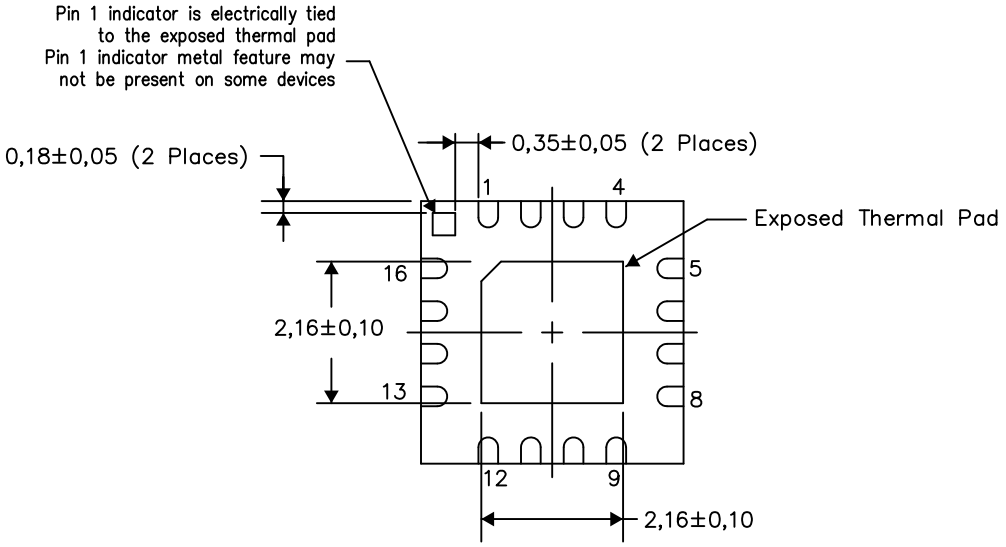
RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



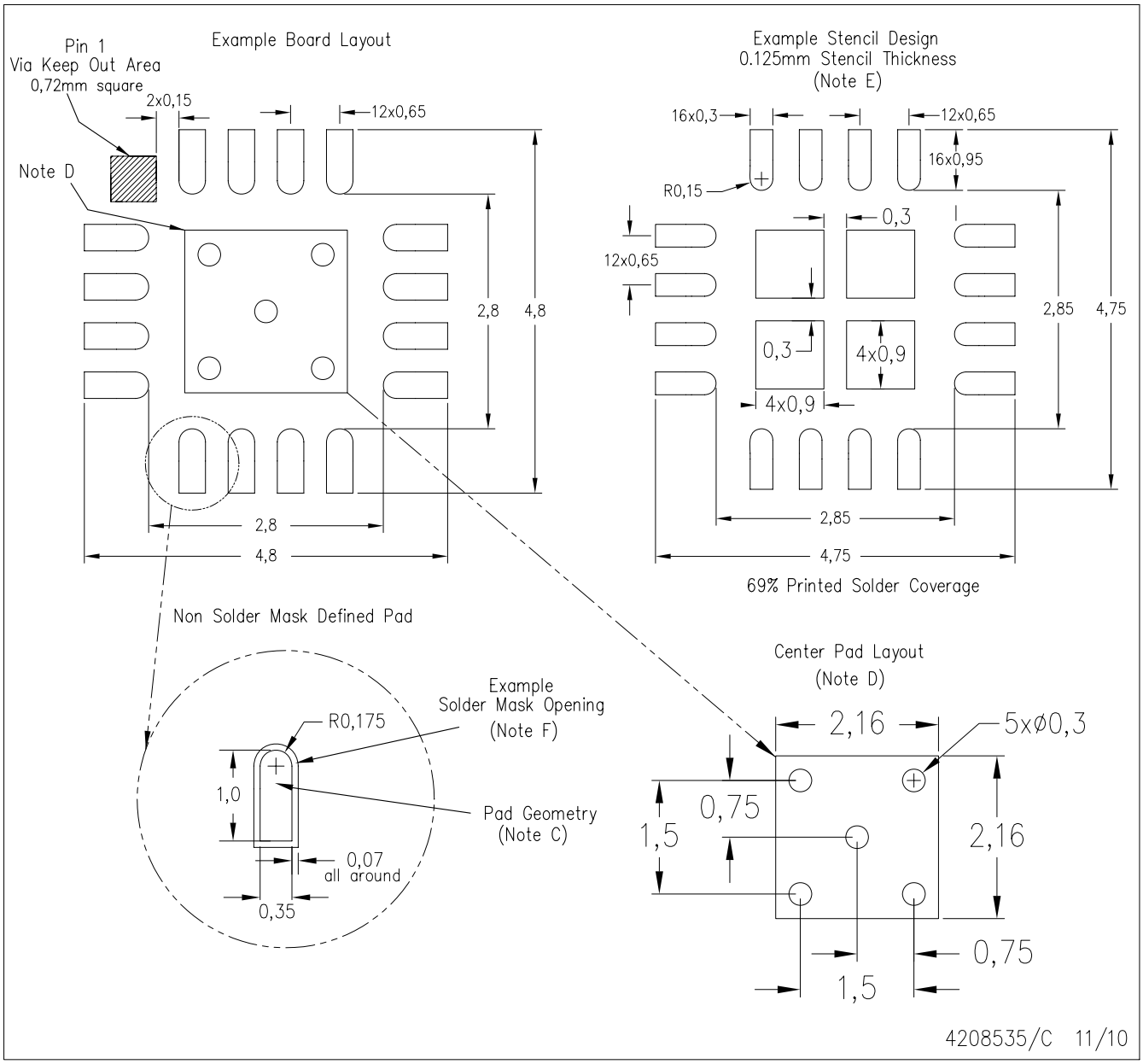
Bottom View

Exposed Thermal Pad Dimensions

4206351–2/L 05/13

NOTE: All linear dimensions are in millimeters

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

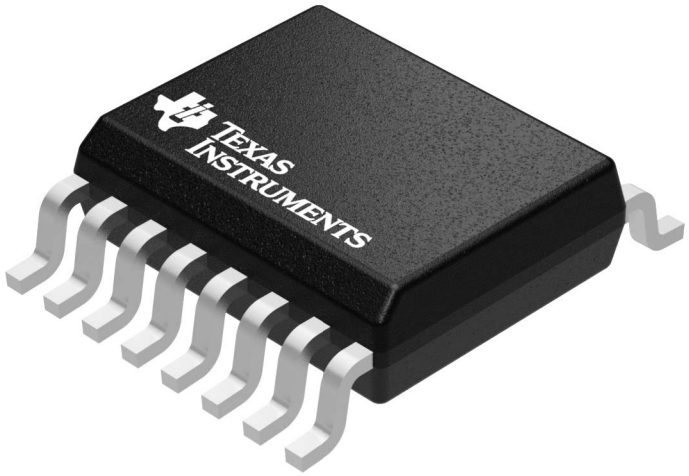


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

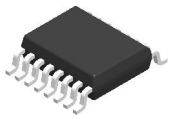
GENERIC PACKAGE VIEW

DBQ 16 SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

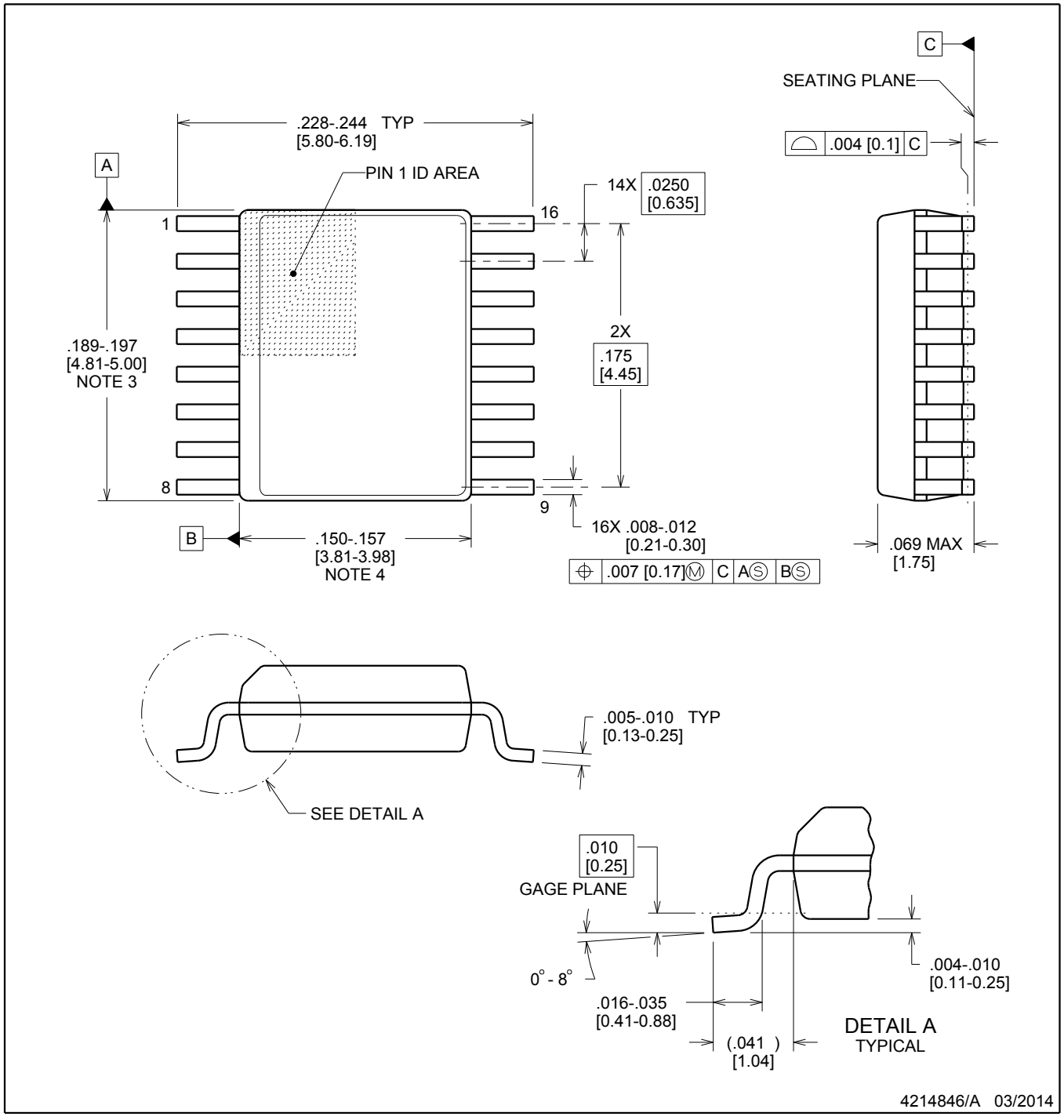


PACKAGE OUTLINE

DBQ0016A

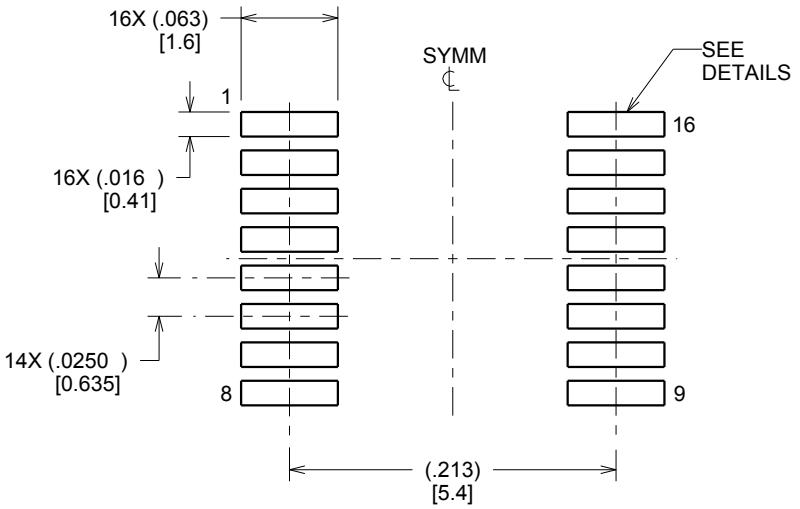
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

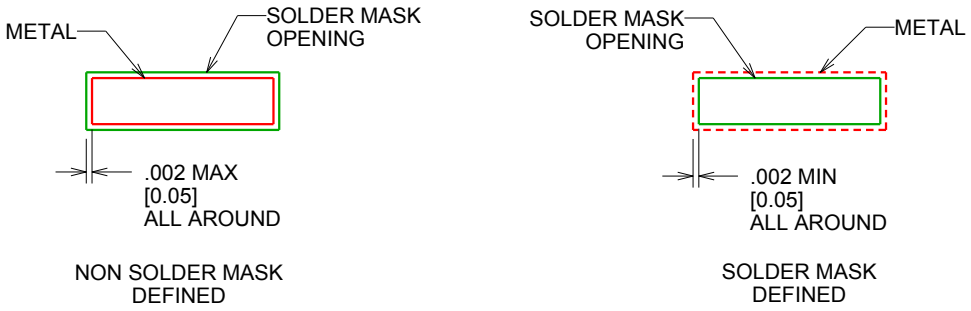


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

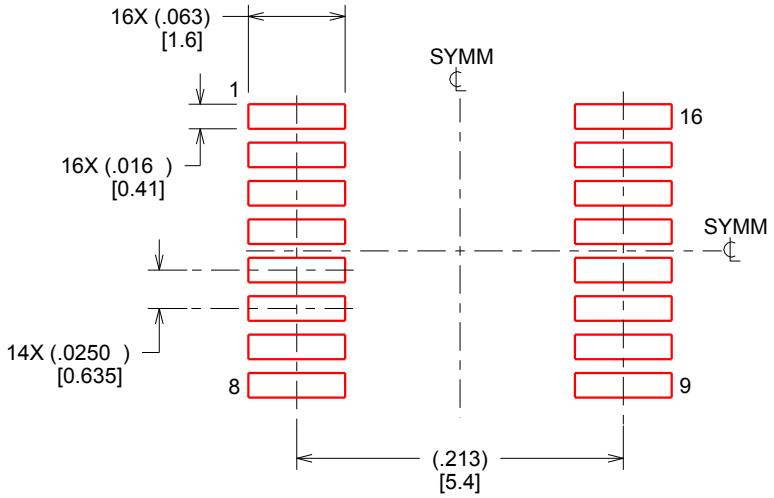
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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