THE DATASHEET OF

LMP8645MKE/NOPB

www.win-source.net 0086-755-83957316

LMP8645, LMP8645HV Precision High Voltage Current Sense Amplifier

1 Features

- Typical Values, T_A = 25°C
- High Common-Mode Voltage Range
  - LMP8645 –2 V to 42 V
  - LMP8645HV –2 V to 76 V
- Supply Voltage Range 2.7 V to 12 V
- Gain Configurable With a Single Resistor
- Maximum Variable Gain Accuracy (With External Resistor) 2%
- Transconductance 200 µA/V
- Low Offset Voltage 1 mV
- Input Bias 12 µA
- PSRR 90 dB
- CMRR 95 dB
- Temperature Range −40°C to 125°C
- 6-Pin SOT Package

2 Applications

- High-Side Current Sense
- Vehicle Current Measurement
- Motor Controls
- Battery Monitoring
- Remote Sensing
- Power Management

3 Description

The LMP8645 and the LMP8645HV devices are precision current sense amplifiers that detect small differential voltages across a sense resistor in the presence of high-input common-mode voltages.

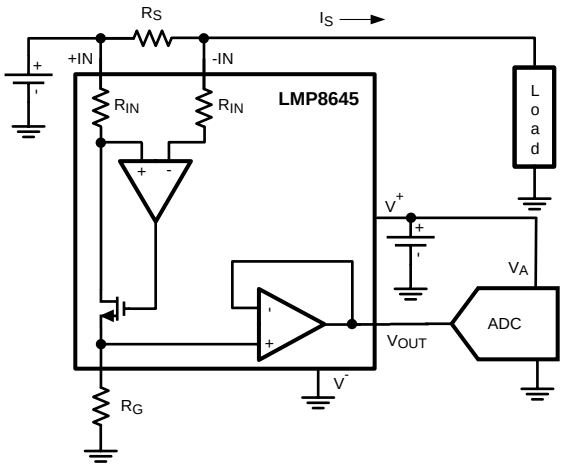
Operating from a supply range of 2.7 V to 12 V, the LMP8645 accepts input signals with a common-mode voltage range of –2 V to 42 V, while the LMP8645HV accepts input signals with a common-mode voltage range of –2 V to 76 V. The LMP8645 and LMP8645HV have adjustable gain for applications where supply current and high common-mode voltage are the determining factors. The gain is configured with a single resistor, providing a high level of flexibility, as well as accuracy as low as 2% (maximum) including the gain setting resistor. The output is buffered to provide low output impedance. This high-side current sense amplifier is ideal for sensing and monitoring currents in DC or battery-powered systems, has excellent AC and DC specifications over temperature, and keeps errors in the current sense loop to a minimum. The LMP8645 is an ideal choice for industrial, automotive, and consumer applications, and is available in SOT-6 package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP8645	SOT (6)	1.60 mm × 2.90 mm
LMP8645HV		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2013) to Revision G **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision E (March 2013) to Revision F **Page**

- Changed layout of National Data Sheet to TI format ... 19

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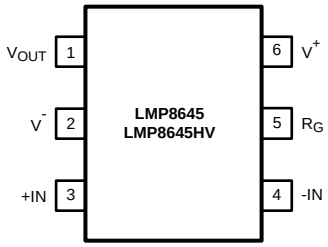
5 Pin Configuration and Functions

DD Package
6-Pin SOT
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{OUT}	1	O	Single-ended output
V^-	2	P	Negative supply voltage
+IN	3	I	Positive input
-IN	4	I	Negative input
R_G	5	I/O	External gain resistor
V^+	6	P	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)(3)

		MIN	MAX	UNIT
Supply Voltage ($V_S = V^+ - V^-$)			13.2	V
Differential voltage +IN- (-IN)			6	V
Voltage at pins +IN, -IN	LMP8645HV	–6	80	V
	LMP8645	–6	60	V
Voltage at R_G pin			13.2	V
Voltage at OUT pin		V^-	V^+	V
Junction temperature (4)			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) For soldering specifications, refer to SNOA549
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/ R_{\theta JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	All pins except 3 and 4	±2000	V
		Pins 3 and 4	±5000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)		±1250	
	Machine Model		±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage ($V_S = V^+ – V^–$)	2.7	12	V
Temperature range (1)	–40	125	°C

(1) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/ R_{\theta JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

6.4 Thermal Information

THERMAL METRIC (1)		LMV8645, LMV8645HV DDC (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	96	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/ R_{\theta JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

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6.5 2.7-V Electrical Characteristics

Unless otherwise specified, all limits specified for at T_A = 25°C, $V_S = V^+ – V^–$, V^+ = 2.7 V, $V^–$ = 0 V, −2 V < V_{CM} < 76 V, R_G = 25 kΩ, R_L = 10 MΩ.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 2.1 V		–1		1	mV
			At the temperature extremes	–1.7		1.7	
TCV_{OS}	Input Offset Voltage Drift(4) (5)	V_{CM} = 2.1 V				7	µV/°C
I_B	Input Bias Current(6)	V_{CM} = 2.1 V			12	20	µA
e_{ni}	Input Voltage Noise(5)	f > 10 kHz, R_G = 5 kΩ			120		nV/√Hz
$V_{SENSE(MAX)}$	Max Input Sense Voltage(5)	V_{CM} = 12 V, R_G = 5 kΩ			600		mV
Gain A_V	Adjustable Gain Setting(7)	V_{CM} = 12 V		1		100	V/V
Gm	Transconductance	V_{CM} = 2.1 V			200		µA/V
	Accuracy	V_{CM} = 2.1 V		–2%		2%	
			At the temperature extremes	–3.4%		3.4%	
	Gm drift(5)	−40°C to 125°C, V_{CM} = 2.1 V				140	ppm /°C
PSRR	Power Supply Rejection Ratio	V_{CM} = 2.1 V, 2.7 V < V^+ < 12 V		90			dB
CMRR	Common-Mode Rejection Ratio	LMP8645HV 2.1 V < V_{CM} < 76 V LMP8645 2.1 V < V_{CM}< 42 V		95			dB
		–2 V <V_{CM} < 2 V		60			
BW	−3-dB Bandwidth(5)	R_G = 10 kΩ, C_G = 4 pF V_{SENSE} = 400 mV, C_L = 30 pF , R_L = 1 MΩ			990		kHz
		R_G = 25 kΩ, C_G = 4 pF, V_{SENSE} = 200 mV, C_L = 30 pF, R_L = 1 MΩ			260		
		Rg = 50 kΩ, C_G = 4 pF, V_{SENSE} = 100 mV, C_L = 30 pF, R_L = 1 MΩ			135		
SR	Slew Rate(8)(5)	V_{CM} = 5 V, C_G = 4 pF, V_{SENSE} from 25 mV to 175 mV, C_L = 30 pF, R_L = 1 MΩ			0.5		V/µs
I_S	Supply Current	V_{CM} = 2.1 V			380	525	uA
			At the temperature extremes			710	
		V_{CM} = –2 V			2000	2500	
			At the temperature extremes			2700	
V_{OUT}	Maximum Output Voltage	V_{CM} = 2.1 V, Rg = 500 kΩ		1.2			V
	Minimum Output Voltage	V_{CM} = 2.1 V				20	mV
I_{OUT}	Output current(5)	Sourcing, V_{OUT} = 600 mV, Rg = 150 kΩ			5		mA
		Sinking, V_{OUT} = 600 mV, Rg = 150 kΩ			5		
C_{LOAD}	Max Output Capacitance Load(5)				30		pF

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are specified by testing, design, or statistical analysis.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) This parameter is specified by design and/or characterization and is not tested in production.
(6) Positive Bias Current corresponds to current flowing into the device.
(7) This parameter is specified by design and/or characterization and is not tested in production.
(8) The number specified is the average of rising and falling slew rates and measured at 90% to 10%.

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6.6 5-V Electrical Characteristics

Unless otherwise specified, all limits specified for at T_A = 25°C, $V_S = V^+ – V^–$, V^+ = 5 V, $V^–$ = 0 V, −2 V < V_{CM} < 76 V, R_g = 25 kΩ, R_L = 10 MΩ. (1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 2.1 V		–1		1	mV
			At the temperature extremes	–1.7		1.7	
TCV_{OS}	Input Offset Voltage Drift (4) (5)	V_{CM} = 2.1 V				7	µV/°C
I_B	Input Bias Current (6)	V_{CM} = 2.1 V			12.5	22	µA
e_{ni}	Input Voltage Noise (5)	f > 10 kHz, R_G = 5 kΩ			120		nV/√Hz
$V_{SENSE(MAX)}$	Max Input Sense Voltage (5)	V_{CM} = 12 V, R_G = 5 kΩ			600		mV
Gain A_V	Adjustable Gain Setting (5)	V_{CM} = 12 V		1		100	V/V
Gm	Transconductance	V_{CM} = 2.1 V			200		µA/V
	Accuracy	V_{CM} = 2.1 V		–2%		2%	
			At the temperature extremes	–3.4%		3.4%	
	Gm drift (5)	−40°C to 125°C, V_{CM} = 2.1 V				140	ppm /°C
PSRR	Power Supply Rejection Ratio	V_{CM} = 2.1 V, 2.7 V < V^+ < 12 V		90			dB
CMRR	Common-Mode Rejection Ratio	LMP8645HV 2.1 V < V_{CM} < 76 V LMP8645 2.1 V < V_{CM} < 42 V		95			dB
		-2 V < V_{CM} < 2 V		60			
BW	−3-dB Bandwidth (5)	R_G= 10 kΩ, C_G = 4 pF, V_{SENSE} = 400 mV, C_L = 30 pF, R_L = 1 MΩ			850		kHz
		R_G= 25 kΩ, C_G = 4 pF, V_{SENSE} = 300 mV, C_L = 30 pF, R_L = 1 MΩ			260		
		R_G= 50 kΩ, C_G = 4 pF, V_{SENSE} = 300 mV, C_L = 30 pF, R_L = 1 MΩ			140		
SR	Slew Rate (7) (5)	V_{CM} = 5 V, C_G = 4 pF, V_{SENSE} from 100 mV to 500 mV, C_L = 30 pF, R_L= 1 MΩ			0.5		V/µs
I_S	Supply Current	V_{CM} = 2.1 V			450	610	uA
			At the temperature extremes			780	
		V_{CM} = −2 V			2100	2800	
			At the temperature extremes			3030	
V_{OUT}	Maximum Output Voltage	V_{CM} = 5 V, Rg = 500 kΩ		3.3			V
	Minimum Output Voltage	V_{CM} = 2.1 V				22	mV
I_{OUT}	Output current (5)	Sourcing, V_{OUT} = 1.65 V, Rg = 150 kΩ			5		mA
		Sinking, V_{OUT} = 1.65 V, Rg = 150 kΩ			5		
C_{LOAD}	Max Output Capacitance Load (5)				30		pF

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are specified by testing, design, or statistical analysis.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) This parameter is specified by design and/or characterization and is not tested in production.
(6) Positive Bias Current corresponds to current flowing into the device.
(7) The number specified is the average of rising and falling slew rates and measured at 90% to 10%.

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6.7 12-V Electrical Characteristics

Unless otherwise specified, all limits specified for at T_A = 25°C, $V_S = V^+ – V^-$, V^+ = 12 V, $V^–$ = 0 V, −2 V < V_{CM} < 76 V, R_g= 25 kΩ, R_L = 10 MΩ.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 2.1 V		–1		1	mV
			At the temperature extremes	–1.7		1.7	
TCV_{OS}	Input Offset Voltage Drift(4)(5)	V_{CM} = 2.1 V				7	µV/°C
I_B	Input Bias Current(6)	V_{CM} = 2.1 V			13	23	µA
e_{ni}	Input Voltage Noise(5)	f > 10 kHz, R_G = 5 kΩ			120		nV/√Hz
$V_{SENSE(MAX)}$	Max Input Sense Voltage(5)	V_{CM} = 12 V, R_G = 5 kΩ			600		mV
Gain A_V	Adjustable Gain Setting(5)	V_{CM} = 12 V		1		100	V/V
Gm	Transconductance	V_{CM} = 2.1 V			200		µA/V
	Accuracy	V_{CM} = 2.1 V		–2%		2%	
			At the temperature extremes	–3.4%		3.4%	
	Gm drift(5)	−40°C to 125°C, V_{CM} = 2.1 V				140	ppm /°C
PSRR	Power Supply Rejection Ratio	V_{CM} = 2.1 V, 2.7 V <V^+ < 12 V		90			dB
CMRR	Common-Mode Rejection Ratio	LMP8645HV 2.1 V < V_{CM} < 76 V LMP8645 2.1 V < V_{CM}< 42 V		95			dB
		–2 V < V_{CM} < 2 V		60			
BW	−3-dB Bandwidth(5)	R_G = 10 kΩ, C_G = 4 pF, V_{SENSE} = 400 mV, C_L = 30 pF, R_L = 1 MΩ			860		kHz
		R_G = 25 kΩ, C_G = 4 pF, V_{SENSE} = 400 mV, C_L = 30 pF, R_L = 1 MΩ			260		
		R_G = 50 kΩ, C_G = 4 pF, V_{SENSE} = 400 mV, C_L = 30 pF, R_L = 1 MΩ			140		
SR	Slew Rate(7) (5)	V_{CM} = 5 V, C_G = 4 pF, V_{SENSE} from 100 mV to 500 mV, C_L = 30 pF, R_L = 1 MΩ			0.6		V/µs
I_S	Supply Current	V_{CM} = 2.1 V			555	765	uA
			At the temperature extremes			920	
		V_{CM} = −2 V			2200	2900	
			At the temperature extremes			3110	
V_{OUT}	Maximum Output Voltage	V_{CM} = 12 V, R_G= 500 kΩ		10.2			V
	Minimum Output Voltage	V_{CM} = 2.1 V				24	mV
I_{OUT}	Output current(5)	Sourcing, V_{OUT} = 5.25 V, Rg = 150 kΩ			5		mA
		Sinking, V_{OUT} = 5.25 V, Rg = 150 kΩ			5		
C_{LOAD}	Max Output Capacitance Load(5)				30		pF

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are specified by testing, design, or statistical analysis.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) This parameter is specified by design and/or characterization and is not tested in production.
(6) Positive Bias Current corresponds to current flowing into the device.
(7) The number specified is the average of rising and falling slew rates and measured at 90% to 10%.

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6.8 Typical Characteristics

Unless otherwise specified: T_A = 25°C, V_S= V^+– V^-, V_{SENSE}= +IN – (–IN), R_L = 10 MΩ.

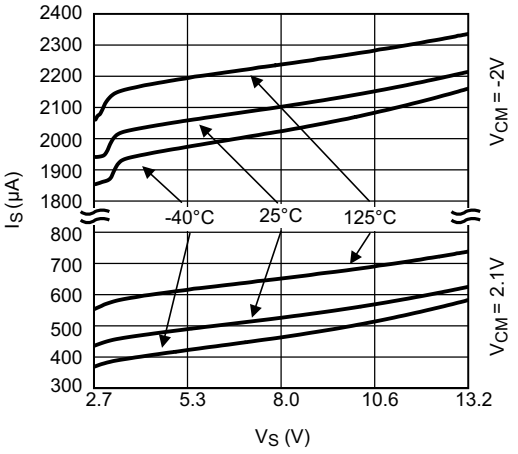

Figure 1. Supply Current vs. Supply Voltage

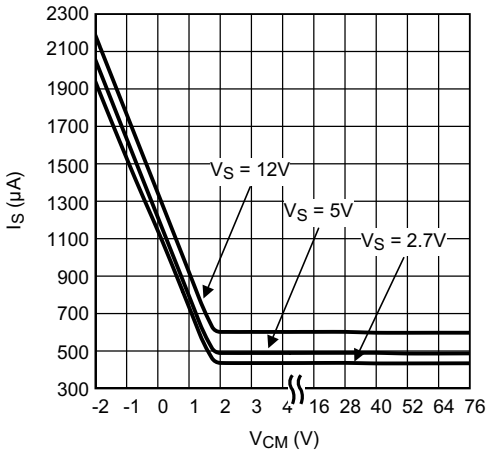

Figure 2. Supply Current vs. V_{CM}

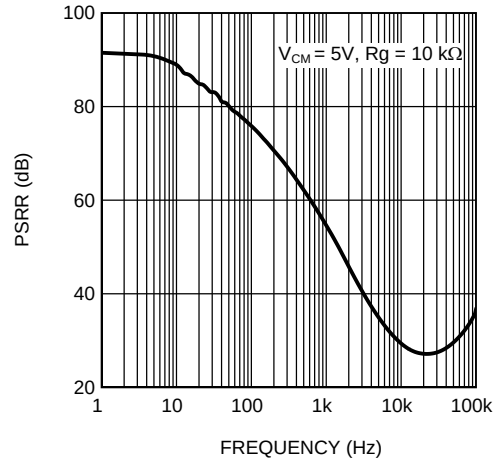

Figure 3. AC PSRR vs. Frequency

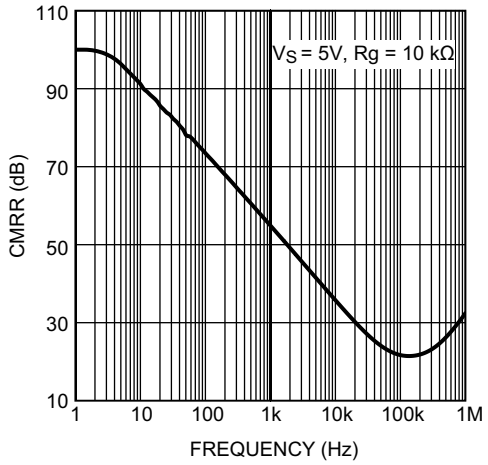

Figure 4. AC CMRR vs. Frequency

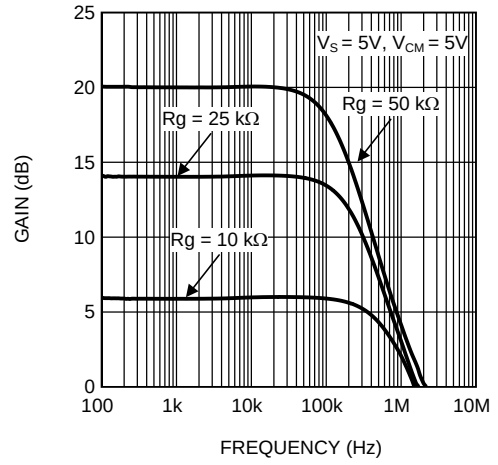

Figure 5. Gain vs. Frequency

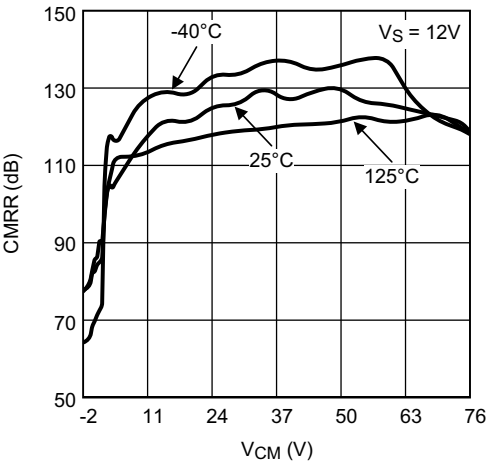

Figure 6. CMRR vs. V_{CM}

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Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_S= V^+– V^-, V_{SENSE}= +IN – (–IN), R_L = 10 MΩ.

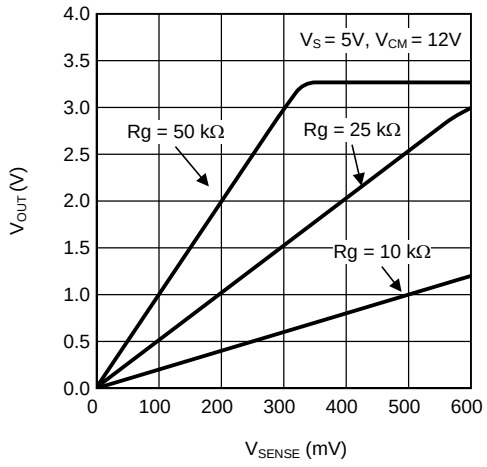

Figure 7. Output Voltage vs. V_{SENSE}

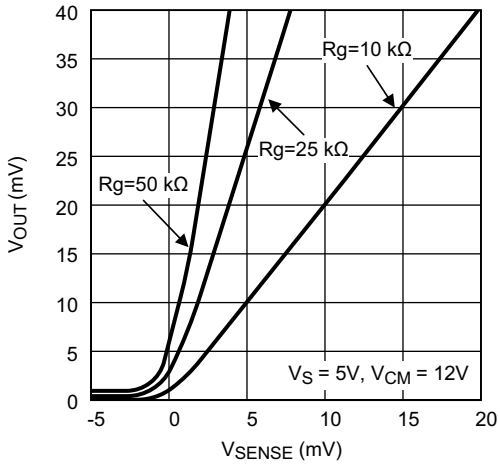

Figure 8. Output Voltage vs. V_{SENSE} (ZOOM Close to 0 V)

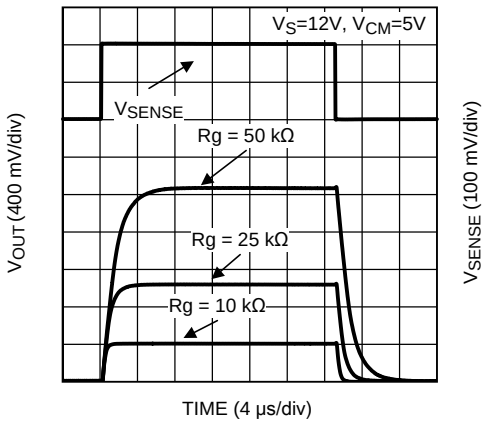

Figure 9. Large Step Response

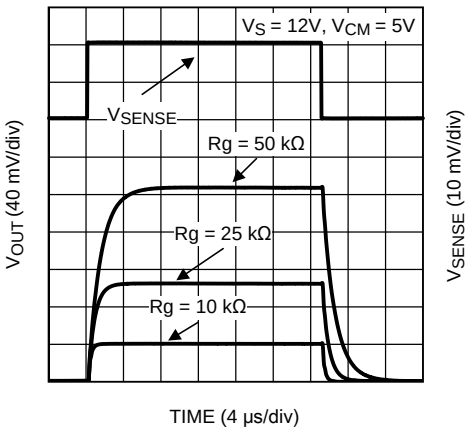

Figure 10. Small Step Response

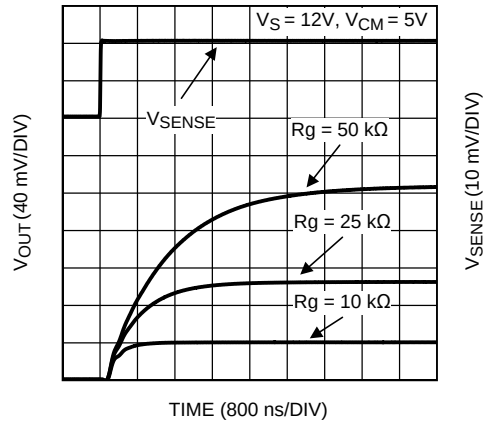

Figure 11. Settling Time (Rise)

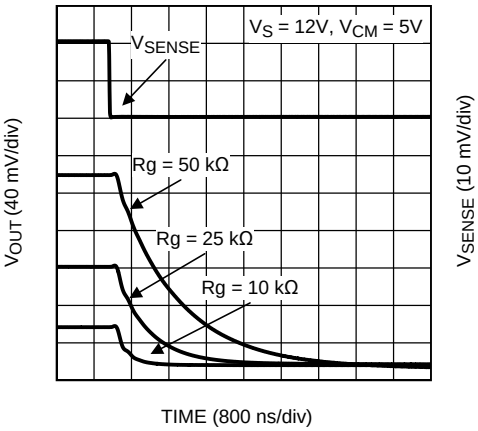

Figure 12. Settling Time (Fall)

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Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_S= V^+– V^-, V_{SENSE}= +IN – (–IN), R_L = 10 MΩ.

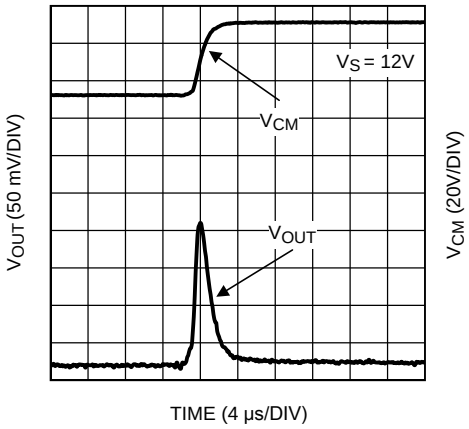

Figure 13. Common-Mode Step Response (Rise)

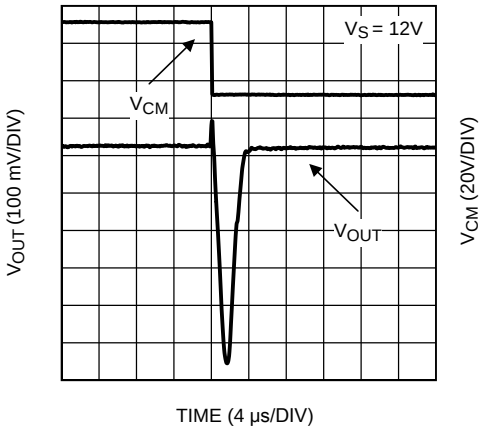

Figure 14. Common-Mode Step Response (Fall)

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7 Detailed Description

7.1 Overview

Operating from a 2.7-V to 12-V supply range, the LMP8645 accepts input signals with a common-mode voltage range of –2 V to 42 V, while the LMP8645HV accepts input signals with a common-mode voltage range of –2 V to 76 V. The LMP8645 and LMP8645HV have adjustable gain, set by a single resistor, for applications where supply current and high common-mode voltage are the determining factors.

7.1.1 Theory of Operation

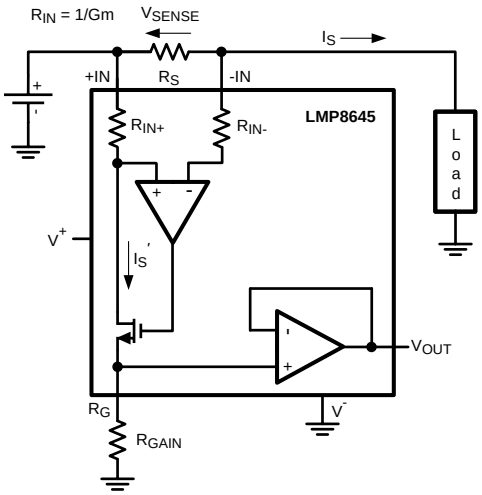

Figure 15. Current Monitor Example Circuit

As seen in Figure 15, the current flowing through the shunt resistor (R_S) develops a voltage drop equal to V_{SENSE} across R_S. The resulting voltage at the –IN pin will now be less than +IN pin proportional to the V_{SENSE} voltage.

The sense amplifier senses this indifference and increases the gate drive to the MOSFET to increase I_S' current flowing through the R_{IN+} string until the amplifer inputs are equal. In this way, the voltage drop across R_{IN+} now matches the votlage drop across V_{SENSE}.

The R_{IN} resistors are trimmed to a nominal value of 5 kΩ each. The current I_S' flows through R_{IN+} , the MOSFET, and R_{GAIN} to ground. The I_S' current generates the voltage V_G across R_{GAIN}. The gain is created bythe ratio of R_{GAIN} and R_{IN}.

A current proportional to I_S is generated according to the following relation:

$$I_S' = V_{SENSE} / R_{IN} = R_S \times I_S / R_{IN}$$

where

- $R_{IN} = 1 / Gm$ (1)

This current flows entirely in the external gain resistor developing a voltage drop equal to:

$$V_G = I_S' \times R_{GAIN} = (V_{SENSE} / R_{IN}) \times R_{GAIN} = ((R_S \times I_S) / R_{IN}) \times R_{GAIN}$$ (2)

This voltage is buffered and presented at the output with a very low output impedance allowing a very easy interface to other devices (ADC, µC…).

$$V_{OUT} = (R_S \times I_S) \times G$$

where

- $G = R_{GAIN} / R_{IN}$ (3)

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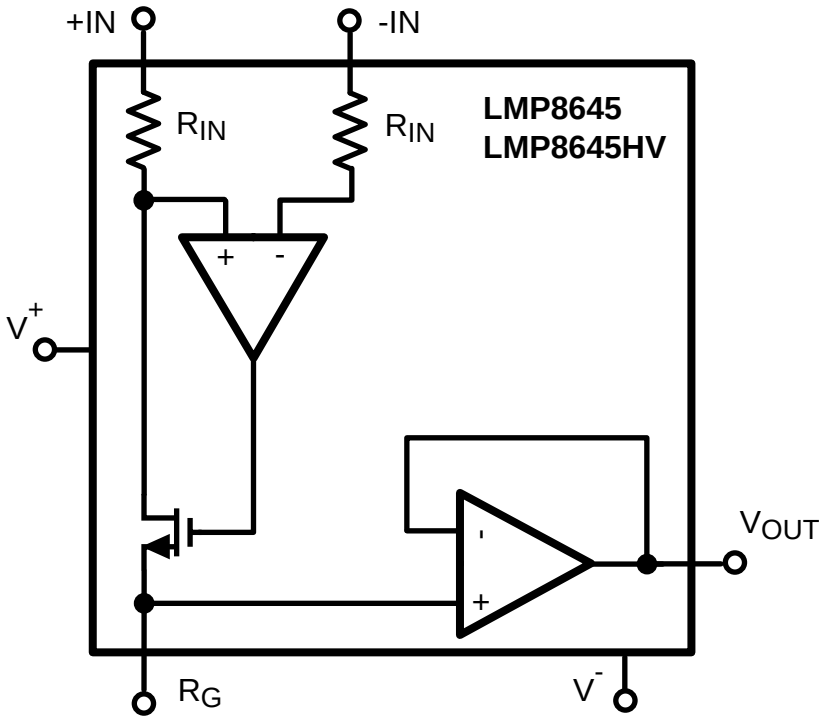
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Driving ADC

The input stage of an Analog-to-Digital converter can be modeled with a resistor and a capacitance versus ground. So if the voltage source does not have a low impedance, an error in the measurement of the amplitude will occur. In this condition a buffer is needed to drive the ADC. The LMP8645 has an internal output buffer able to drive a capacitance load up to 30 pF or the input stage of an ADC. If required an external lowpass RC filter can be added at the output of the LMP8645 to reduce the noise and the bandwidth of the current sense. Any other filter solution that implies a capacitance connected to the R_G pin is not suggested due to the high impedance of that pin.

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Feature Description (continued)

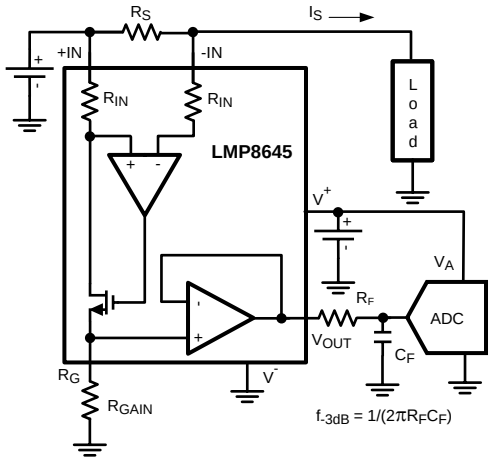

Figure 16. LMP8645 to ADC Interface

7.3.2 Applying Input Voltage With No Supply Voltage

The full specified input common-mode voltage range may be applied to the inputs while the LMP8645 power is off (V+ = 0 V). When the LMP8640 is powered off, the R_{IN} resistors are disconnected internally by MOSFETS and the leakage currents are very low (sub µA).

The 6-V input differential limit still applies, so at no time should the two inputs be more than 6-V apart. There are also Zener clamps on the inputs to ground, so do not exceed the input limits specified in the *Absolute Maximum Ratings*(8)(9)(10).

7.4 Device Functional Modes

7.4.1 Selection of the Gain Resistor

For the LMP8645 and LMP8645HV, the gain is selected through an external gain set resistor connected to the R_G pin. Moreover, the gain resistor R_{GAIN} determines the voltage of the output buffer, which is related to the supply voltage and also to the common-mode voltage of the input signal.

7.4.2 Gain Range Limitations

The gain resistor must be chosen such that the theoretical maximum output voltage does not exceed the LMP8645 maximum output voltage rating for a given common-mode voltage. These limits are due to the internal amplifier bias point and the V_{CM} headroom required to generate the required currents across the R_{IN} and R_{GAIN} resistors.

The following sections explain how to select the gain resistor for various ranges of the input common-mode voltage.

7.4.2.1 Range 1: V_{CM} is –2 V to 1.8 V

The maximum voltage at the RG pin is given by the following inequality:

$$V_{RG} = V_{sense} \times R_{GAIN} \times Gm \leq \min (1.3\ V; Vout_max) \quad (4)$$

where

- Vout_max is the maximum allowable output voltage according to the Electrical Tables

(8) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(9) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(10) For soldering specifications, refer to SNOA549

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Device Functional Modes (continued)

All the gain resistors (R_{GAIN}) values which respect the previous inequality are allowed. The graphical representation of Figure 17 helps in the selection.

All the combinations (V_{SENSE} , R_{GAIN}) below the curve are allowed.

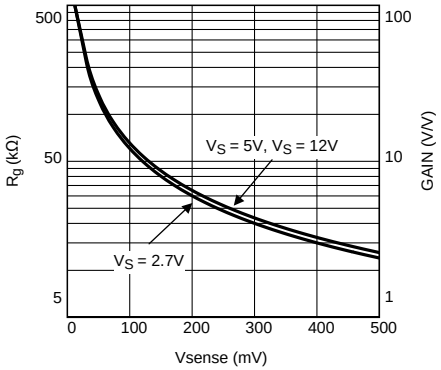

Figure 17. Allowed Gains for Range 1

As a consequence, once selected, the gain (R_{GAIN}) and the V_{SENSE} range is fixed, too.

For example if an application required a Gain of 10, R_G will be 50 kΩ and V_{SENSE} will be in the range 10 mV to 100 mV.

7.4.2.2 Range 2: V_{CM} is 1.8 V to V_S

In this range, the maximum voltage at the R_G pin is related to the common-mode voltage and V_{SENSE}. So all the R_{GAIN} resistor values which respect the following inequalities are allowed:

$$V_{RG} \leq \min (Vout_max; (V_{CM} - V_{sense} - 250\ mV)) \quad (5)$$

where

- $V_{RG} = V_{SENSE} * R_{GAIN} * Gm$
- Vout_max is the maximum allowable output voltage according to the *2.7-V Electrical Characteristics*, *5-V Electrical Characteristics*, and *12-V Electrical Characteristics*.

The graphical representation in Figure 18 helps in the selection.

All the combinations (V_{SENSE}, R_{GAIN}) below the curves for given V_{CM} and supply voltage are allowed.

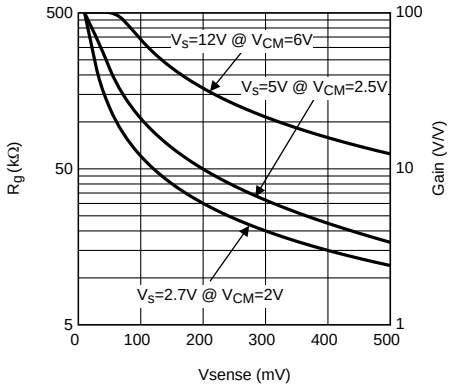

Figure 18. Allowed Gains for Range 2

Also in this range, once selected, the R_{GAIN} (Gain) and the V_{SENSE} range is fixed too.

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Device Functional Modes (continued)

7.4.2.3 Range 3: V_{CM} is greater than V_S

The maximum voltage at the R_G pin is Vout_max, it means that:

$$V_{OUT} = V_{SENSE} \times R_{GAIN} / R_{IN} \leq Vout_max \quad (6)$$

where

- Vout_max is the maximum allowable output voltage according to the Electrical Tables

So all the R_{GAIN} resistors which respect the previous inequality are allowed. The graphical representation in Figure 19 helps with the selection.

All the combinations (V_{SENSE}, R_{GAIN}) below the curves are allowed.

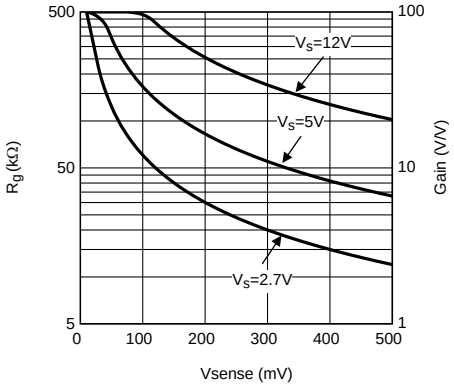

Figure 19. Allowed Gains for Range 3

Also in this range once selected the R_{GAIN} (Gain) the V_{SENSE} range is fixed too.

From the ranges shown above, a good way to maximize the output voltage swing of the LMP8645 is to select the maximum allowable R_{GAIN} according to the previous equations. For a fixed supply voltage and V_{SENSE} as the common-mode voltage increases, the maximum allowable R_{GAIN} increases too.

7.4.3 Selection of Sense Resistor

The accuracy of the current measurement highly depends on the value of the shunt resistor R_S. Its value depends on the application and it is a compromise between small-signal accuracy and maximum permissible voltage (and power) loss in the sense resistor. High values of R_S provide better accuracy at lower currents by minimizing the effects of amplifier offset. Low values of R_S minimize voltage and power loss in the supply section, but at the expense of low current accuracy. For most applications, best performance is obtained with an R_S value that provides a full-scale shunt voltage range of 100 mV to 200 mV.

In applications where a small current is sensed, a larger value of R_S is selected to minimize the error in the proportional output voltage. Higher resistor value improves the signal-to-noise ratio (SNR) at the input of the current sense amplifier and hence gives a more accurate output.

Similarly when high current is sensed, the power losses in R_S can be significant so a smaller value of R_S is desired. In this condition it is also required to take in account also the power rating of R_S resistor. The low input offset and customizable gain of the LMP8645 allows the use of small sense resistors to reduce power dissipation still providing a good input dynamic range. The input dynamic range is the ratio between the maximum signal that can be measured and the minimum signal that can be detected, where usually the input offset and amplifier noise are the principal limiting factors.

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Device Functional Modes (continued)

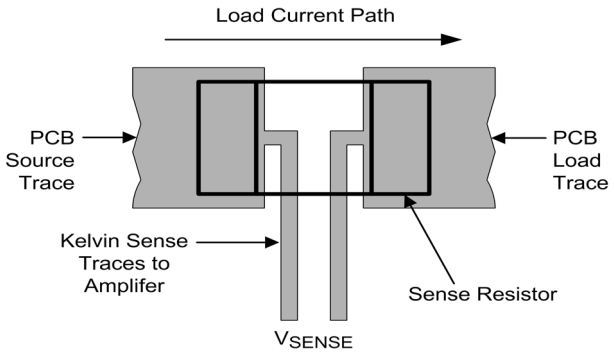

Figure 20. Example of a Kelvin (4-Wire) Connection to a Two-Terminal Resistor

The amplifier inputs should be directly connected to the sense resistor pads using *Kelvin* or *4-wire* connection techniques. The paths of the input traces should be identical, including connectors and vias, so that these errors will be equal and cancel.

7.4.3.1 Resistor Power Rating and Thermal Issues

The power dissipated by the sense resistor can be calculated from:

$$P_D = I_{MAX}^2 * R_S \quad (7)$$

where

- P_D is the power dissipated by the resistor in Watts
- I_{MAX} is the maximum load current in A
- R_S is the sense resistor value in Ω.

The resistor must be rated for more than the expected maximum power (P_D), with margin for temperature derating. Be sure to observe any power derating curves provided by the resistor manufacturer.

Running the resistor at higher temperatures will also affect the accuracy. As the resistor heats up, the resistance generally goes up, which will cause a change in the measurement. The sense resistor should have as much heat-sinking as possible to remove this heat through the use of heatsinks or large copper areas coupled to the resistor pads. A reading drifting slightly after turnon can usually be traced back to sense resistor heating.

7.4.3.2 Using PCB Trace as a Sense Resistor

While it may be tempting to use the resistance of a known area of PCB trace or copper area as a sense resistor, TI does not recommend this for precision measurements.

The tempco of copper is typically 3300 to 4000 ppm/°K (0.33% to 0.4% per °C), which can vary with PCB processes.

A typical surface mount sense resistor temperature coefficient (tempco) is in the 50 ppm to 500 ppm per °C range offering more measurement consistency and accuracy over the copper trace. Special low tempco resistors are available in a range from 0.1 ppm to 50 ppm, but at a much higher cost.

7.4.4 Sense Line Inputs

The sense lines should be connected to a point on the resistor that is not shared with the main current path, as shown in Figure 20. For lowest drift, the amplifier must be mounted away from any heat generating devices, which may include the sense resistor. The traces should be one continuous trace of copper from the sense resistor pad to the amplifier input pin pad, and ideally on the same copper layer with minimal vias or connectors. This can be important around the sense resistor if it is generating any significant heat gradients. Vias in the sense lines should be formed from continuous plated copper and routing through mating connectors or headers should be avoided. It is better to extend the sense lines than to place the amplifier in a hostile environment.

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Device Functional Modes (continued)

To minimize noise pickup and thermal errors, the input traces should be treated like a high-speed differential signal pair and routed tightly together with a direct path to the input pins on the same copper layer. They do not need to be *impedance matched*, but should follow the same matching rules about vias, spacing and equal lengths. The input traces should be run away from noise sources, such as digital lines, switching supplies, or motor drive lines.

Remember that these input traces can contain high voltage (up to 76 V), and should have the appropriate trace routing clearances to other components, traces and layers. Because the sense traces only carry the amplifier bias current, the connecting input traces can be thin traces running close together. This can help with routing or creating the required spacings.

NOTE

Due to the nature of the device topology, the positive input bias current will vary with V_{SENSE} with an extra current approximately equivalent to V_{SENSE} / 5 kΩ on top of the typical 12 uA bias current.

The negative input bias current is not in the feedback path and will not change over V_{SENSE}. High or miss-matched source impedances should be avoided as this imbalance will create an additional error term over input voltage.

7.4.4.1 Effects of Series Resistance on Sense Lines

While the sense amplifier is depicted as a conventional operational amplifier, it really is based on a current-differencing topology. The input stage uses precision 5-kΩ resistors internally to convert the voltage on the input pin onto a current, so any resistance added in series with the input pins will change this resistance, and thus the resulting current, causing an error. TI recommends that the total path resistance be less than 10 Ω and equal to both inputs.

If a resistance is added in series with an input, the gain of that input will not track that of the other input, causing a constant gain error.

TI does not recommend using external resistance to alter the gain, as external resistors do not have the same thermal matching and tracking as the internal thin film resistors. Any added resistance will severely degrade the offset and CMRR specifications.

If resistors are purposely added for filtering, resistance should be added equally to both inputs and be less than 10 Ω, and the user should be aware that the gain will change slightly.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMP8645 device measures the small voltage developed across a current-sensing resistor when current passes through it in the presence of high common-mode voltage. The gain is set by a single resistor and buffered to a single-ended output.

8.2 Typical Applications

8.2.1 Typical Current Monitor Application

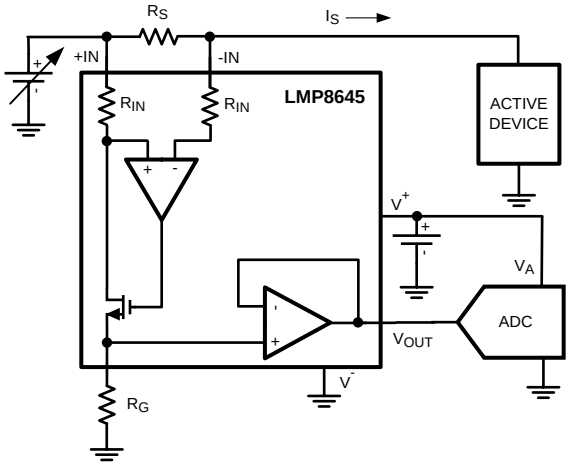

Figure 21. LMP8645 in Current Monitor Application

8.2.1.1 Design Requirements

In this example, the LMP8645 is used to monitor the supply current of an active device (Refer to Figure 21). The LMP8645 supply voltage is 5 V and the active device is supplied with 12 V. The maximum load current is 1 A.

The LMP8645 will operate in all 3 ranges: in *Range 1* when turning on the power of the active device (rising from 0 V to 12 V), while briefly passing through *Range 2* as the load supply rises, and finally into *Range 3* for normal load operation.

Because the purpose of the application is monitor the current of the active device in any operating condition (power on, normal operation, fault, and so forth), the gain resistor will be selected according to *Range 1*, the range that puts the most constraints to the maximum output voltage swing of the LMP8645.

8.2.1.2 Detailed Design Procedure

At the start-up of the monitored device, the LMP8645 works at a common-mode voltage of 0 V, which means that the maximum output limit is 1.3 V (Range 1). To maximize the resolution, the R_{SENSE} value is calculated as maximum allowed V_{SENSE} (Refer to Figure 17) divided by maximum current (1 A), so R_{SENSE}=0.5 Ω.

Due to the output limitation at low common-mode voltage, the maximum allowed gain will be 2.6 V/V, which corresponds to R_{GAIN} = 13 kΩ. With this approach the current is monitored correctly at any working condition, but does not use the full output swing range of the LMP8645.

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Typical Applications (continued)

Alternatively if the monitored device doesn't sink the full 1 A at any supply voltage, it is possible to design with the full maximum output voltage of the LMP8645 when operating in Range 3 ($V_{CM} \geq V_S$).

Also in this case it is possible to maximize the resolution using Rsense = 0.5 Ω, and maximize the output dynamic range with R_{GAIN}=33 kΩ. With this approach the maximum detectable current, when V_{CM} is less than 1.8 V, is about 400 mA. While for common-mode voltages of less than 2.5 V the maximum detectable current is 600 mA (Refer to Figure 17), and for common-mode voltages at or above the LMP8645 supply voltage, the maximum current is 1 A.

The second approach maximizes the output dynamic but implies some knowledge on the monitored current.

8.2.1.3 Application Curves

Figure 22 shows the resulting circuit voltages with the input load swept from 0 A to 1 A, with R_{GAIN}= 13 kΩ for operation in Range 1 (preferring accuracy over all load operating conditions).

Also shown in Figure 23 is the resulting output voltage with R_{GAIN} = 33 kΩ for operation in Range 3 (sacrificing low load supply accuracy while optimizing overall resolution at *normal* load operating conditions).

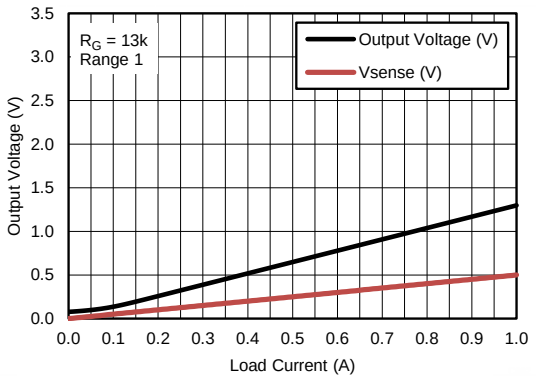

Figure 22. Resulting Input and Output Voltages vs Load Current for Range 1

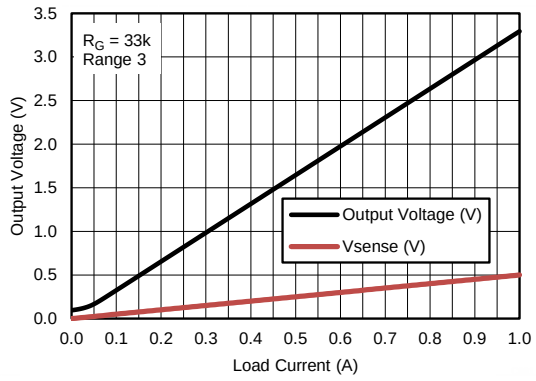

Figure 23. Resulting Input and Output Voltages vs Load Current For Range 3

8.2.2 High Brightness LED Driver

The LMP8645 is the right choice in applications which require high-side current sense, such as High Brightness LED for automotive where the cathode of the LED must be connected to the ground (chassis) of the car. In Figure 24, the LMP8645 is used to monitor the current High Side in a high brightness LED together with a LM3406 constant current buck regulator LED driver.

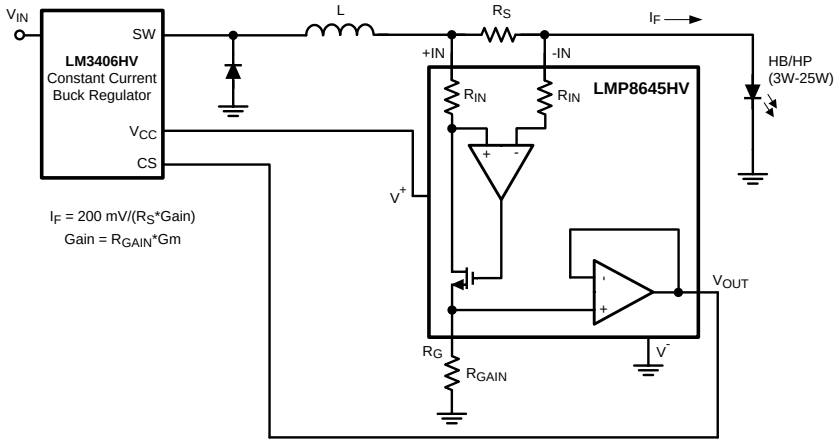

Figure 24. High-Side Current Sensing in Driving HP/HB LED

Typical Applications (continued)

Even though LMP8645 will work in all 3 Ranges, R_{GAIN} will be calculated according to Range 3 because the purpose is regulating the current in the LEDs when the external MOSFET is OFF (LMP8645 at high V_{CM}). Even if this approach makes the LMP8645 able to sense high peak current only in Range 3 where the dynamic output is higher than Range 1 the current resolution is maximized. At each switch ON/OFF of the MOSFET the LMP8645 goes from Range 1 (MOSFET ON, string of LED OFF), to Range 3 (MOSFET OFF, string of LED ON) passing through Range 2 (MOSFET OFF, string of LED OFF). Because the purpose of the application is to sense the current with high precision when the LED string is ON, the R_{GAIN} will be calculated according to the Range 3.

The LMP8645 supply voltage is supplied by the internal LDO of the LM3406 thorough the pin VCC. The LM340x is expecting a 200-mV feedback signal at the current sense (SNS) pin. The LMP8645 must provide this 200 mV at the determined current limit.

The current which flows through the LED is programmed according to Equation 8:

$$I_F = V_{CS} / (R_S \times \text{Gain}) \quad (8)$$

where:

- Gain = $R_{GAIN} \times Gm$
- V_{CS} = 200 mV

In this application the current which flows in the HB LED is in the Range from 350 mA to 1 A, so to reduce the power dissipation on the shunt resistor and have a good accuracy, the R_S must be in the range from 50 mΩ and 200 mΩ. In Table 1, two examples are analyzed.

To summarize, calculate the R_{GAIN} according to the range of operation in which the application mainly works. Once selected, the range considers the more stringent constraint

Table 1. Comparison of Two Ranges

	I_F=350 mA	**I_F=1 A**
R_{GAIN}	40 kΩ	36 kΩ
R_S	77 mΩ	27 mΩ
Dissipated Power	9.5 mW	27 mW
Total Accuracy	≅5%	≅5%

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9 Power Supply Recommendations

To decouple the LMP8645 from AC noise on the power supply, TI recommends using a 0.1-µF bypass capacitor between the V_S and GND pins. This capacitor must be placed as close as possible to the supply pins. In some cases, an additional 10-µF bypass capacitor may further reduce the supply noise.

10 Layout

10.1 Layout Guidelines

The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors (< 100 mΩ), any trace resistance shared with the load current can cause significant errors.

The amplifier inputs should be directly connected to the sense resistor pads using *Kelvin* or *4-wire* connection techniques. The traces should be one continuous piece of copper from the sense resistor pad to the amplifier input pin pad, and ideally on the same copper layer with minimal vias or connectors. This can be important around the sense resistor if it is generating any significant heat gradients.

To minimize noise pick-up and thermal errors, the input traces should be treated like a differential signal pair and routed tightly together with a direct path to the input pins (preferably on the same copper layer). The input traces should be run away from noise sources, such as digital lines, switching supplies or motor drive lines.

Ensure that the sense traces have the appropriate trace routing clearances for the expected load supply voltages.

Because the sense traces only carry the amplifier bias current, the connecting input traces can be thinner, signal level traces. Excessive Resistance in the trace should also be avoided.

The paths of the traces should be identical, including connectors and vias, so that any errors will be equal and cancel.

The sense resistor will heat up as the load increases. As the resistor heats up, the resistance generally goes up, which will cause a change in the readings. The sense resistor should have as much heatsinking as possible to remove this heat through the use of heatsinks or large copper areas coupled to the resistor pads.

The gain set resistor pin is a sensitive node and can pick up noise. Keep the gain set resistor close to the RG pin and minimize R_{GAIN} trace length. Connect the grounded end of R_{GAIN} directly to the LMP8645 ground pin.

10.2 Layout Example

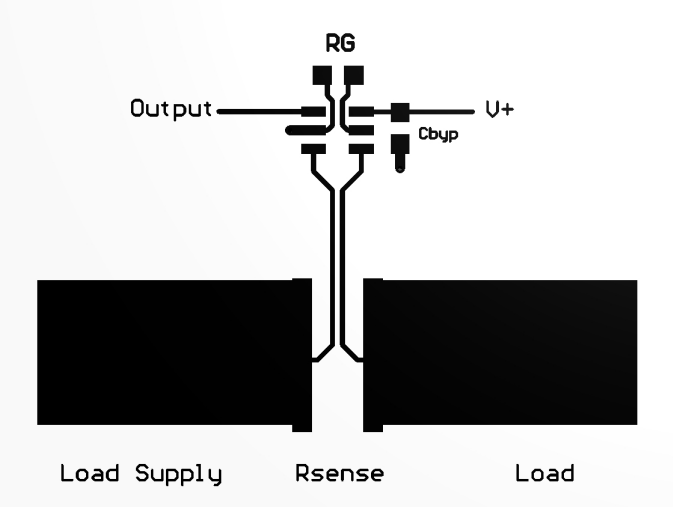

Figure 25. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LMP8645 TINA SPICE Model, SNOM087

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

Evaluation Board for the LMP8645, http://www.ti.com/tool/lmp8645mkeval

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

AN-1975 LMP8640 / LMP8645 Evaluation Board User Guide, SNOA546

11.3 Related Links

The following table lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMP8645	Click here	Click here	Click here	Click here	Click here
LMP8645HV	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

For support, visit the Current Sense Amplifier E2E support forum at https://e2e.ti.com/support/amplifiers/current-shunt-monitors/

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP8645HVMK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AK6A	Samples
LMP8645HVMKE/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AK6A	Samples
LMP8645HVMKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AK6A	Samples
LMP8645MK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AJ6A	Samples
LMP8645MKE/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AJ6A	Samples
LMP8645MKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AJ6A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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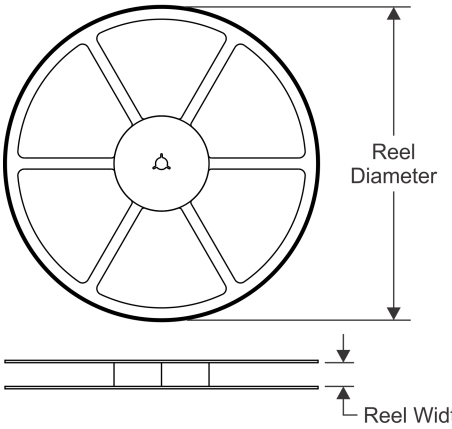
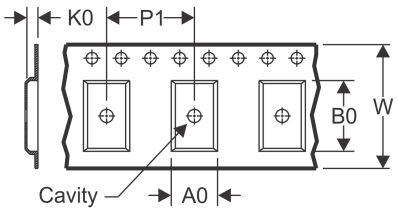
TAPE AND REEL INFORMATION

REEL DIMENSIONS

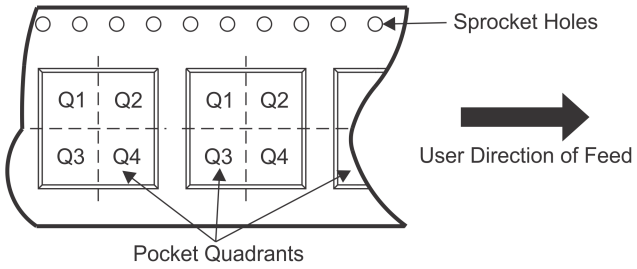


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

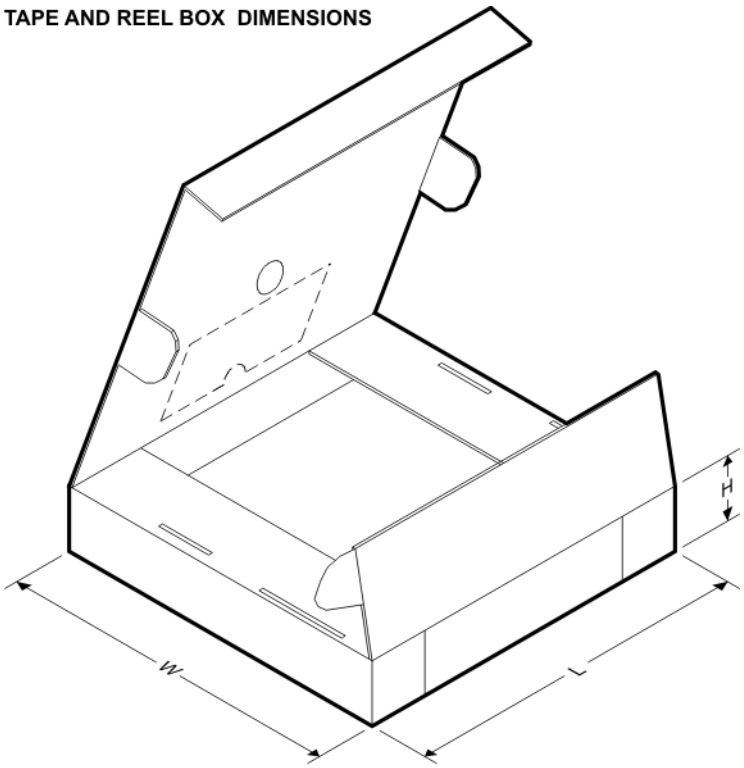
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8645HVMK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8645HVMKE/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8645HVMKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8645MK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8645MKE/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8645MKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

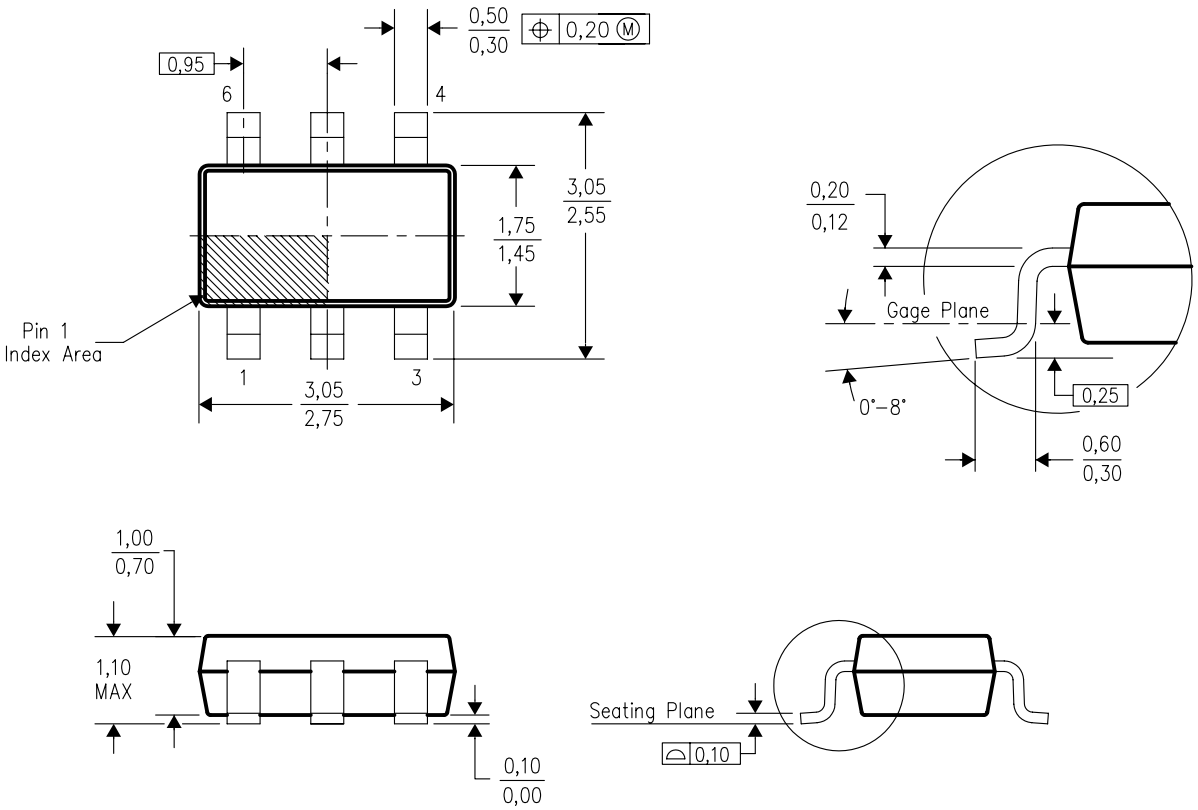
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8645HVMK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LMP8645HVMKE/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMP8645HVMKX/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMP8645MK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LMP8645MKE/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMP8645MKX/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0

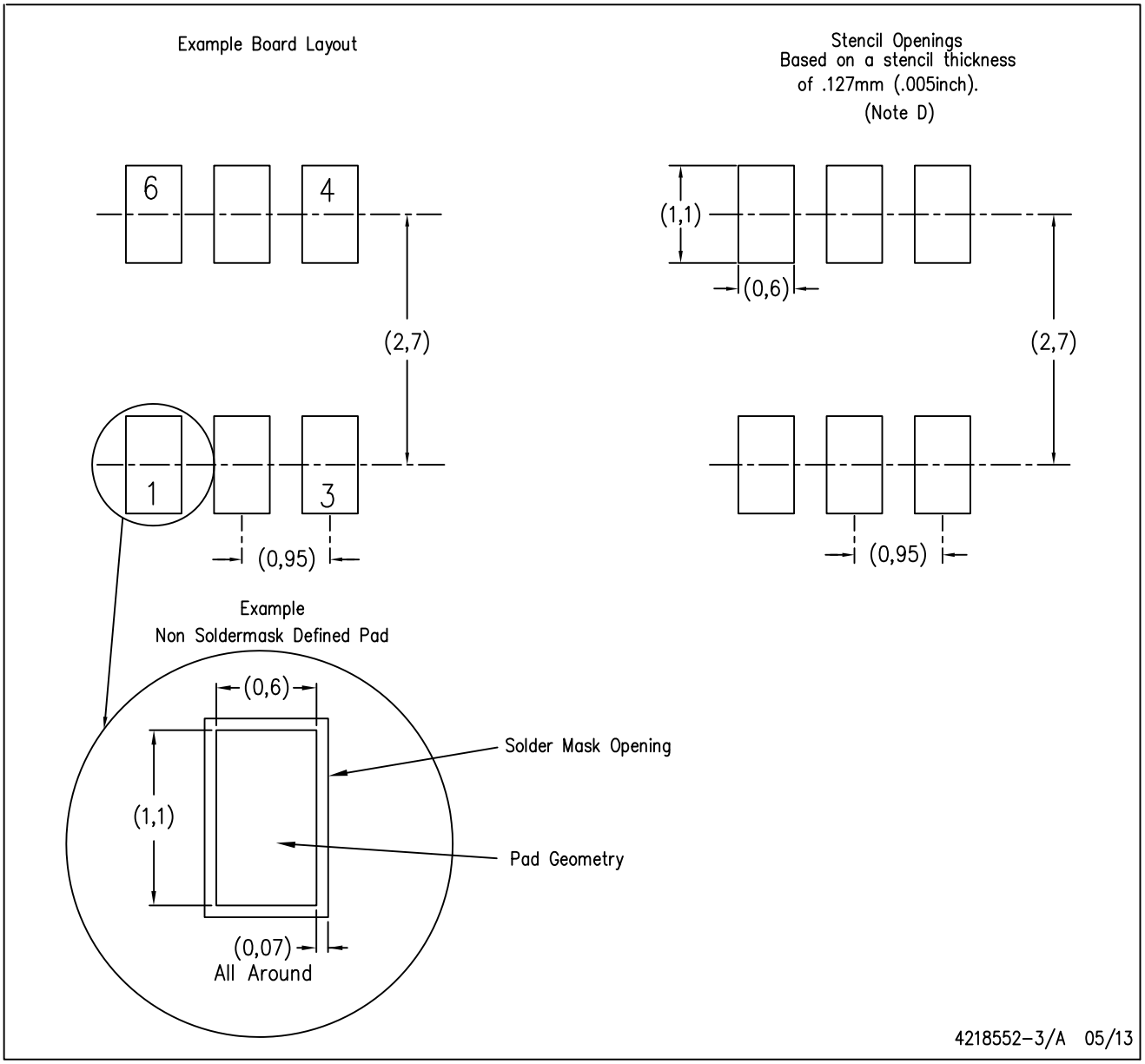
DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4204403–3/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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