



**THE DATASHEET OF  
SN74LVC1G17MDCKREP**



## SINGLE SCHMITT-TRIGGER BUFFER

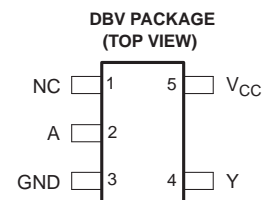
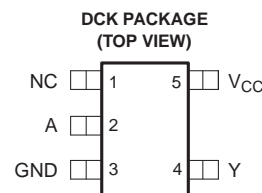
### FEATURES

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Qualification Pedigree<sup>(1)</sup>**
- **Supports 5-V V<sub>CC</sub> Operation**
- **Max t<sub>pd</sub> of 4.6 ns at 3.3 V**
- **Low Power Consumption, 10 µA Max I<sub>CC</sub>**
- **±24 mA Output Drive at 3.3 V**
- **I<sub>off</sub> Supports Partial Power Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

- **ESD Protection Exceeds JEDEC 22**

- **2000-V Human-Body Model (A114-A)**
- **200-V Machine Model (A115-A)**
- **1000-V Charged-Device Model (C101)**

<sup>(1)</sup> Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



### DESCRIPTION/ORDERING INFORMATION

This single Schmitt-trigger buffer is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G17 contains one buffer and performs the Boolean function  $Y = A$ . The device functions as an independent buffer, but because of Schmitt action, it may have different input threshold levels for positive-going (V<sub>T+</sub>) and negative-going (V<sub>T-</sub>) signals.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOT (SC-70) - DCK	Reel of 3000	SN74LVC1G17MDCKREP	C70
	SOP (SOT-23) - DBV	Reel of 3000	SN74LVC1G17MDBVREP	C170

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLE

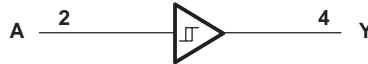
INPUT A	OUTPUT Y
H	H
L	L



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar, NanoFree are trademarks of Texas Instruments.

## LOGIC DIAGRAM (POSITIVE LOGIC)



## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	VALUE	UNIT
V <sub>CC</sub> Supply voltage range	–0.5 to 6.5	V
V <sub>I</sub> Input voltage range <sup>(2)</sup>	–0.5 to 6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state	–0.5 to 6.5
	Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>	–0.5 to V <sub>CC</sub> + 0.5
I <sub>IK</sub> Input clamp current (V <sub>I</sub> < 0)	–50	mA
I <sub>OK</sub> Output clamp current (V <sub>O</sub> < 0)	–50	mA
I <sub>O</sub> Continuous output current		±50
	Continuous current through V <sub>CC</sub> or GND	±100
θ <sub>JA</sub> Package thermal impedance <sup>(4)</sup> : DCK package	252	°C/W
T <sub>stg</sub> Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

		MAX	MAX	UNIT
V <sub>CC</sub> Supply voltage	Operating	1.65	5.5	V
	Data retention only	1.5		
V <sub>I</sub> Input voltage		0	5.5	V
V <sub>O</sub> Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub> High	V <sub>CC</sub> = 1.65 V		–4	mA
	V <sub>CC</sub> = 2.3 V		–8	
	V <sub>CC</sub> = 3 V		–16	
			–24	
I <sub>OL</sub> Low-level output current	V <sub>CC</sub> = 1.65 V		4	mA
	V <sub>CC</sub> = 2.3 V		8	
	V <sub>CC</sub> = 3 V		16	
			24	
V <sub>CC</sub> = 4.5 V		32		
T <sub>A</sub> Operating free-air temperature		–55	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

**ELECTRICAL CHARACTERISTICS**

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>T+</sub> Positive-going input threshold voltage		1.65 V to 4.5 V	0.76		1.13	V
		2.3 V	1.08		1.56	
		3 V	1.48		1.92	
		4.5 V	2.19		2.74	
		5.5 V	2.65		3.33	
V <sub>T-</sub> Negative-going input threshold voltage		1.65 V to 4.5 V	0.35		0.59	V
		2.3 V	0.56		0.88	
		3 V	0.89		1.2	
		4.5 V	1.51		1.97	
		5.5 V	1.88		2.4	
ΔV <sub>hys</sub> Hysteresis (V <sub>T+</sub> – V <sub>T-</sub> )		1.65 V to 4.5 V	0.36		0.64	V
		2.3 V	0.45		0.78	
		3 V	0.51		0.83	
		4.5 V	0.58		0.93	
		5.5 V	0.69		1.04	
V <sub>OH</sub>	I <sub>OH</sub> = –100 mA	1.65 V to 4.5 V	V <sub>CC</sub> – 0.1			V
	I <sub>OH</sub> = –4 mA	1.65 V	1.2			
	I <sub>OH</sub> = –8 mA	2.3 V	1.9			
	I <sub>OH</sub> = –16 mA	3 V	2.4			
	I <sub>OH</sub> = –24 mA		2.3			
	I <sub>OH</sub> = –32 mA	4.5 V	3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 100 mA	1.65 V to 4.5 V			0.1	V
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
	I <sub>OL</sub> = 8 mA	2.3 V			0.3	
	I <sub>OL</sub> = 16 mA	3 V			0.4	
	I <sub>OL</sub> = 24 mA				0.55	
	I <sub>OL</sub> = 32 mA	4.5 V			0.55	
I <sub>I</sub> A input	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μA
I <sub>CC</sub>	V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V			10	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			4.5	pF

 (1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

**SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $C_L = 15$  pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8$ V $\pm 0.15$ V		$V_{CC} = 2.5$ V $\pm 0.2$ V		$V_{CC} = 3.3$ V $\pm 0.3$ V		$V_{CC} = 5$ V $\pm 0.5$ V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	2.8	9.9	1.6	5.5	1.5	4.6	0.9	4.4	ns

**SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $C_L = 30$  pF or 50 pF (unless otherwise noted) (see [Figure 2](#))

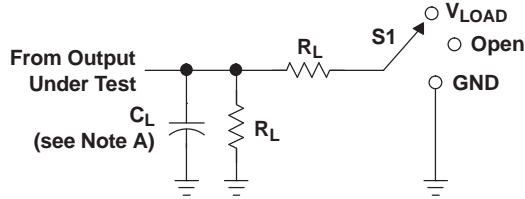
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8$ V $\pm 0.15$ V		$V_{CC} = 2.5$ V $\pm 0.2$ V		$V_{CC} = 3.3$ V $\pm 0.3$ V		$V_{CC} = 5$ V $\pm 0.5$ V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	3.8	11	2	6.5	1.8	5.5	1.2	5	ns

**OPERATING CHARACTERISTICS,**

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8$ V	$V_{CC} = 2.5$ V	$V_{CC} = 3.3$ V	$V_{CC} = 5$ V	UNIT
		TYP	TYP	TYP	TYP	
$C_{pd}$ Power dissipaton capacitance	$f = 10$ MHz	20	21	22	26	

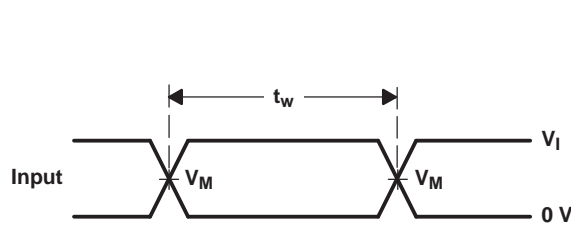
PARAMETER MEASUREMENT INFORMATION



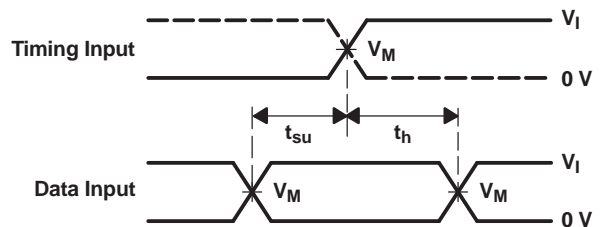
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

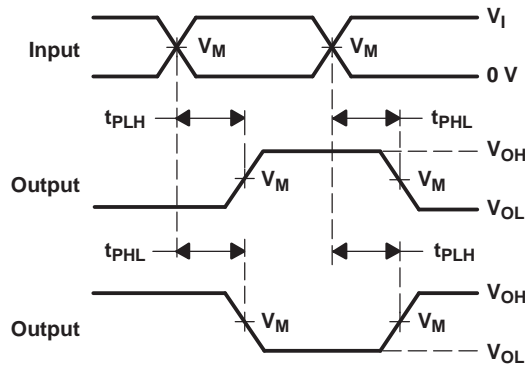
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.3 V



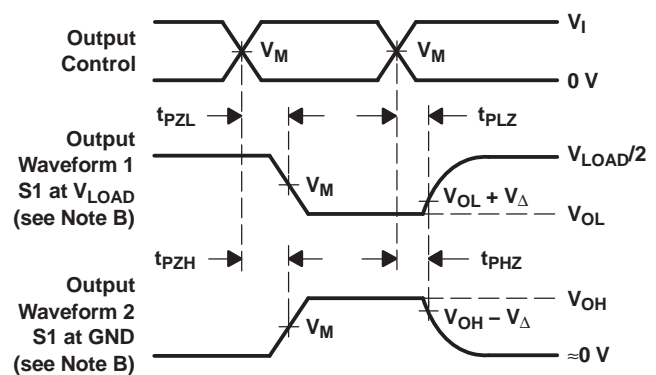
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS

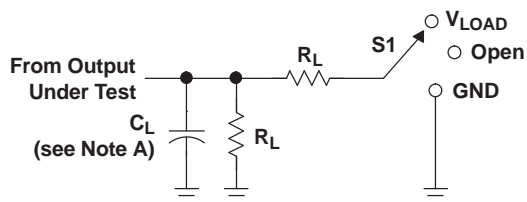


VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

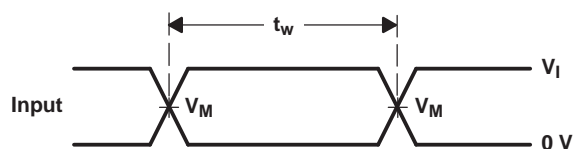
PARAMETER MEASUREMENT INFORMATION (continued)



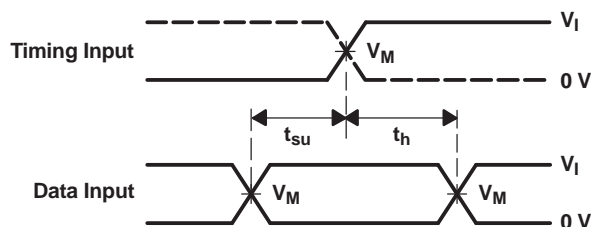
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

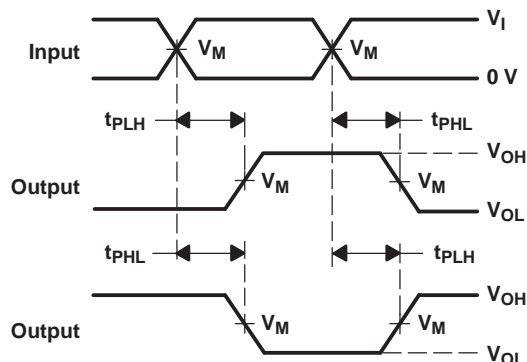
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



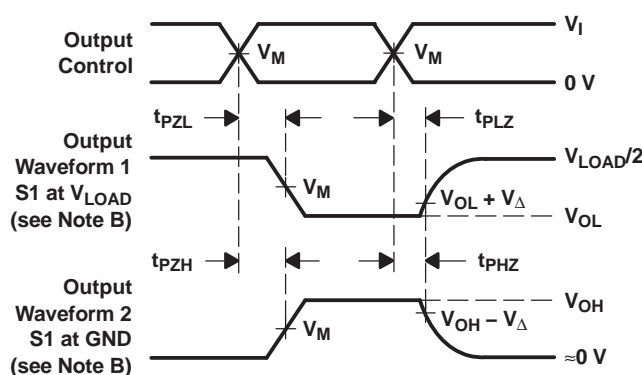
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



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- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G17MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	C170	<a href="#">Samples</a>
SN74LVC1G17MDCKREP	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	C70	<a href="#">Samples</a>
V62/06621-01XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	C170	<a href="#">Samples</a>
V62/06621-01YE	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	C70	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC1G17-EP :**

- Catalog: [SN74LVC1G17](#)
- Automotive: [SN74LVC1G17-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

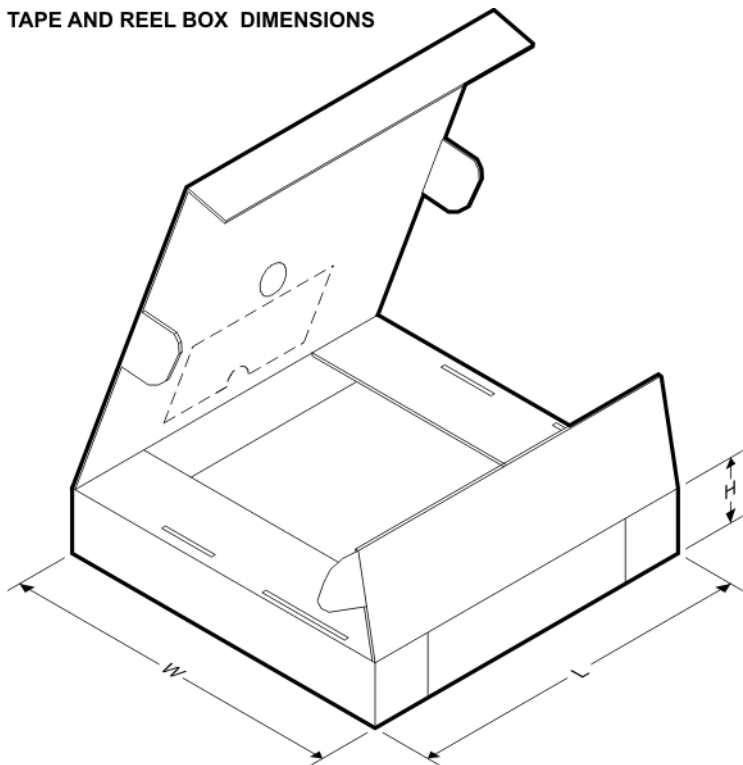


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G17MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G17MDCKREP	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G17MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0
SN74LVC1G17MDCKREP	SC70	DCK	5	3000	203.0	203.0	35.0

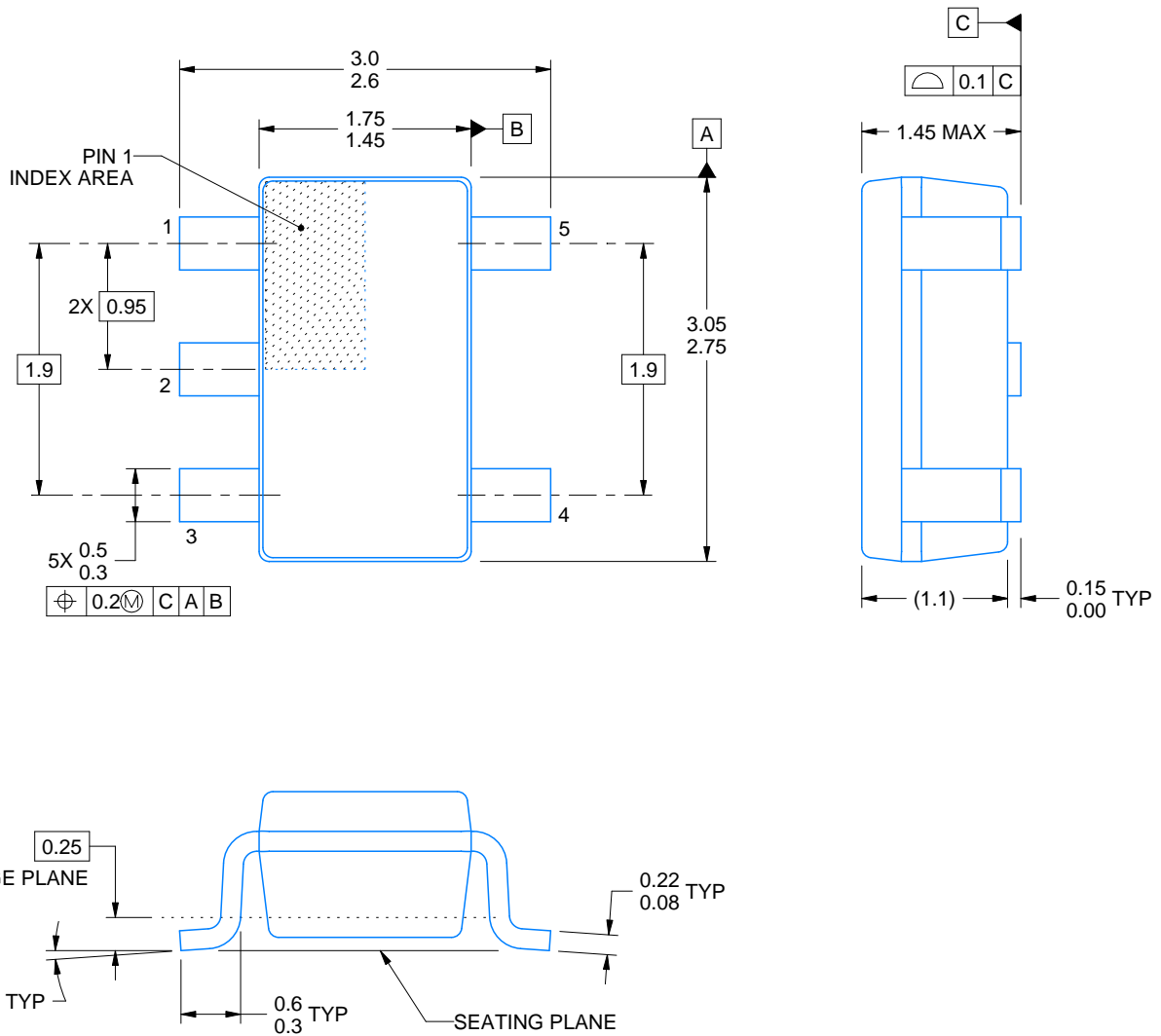
DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

## NOTES:

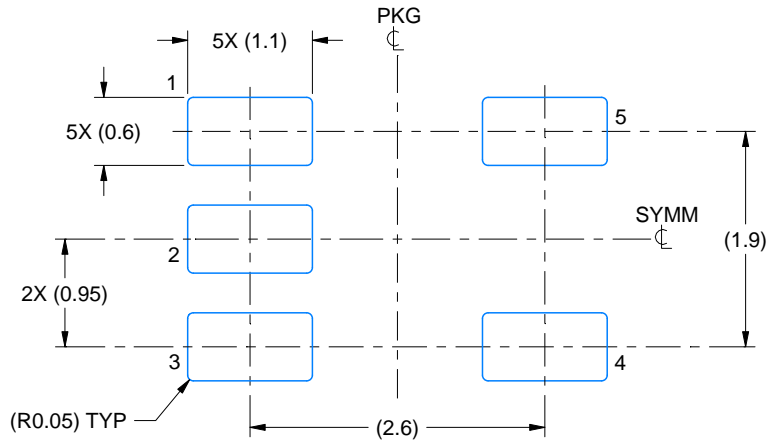
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

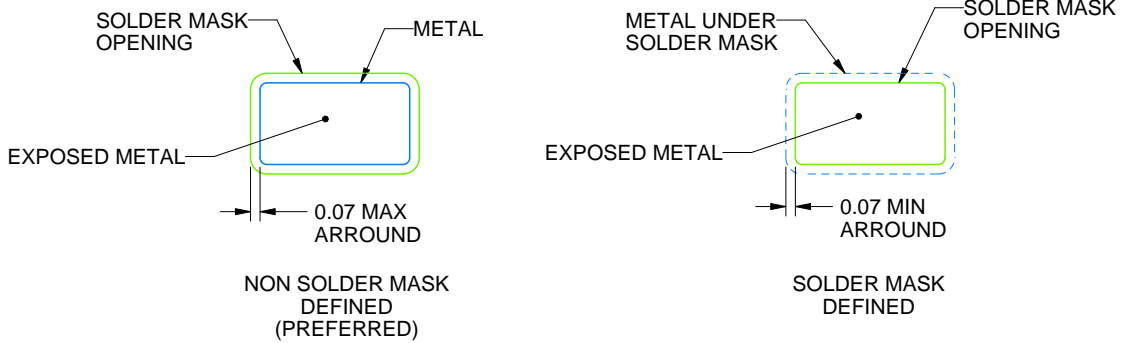
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

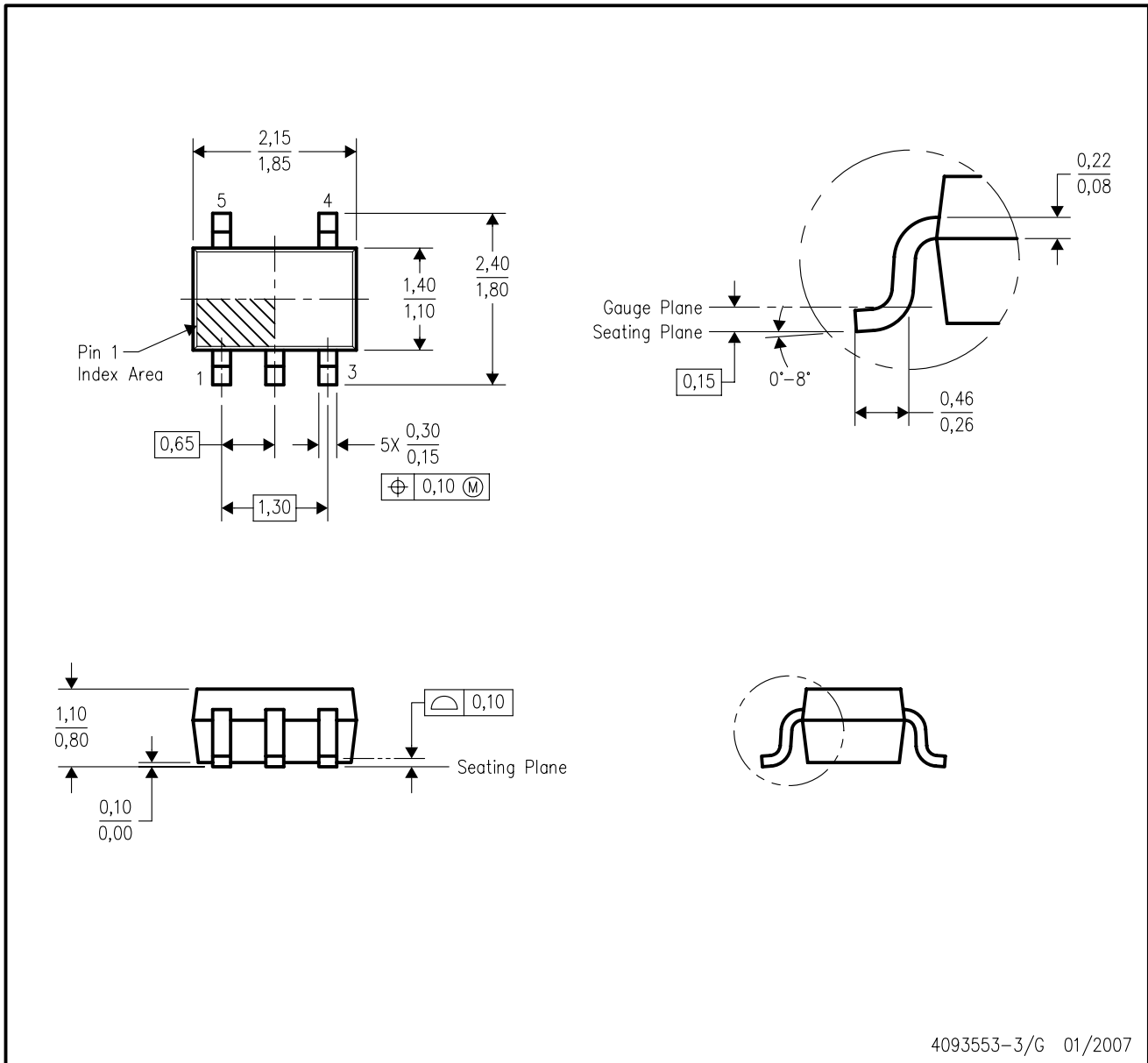
4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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