



**THE DATASHEET OF
CY24292LFXCT**



Four Outputs PCI-Express Clock Generator

Features

- 25 MHz Crystal or Clock Input
- Four Differential 100 MHz PCI-Express Clocks
- Supports HCSL Compatible Output Levels
- One Single-ended 25 MHz Output
- Spread Spectrum Capability on all 100 MHz PCI-Express Clock Outputs
- SMBus Interface with Read Back Capability
- 32-pin QFN Package
- Operating Voltage 3.3 V
- Commercial and Industrial Operating Temperature Range

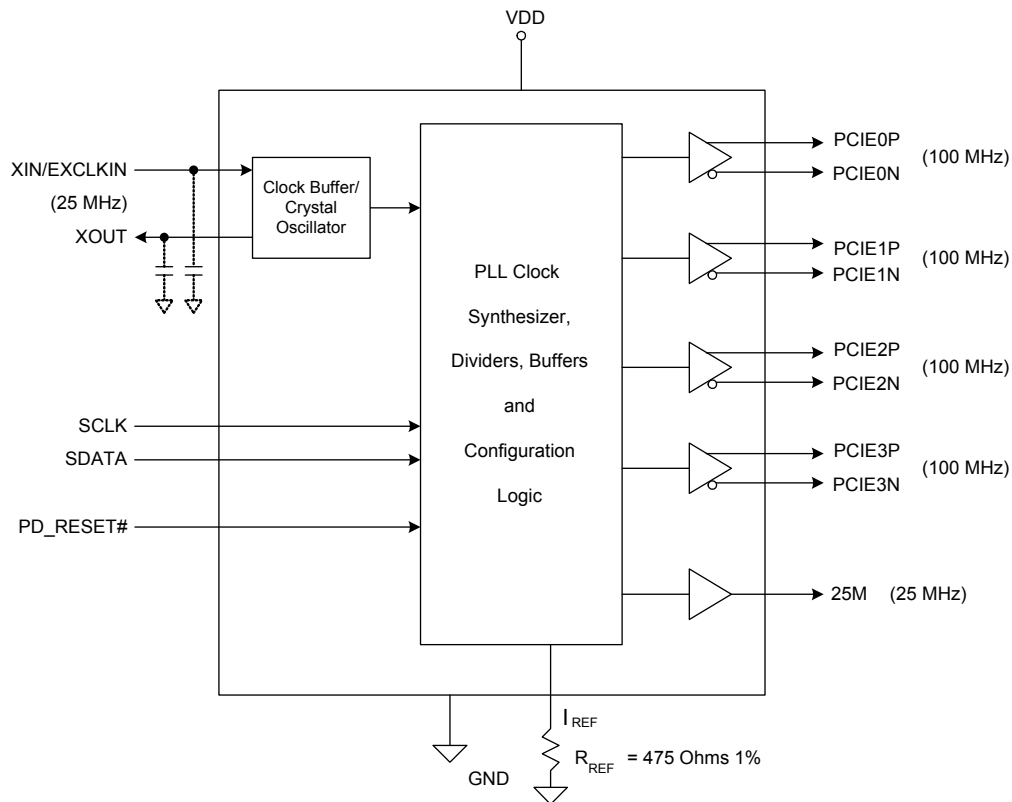
Functional Description

CY24292 is a clock generator device intended for PCI-Express applications. The device includes: four 100 MHz differential clocks with HCSL Compatible outputs for PCI-Express, and one single-ended 25 MHz output.

Using a serially programmable SMBus interface, the CY24292 incorporates spread spectrum modulation on all four 100 MHz outputs. The device incorporates a Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction. The spread feature or individual outputs can also be disabled using the SMBus interface.

For a complete list of related documentation, click [here](#).

Logic Block Diagram

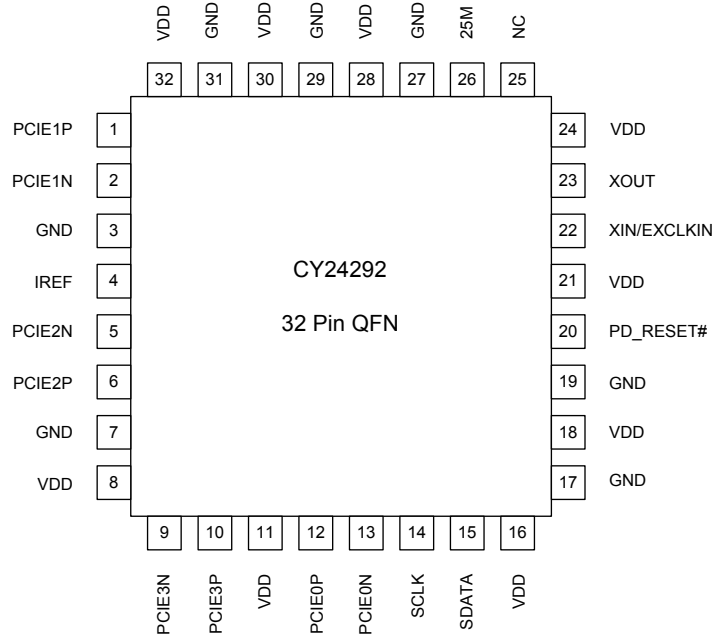


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Pin Configuration

Figure 1. 32-pin QFN Pinout CY24292



Pin Definitions

| Pin Number | Pin Name | Pin Type | Description |
|------------|----------|----------|--|
| 1 | PCIE1P | Output | Differential 100 MHz PCI-Express true clock output. High impedance when disabled. |
| 2 | PCIE1N | Output | Differential 100 MHz PCI-Express complementary clock output. High impedance when disabled. |
| 3 | GND | Power | Ground |
| 4 | IREF | Output | Current set for all differential clock drivers. Connect 475 Ω resistor to ground. |
| 5 | PCIE2N | Output | Differential 100 MHz PCI-Express complementary clock output. High impedance when disabled. |
| 6 | PCIE2P | Output | Differential 100 MHz PCI-Express true clock output. High impedance when disabled. |
| 7 | GND | Power | Ground |
| 8 | VDD | Power | 3.3 V Power supply |
| 9 | PCIE3N | Output | Differential 100 MHz PCI-Express complementary clock output. High impedance when disabled. |
| 10 | PCIE3P | Output | Differential 100 MHz PCI-Express true clock output. High impedance when disabled. |
| 11 | VDD | Power | 3.3 V Power supply |
| 12 | PCIE0P | Output | Differential 100 MHz PCI-Express true clock output. High impedance when disabled. |
| 13 | PCIE0N | Output | Differential 100 MHz PCI-Express complementary clock output. High impedance when disabled. |
| 14 | SCLK | Input | SMBus clock input |
| 15 | SDATA | Input | SMBus data input |
| 16 | VDD | Power | 3.3 V Power supply |
| 17 | GND | Power | Ground |

Pin Definitions (continued)

| Pin Number | Pin Name | Pin Type | Description |
|------------|-------------|----------|---|
| 18 | VDD | Power | 3.3 V Power supply |
| 19 | GND | Power | Ground |
| 20 | PD_RESET# | Input | Global reset pin. Powers down PLLs, disables outputs and sets the SMBus tables to their default state when pulled low. Has internal weak pull up. |
| 21 | VDD | Power | 3.3 V Power supply |
| 22 | XIN/EXCLKIN | Input | Crystal or clock input. Connect to 25 MHz fundamental mode crystal or clock. |
| 23 | XOUT | Output | Crystal output. Connect to 25 MHz fundamental mode crystal. Float for clock input. |
| 24 | VDD | Power | 3.3 V Power supply |
| 25 | NC | – | No connect. Pin has no internal connection. |
| 26 | 25M | Output | 25 MHz Single-ended LVCMOS output. Pull-down when disabled by PD_RESET#. Driven low when individually disabled (via SMBus byte 0, bit 0). |
| 27 | GND | Power | Ground |
| 28 | VDD | Power | 3.3 V Power supply |
| 29 | GND | Power | Ground |
| 30 | VDD | Power | 3.3 V Power supply |
| 31 | GND | Power | Ground |
| 32 | VDD | Power | 3.3 V Power supply |

Functional Overview
SMBus Serial Data Interface

A two-signal serial interface is provided to enhance the flexibility and function of the clock synthesizer. Through the serial data interface, various device functions such as clock output buffers can be individually enabled or disabled. The registers associated with the serial data interface initialize to their default setting upon power up, and therefore this interface is optional. Clock device register changes are normally made upon system initialization, if required. This is a RAM-based technology which does not keep its value when power is off or during a power transition.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write and read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in [Table 1](#).

The block write and block read protocol is outlined in [Table 2 on page 5](#), while [Table 3 on page 5](#) outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h) for write and 11010011 (D3h) for read.

Table 1. Command Code Definition

| Bit | Description |
|-------|--|
| 7 | 0 = block read or block write operation, 1 = byte read or byte write operation |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits must be '000000' |

Table 2. Block Read and Block Write Protocol

| Block Write Protocol | | Block Read Protocol | |
|----------------------|--|---------------------|--|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 2:8 | Slave address – 7 bits | 2:8 | Slave address – 7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command code – 8-bit '00000000' stands for block operation | 11:18 | Command code – 8-bit '00000000' stands for block operation |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Byte count – 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address – 7 bits |
| 29:36 | Data byte 0 – 8 bits | 28 | Read |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 38:45 | Data byte 1 – 8 bits | 30:37 | Byte count from slave – 8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge |
| | Data byte N/Slave acknowledge | 39:46 | Data byte from slave – 8 bits |
| | Data byte N – 8 bits | 47 | Acknowledge |
| | Acknowledge from slave | 48:55 | Data byte from slave – 8 bits |
| | Stop | 56 | Acknowledge |
| | | | Data bytes from slave/acknowledge |
| | | | Data byte N from slave – 8 bits |
| | | | Not acknowledge |
| | | | Stop |

Table 3. Byte Read and Byte Write Protocol

| Byte Write Protocol | | Byte Read Protocol | |
|---------------------|---|--------------------|---|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 2:8 | Slave address – 7 bits | 2:8 | Slave address – 7 bits |
| 9 | Write = 0 | 9 | Write = 0 |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command code – 8 bits '1xxxxxx' stands for byte operation, bits[6:0] of bits[6:0] the command code represents the offset of the byte to be accessed | 11:18 | Command code – 8 bits '1xxxxxx' stands for byte operation, of the command code represents the offset of the byte to be accessed |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Data byte from master – 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address – 7 bits |
| 29 | Stop | 28 | Read = 1 |
| | | 29 | Acknowledge from slave |
| | | 30:37 | Data byte from slave – 8 bits |
| | | 38 | Not acknowledge |
| | | 39 | Stop |

Control Registers

Table 4. Byte 0: Spread Spectrum Control Register

| Bit | Type | At Power up | Outputs Affected | Description | Notes |
|-----|------|-------------|---------------------------------|--|----------------------------------|
| 7 | R/W | 1 | All 100 MHz PCI-Express outputs | Spread select for 100 MHz PCI-Express clocks | 0 = spread off 1 = -0.5% down |
| 6 | R | Undefined | Not applicable | Not used | |
| 5 | R/W | 1 | All outputs | Global OE bit. Enables or disables all outputs. | 0 = disabled 1 = enabled |
| 4 | R | Undefined | Not applicable | Not used | |
| 3 | R | Undefined | Not applicable | Not used | |
| 2 | R | Undefined | Not applicable | Not used | |
| 1 | R | Undefined | Not applicable | Not used | |
| 0 | R/W | 1 | Single-ended 25 MHz output, 25M | OE for single-ended 25 MHz output, 25M. Output driven low when disabled. | 0 = disabled 1 = enabled |

Table 5. Byte 1: Control Register

| Bit | Type | At Power up | Outputs Affected | Description | Notes |
|--------|------|-------------|------------------|-------------|-------|
| 0 to 7 | R | Undefined | Not applicable | Not used | |

Table 6. Byte 2: Control Register

| Bit | Type | At Power up | Outputs Affected | Description | Notes |
|--------|------|-------------|------------------|-------------|-------|
| 0 to 7 | R | Undefined | Not applicable | Not used | |

Table 7. Byte 3: Control Register

| Bit | Type | At Power up | Outputs Affected | Description | Notes |
|-----|------|-------------|----------------------------------|---|-----------------------------|
| 6,7 | R | 0 | Not applicable | Not used | |
| 5 | R/W | 1 | 100 MHz PCI-Express output PCIE3 | OE for 100 MHz PCI-Express output PCIE3 | 0 = disabled 1 = enabled |
| 4 | R/W | 1 | 100 MHz PCI-Express output PCIE2 | OE for 100 MHz PCI-Express output PCIE2 | 0 = disabled 1 = enabled |
| 3 | R | 0 | Not applicable | Not used | |
| 2 | R/W | 1 | 100 MHz PCI-Express output PCIE1 | OE for 100 MHz PCI-Express output PCIE1 | 0 = disabled 1 = enabled |
| 1 | R/W | 1 | 100 MHz PCI-Express output PCIE0 | OE for 100 MHz PCI-Express output PCIE0 | 0 = disabled 1 = enabled |
| 0 | R | Undefined | Not applicable | Not used | |

Table 8. Byte 4: Control Register

| Bit | Type | At Power up | Outputs Affected | Description | Notes |
|--------|------|-------------|------------------|-------------|-------|
| 0 to 7 | R | Undefined | Not applicable | Not used | |

Table 9. Byte 5: Control Register

| Bit | Type | At Power up | Outputs Affected | Description | Notes |
|-----|------|-------------|------------------|-------------------|-------|
| 7 | R | 0 | Not applicable | Revision ID bit 3 | |
| 6 | R | 0 | Not applicable | Revision ID bit 2 | |
| 5 | R | 0 | Not applicable | Revision ID bit 1 | |
| 4 | R | 1 | Not applicable | Revision ID bit 0 | |
| 3 | R | 1 | Not applicable | Vendor ID bit 3 | |
| 2 | R | 0 | Not applicable | Vendor ID bit 2 | |
| 1 | R | 0 | Not applicable | Vendor ID bit 1 | |
| 0 | R | 0 | Not applicable | Vendor ID bit 0 | |

Table 10. Byte 6: Control Register

| Bit | Type | At Power up | Outputs Affected | Description | Notes |
|--------|------|-------------|------------------|-------------|-------|
| 0 to 7 | R | Undefined | Not applicable | Not used | |

The state of the clock outputs upon assertion of the PD_RESET# signal from input pin or Global OE control bit from byte 0, bit 5 of the SMBus is shown in the following table.

Table 11. Power Down Reset Table

| H/W PD_RESET# (pin 24) | S/W PD_RESET# (Byte 0 bit 5) | All Clock Outputs |
|------------------------|------------------------------|---|
| 0 | 0 | Disabled, Hi-Z. 25M has weak pull-down. |
| 0 | 1 | Disabled, Hi-Z. 25M has weak pull-down. |
| 1 | 0 | Disabled, Hi-Z. 25M has weak pull-down. |
| 1 | 1 | Enabled |

Application Information

Crystal Recommendations

The CY24292 requires a parallel resonance crystal. Substituting a series resonance crystal causes the CY24292 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300 ppm frequency shift between the series and parallel crystals due to incorrect loading.

Table 12. Crystal Recommendations

| Frequency | Cut | Load Cap (max) | Eff Series Rest (max) | Drive (max) | Tolerance (max) | Stability (max) | Aging (max) |
|-----------|----------|----------------|-----------------------|-------------|-----------------|-----------------|-------------|
| 25.00 MHz | Parallel | 16 pF | 30 Ω | 1.0 mW | 30 ppm | 10 ppm | 5 ppm/yr |

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, consider the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

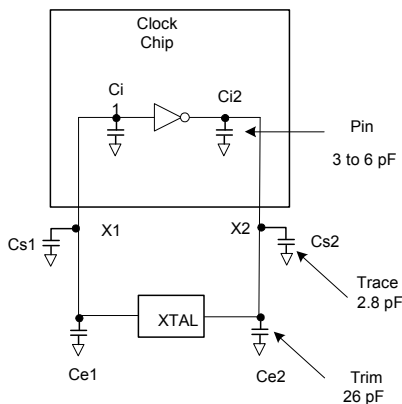
Figure 2 shows a typical crystal configuration using two trim capacitors. It is important to note that the trim capacitors in series with the crystal are not parallel. It is a common misconception that load capacitors are in parallel with the crystal and are approximately equal to the load capacitance of the crystal. This is not true.

Calculating Load Capacitors

In addition to the standard external trim capacitors, the trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading.

As mentioned in the previous section, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, the trim capacitors (Ce1, Ce2) must be calculated to provide equal capacitive loading on both sides.

Figure 2. Crystal Loading Example



Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load capacitance (each side)

$$C_e = 2 * CL - (C_s + C_i)$$

Total capacitance (as seen by the crystal)

$$CL_e = \frac{1}{\left(\frac{1}{C_{e1} + C_{s1} + C_{i1}} + \frac{1}{C_{e2} + C_{s2} + C_{i2}} \right)}$$

- CL Crystal load capacitance
- CLe Actual loading seen by crystal using standard value trim capacitors
- Ce External trim capacitors
- Cs Stray capacitance (terraced)
- Ci Internal capacitance

Current Source (Iref) Reference Resistor

If the board target trace impedance (Z) is 50 Ω, then for R_{REF} = 475 Ω (1%) provides I_{REF} of 2.32 mA. The output current (I_{OH}) is equal to 6 × I_{REF}.

Output Termination

The PCI-Express differential clock outputs of CY24292 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are explained in detail in the section [PCI-Express Layout Guidelines on page 9](#).

PCB Layout Recommendations

For optimum device performance and lowest phase noise, the following guidelines must be observed.

1. Each 0.01 μF decoupling capacitor must be mounted on the component side of the board as close to the VDD pin as possible.
2. No vias must be used between the decoupling capacitor and the VDD pin.
3. The PCB trace to the VDD pin and the ground via must be kept as short as possible. The distance of the ferrite bead and bulk decoupling from the device is less critical.

4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces must be routed away from the CY24292. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Decoupling Capacitors

Decoupling capacitors of 0.01 μF must be connected between VDD and GND as close to the device as possible. Do not share ground vias between components. Route power from power source through the capacitor pad, and then into the CY24292 pin.

PCI-Express Layout Guidelines

HCSL Compatible Layout Guidelines

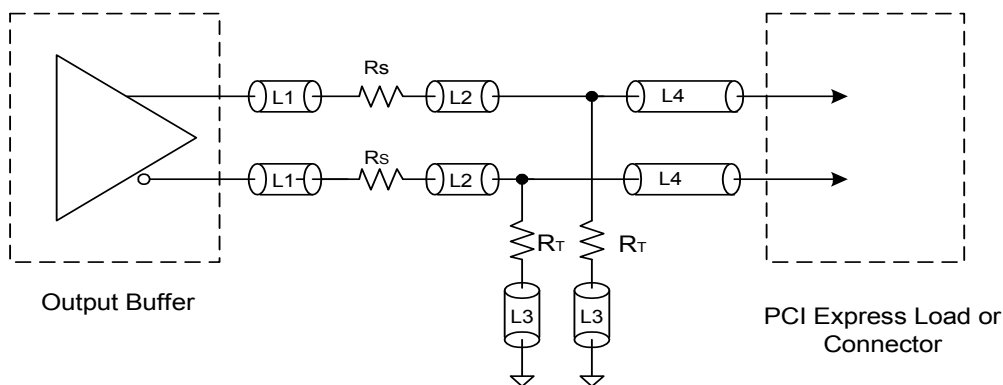
Table 13. Common Recommendations for Differential Routing

| Differential Routing ^[1] | Dimension or Value | Unit |
|---|--------------------|----------|
| L1 length, route as non-coupled 50 Ω trace | 0.5 max | inch |
| L2 length, route as non-coupled 50 Ω trace | 0.2 max | inch |
| L3 length, route as non-coupled 50 Ω trace | 0.2 max | inch |
| R_S | 33 | Ω |
| R_T | 49.9 | Ω |

Table 14. Differential Routing for PCI-Express Load or Connector

| Differential Routing ^[1] | Dimension or Value | Unit |
|--|--------------------|------|
| L4 length, route as coupled microstrip 100 Ω differential trace | 2 to 32 | inch |
| L4 length, route as coupled stripline 100 Ω differential trace | 1.8 to 30 | inch |

Figure 3. PCI-Express Device Routing



Note

1. Refer to Figure 3.

Absolute Maximum Ratings

| Parameter | Description | Condition | Min | Max | Unit |
|--------------------|-----------------------------------|-----------------------------|----------------|-----------------------|------|
| V _{DD} | Supply voltage | | -0.5 | 4.6 | V |
| V _{IN} | Input voltage | Relative to V _{SS} | -0.5 | V _{DD} + 0.5 | V |
| T _S | Temperature, Storage | Non Operating | -65 | 150 | °C |
| T _J | Temperature, Junction | | - | 125 | °C |
| ESD _{HBM} | ESD Protection (Human Body Model) | JEDEC EIA/JESD22-A114-E | 2000 | - | V |
| UL-94 | Flammability rating | | V-0 at 1/8 in. | | |
| MSL | Moisture sensitivity level | | 3 | | |

Recommended Operation Conditions

| Parameter | Description | Min | Typ | Max | Unit |
|---------------------|--|------|-----|-----|------|
| V _{DD} | Supply voltage | 3.0 | - | 3.6 | V |
| T _{AC} | Commercial ambient temperature | 0 | - | 70 | °C |
| T _{AI} | Industrial ambient temperature | -40 | - | 85 | °C |
| t _{PU} | Power up time for all V _{DD} to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | - | 500 | ms |
| t _{PD} | Minimum pulse width of PD_RESET# input | 100 | - | - | ns |
| V _{SMB} | SMBus Voltage | 3.0 | - | 3.6 | V |
| R _{REFTOL} | Tolerance on the 475Ω R _{REF} resistor that sets output currents on 100MHz ports | - | - | 1 | % |

DC Electrical Characteristics

Unless otherwise stated, $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$, ambient temperature = $-40 \text{ }^\circ\text{C}$ to $85 \text{ }^\circ\text{C}$ Industrial, $0 \text{ }^\circ\text{C}$ to $70 \text{ }^\circ\text{C}$ Commercial, $R_{REF} = 475 \text{ } \Omega$

| Parameter ^[2] | Description | Condition | Min | Typ | Max | Unit |
|--------------------------|---|--|----------------|-------|----------------|---------------|
| V_{OL1} | Low level output voltage of 25M clock | $I_{OL} = 8 \text{ mA}$ | – | – | 0.4 | V |
| V_{OH1} | High level output voltage of 25M clock | $I_{OH} = -8 \text{ mA}$ | $V_{DD} - 0.4$ | – | – | V |
| V_{OL2} | Low level output voltage of 100M clocks | HCSL termination ($R_S = 33 \text{ } \Omega$, $R_T = 49.9 \text{ } \Omega$) | -0.2 | 0 | 0.05 | V |
| V_{OH2} | High level output voltage of 100M clocks | HCSL termination ($R_S = 33 \text{ } \Omega$, $R_T = 49.9 \text{ } \Omega$) | 0.65 | 0.71 | 0.95 | V |
| V_{OL3} | Low level output voltage SDATA | $I_{OL} = 4 \text{ mA}$ | – | – | 0.4 | V |
| I_{OH} | Output high current for differential clocks | $I_{OH} = 6 \times I_{REF}$ | -13 | -15.2 | -17 | mA |
| V_{IL1} | Low level input voltage of SCLK, SDATA | | -0.3 | – | 0.8 | V |
| V_{IH1} | High level input voltage of SCLK, SDATA | | 2.1 | – | $V_{DD} + 0.3$ | V |
| V_{IL2} | Low level input voltage of XIN/EXCLKIN, PD_RESET# pins | | -0.3 | – | 0.8 | V |
| V_{IH2} | High level input voltage of XIN/EXCLKIN, PD_RESET# pins | | 2.0 | – | $V_{DD} + 0.3$ | V |
| I_{DD} | Operating supply current | No load, PD_RESET# pin = 1 | – | 50 | 70 | mA |
| | | Full load, PD_RESET# pin = 1 | – | 135 | 170 | mA |
| I_{DDPD} | Power down current | PD_RESET# pin = 0 | – | 250 | 350 | μA |
| C_{IN} | Input capacitance | All input pins | – | 5 | – | pF |
| R_{PU} | Pull up resistor, PD_RESET# | | – | 90 | – | k Ω |
| R_{PD} | Pull down resistor, 25M output | PD_RESET# = 0 | 50 | – | 150 | k Ω |

Thermal Resistance

| Parameter ^[3] | Description | Test Conditions | 32-pin QFN | Unit |
|--------------------------|--|---|------------|---------------------------|
| θ_{JA} | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 22 | $^\circ\text{C}/\text{W}$ |
| θ_{JC} | Thermal resistance (junction to case) | | 19.5 | $^\circ\text{C}/\text{W}$ |

Notes

- Parameters are guaranteed by design and characterization. Not 100% tested in production.
- These parameters are guaranteed by design and are not tested.

AC Electrical Characteristics

Unless otherwise stated, $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$, ambient temperature = $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ Industrial, $0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ Commercial, $R_{REF} = 475\ \Omega$.

Table 15. Single-Ended 25 MHz Output

| Parameter ^[4] | Description | Condition | Min | Typ | Max | Unit |
|--------------------------|---|---|-----|-----|-----|------|
| F_{IN} | Input clock frequency (crystal or external clock) | – | – | 25 | – | MHz |
| T_{INDC} | Input clock duty cycle | – | 40 | – | 60 | % |
| F_{OUT} | Output clock frequency, 25M | – | – | 25 | – | MHz |
| T_R | Output rise time ^[5] | 20% to 80% of VDD | – | 0.5 | 1 | ns |
| T_F | Output fall time ^[5] | 80% to 20% of VDD | – | 0.5 | 1 | ns |
| T_{DC} | Output clock duty cycle ^[5] | Measured at VDD/2 | 45 | 50 | 55 | % |
| T_{CCJ} | Cycle-to-cycle jitter ^[5] | – | – | – | 200 | ps |
| T_{OEPD} | Output enable from power down reset | PD_RESET# going high to 99% of final frequency | – | – | 2 | ms |
| T_{LOCK} | Clock stabilization from power up | Measured from 90% of the applied power supply level | – | 1 | 2 | ms |

Notes

4. Parameters are guaranteed by design and characterization. Not 100% tested in production.
5. Measured with Cload = 15 pF lumped load.

Table 16. Differential 100 MHz, HCSL Terminated Outputs

| Parameter ^[6] | Description | Test Condition | Min | Typ | Max | Unit |
|--------------------------|---|---|-------|------|---------|------|
| F _{OUT} | Output frequency | | – | – | 100 | MHz |
| SP _{PROFILE} | Spread modulation profile | | – | – | Lexmark | type |
| SP _{MOD} | Spread modulation frequency | | 30 | 32 | 33 | kHz |
| T _{CCJ} | Cycle-to-cycle jitter ^[7] | | – | – | 90 | ps |
| T _{PHJ} | Peak-to-peak phase jitter ^[7, 8] | | – | – | 86 | ps |
| T _{DC} | Output clock duty cycle ^[7] | | 45 | 50 | 55 | % |
| ER _R | Rising edge rate ^[7, 9] | See notes 7 and 9 | 0.6 | – | 4.0 | V/ns |
| ER _F | Falling edge rate ^[7, 9] | See notes 7 and 9 | 0.6 | – | 4.0 | V/ns |
| V _{CROSS} | Absolute crossing point voltage ^[10, 11, 12] | See notes 10, 11, and 12 | 0.25 | 0.35 | 0.55 | V |
| V _{Xdelta} | Variation of V _{CROSS} over all rising clock edges ^[10, 11, 13] | See notes 10, 11, and 13 | – | – | 140 | mV |
| T _{PERIOD AVG} | Average clock period accuracy ^[7, 14] | See notes 7 and 14 | –300 | – | 2800 | ppm |
| T _{PERIOD ABS} | Absolute clock period ^[7, 15] | See notes 7 and 15 | 9.847 | – | 10.203 | ns |
| T _{OSKEW ALL} | Output skew, all pairs ^[16] | Measured at V _{CROSS} point See note 16 | – | – | 100 | ps |
| T _{OSKEW P-P} | PCIE0P/N to PCIE3P/N skew and PCIE1P/N to PCIE2P/N skew ^[16] | Measured at V _{CROSS} point See note 16 | – | – | 50 | ps |
| T _{OE PD} | Output enable from power down reset | PD_RESET# going high to 99% of final frequency | – | – | 2 | ms |
| T _{LOCK} | Clock stabilization from power up | Measured from 90% of the applied power supply level | – | 1 | 2 | ms |

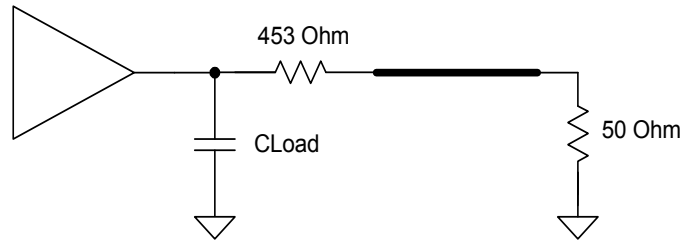
Notes

6. Parameters are guaranteed by design and characterization. Not 100% tested in production.
7. Measurement taken from differential waveform (PCIEP minus PCIEN). Either single ended probes with math or a differential probe can be used.
8. Phase jitter is determined using data captured on an oscilloscope at a sample rate of 20 GS/sec, for a minimum 100,000 continuous clock periods. This data is then processed using the ClockJitter 1.3.0 software from PCISIG, using the PCI_E_1_1 template.
9. Measured from -150 mV to +150 mV on the differential waveform (derived from PCIEP minus PCIEN). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
10. Measurement taken from a single-ended waveform.
11. Measured at crossing point where the instantaneous voltage value of the rising edge of PCIEP equals the falling edge of PCIEN.
12. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
13. Defined as the total variation of all crossing voltages of Rising PCIEP and Falling PCIEN. This is the maximum allowed variance in V_{CROSS} for any particular system.
14. PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly, or 100 Hz. For 300 PPM then we have an error budget of 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 PPM applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum, there is an additional 2500 PPM nominal shift in maximum period resulting from the 0.5% down spread, resulting in a maximum average period specification of +2800 PPM.
15. Defined as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation.
16. Measured at the rising 0 V point of the differential signal. Skew is the time difference of the rising 0 V point between any two differential signal pairs. The measurement is taken over 1000 samples, and the average value is used.

Test and Measurement Setup

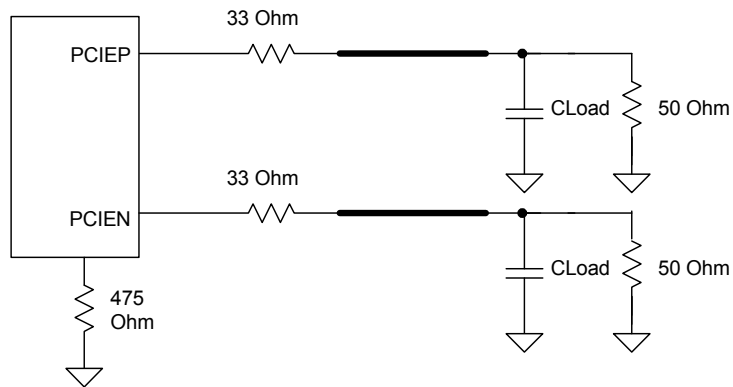
Single-ended Signals

Figure 4. Test Load Configuration for Single-ended Output Signal



Differential Signals

Figure 5. Test Load Configuration for Differential Output Signal

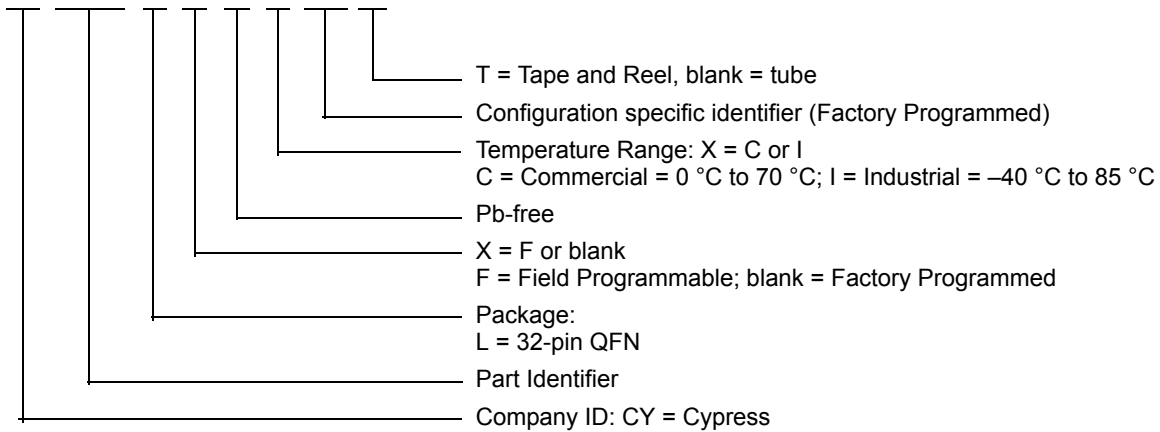


Ordering Information

| Ordering Code | Package Type | Production Flow |
|----------------|----------------------------|-----------------------------|
| Pb-free | | |
| CY24292LFXC | 32-pin QFN | Commercial, 0 °C to 70 °C |
| CY24292LFXCT | 32-pin QFN – Tape and Reel | Commercial, 0 °C to 70 °C |
| CY24292LFXI | 32-pin QFN | Industrial, –40 °C to 85 °C |
| CY24292LFXIT | 32-pin QFN – Tape and Reel | Industrial, –40 °C to 85 °C |

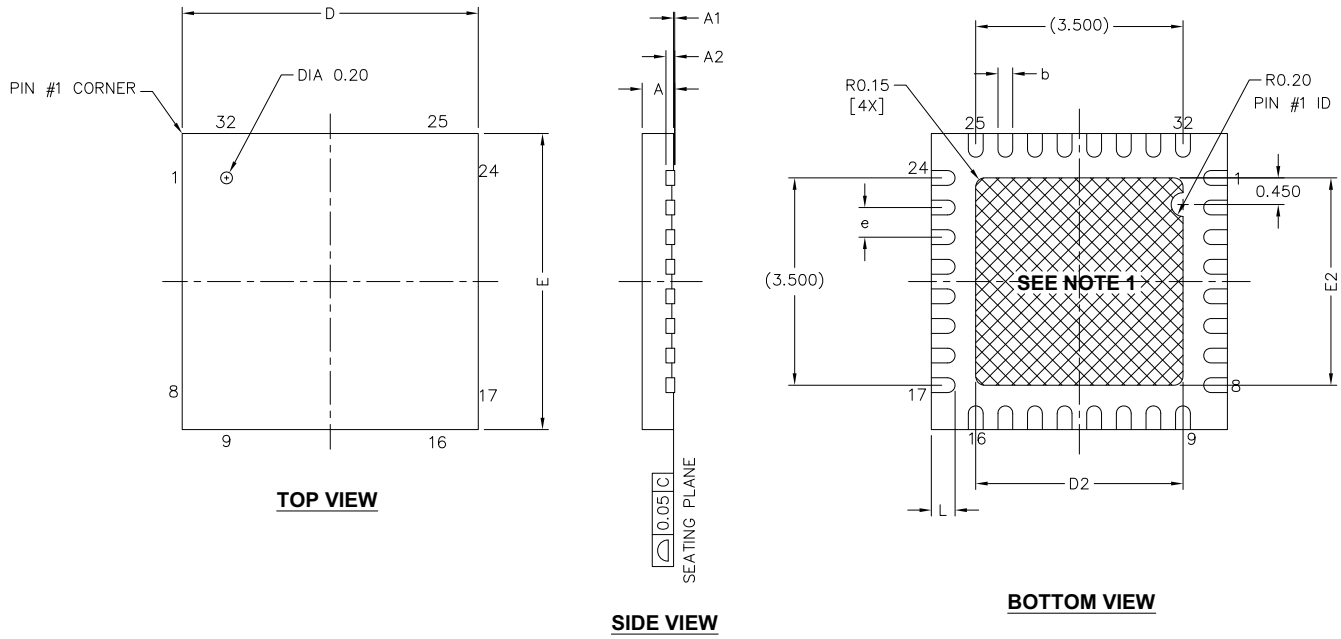
Ordering Code Definitions

CY 24292 L X X X -xxx T




Package Diagram

Figure 6. 32-pin QFN (5 x 5 x 0.55 mm) LQ32 3.5 x 3.5 E-Pad (Sawn) Package Outline, 001-42168



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *F

Acronyms

Table 17. Acronyms Used in this Document

| Acronym | Description |
|---------|---|
| EIA | electronic industries alliance |
| EMI | electromagnetic interference |
| ESD | electrostatic discharge |
| HCSL | host clock signal level |
| JEDEC | joint electron devices engineering council |
| LVC MOS | low voltage complementary metal oxide semiconductor |
| OE | output enable |
| PCI | peripheral component interconnect |
| PLL | phase-locked loop |
| QFN | quad-flat no-leads |
| RAM | random access memory |

Document Conventions

Units of Measure

Table 18. Units of Measure

| Symbol | Unit of Measure |
|--------|-------------------|
| °C | degree Celsius |
| kHz | kilohertz |
| kΩ | kilohm |
| MHz | megahertz |
| μF | microfarad |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| V | volt |

Document History Page

| Document Title: CY24292, Four Outputs PCI-Express Clock Generator | | | | |
|---|---------|------------------|-----------------|---|
| Document Number: 001-46142 | | | | |
| Rev. | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 2490167 | PYG / DPF / AESA | See ECN | New data sheet. |
| *A | 2507681 | DPF / AESA | 05/23/2008 | Updated Pin Configuration (Changed pinout based on PCIE_Bonding_Rev G). Updated DC Electrical Characteristics (Added Note 2 and referred the same note in parameter column, added HCSL termination in Condition column for V_{OL2} , V_{OH2}). Updated AC Electrical Characteristics (updated Note 5, added Note 11 and referred the same note in T_{DC} parameter in Table 16, changed Clod from 2 pF to 4 pF in a Note below, added maximum value of V_{Xdelta} (140 mV) in the Table 16). Updated to new template. |
| *B | 2811340 | CXQ | 12/03/2009 | <p>Changed status from Preliminary to Final.</p> <p>Updated Pin Definitions (Added explanation of 25M output disable feature).</p> <p>Updated Control Registers (Changed default setting (At Power up column) for bit 7 in Table 4 to '1', changed description of bit 5 in Table 4 to 'Global OE bit', added explanation of 25M output disable feature in Table 4, changed unused bits (Type Column) from R/W to R in Table 7, changed default setting (At Power up column) for bit 4 in Table 9 to '1', added explanation of 25M output disable feature in Table 11).</p> <p>Updated the sub-section Crystal Recommendations under the main section Application Information (Added "max" to Load Cap and Eff Series Rest columns in Table 12).</p> <p>Updated sub-section "LVDS Compatible Layout Guidelines" under the main section PCI-Express Layout Guidelines (changed "LVDS Down Device" to "LVDS Device" in all instances).</p> <p>Updated Absolute Maximum Ratings (Changed maximum value of T_J parameter to 125 °C).</p> <p>Updated Recommended Operation Conditions (Added V_{SMB} and R_{REFTOL} parameters and its details).</p> <p>Updated DC Electrical Characteristics (added R_{REF} value to conditions at top, removed V_{OHSD} and V_{OLSD} parameters and their details, changed maximum value of V_{OH2} parameter from 0.85 V to 0.95 V, added V_{OL3} parameter and its details, changed typical value of I_{OH} parameter from -14.2 mA to -15.2 mA, added minimum value of V_{IL1} parameter, changed maximum value of V_{IL1} parameter from 1 V to 0.8 V, changed minimum value of V_{IH1} parameter from 2.2 V to 2.1 V, added typical and maximum values for I_{DD} no load and full load parameters, changed typical value of I_{DDPD} parameter from TBD to 250 μA, changed maximum value of I_{DDPD} parameter from TBD to 350 μA, added R_{PU} parameter and its details, changed R_{PD} parameter to apply to 25M output only).</p> <p>Updated AC Electrical Characteristics (added R_{REF} value to conditions at top, removed F_{ERR} parameter and its details in Table 15, added $SP_{PROFILE}$ parameter and its details in Table 16, added minimum and maximum values for SP_{MOD} parameter, changed maximum value of T_{CCJ} parameter from 100 ps to 90 ps in Table 16, added T_{PHJ} parameter and its details in Table 16, changed T_R and T_F parameters and its details into ER_R and ER_F parameters in Table 16, removed $T_{RFMATCH}$ parameter and its details in Table 16, splitted T_{OSKEW} parameter into two parameters namely T_{OSKEW_ALL} and T_{OSKEW_P-P} parameter and also changed their details in Table 16, added minimum value of V_{CROSS} parameter and also changed the description of the same parameter in Table 16, changed description of V_{Xdelta} parameter in Table 16).</p> <p>Updated Package Diagram (to spec 001-42168 Rev *C).</p> <p>Fixed various typos.</p> |
| *C | 2901711 | KVM | 05/14/10 | Updated Package Diagram . |

Document History Page (continued)

| Document Title: CY24292, Four Outputs PCI-Express Clock Generator Document Number: 001-46142 | | | | |
|---|---------|-----------------|-----------------|--|
| Rev. | ECN | Orig. of Change | Submission Date | Description of Change |
| *D | 3448896 | PURU | 11/28/2011 | Updated Features (Removed LVDS related information). Updated Functional Description (Removed LVDS related information). Updated Output Termination under Application Information (Removed LVDS related information). Removed the sub-section "LVDS Compatible Layout Guidelines" under the main section PCI-Express Layout Guidelines . Added Ordering Code Definitions . Added Acronyms and Units of Measure . Updated to new template. |
| *E | 4580588 | TAVA | 12/05/2014 | Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Updated Package Diagram . |
| *F | 5281281 | PSR | 04/26/2017 | Added Thermal Resistance . Updated to new template. |
| *G | 5784045 | PSR | 06/27/2017 | Updated AC Electrical Characteristics : Added F_{IN} and T_{INDC} parameters. Updated Figure 6 in Package Diagram (spec 001-42168 *E to *F). |

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