THE DATASHEET OF

PL500-17TC-R

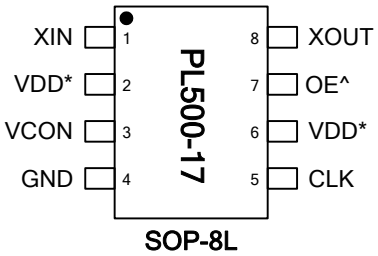
PL500-17

Low Phase Noise VCXO (17MHz to 36MHz)

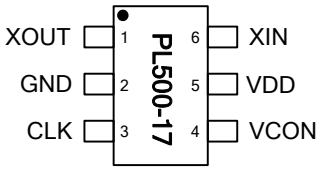
FEATURES

- VCXO output for the 17MHz to 36MHz range
- Low phase noise (-130dBc @ 10kHz offset at 35.328MHz)
- LVCMOS output with OE tri-state control
- 17 to 36MHz fundamental crystal input
- Integrated high linearity variable capacitors
- 8mA drive capability at TTL output
- ±150 ppm pull range, max 5% (typ.) linearity
- Low jitter (RMS): 2.5ps period jitter
- 2.5 to 3.3V operation
- Available in 8-Pin SOP, 6-pin SOT23 GREEN/ RoHS compliant packages, or Die

PIN CONFIGURATION



SOP-8L



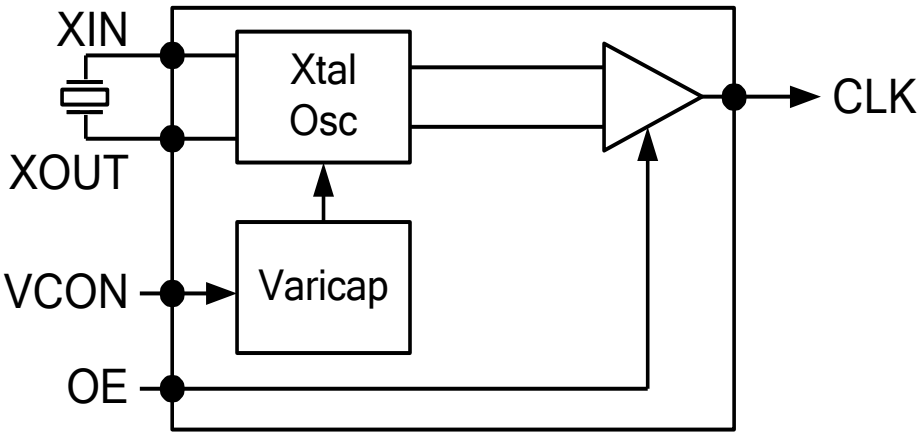
SOT23-6L

^: Denotes internal Pull-up
*: Only one VDD pin needs to be connected

DESCRIPTION

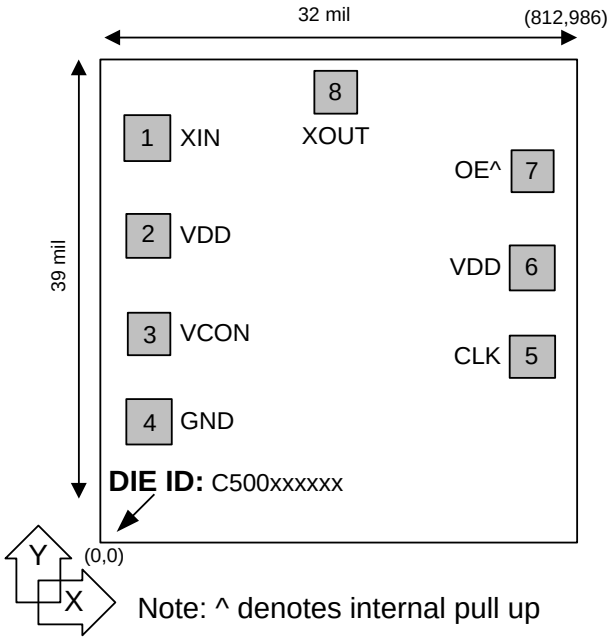
The PL500-17 is a low cost, high performance and low phase noise VCXO for the 17 to 36MHz range, providing less than -130dBc at 10kHz offset at 35.328MHz. The very low jitter (2.5 ps RMS period jitter) makes this chip ideal for applications requiring voltage controlled frequency sources. Input crystal can range from 17 to 36MHz (fundamental resonant mode).

BLOCK DIAGRAM



Low Phase Noise VCXO (17MHz to 36MHz)

DIE PAD LAYOUT



Note: ^ denotes internal pull up

DIE SPECIFICATIONS

Name	Value
Size	39 x 32 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	8 mil

PACKAGE PIN AND DIE PAD ASSIGNMENT

Name	Pin#		Die Pad Position		Type	Description
	SOP-8	SOT23-6	X (µm)	Y (µm)		
XIN	1	6	94.183	768.599	I	Crystal input pin.
VDD	2	5	94.157	605.029	P	VDD power supply pin. Only one VDD pin is necessary.
VCON	3	4	94.183	331.756	I	Frequency control voltage input pin.
GND	4	2	94.193	140.379	P	Ground pin.
CLK	5	3	715.472	203.866	O	Output clock pin.
VDD	6	-	715.307	455.726	P	VDD power supply pin. Only one VDD pin is necessary.
OE*	7	-	715.472	626.716	I	Output Enable input pin. Disables the output when low. Internal pull-up enables output by default if pin is not connected to low.
XOUT	8	1	476.906	888.881	I	Crystal output pin. Ref Clock input.

* OE (Output Enable) pin is not available in SOT23-6L package, the output will always be enabled by the build in pull-up resister.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Machine Model		200		V
ESD Protection, Human Body Model		2		kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		XTAL C_0/C_1 < 250 0V ≤ VCON ≤ 3.3V		300		ppm
CLK Output Pullability		VCON=1.65V, ±1.65V	±150			ppm
VCXO Tuning Characteristic				100		ppm/V
Pull Range Linearity					5	%
Power Supply Rejection	PWSRR	Frequency change, V_{DD} ±10%	-1		+1	ppm
VCON Pin Input Impedance			5000			kΩ
VCON Modulation BW		0V ≤ VCON ≤ 3.3V, -3dB	18			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

3. AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency	F_{in}	Fundamental Mode	17		36	MHz
Output Clock Rise/Fall Time	t_r / t_f	0.8V to 2.0V, 10 pF load		1.15		ns
	t_r / t_f	0.3V to 3.0V, 15 pF load		3.7		
Output Clock Duty Cycle			45	50	55	%
Output Enable/Disable Time	t_{OE}			5		ns
Start-Up Time	t_{SU}			1		ms

4. Jitter and Phase Noise Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
RMS Period Jitter (1 sigma – 1000 samples)	With capacitive decoupling between V_{DD} and GND.		2.5		ps
Phase Noise, Relative to Carrier	27MHz @100Hz offset		-100		dBc/Hz
	27MHz @1kHz offset		-125		dBc/Hz
	27MHz @10kHz offset		-142		dBc/Hz
	27MHz @100kHz offset		-150		dBc/Hz
	27MHz @1MHz offset		-150		dBc/Hz

5. DC Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic	I_{DD}	27MHz, 15pF Load, 3.3V		3.7	5	mA
		27MHz, 15pF Load, 2.5V		2.4	3.5	
Supply Current, Output Disabled	I_{DD_OE}	27MHz, 3.3V, OE=Low		1.4		mA
		27MHz, 2.5V, OE=Low		1		
Operating Voltage	V_{DD}		2.25		3.63	V
Output Low Voltage,CMOS	V_{OLC}	I_{OL} = +4mA			0.4	V
Output High Voltage, CMOS	V_{OHC}	I_{OH} = -4mA	V_{DD} – 0.4			V
Output Drive Current		For V_{OL}<0.4V or V_{OH}>2.4V	8	9.5		mA
VCXO Control Voltage	VCON		0		V_{DD}	V

6. Crystal Specifications

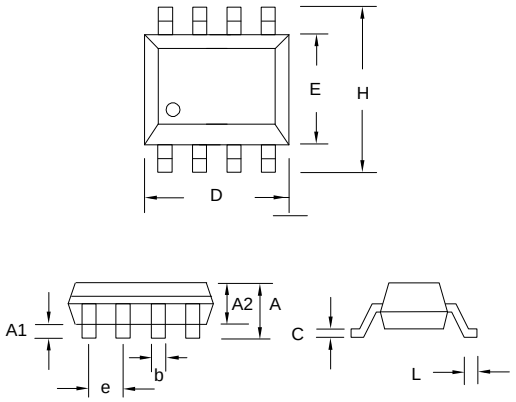
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Crystal Loading Rating (VCON = 1.65V, 3.3V Operation)	$C_{L\ (xtal)}$ (see note below)		7.8		pF
Crystal Loading Rating (VCON = 1.25V, 2.5V Operation)			8.9		
Maximum Sustainable Drive Level				200	µW
Operating Drive Level			50		µW
Max C0				5	pF
C0/C1				250	-
ESR	R_S			30	Ω

Note: The crystal must be such that it oscillates (parallel resonant) at nominal frequency when presented a C Load as specified above. If the crystal requires more load to be at nominal frequency, the additional load must be added externally. This however may reduce the pull range. Note that the Cload values above are for the IC only, and do not include PCB parasitics. Crystal specifications for Cload include PCB parasiti cs.

PACKAGE INFORMATION (GREEN PACKAGE COMPLIANT)

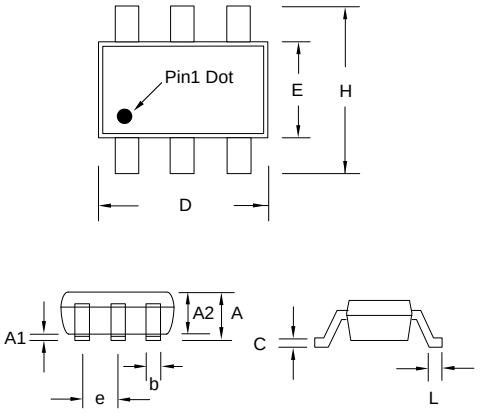
SOP-8L

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	



SOT23-6 L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.0
L	0.35	0.55
e	0.95 BSC	



ORDERING INFORMATION (GREEN PACKAGE)

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL500-17 X X - X

Part Number

Package Type
D=Die
W=Wafer
S=SOP-8L
T=SOT23-

Temperature Range
C=Commercial (0°C to 70°C)
I=Industrial (-40°C to

Shipping Option
Blank=Tube
R=Tape & Reel

Part / Order Number	Marking*	Package Option
PL500-17DC	N/A	Die (Waffle Pack)
PL500-17WC	N/A	WAFER
PL500-17SC	P500-17 SC LLLLL	8-Pin SOP (Tube)
PL500-17SC-R		8-Pin SOP (Tape and Reel)
PL500-17TC-R	B17 LLL	6-Pin SOT23 (Tape and Reel)

*Note: LLL and LLLLL represent the production lot number

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