THE DATASHEET OF

CY23EP05SXI-1HT

CY23EP05

2.5 V or 3.3 V,10–220 MHz, Low Jitter, 5 Output Zero Delay Buffer

Features

- 10 MHz to 220 MHz maximum operating range
- Zero input-output propagation delay, adjustable by loading on CLKOUT pin
- Multiple low-skew outputs
  - 30 ps typical output-output skew
  - One input drives five outputs
- 22 ps typical cycle-to-cycle jitter
- 13 ps typical period jitter
- Standard and high drive strength options
- Available in space-saving 150-mil SOIC package
- 3.3 V or 2.5 V operation
- Industrial temperature available

Functional Description

The CY23EP05 is a 2.5 V or 3.3 V zero delay buffer designed to distribute low-jitter high-speed clocks and is available in a 8-pin SOIC package. It accepts one reference input, and drives out five low-skew clocks. The -1H version operates up to 220 (200) MHz frequencies at 3.3 V (2.5 V), and has a higher drive strength than the -1 devices. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

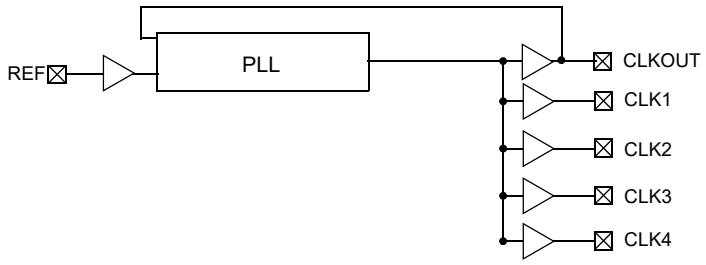
The CY23EP05 PLL enters a power-down mode when there are no rising edges on the REF input (< ~2 MHz). In this state, the outputs are three-stated and the PLL is turned off, resulting in less than 25 μA of current draw.

The CY23EP05 is available in different configurations, as shown in the Ordering Information table. The CY23EP05-1 is the base part. The CY23EP05-1H is the high-drive version of the -1, and its rise and fall times are much faster than the -1.

These parts are not intended for 5 V input-tolerant applications.

For a complete list of related documentation, click here.

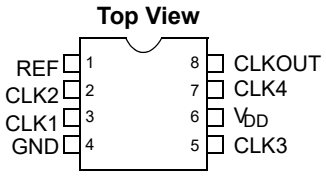
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 8-pin SOIC pinout (Top View)



Pin Description

Pin No.	Signal	Description
1	REF [1]	Input reference frequency
2	CLK2 [2]	Buffered clock output
3	CLK1 [2]	Buffered clock output
4	GND	Ground
5	CLK3 [2]	Buffered clock output
6	V_{DD}	3.3 V or 2.5 V supply
7	CLK4 [2]	Buffered clock output
8	CLKOUT [2, 3]	Buffered clock output, internal feedback on this pin

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve zero delay between the input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay.

The output driving the CLKOUT pin will be driving a total load of 5 pF (internal load) plus any additional load externally connected to this pin. For applications requiring zero input-output delay, the total load on each output pin (including CLKOUT) must be the same. For example, if there is no external load on the CLKOUT pin, add 5 pF to each of the remaining outputs to match the internal load on the CLKOUT pin. If input-output delay adjustments are required, the CLKOUT load may be changed to vary the delay between the REF input and remaining outputs.

For zero output-output skew, be sure to load all outputs equally. For further information refer to the application note titled “AN1234 - Understanding Cypress’s Zero Delay Buffers”.

Notes
1. Weak pull-down.
2. Weak pull-down on all outputs.
3. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Supply voltage to ground potential .....–0.5 V to 4.6 V

DC input voltage .....V_{SS} – 0.5 V to 4.6 V

Storage temperature ..... –65 °C to 150 °C

Junction temperature ..... 150 °C

Static discharge voltage
(per MIL-STD-883, Method 3015 ..... > 2000 V

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
$V_{DD3.3}$	3.3 V supply voltage	3.0	3.3	3.6	V
$V_{DD2.5}$	2.5 V supply voltage	2.3	2.5	2.7	V
T_A	Operating temperature (ambient temperature) – Commercial	0	–	70	°C
	Operating temperature (ambient temperature) – Industrial	–40	–	85	°C
C_L [4]	Load capacitance, < 100 MHz, 3.3 V	–	–	30	pF
	Load capacitance, < 100 MHz, 2.5 V with high drive	–	–	30	pF
	Load capacitance, < 133.3 MHz, 3.3 V	–	–	22	pF
	Load capacitance, < 133.3 MHz, 2.5 V with high drive	–	–	22	pF
	Load capacitance, < 133.3 MHz, 2.5 V with standard drive	–	–	15	pF
	Load capacitance, > 133.3 MHz, 3.3 V	–	–	15	pF
	Load capacitance, > 133.3 MHz, 2.5 V with high drive	–	–	15	pF
C_{IN}	Input capacitance [5]	–	–	5	pF
BW	Closed-loop bandwidth, 3.3 V	–	1–1.5	–	MHz
	Closed-loop bandwidth, 2.5 V	–	0.8	–	MHz
R_{OUT}	Output impedance, 3.3 V high drive	–	29	–	Ω
	Output impedance, 3.3 V standard drive	–	41	–	Ω
	Output impedance, 2.5 V high drive	–	37	–	Ω
	Output Impedance, 2.5 V standard drive	–	41	–	Ω
t_{PU}	Power-up time for all V_{DDs} to reach minimum specified voltage (power ramps must be monotonic)	0.01	–	50	ms

Notes
4. Applies to Test Circuit #1.
5. Applies to both REF Clock and internal feedback path on CLKOUT.

Electrical Specifications (3.3 V DC)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		3.0	3.3	3.6	V
V_{IL}	Input LOW voltage		–	–	0.8	V
V_{IH}	Input HIGH voltage		2.0	–	V_{DD} + 0.3	V
I_{IL}	Input leakage current	$0 < V_{IN} < V_{IL}$	–10	–	10	µA
I_{IH}	Input HIGH current	$V_{IN} = V_{DD}$	–	–	100	µA
V_{OL}	Output LOW voltage	I_{OL} = 8 mA (Standard Drive)	–	–	0.4	V
		I_{OL} = 12 mA (High Drive)	–	–	0.4	V
V_{OH}	Output HIGH voltage	I_{OH} = –8 mA (Standard Drive)	2.4	–	–	V
		I_{OH} = –12 mA (High Drive)	2.4	–	–	V
I_{DD} (PD mode)	Power down supply current	REF = 0 MHz (Commercial)	–	–	12	µA
		REF = 0 MHz (Industrial)	–	–	25	µA
I_{DD}	Supply current	Unloaded outputs, 66 MHz REF	–	–	30	mA

Electrical Specifications (2.5 V DC)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		2.3	2.5	2.7	V
V_{IL}	Input LOW voltage		–	–	0.7	V
V_{IH}	Input HIGH voltage		1.7	–	V_{DD} + 0.3	V
I_{IL}	Input leakage current	$0 < V_{IN} < V_{DD}$	–10	–	10	µA
I_{IH}	Input HIGH current	$V_{IN} = V_{DD}$	–	–	100	µA
V_{OL}	Output LOW voltage	I_{OL} = 8 mA (standard drive)	–	–	0.5	V
		I_{OL} = 12 mA (high drive)	–	–	0.5	V
V_{OH}	Output HIGH voltage	I_{OH} = –8 mA (standard drive)	V_{DD} – 0.6	–	–	V
		I_{OH} = –12 mA (high drive)	V_{DD} – 0.6	–	–	V
I_{DD} (PD mode)	Power Down supply current	REF = 0 MHz (commercial)	–	–	12	µA
		REF = 0 MHz (industrial)	–	–	25	µA
I_{DD}	Supply current	Unloaded outputs, 66 MHz REF	–	–	45	mA

Thermal Resistance

Parameter [6]	Description	Test Conditions	8-pin SOIC	Unit
Theta J_A	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	145	°C/W
Theta J_C	Thermal resistance (junction to case)		62	°C/W

Note
6. These parameters are guaranteed by design and are not tested.

Electrical Specifications (3.3 V and 2.5 V AC)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
$1/t_1$	Maximum frequency [7] (input/output)	3.3 V high drive	10	–	220	MHz
		3.3 V standard drive	10	–	167	MHz
		2.5 V high drive	10	–	200	MHz
		2.5 V standard drive	10	–	133	MHz
T_{IDC}	Input duty cycle	< 133.3 MHz	25	–	75	%
		> 133.3 MHz	40	–	60	%
$t_2 \div t_1$	Output duty cycle [8]	< 133.3 MHz	47	–	53	%
		> 133.3 MHz	45	–	55	%
t_3, t_4	Rise, fall time (3.3 V) [8]	Std drive, CL = 30 pF, < 100 MHz	–	–	1.6	ns
		Std drive, CL = 22 pF, < 133.3 MHz	–	–	1.6	ns
		Std drive, CL = 15 pF, < 167 MHz	–	–	0.6	ns
		High drive, CL = 30 pF, < 100 MHz	–	–	1.2	ns
		High drive, CL = 22 pF, < 133.3 MHz	–	–	1.2	ns
		High drive, CL = 15 pF, > 133.3 MHz	–	–	0.5	ns
t_3, t_4	Rise, fall time (2.5 V)[8]	Std drive, CL = 15 pF, < 133.33 MHz	–	–	1.5	ns
		High drive, CL = 30 pF, < 100 MHz	–	–	2.1	ns
		High drive, CL = 22 pF, < 133.3 MHz	–	–	1.3	ns
		High drive, CL = 15 pF, > 133.3 MHz	–	–	1.2	ns
t_5	Output to output skew [8]	All outputs equally loaded	–	30	100	ps
t_6	Delay, REF rising edge to CLKOUT rising edge [8]	PLL enabled at 3.3 V	–100	–	100	ps
		PLL enabled at 2.5 V	–200	–	200	ps
t_7	Part to part skew [8]	Measured at $V_{DD}/2$. Any output to any output, 3.3 V supply	–150	–	150	ps
		Measured at $V_{DD}/2$. Any output to any output, 2.5 V supply	–300	–	300	ps

Notes
7. For the given maximum loading conditions. See C_L in Operating Conditions Table.
8. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Specifications (3.3 V and 2.5 V AC) (continued)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_{LOCK}	PLL lock time [9]	Stable power supply, valid clocks presented on REF and CLKOUT pins	–	–	1.0	ms
T_{JCC} [9, 10]	Cycle-to-cycle jitter, peak	3.3 V supply, > 66 MHz, < 15 pF	–	22	55	ps
		3.3 V supply, > 66 MHz, < 30 pF, standard drive	–	45	125	ps
		3.3 V supply, > 66 MHz, < 30 pF, high drive	–	45	100	ps
		2.5 V supply, > 66 MHz, < 15 pF, standard drive	–	40	100	ps
		2.5 V supply, > 66 MHz, < 15 pF, high drive	–	35	80	ps
		2.5 V supply, > 66 MHz, < 30 pF, high drive	–	52	125	ps
T_{PER} [9, 10]	Period jitter, peak	3.3 V supply, 66–100 MHz, < 15 pF	–	18	60	ps
		3.3 V supply, > 100 MHz, < 15 pF	–	13	35	ps
		3.3 V supply, > 66 MHz, < 30 pF, standard drive	–	28	75	ps
		3.3 V supply, > 66 MHz, < 30 pF, high drive	–	26	70	ps
		2.5 V supply, > 66 MHz, < 15 pF, standard drive	–	25	60	ps
		2.5 V supply, 66–100 MHz, < 15 pF, high drive	–	22	60	ps
		2.5 V supply, > 100 MHz, < 15 pF, high drive	–	19	45	ps

Notes
9. Parameter is guaranteed by design and characterization. Not 100% tested in production.
10. Typical jitter is measured at 3.3 V or 2.5 V, 29°C, with all outputs driven into the maximum specified load. Further information regarding jitter specifications may be found in the application notes, “Understanding Data Sheet Jitter Specifications for Cypress Products.”

Switching Waveforms

Figure 2. Duty Cycle Timing

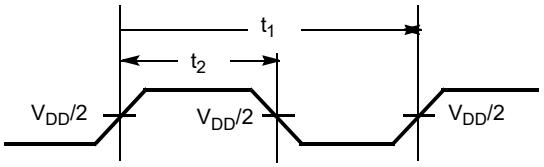


Figure 3. All Outputs Rise/Fall Time

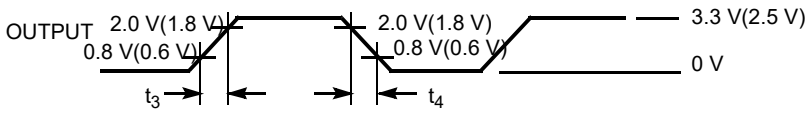


Figure 4. Output-Output Skew

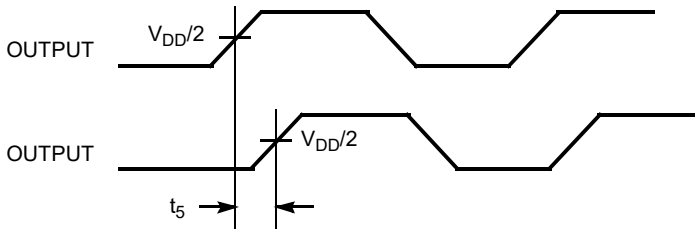


Figure 5. Input-Output Propagation Delay

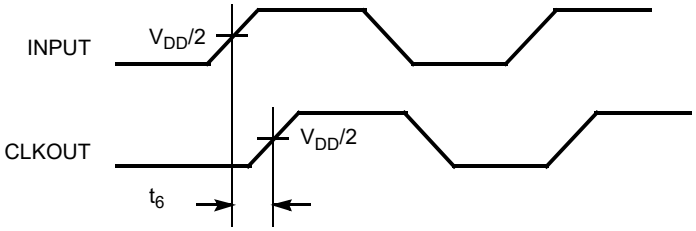
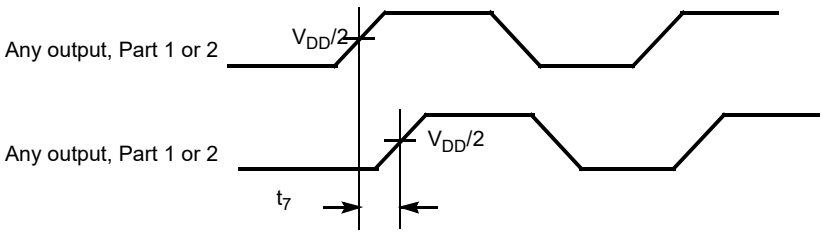
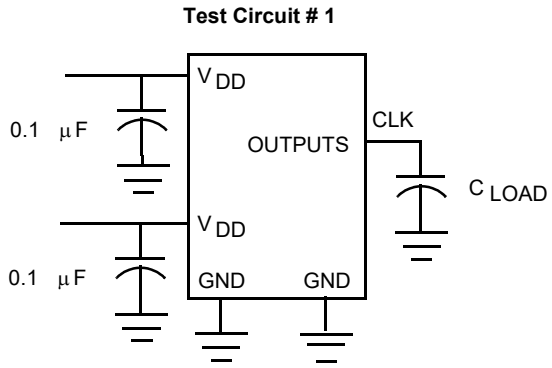


Figure 6. Part-Part Skew



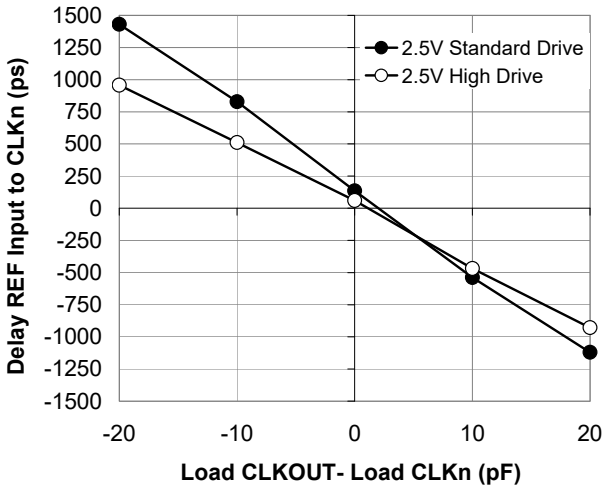
Test Circuits

Figure 7. Test Circuit



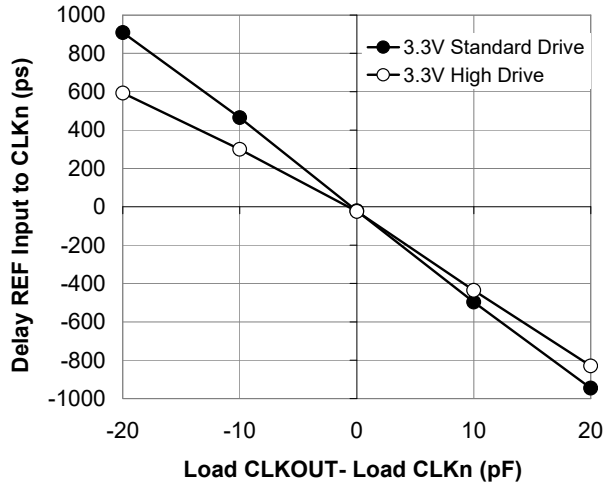
Supplemental Parametric Information

Figure 8. 2.5 V Typical Room Temperature Graph for REF Input to CLKn Delay versus Loading Difference between CLKOUT and CLKn



Data is shown for 66 MHz. Delay is a weak function of frequency.

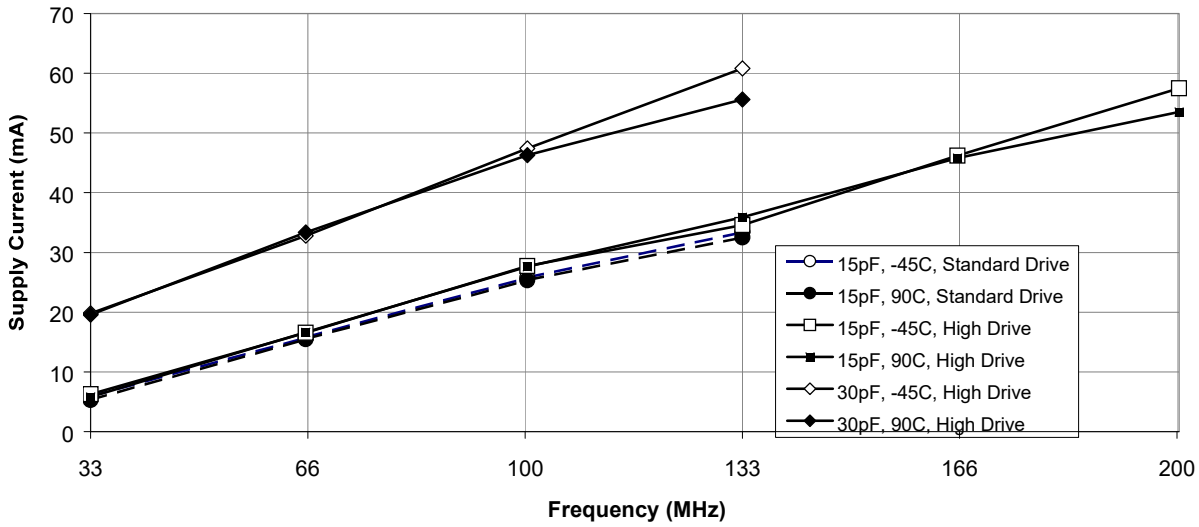
Figure 9. 3.3 V Typical Room Temperature Graph for REF Input to CLKn Delay versus Loading Difference between CLKOUT and CLKn



Data is shown for 66 MHz. Delay is a weak function of frequency.

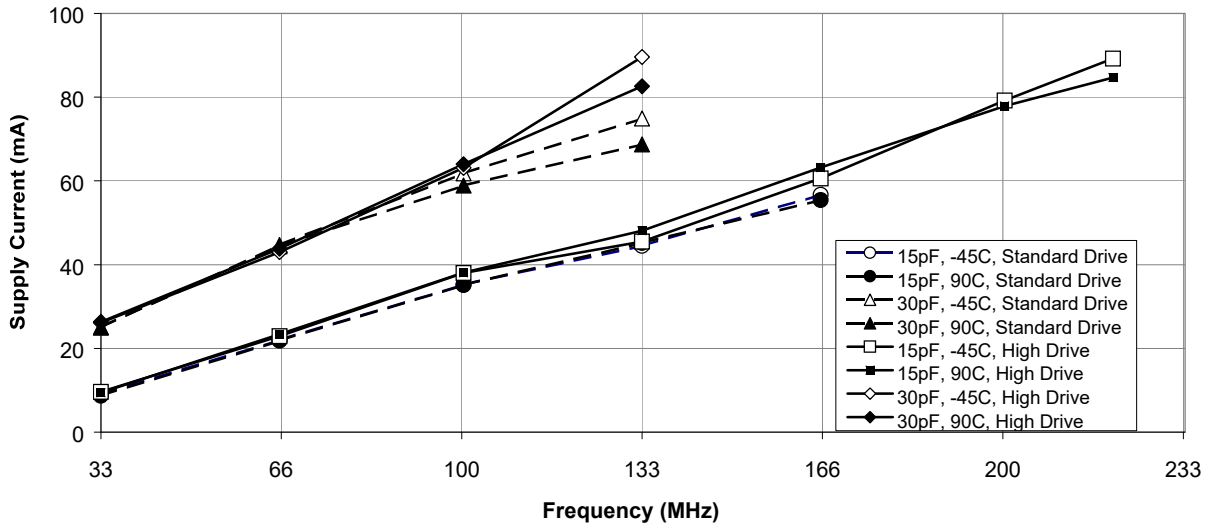
Supplemental Parametric Information (continued)

Figure 10. 2.7 V Measured Supply Current versus Frequency, Drive Strength, Loading, and Temperature



Note that the 30 pF data above 100 MHz is beyond the data sheet specification of 22 pF.

Figure 11. 3.6 V Measured Supply Current versus Frequency, Drive Strength, Loading, and Temperature



Note that the 30-pF high-drive data above 100 MHz is beyond the data sheet specification of 22 pF.

Supplemental Parametric Information (continued)

Figure 12. Typical 3.3 V Measured Cycle-to-cycle Jitter at 29 °C, versus Frequency, Drive Strength, and Loading

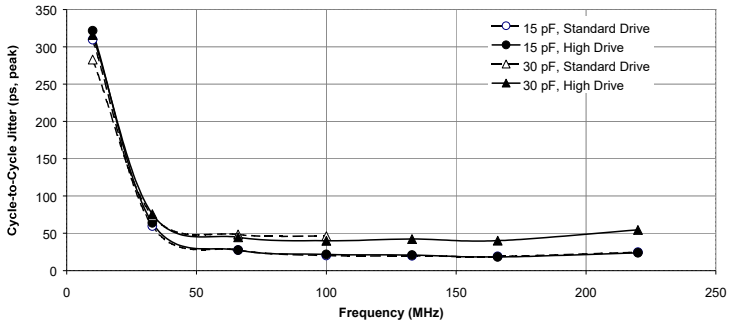


Figure 13. Typical 2.5 V Measured Cycle-to-cycle Jitter at 29 °C, versus Frequency, Drive Strength, and Loading

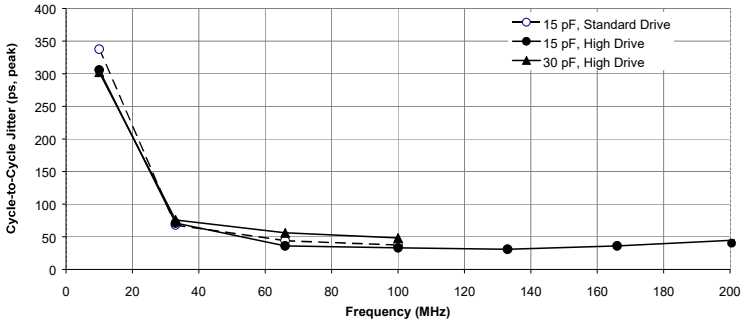


Figure 14. Typical 3.3 V Measured Period Jitter at 29 °C, versus Frequency, Drive Strength, and Loading

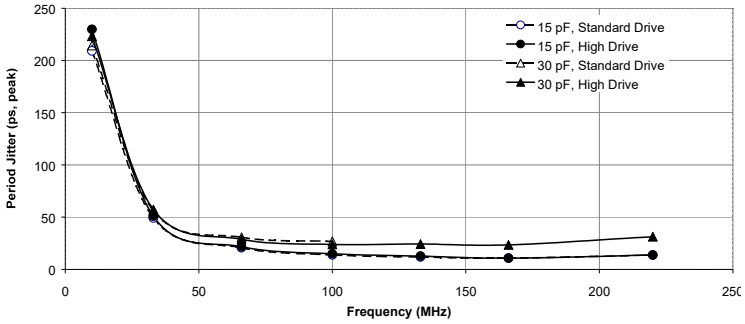
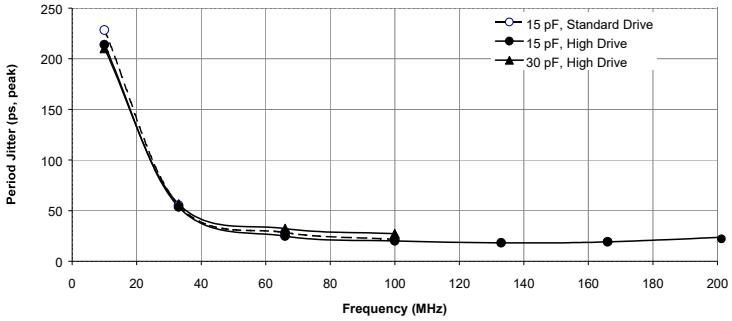
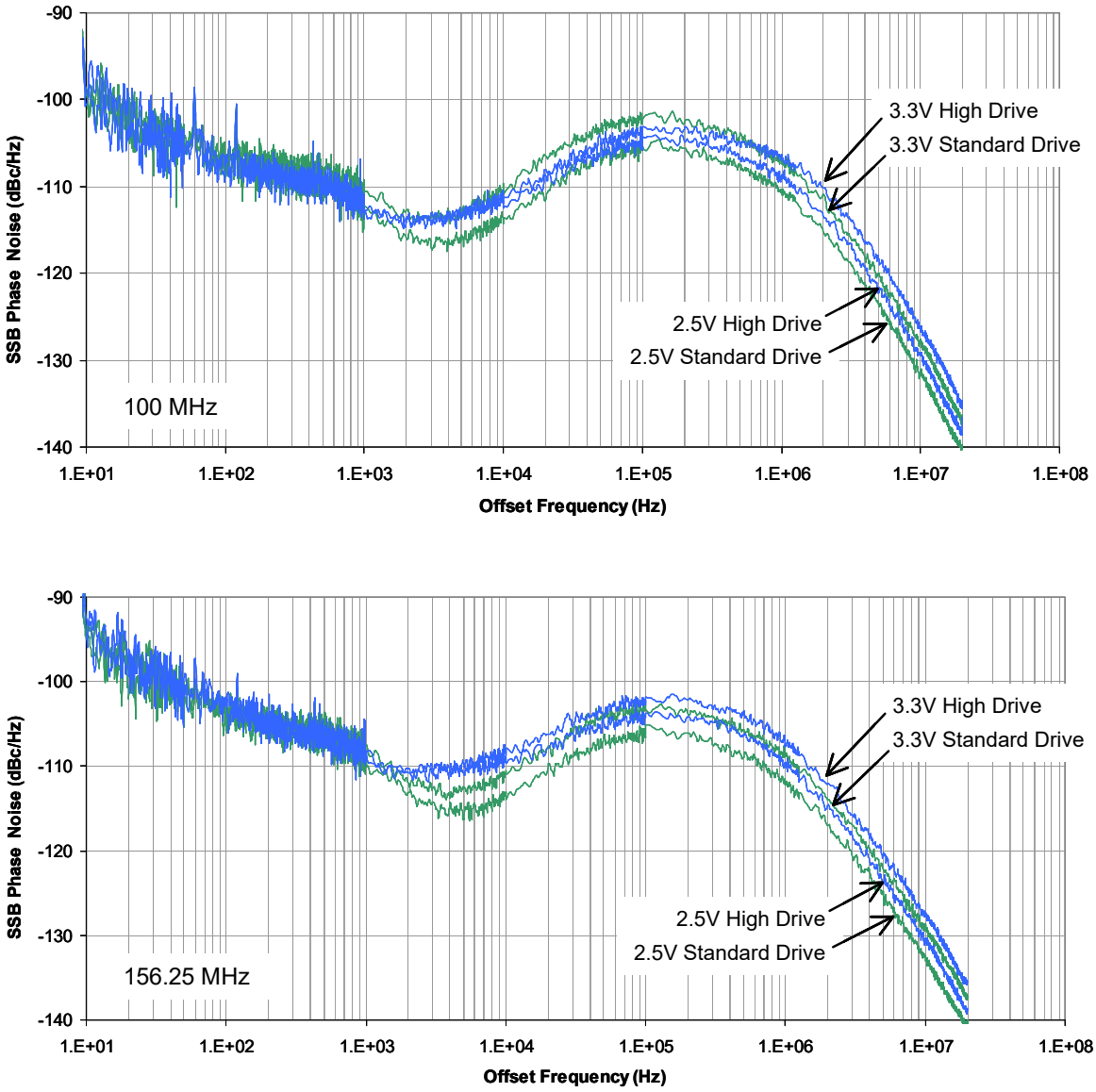


Figure 15. Typical 2.5 V Measured Period Jitter at 29 °C, versus Frequency, Drive Strength, and Loading



Supplemental Parametric Information (continued)

Figure 16. 100 MHz (top) and 156.25 MHz (bottom) Typical Phase-noise Data versus V_{DD} and Drive Strength [11]



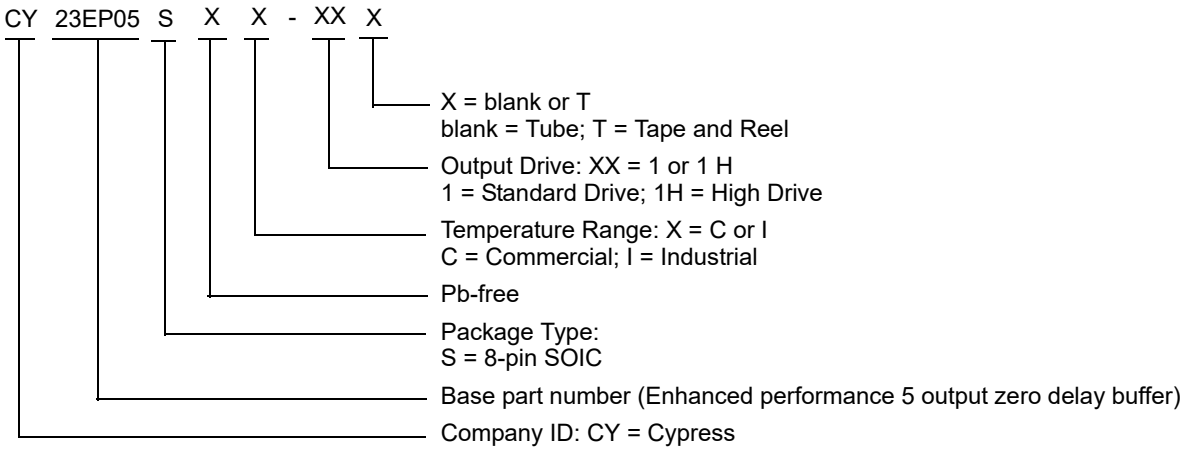
Note

11. Typical jitter is measured at 3.3 V or 2.5 V, 29°C, with all outputs driven into the maximum specified load. Further information regarding jitter specifications may be found in the application notes, “Understanding Data Sheet Jitter Specifications for Cypress Products.”

Ordering Information

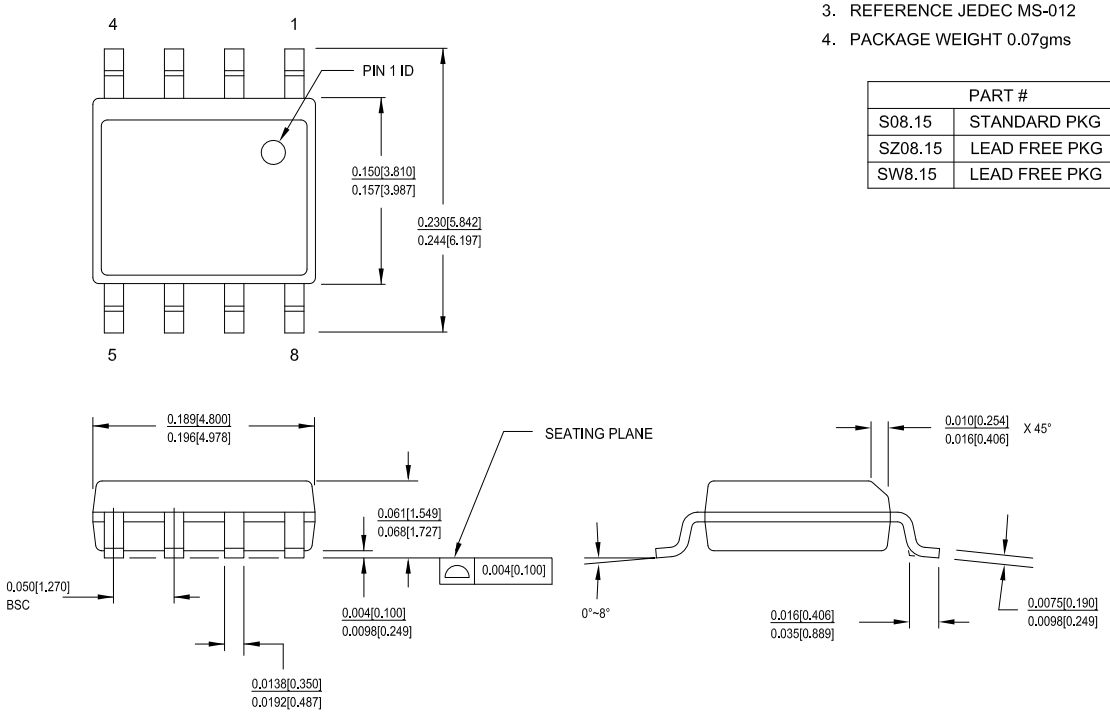
Ordering Code	Package Type	Operating Range
Pb-free		
CY23EP05SXC-1	8-pin SOIC	Commercial
CY23EP05SXC-1T	8-pin SOIC – Tape and Reel	Commercial
CY23EP05SXI-1	8-pin SOIC	Industrial
CY23EP05SXI-1T	8-pin SOIC – Tape and Reel	Industrial
CY23EP05SXC-1H	8-pin SOIC	Commercial
CY23EP05SXC-1HT	8-pin SOIC – Tape and Reel	Commercial
CY23EP05SXI-1H	8-pin SOIC	Industrial
CY23EP05SXI-1HT	8-pin SOIC – Tape and Reel	Industrial

Ordering Code Definitions



Package Drawing and Dimensions

Figure 17. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066



1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG

51-85066 *I

Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
AC	Alternating Current
DC	Direct Current
PCI	Peripheral Component Interconnect
PLL	Phase-Locked Loop
SDRAM	Synchronous Dynamic Random Access Memory
SOIC	Small-Outline Integrated Circuit

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
dBc	decibels relative to carrier
°C	degree Celsius
Hz	hertz
MHz	megahertz
µA	microampere
mA	milliampere
W	ohm
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY23EP05, 2.5 V or 3.3 V,10–220 MHz, Low Jitter, 5 Output Zero Delay Buffer Document Number: 38-07759				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	349620	RGL	04/14/2005	New data sheet.
*A	401073	RGL	10/10/2005	Updated Supplemental Parametric Information: Updated Figure 8. Updated Figure 9. Added Figure 16.
*B	413826	RGL	12/13/2005	Minor Change: Updated Ordering Information: Fixed typo (Replaced CY23EP05SXC-T with CY23EP05SXC-1T).
*C	3273677	CXQ	06/07/2011	Updated Operating Conditions: Added a column “Typ”. Added typical values of $V_{DD3.3}$ and $V_{DD2.5}$ parameters. Moved all values of BW, R_{OUT}, Theta J_A, and Theta J_C parameters to “Typ” column and added dashes in “Min” and “Max” columns. Removed “(typical)” in “Description” column for BW, and R_{OUT} parameters. “Typ” column is left blank with a dash for all other parameters. Updated Electrical Specifications (3.3 V DC): Added typical value of V_{DD} parameter. Changed minimum value of I_{IL} parameter from “–” to –10 µA. Changed maximum value of I_{IL} parameter from $\pm$10 µA to 10 µA. “Typ” column is left blank with a dash for all other parameters. Updated Electrical Specifications (2.5 V DC): Added typical value of V_{DD} parameter. Changed minimum value of I_{IL} parameter from “–” to –10 µA. Changed maximum value of I_{IL} parameter from $\pm$10 µA to 10 µA. “Typ” column is left blank with a dash for all other parameters. Updated Electrical Specifications (3.3 V and 2.5 V AC): Changed minimum value of t_7 parameter from “–” to –150 ps corresponding to “3.3V supply”. Changed maximum value of t_7 parameter from $\pm$150 ps to 150 ps corresponding to “3.3V supply”. Changed minimum value of t_7 parameter from “–” to –300 ps corresponding to “2.5V supply”. Changed maximum value of t_7 parameter from $\pm$300 ps to 300 ps corresponding to “2.5V supply”. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *C to *D. Added Acronyms, and Units of Measure. Updated to new template. Completing Sunset Review.
*D	4402737	AJU	06/09/2014	Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *D to *F. Updated to new template. Completing Sunset Review.
*E	4578443	AJU	11/25/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.

Document History Page (continued)

Document Title: CY23EP05, 2.5 V or 3.3 V,10–220 MHz, Low Jitter, 5 Output Zero Delay Buffer Document Number: 38-07759				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F	5260402	PSR	05/05/2016	Updated Zero Delay and Skew Control: Updated description. Added Thermal Resistance. Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *F to *H. Updated to new template. Completing Sunset Review.
*G	6063917	RMES	02/08/2018	Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *H to *I. Updated to new template.

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