

## 3.3V Dual Differential LVPECL-to-LVTTL Translator

### Features

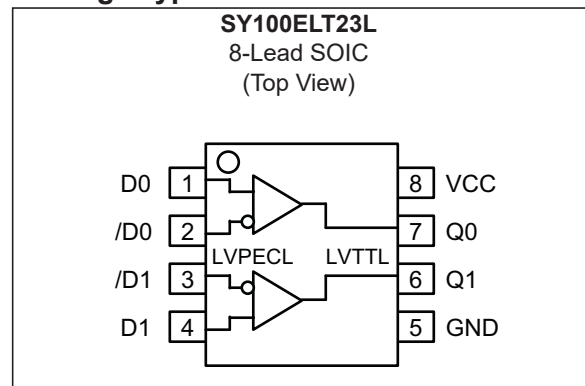
- 3.3V Power Supply
- 2.0 ns Typical Propagation Delay
- <300 ps Typical Within-Device Skew
- Differential LVPECL Inputs
- 24 mA LVTTL Outputs
- Flow-Through Pinouts
- Available in 8-Lead SOIC Package

### General Description

The SY100ELT23L is a dual differential LVPECL-to-LVTTL translator with +3.3V power supply. Because LVPECL (low voltage positive ECL) levels are used, only +3.3V and ground are required. The small outline 8-lead SOIC package and low skew, dual gate design make the ELT23L ideal for applications that require the translation of a clock or data signal.

The ELT23L is compatible with positive ECL 100K logic levels.

### Package Type



# SY100ELT23L

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

|   |       |                                |
|---|-------|--------------------------------|
| Power Supply Voltage ( $V_{CC}$ )                     | ..... | -0.5V to +3.8V                 |
| PECL Input Voltage ( $V_{IN}$ )                       | ..... | 0V to $V_{CC}+0.5V$            |
| Voltage Applied to Output at High State ( $V_{OUT}$ ) | ..... | -0.5V to $V_{CC}$              |
| Current Applied to Output at Low State ( $I_{OUT}$ )  | ..... | Twice the Rated $I_{OL}$ in mA |

† **Notice:** Permanent device damage can occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### LVTTTL DC ELECTRICAL CHARACTERISTICS

| Electrical Characteristics: $V_{CC} = +3.3V \pm 5\%$ ; Values valid from $-40^{\circ}C$ to $+85^{\circ}C$ unless otherwise noted. |          |      |      |      |       |                    |
|---|----------|------|------|------|-------|--------------------|
| Parameter   | Symbol   | Min. | Typ. | Max. | Units | Conditions         |
| Power Supply Current  | $I_{CC}$ | —    | —    | 30   | mA    | —                  |
| Output High Voltage   | $V_{OH}$ | 2.0  | —    | —    | V     | $I_{OH} = -3.0$ mA |
| Output Low Voltage  | $V_{OL}$ | —    | —    | 0.5  | V     | $I_{OL} = 24$ mA   |
| Output Short Circuit Current  | $I_{OS}$ | -240 | —    | -80  | mA    | $V_{OUT} = 0V$     |

### LVPECL DC ELECTRICAL CHARACTERISTICS

| Electrical Characteristics: $V_{CC} = +3.3V \pm 5\%$ ; Values valid from $-40^{\circ}C$ to $+85^{\circ}C$ unless otherwise noted. |           |      |      |          |         |            |
|---|-----------|------|------|----------|---------|------------|
| Parameter   | Symbol    | Min. | Typ. | Max.     | Units   | Conditions |
| Input High Current  | $I_{IH}$  | —    | —    | 150      | $\mu A$ | —          |
| Input Low Current   | $I_{IL}$  | 0.5  | —    | —        | $\mu A$ | —          |
| Common Mode Range   | $V_{CMR}$ | 1.5  | —    | $V_{CC}$ | V       | —          |
| Input High Voltage  | $V_{IH}$  | 2135 | —    | 2420     | mV      | Note 1     |
| Input Low Voltage   | $V_{IL}$  | 1490 | —    | 1825     | mV      | Note 1     |

**Note 1:** These values are for  $V_{CC} = 3.3V$ . Level specifications will vary 1:1  $V_{CC}$ .

## AC ELECTRICAL CHARACTERISTICS

| Electrical Characteristics: $V_{CC} = +3.3V \pm 5\%$ ; Values valid from $-40^{\circ}C$ to $+85^{\circ}C$ unless otherwise noted. |              |      |      |      |       |  |
|---|--------------|------|------|------|-------|--|
| Parameter   | Symbol       | Min. | Typ. | Max. | Units | Condition  |
| Maximum Input Frequency   | $f_{MAX}$    | 160  | —    | —    | MHz   | $C_L = 20$ pF, <a href="#">Note 1</a> , <a href="#">Note 2</a> |
| Propagation Delay   | $t_{PD}$     | 1.5  | 2.0  | 2.5  | ns    | $C_L = 20$ pF  |
| Part-to-Part Skew   | $t_{SKPP}$   | —    | —    | 0.5  | ns    | $C_L = 20$ pF, <a href="#">Note 3</a> , <a href="#">Note 6</a> |
| Within-Device Skew  | $t_{SKEW++}$ | —    | —    | 0.3  | ns    | <a href="#">Note 4</a> , <a href="#">Note 6</a>                |
|   | $t_{SKEW--}$ | —    | —    |      |       | <a href="#">Note 5</a> , <a href="#">Note 6</a>                |
| Input Swing   | $V_{PP}$     | 200  | —    | 1000 | mV    | <a href="#">Note 7</a>   |
| Output Rise/Fall Time (1.0V to 2.0V)  | $t_r/t_f$    | 0.5  | —    | 1.0  | ns    | $C_L = 20$ pF  |

- Note 1:** Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
- Note 2:** The  $f_{MAX}$  value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.
- Note 3:** Part-to-Part skew considering HIGH-to-HIGH transitions at common  $V_{CC}$  level
- Note 4:** Within-Device skew considering HIGH-to-HIGH transitions at common  $V_{CC}$  level.
- Note 5:** Within-Device skew considering LOW-to-LOW transitions at common  $V_{CC}$  level.
- Note 6:** All skew parameters are guaranteed, but not tested.
- Note 7:** Input swing for which AC parameters are guaranteed. 200 mV input guarantees full logic at output.

## TEMPERATURE SPECIFICATIONS

| Parameters                    | Symbol | Min. | Typ. | Max. | Units       | Conditions         |
|-------------------------------|--------|------|------|------|-------------|--------------------|
| <b>Temperature Ranges</b>     |        |      |      |      |             |                    |
| Lead Temperature              | —      | —    | —    | +260 | $^{\circ}C$ | Soldering, 20 sec. |
| Ambient Operating Temperature | $T_A$  | -40  | —    | +85  | $^{\circ}C$ | —                  |
| Storage Temperature           | $T_S$  | -65  | —    | +150 | $^{\circ}C$ | —                  |

## TRUTH TABLE

| D    | /D   | Q |
|------|------|---|
| L    | H    | L |
| H    | L    | H |
| Open | Open | L |

# SY100ELT23L

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## 2.0 PIN DESCRIPTIONS

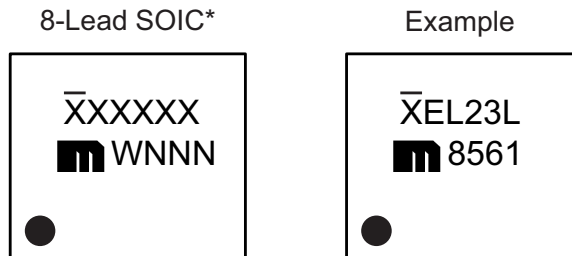
The descriptions of the pins are listed in [Table 2-1](#).

**TABLE 2-1: PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description                 |
|------------|----------|-----------------------------|
| 1, 2       | D0, /D0  | No Connect.                 |
| 4, 3       | D1, /D1  | Differential LVPECL Inputs. |
| 5          | GND      | Ground.                     |
| 7, 6       | Q0, /Q1  | LVTTL Outputs.              |
| 8          | VCC      | +3.3V Supply.               |

## 3.0 PACKAGING INFORMATION

### 3.1 Package Marking Information



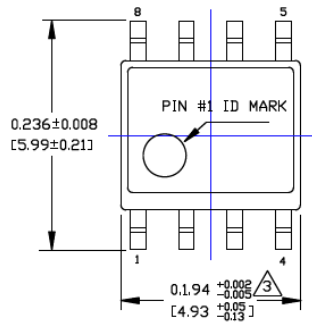
|                |  |  |
|----------------|--|--|
| <b>Legend:</b> | XX...X   | Product code or customer-specific information  |
|                | Y  | Year code (last digit of calendar year)  |
|                | YY   | Year code (last 2 digits of calendar year)   |
|                | WW   | Week code (week of January 1 is week '01')   |
|                | NNN  | Alphanumeric traceability code   |
|                | (e3)   | Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn)   |
|                | *  | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |
|                | •, ▲, ▼  | Pin one index is identified by a dot, delta up, or delta down (triangle mark).                                   |
| <b>Note:</b>   | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. |  |
|                | Underbar ( _ ) and/or Overbar ( ¯ ) symbol may not be to scale.  |  |

# SY100ELT23L

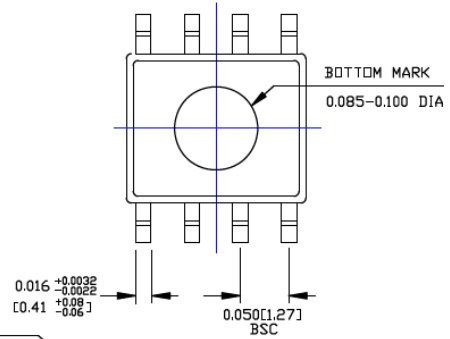
## TITLE

8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

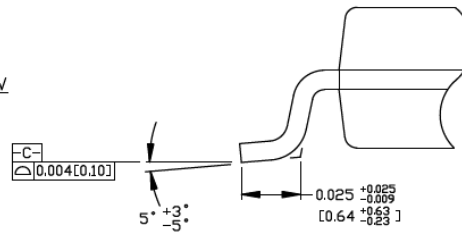
| DRAWING # | SOICN-8LD-PL-1 | UNIT | INCH [MM] |
|-----------|----------------|------|-----------|
|-----------|----------------|------|-----------|



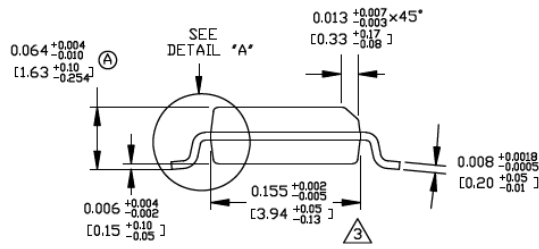
TOP VIEW



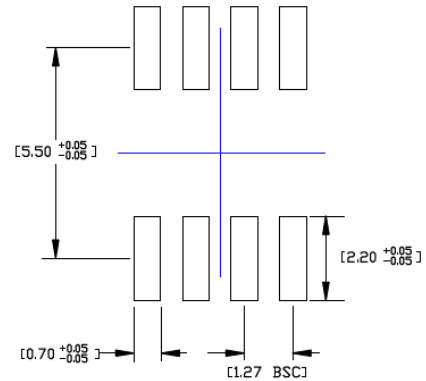
BOTTOM VIEW



DETAIL "A"



END VIEW



RECOMMENDED LAND PATTERN

### NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

## APPENDIX A: REVISION HISTORY

### Revision A (August 2019)

- Converted Micrel document SY100ELT23L to Microchip data sheet DS20006236A.
- Minor text changes throughout.
- Removal of all reference to the discontinued SY10ELT23L.

# SY100ELT23L

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| <u>Part No.</u>           | <u>X</u>   | <u>X</u> | <u>X</u>                          | <u>-XX</u> | <b>Examples:</b>  |
|---------------------------|--|----------|-----------------------------------|------------|---|
| Device                    | Supply Voltage   | Package  | Temp. Range                       | Packing    |   |
| <b>Device:</b>            | SY100ELT23: 3.3V Differential LVPECL-to-LVTTL Translator |          |                                   |            | a) SY100ELT23LZG:<br>SY100ELT23, 3.3V Supply Voltage,<br>8-Lead SOIC, -40°C to +85°C Temperature Range,<br>95/Tube  |
| <b>Supply Voltage:</b>    | L  | =        | 3.3V                              |            | b) SY100ELT23LZG-TR:<br>SY100ELT23, 3.3V Supply Voltage,<br>8-Lead SOIC, -40°C to +85°C Temperature Range,<br>1,000/Reel  |
| <b>Package:</b>           | Z  | =        | 8-Lead SOIC                       |            | <b>Note 1:</b> Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. |
| <b>Temperature Range:</b> | G  | =        | -40°C to +85°C (NiPdAu Lead-Free) |            |   |
| <b>Tape and Reel:</b>     | <blank>  | =        | 95/Tube                           |            |   |
|                           | TR   | =        | 1,000/Reel                        |            |   |

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NOTES:

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