SSTVF16859

13-bit 1 : 2 SSTL_2 registered buffer for DDR

Rev. 02 — 19 July 2005 | Product data sheet

1. General description

The SSTVF16859 is a 13-bit to 26-bit SSTL_2 registered driver with differential clock inputs, designed to operate between 2.3 V and 2.7 V for PC1600-PC2700 applications or between 2.5 V and 2.7 V for PC3200 applications. All inputs are compatible with the JEDEC standard for SSTL_2 with V_{ref} normally at $0.5 \times V_{DD}$, except the LVCMOS reset ($\overline{RESET}$) input. All outputs are SSTL_2, Class II compatible, which can be used for standard stub-series applications or capacitive loads. Master reset ($\overline{RESET}$) asynchronously resets all registers to zero.

The SSTVF16859 is intended to be incorporated into standard DIMM (Dual In-Line Memory Module) designs defined by JEDEC, such as DDR (Double Data Rate) SDRAM and SDRAM II Memory Modules. Different from traditional SDRAM, DDR SDRAM transfers data on both clock edges (rising and falling), thus doubling the peak bus bandwidth. A DDR DRAM rated at 133 MHz will have a burst rate of 266 MHz.

The device data inputs consist of different receivers. One differential input is tied to the input pin while the other is tied to a reference input pad, which is shared by all inputs.

The clock input is fully differential (CK and $\overline{CK}$) to be compatible with DRAM devices that are installed on the DIMM. Data are registered at the crossing of CK going HIGH, and $\overline{CK}$ going LOW. However, since the control inputs to the SDRAM change at only half the data rate, the device must only change state on the positive transition of the CK signal. In order to be able to provide defined outputs from the device even before a stable clock has been supplied, the device has an asynchronous input pin ($\overline{RESET}$), which when held to the LOW state, resets all registers and all outputs to the LOW state.

The device supports low-power standby operation. When $\overline{RESET}$ is LOW, the differential input receivers are disabled, and un-driven (floating) data, clock, and reference voltage (VREF) inputs are allowed. In addition, when $\overline{RESET}$ is LOW, all registers are reset, and all outputs are forced LOW. The LVCMOS $\overline{RESET}$ input must always be held at a valid logic HIGH or LOW level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the LOW state during power-up.

In the DDR DIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CK and $\overline{CK}$. Therefore, no timing relationship can be guaranteed between the two. When entering $\overline{RESET}$, the register will be cleared and the outputs will be driven LOW. As long as the data inputs are LOW, and the clock is stable during the time from the LOW-to-HIGH transition of $\overline{RESET}$ until the input receivers are fully enabled, the outputs will remain LOW.

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2. Features

- Stub-series terminated logic for 2.5 V V_{DD} (SSTL_2)
- Designed for PC1600-PC2700 (at 2.5 V) and PC3200 (at 2.6 V) applications
- Pin and function compatible with JEDEC standard SSTV16859
- Supports SSTL_2 signal inputs as per JESD 8-9
- Flow-through architecture optimizes printed-circuit board layout
- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V to HBM per method A114.
- Latch-up testing is done to JEDEC Standard JESD78, which exceeds 100 mA
- Supports efficient low power standby operation
- Full DDR solution when used with PCKVF857
- Available in TSSOP64, LFBGA96 and HVQFN56 packages

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}/t_{PLH}	propagation delay, CK/$\overline{CK}$ to Qn	C_L = 30 pF; V_{DD} = 2.5 V		-	1.7	-	ns
C_i	input capacitance	V_{DD} = 2.5 V	[1]	-	2.8	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{DD}^2 \times f_i + \Sigma (C_L \times V_{DD}^2 \times f_o)$ where:
f_i = input frequency in MHz;
C_L = output load capacitance in pF;
f_o = output frequency in MHz;
V_{DD} = supply voltage in V;
$\Sigma (C_L \times V_{DD}^2 \times f_o)$ = sum of the outputs.

4. Ordering information

Table 2: Ordering information

T_{amb} = 0 °C to +70 °C

Type number	Package		
	Name	Description	Version
SSTVF16859BS	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm	SOT684-1
SSTVF16859DGG	TSSOP64	plastic thin shrink small outline package; 64 leads; body width 6.1 mm	SOT646-1
SSTVF16859EC	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1

5. Functional diagram

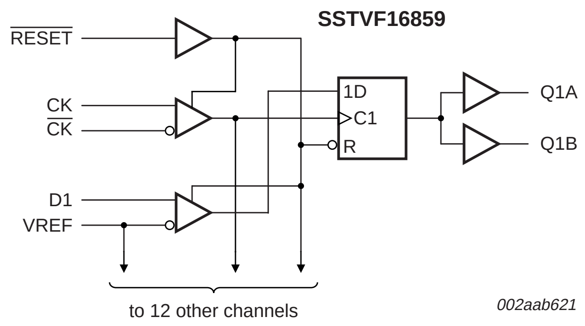

Fig 1. Logic diagram of SSTVF16859

6. Pinning information

6.1 Pinning

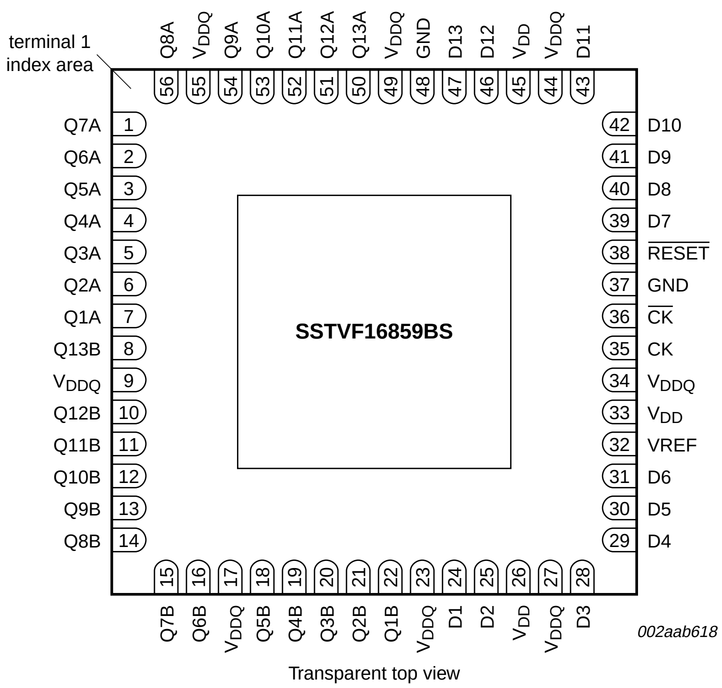

Fig 2. Pin configuration for HVQFN56

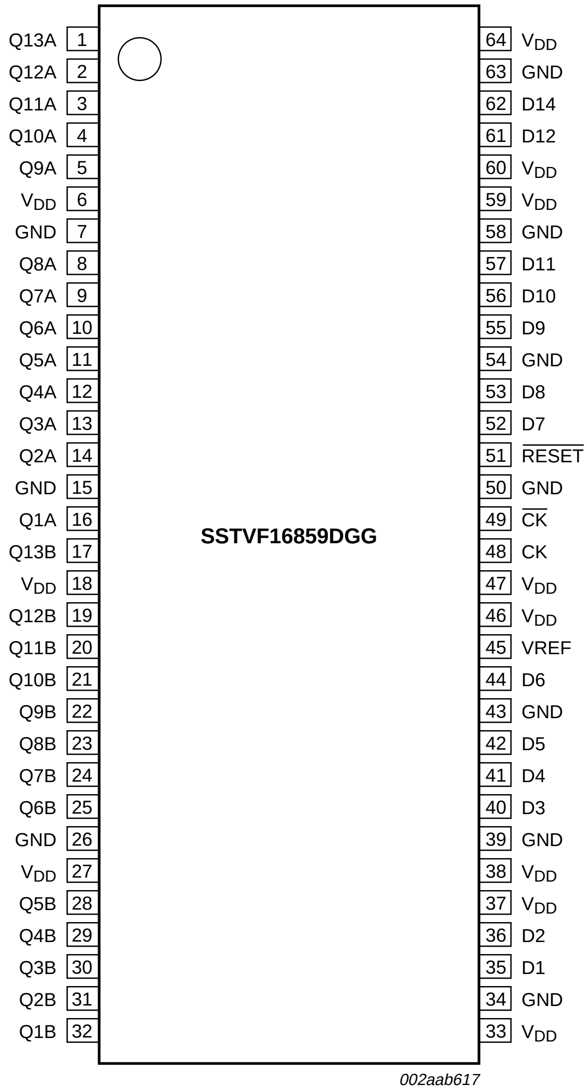

Fig 3. Pin configuration for TSSOP64

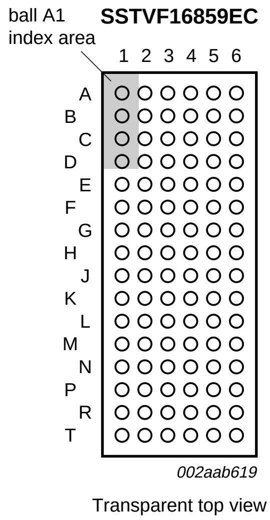

Fig 4. Pin configuration for LFBGA96

	1	2	3	4	5	6
A	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.
B	Q12A	Q13A	GND	GND	n.c.	n.c.
C	Q10A	Q11A	GND	GND	n.c.	n.c.
D	Q8A	Q9A	V_{DDQ}	V_{DDQ}	D13	D12
E	Q6A	Q7A	V_{DDQ}	V_{DDQ}	D11	D10
F	Q4A	Q5A	V_{DDQ}	V_{DDQ}	D9	D8
G	Q2A	Q3A	GND	GND	D7	$\overline{RESET}$
H	Q1A	Q13B	GND	GND	n.c.	$\overline{CK}$
J	Q12B	Q11B	GND	VREF	n.c.	CK
K	Q10B	Q9B	V_{DDQ}	V_{DDQ}	n.c.	n.c.
L	Q8B	Q7B	V_{DDQ}	V_{DDQ}	D5	D6
M	Q6B	Q5B	V_{DDQ}	V_{DDQ}	D3	D4
N	Q4B	Q3B	GND	GND	D1	D2
P	Q2B	Q1B	GND	GND	n.c.	n.c.
R	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.
T	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.

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All V_{DD} and V_{DDQ} are tied internally.

Fig 5. Ball mapping for LFBGA96

6.2 Pin description

Table 3: Pin description

Symbol	Pin			Description
	TSSOP64	HVQFN56	LFBGA96	
Q1A	16	7	H1	data output
Q2A	14	6	G1	
Q3A	13	5	G2	
Q4A	12	4	F1	
Q5A	11	3	F2	
Q6A	10	2	E1	
Q7A	9	1	E2	
Q8A	8	56	D1	
Q9A	5	54	D2	
Q10A	4	53	C1	
Q11A	3	52	C2	
Q12A	2	51	B1	
Q13A	1	50	B2	
Q1B	32	22	P2	data output
Q2B	31	21	P1	
Q3B	30	20	N2	
Q4B	29	19	N1	
Q5B	28	18	M2	
Q6B	25	16	M1	
Q7B	24	15	L2	
Q8B	23	14	L1	
Q9B	22	13	K2	
Q10B	21	12	K1	
Q11B	20	11	J2	
Q12B	19	10	J1	
Q13B	17	8	H2	
V_{DD}	37, 46, 60	26, 33, 45	-	power supply voltage
V_{DDQ}	6, 18, 27, 33, 38, 47, 59, 64	9, 17, 23, 27, 34, 44, 49, 55	D3, D4, E3, E4, F3, F4, K3, K4, L3, L4, M3, M4,	output supply voltage
GND	7, 15, 26, 34, 39, 43, 50, 54, 58, 63	37, 48	B3, B4, C3, C4, G3, G4, H3, H4, J3, N3, N4, P3, P4	ground

Table 3: Pin description *...continued*

Symbol	Pin			Description
	TSSOP64	HVQFN56	LFBGA96	
D1	35	24	N5	Data input. Clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{\text{CK}}$.
D2	36	25	N6	
D3	40	28	M5	
D4	41	29	M6	
D5	42	30	L5	
D6	44	31	L6	
D7	52	39	G5	
D8	53	40	F6	
D9	55	41	F5	
D10	56	42	E6	
D11	57	43	E5	
D12	61	46	D6	
D13	62	47	D5	
VREF	45	32	J4	input reference voltage
CK	48	35	J6	positive master clock input
$\overline{\text{CK}}$	49	36	H6	negative master clock input
$\overline{\text{RESET}}$	51	38	G6	Asynchronous reset input. Resets registers and disables data and clock differential input receivers.
n.c.	-	-	A1, A2, A3, A4, A5, A6, B5, B6, C5, C6, H5, J5, K5, K6, P5, P6, R1, R2, R3, R4, R5, R6, T1, T2, T3, T4, T5, T6	not connected

7. Functional description

Refer to Figure 1 "Logic diagram of SSTVF16859".

7.1 Function table

Table 4: Function selection (each flip-flop)

H = HIGH voltage level; L = LOW voltage level; ↓ = HIGH-to-LOW transition; ↑ = LOW-to-HIGH transition; X = Don't care

Inputs				Output
$\overline{\text{RESET}}$	CK	$\overline{\text{CK}}$	Dn	Qn
H	↑	↓	L	L
H	↑	↓	H	H
H	L or H	L or H	X	Q_0 [1]
L	X or floating	X or floating	X or floating	L

[1] Q_0 is the previous state of output Qn.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+3.6	V
V_I	input voltage		–0.5 [1]	V_{DD} + 0.5 [2]	V
V_O	output voltage		–0.5 [1]	V_{DD} + 0.5 [2]	V
I_{IK}	input clamp current	V_I < 0 V or V_I > V_{DD}	-	±50	mA
I_{OK}	output clamp current	V_O < 0 V or V_O > V_{DD}	-	±50	mA
I_O	continuous output current	V_O = 0 V to V_{DD}	-	±50	mA
I_{CCC}	continuous current through each V_{DD} or GND		-	±100	mA
T_{stg}	storage temperature	[3]	–65	+150	°C

[1] The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

[2] This value is limited to 3.6 V maximum.

[3] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures that are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		V_{DD}	-	2.7	V
V_{ref}	reference voltage (V_{ref} = V_{DD}/2)	PC1600-PC2700	1.15	1.25	1.35	V
		PC3200	1.25	1.3	1.35	V
V_{TT}	termination voltage		V_{ref} – 0.040	V_{ref}	V_{ref} + 0.040	V
V_I	input voltage		0	-	V_{DD}	V
$V_{IH(AC)}$	AC HIGH-level input voltage	data inputs	V_{ref} + 0.310	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage	data inputs	-	-	V_{ref} – 0.310	V
$V_{IH(DC)}$	DC HIGH-level input voltage	data inputs	V_{ref} + 0.150	-	-	V
$V_{IL(DC)}$	DC LOW-level input voltage	data inputs	-	-	V_{ref} – 0.150	V
V_{IH}	HIGH-level input voltage	$\overline{RESET}$	1.7	-	V_{DD}	V
V_{IL}	LOW-level input voltage		0	-	0.7	V
V_{ICR}	common-mode input voltage range	CK, $\overline{CK}$	0.97	-	1.53	V
V_{ID}	differential input voltage	CK, $\overline{CK}$	360	-	-	mV
I_{OH}	HIGH-level output current		-	-	–16	mA
I_{OL}	LOW-level output current		-	-	16	mA
T_{amb}	ambient temperature	operating in free air	0	-	+70	°C

[1] The $\overline{RESET}$ input of the device must be held at V_{DD} or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{RESET}$ is LOW.

10. Static characteristics

Table 7: Static characteristics (PC1600-PC2700)

T_{amb} = 0 °C to +70 °C; over recommended operating conditions; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IK}	input clamping voltage	I_I = –18 mA; V_{DD} = 2.3 V	-	-	–1.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –100 µA; V_{DD} = 2.3 V to 2.7 V	V_{DD} – 0.2	-	-	V
		I_{OH} = –16 mA; V_{DD} = 2.3 V	1.95	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA; V_{DD} = 2.3 V to 2.7 V	-	-	0.2	V
		I_{OL} = 16 mA; V_{DD} = 2.3 V	-	-	0.35	V
I_I	input current (all inputs)	V_I = V_{DD} or GND; V_{DD} = 2.7 V	-	-	±5	µA
I_{DD}	supply current	I_O = 0 mA; V_{DD} = 2.7 V				
		static standby; $\overline{RESET}$ = GND	-	-	0.01	mA
		static operating; $\overline{RESET}$ = V_{DD}; V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$	-	-	45	mA
I_{DDD}	dynamic operating current per MHz, clock only	I_O = 0 mA; V_{DD} = 2.7 V; $\overline{RESET}$ = V_{DD}; V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching 50 % duty cycle	-	15	-	µA
	dynamic operating current per MHz, per each data input	I_O = 0 mA; V_{DD} = 2.7 V; $\overline{RESET}$ = V_{DD}; V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching 50 % duty cycle; one data input switching at half clock frequency, 50 % duty cycle	-	9	-	µA
C_i	input capacitance	data inputs; V_I = V_{ref} ± 310 mV; V_{DD} = 2.5 V	2.5	2.8	3.5	pF
		CK and $\overline{CK}$; V_{ICR} = 1.25 V; $V_{I(p-p)}$ = 360 mV; V_{DD} = 2.5 V	2.5	3.2	3.5	pF
		$\overline{RESET}$; V_I = V_{DD} or GND; V_{DD} = 2.5 V	-	2.4	3.5	pF

Table 8: Static characteristics (PC3200)

At recommended operating conditions; T_{amb} = 0 °C to +70 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IK}	input clamping voltage	I_I = –18 mA; V_{DD} = 2.5 V	-	-	–1.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –100 µA; V_{DD} = 2.5 V to 2.7 V	V_{DD} – 0.2	-	-	V
		I_{OH} = –16 mA; V_{DD} = 2.5 V	1.95	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA; V_{DD} = 2.5 V to 2.7 V	-	-	0.2	V
		I_{OL} = 16 mA; V_{DD} = 2.5 V	-	-	0.35	V
I_I	input current (all inputs)	V_I = V_{DD} or GND; V_{DD} = 2.7 V	-	-	±5	µA
I_{DD}	supply current	I_O = 0 mA; V_{DD} = 2.7 V				
		static standby; $\overline{RESET}$ = GND	-	-	0.01	mA
		static operating; $\overline{RESET}$ = V_{DD}; V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$	-	-	45	mA
I_{DDD}	dynamic operating current per MHz, clock only	I_O = 0 mA; V_{DD} = 2.7 V; $\overline{RESET}$ = V_{DD}; V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching 50 % duty cycle	-	15	-	µA
	dynamic operating current per MHz, per each data input	I_O = 0 mA; V_{DD} = 2.7 V; $\overline{RESET}$ = V_{DD}; V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching 50 % duty cycle; one data input switching at half clock frequency, 50 % duty cycle	-	9	-	µA
C_i	input capacitance, data inputs	V_I = V_{ref} ± 310 mV; V_{DD} = 2.6 V	2.5	2.8	3.5	pF
	input capacitance, CK and $\overline{CK}$	V_{ICR} = 1.25 V; $V_{I(p-p)}$ = 360 mV; V_{DD} = 2.6 V	2.5	3.2	3.5	pF
	input capacitance, $\overline{RESET}$	V_I = V_{DD} or GND; V_{DD} = 2.6 V	-	2.4	3.5	pF

11. Dynamic characteristics

Table 9: Timing requirements (PC1600-PC2700)

At recommended operating conditions; V_{DD} = 2.5 V ± 0.2 V; T_{amb} = 0 °C to +70 °C; unless otherwise specified. See Figure 11.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clock}	clock frequency			-	-	200	MHz
t_W	pulse duration, CK, $\overline{CK}$, HIGH or LOW			2.5	-	-	ns
t_{ACT}	differential inputs active time		[1] [2]	-	-	22	ns
t_{INACT}	differential inputs inactive time		[1] [3]	-	-	22	ns
t_{su}	setup time, fast slew rate	data before CK↑, $\overline{CK}$↓	[4] [6]	0.65	-	-	ns
	setup time, slow slew rate	data before CK↑, $\overline{CK}$↓	[5] [6]	0.75	-	-	ns
t_h	hold time, fast slew rate	data after CK↑, $\overline{CK}$↓	[4] [6]	0.75	-	-	ns
	hold time, slow slew rate	data after CK↑, $\overline{CK}$↓	[5] [6]	0.9	-	-	ns

[1] This parameter is not necessarily production tested.

[2] Data inputs must be below a minimum time to $t_{ACT(max)}$, after $\overline{RESET}$ is taken HIGH.

[3] Data and clock inputs must be held at valid levels (not floating) a minimum time of $t_{INACT(max)}$, after $\overline{RESET}$ is taken LOW.

[4] For data signal input slew rate ≥ 1 V/ns.

[5] For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.

[6] CK, $\overline{CK}$ signals input slew rates are ≥ 1 V/ns.

Table 10: Timing requirements (PC3200)

At recommended operating conditions; V_{DD} = 2.6 V ± 0.1 V; T_{amb} = 0 °C to +70 °C; unless otherwise specified. See Figure 11.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clock}	clock frequency			-	-	210	MHz
t_W	pulse duration, CK, $\overline{CK}$, HIGH or LOW			2.5	-	-	ns
t_{ACT}	differential inputs active time		[1] [2]	-	-	22	ns
t_{INACT}	differential inputs inactive time		[1] [3]	-	-	22	ns
t_{su}	setup time, fast slew rate	data before CK↑, $\overline{CK}$↓	[4] [6]	0.65	-	-	ns
	setup time, slow slew rate	data before CK↑, $\overline{CK}$↓	[5] [6]	0.75	-	-	ns
t_h	hold time, fast slew rate	data after CK↑, $\overline{CK}$↓	[4] [6]	0.65	-	-	ns
	hold time, slow slew rate	data after CK↑, $\overline{CK}$↓	[5] [6]	0.8	-	-	ns

[1] This parameter is not necessarily production tested.

[2] Data inputs must be below a minimum time to $t_{ACT(max)}$, after $\overline{RESET}$ is taken HIGH.

[3] Data and clock inputs must be held at valid levels (not floating) a minimum time of $t_{INACT(max)}$, after $\overline{RESET}$ is taken LOW.

[4] For data signal input slew rate ≥ 1 V/ns.

[5] For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.

[6] CK, $\overline{CK}$ signals input slew rates are ≥ 1 V/ns.

Table 11: Switching characteristics (PC1600-PC2700)

At recommended operating conditions; V_{DD} = 2.5 V ± 0.2 V; T_{amb} = 0 °C to +70 °C; Class I; V_{ref} = V_{TT} = V_{DD} × 0.5 and C_L = 10 pF; unless otherwise specified. See Figure 11.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MAX}	maximum input clock frequency		200	-	-	MHz
t_{PD}	propagation delay	from CK, $\overline{CK}$ to Qn	1.1	-	2.5	ns
t_{PDMSS}	propagation delay, simultaneous switching	from CK, $\overline{CK}$ to Qn	-	-	2.9	ns
t_{PHL}	HIGH-to-LOW transition time	from $\overline{RESET}$ to Qn	1.1	-	5	ns

Table 12: Switching characteristics (PC3200)

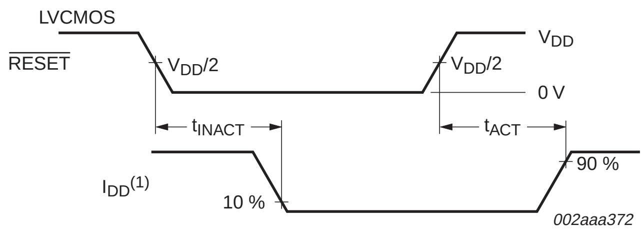
At recommended operating conditions; V_{DD} = 2.6 V ± 0.1 V; T_{amb} = 0 °C to +70 °C; Class I; V_{ref} = V_{TT} = V_{DD} × 0.5 and C_L = 10 pF; unless otherwise specified. See Figure 11.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MAX}	maximum input clock frequency		210	-	-	MHz
t_{PD}	propagation delay	from CK, $\overline{CK}$ to Qn	1.1	-	2.2	ns
t_{PDMSS}	propagation delay, simultaneous switching	from CK, $\overline{CK}$ to Qn	-	-	2.48	ns
t_{PHL}	HIGH-to-LOW transition time	from $\overline{RESET}$ to Qn	1.1	-	5	ns

11.1 AC waveforms

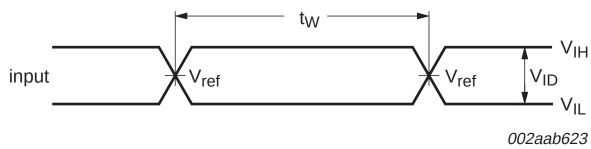
All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20 %; unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.



(1) I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

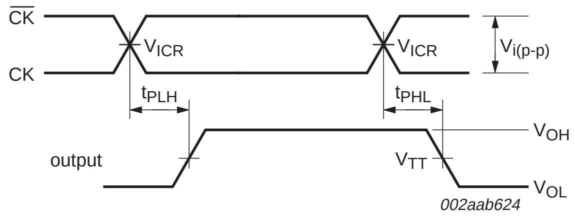
Fig 6. Inputs active and inactive times



V_{IH} = V_{ref} + 310 mV (AC voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS input.

V_{IL} = V_{ref} – 310 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.

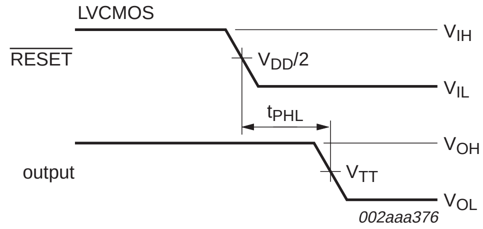
Fig 7. Pulse duration



$V_{TT} = V_{ref} = V_{DD}/2$

t_{PLH} and t_{PHL} are the same as t_{PD}.

Fig 8. Propagation delay times (clock to output)



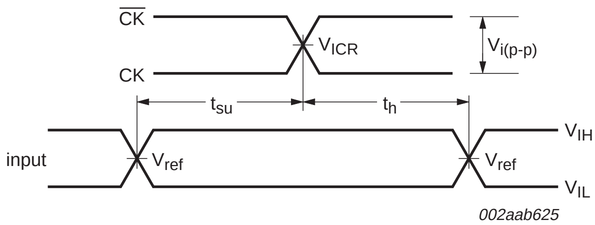
$V_{TT} = V_{ref} = V_{DD}/2$

t_{PLH} and t_{PHL} are the same as t_{PD}.

$V_{IH} = V_{ref}$ + 310 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.

$V_{IL} = V_{ref}$ – 310 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.

Fig 9. Propagation delay times (reset to output)



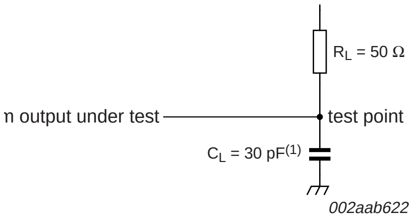
$V_{ref} = V_{DD}/2$

$V_{IH} = V_{ref}$ + 310 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.

$V_{IL} = V_{ref}$ – 310 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.

Fig 10. Setup and hold times

12. Test information

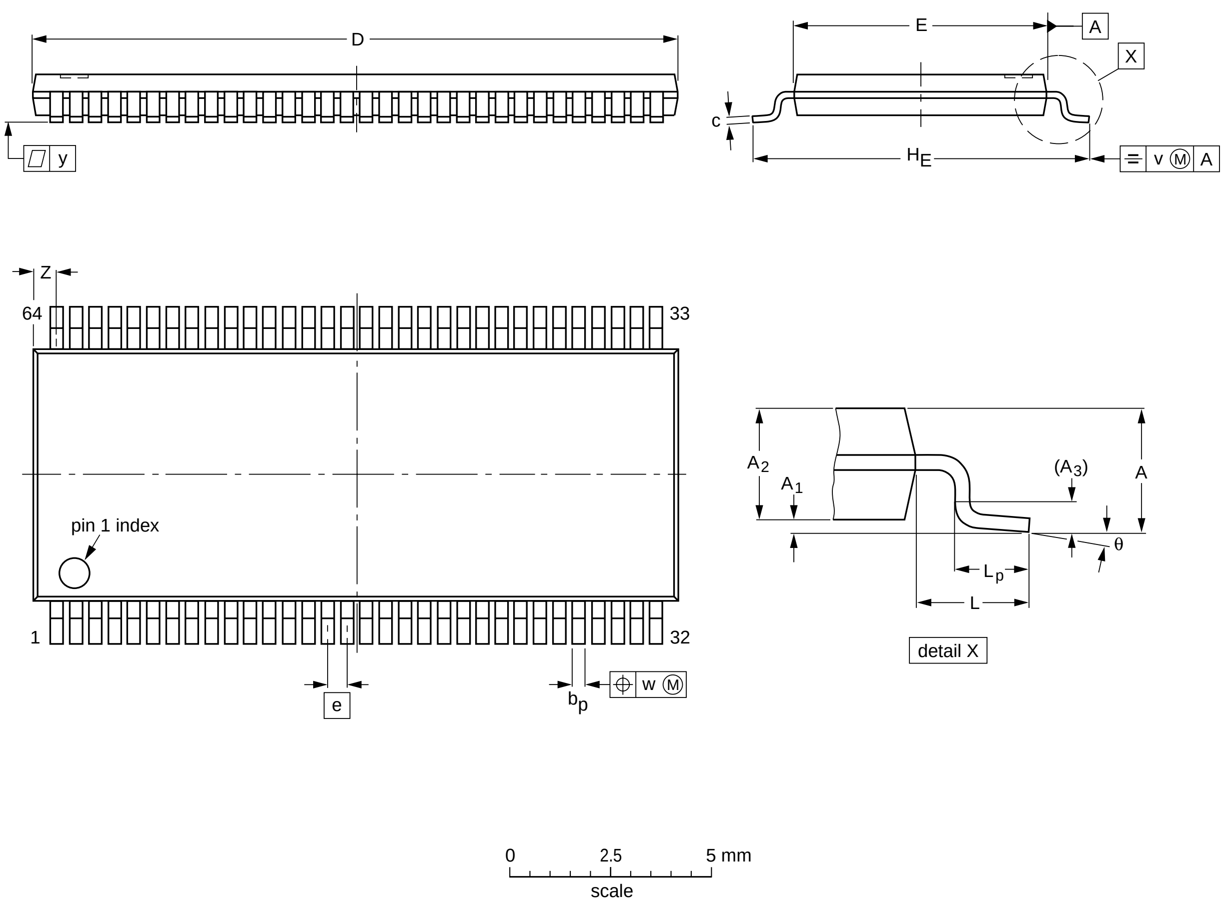


(1) C_L includes probe and jig capacitance.

Fig 11. Load circuit

13. Package outline

TSSOP64: plastic thin shrink small outline package; 64 leads; body width 6.1 mm **SOT646-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.27 0.17	0.2 0.1	17.1 16.9	6.2 6.0	0.5	8.3 7.9	1	0.75 0.45	0.2	0.08	0.1	0.89 0.61	8° 0°

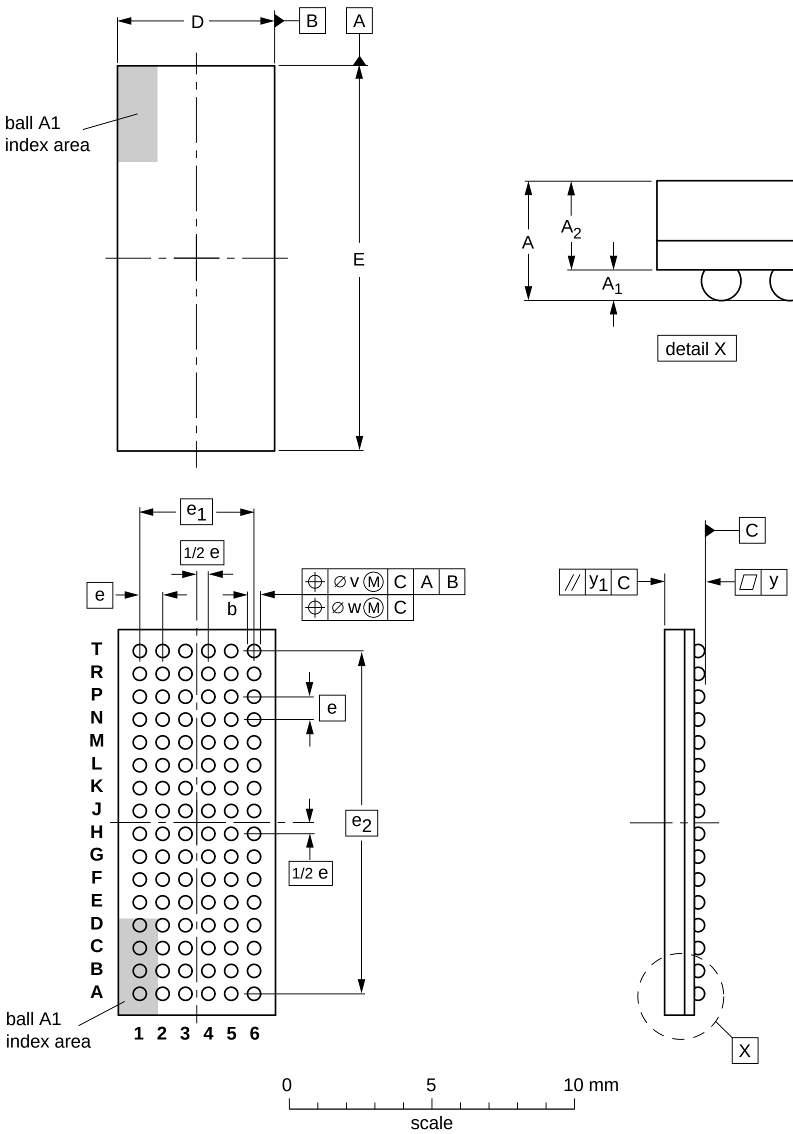
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT646-1		MO-153				~~00-08-21~~ 03-02-18

Fig 12. Package outline SOT646-1 (TSSOP64)

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	4	12	0.15	0.1	0.1	0.2

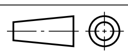
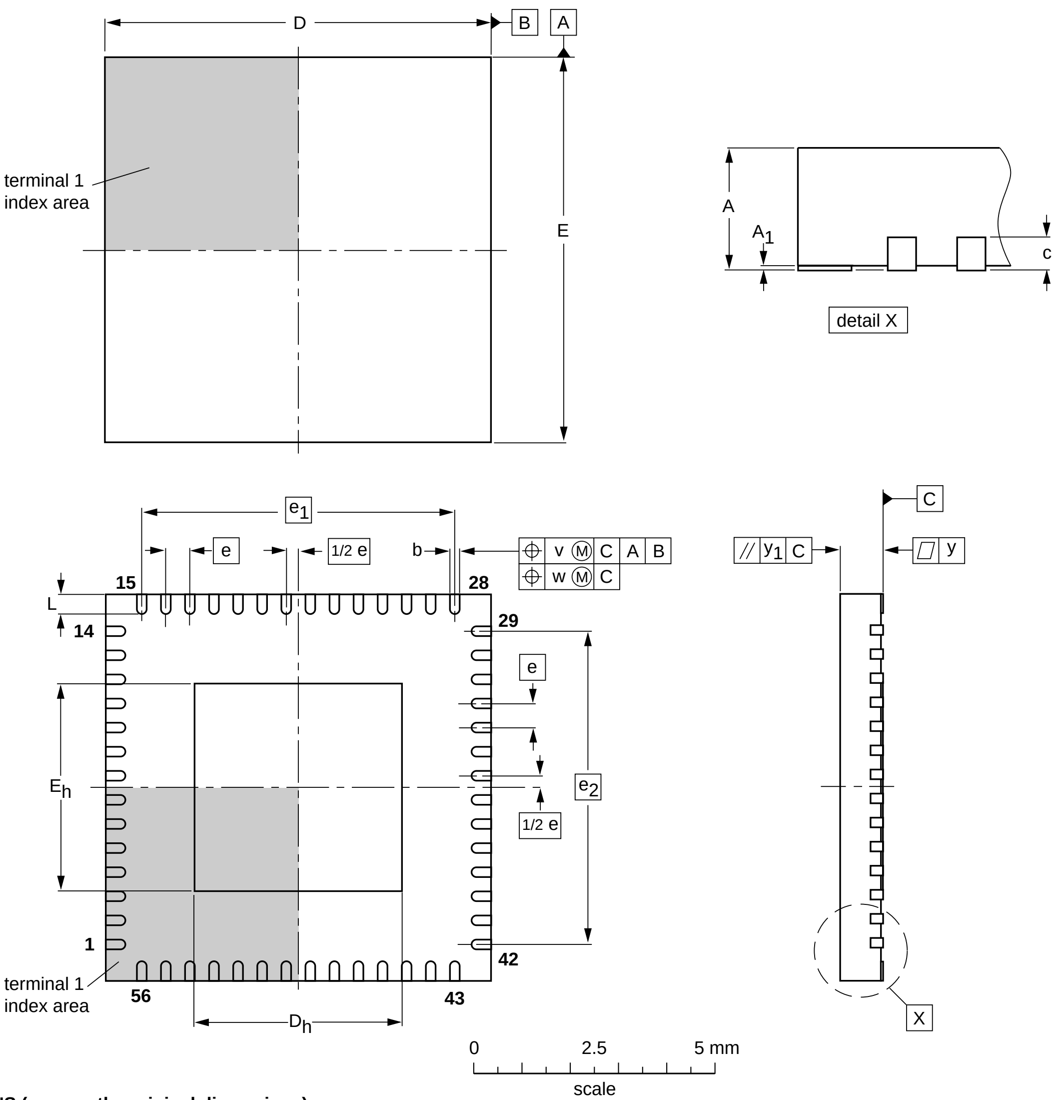
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT536-1						~~00-03-04~~ 03-02-05

Fig 13. Package outline SOT536-1 (LFBGA96)

HVQFN56: plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 x 8 x 0.85 mm — **SOT684-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	8.1 7.9	4.45 4.15	8.1 7.9	4.45 4.15	0.5	6.5	6.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT684-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 14. Package outline SOT684-1 (HVQFN56)

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 13: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	**Soldering method**	
	Wave	**Reflow** [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Abbreviations

Table 14: Abbreviations

Acronym	Description
DDR	Double Data Rate
DIMM	Dual In-line Memory Module
ESD	Electro Static Discharge
HBM	Human Body Model
PRR	Pulse Rate Repetition
SSTL	Stub Series Terminated Logic

16. Revision history

Table 15: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
SSTVF16859_2	20050719	Product data sheet	-	9397 750 15157	SSTVF16859_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Table 1 "Quick reference data": – parameter for t_{PHL}/t_{PLH} changed from 'propagation delay; CLK to Qn' to 'propagation delay; CK/$\overline{CK}$ to Qn' – Condition column for input capacitance changed from 'V_{CC} = 2.5 V' to 'V_{DD} = 2.5 V' • Section 6 "Pinning information": – Figure 3 "Pin configuration for TSSOP64": pins 6, 18, 27, 33, 38 47, 59 and 64 changed from 'V_{DD}' to 'V_{DDQ}' – pin description tables consolidated with columns for package-type • Symbol 'V_{REF}' changed to 'VREF' for pin name, and to 'V_{ref}' for reference voltage • Figure 2 "Pin configuration for HVQFN56" on page 3: – terminals 26, 33, 45 symbols changed from 'V_{DDI}' to 'V_{DD}' – terminal 56 symbol changed from 'Q8B' to 'Q8A' • Table 4 "Function selection (each flip-flop)" on page 7: moved definitions above table; added Table note 1. • Table 5 "Limiting values" on page 8: – deleted (old) Table note 1; this information is now placed in Section 18 "Definitions" on page 22. – Added symbol 'I_{CCC}' to parameter 'continuous current through each V_{DD} or GND' • Section 9 "Recommended operating conditions" on page 8: under Min and Max columns, values previously expressed with unit 'mV' re-written as equivalent 'V' value. • Table 7 "Static characteristics (PC1600-PC2700)" on page 9: – $I_{DD(max)}$ for 'static operating' condition changed from '25 mA' to '45 mA' – $I_{DDD(typ)}$ for 'clock only' changed from '20 µA' to '15 µA' – parameter for I_{DDD} modified: added 'per MHz' to parameter, changed Unit to 'µA' • Table 8 "Static characteristics (PC3200)" on page 10: parameter for I_{DDD} modified: added 'per MHz' to parameter, changed Unit to 'µA' • Added Section 14 "Soldering", Section 15 "Abbreviations", and Section 20 "Trademarks".				
SSTVF16859_1	20040712	Product data sheet	-	9397 750 13077	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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22. Contents

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