



MICROCHIP TC4423/TC4424/TC4425

3A Dual High-Speed Power MOSFET Drivers

Features

- High Peak Output Current: 3A
- Wide Input Supply Voltage Operating Range:
 - 4.5V to 18V
- High Capacitive Load Drive Capability:
 - 1800 pF in 25 ns
- Short Delay Times: <40 ns (typ)
- Matched Rise/Fall Times
- Low Supply Current:
 - With Logic '1' Input – 3.5 mA (Max)
 - With Logic '0' Input – 350 μ A (Max)
- Low Output Impedance: 3.5 Ω (typ)
- Latch-Up Protected: Will Withstand 1.5A Reverse Current
- Logic Input Will Withstand Negative Swing Up To 5V
- ESD Protected: 4 kV
- Pin compatible with the TC1426/TC1427/TC1428, TC4426/TC4427/TC4428 and TC4426A/TC4427A/TC4428A devices.
- Space-saving 8-Pin 6x5 DFN Package

General Description

The TC4423/TC4424/TC4425 devices are a family of 3A, dual-output buffers/MOSFET drivers. Pin compatible with the TC1426/27/28, TC4426/27/28 and TC4426A/27A/28A dual 1.5A driver families, the TC4423/24/25 family has an increased latch-up current rating of 1.5A, making them even more robust for operation in harsh electrical environments.

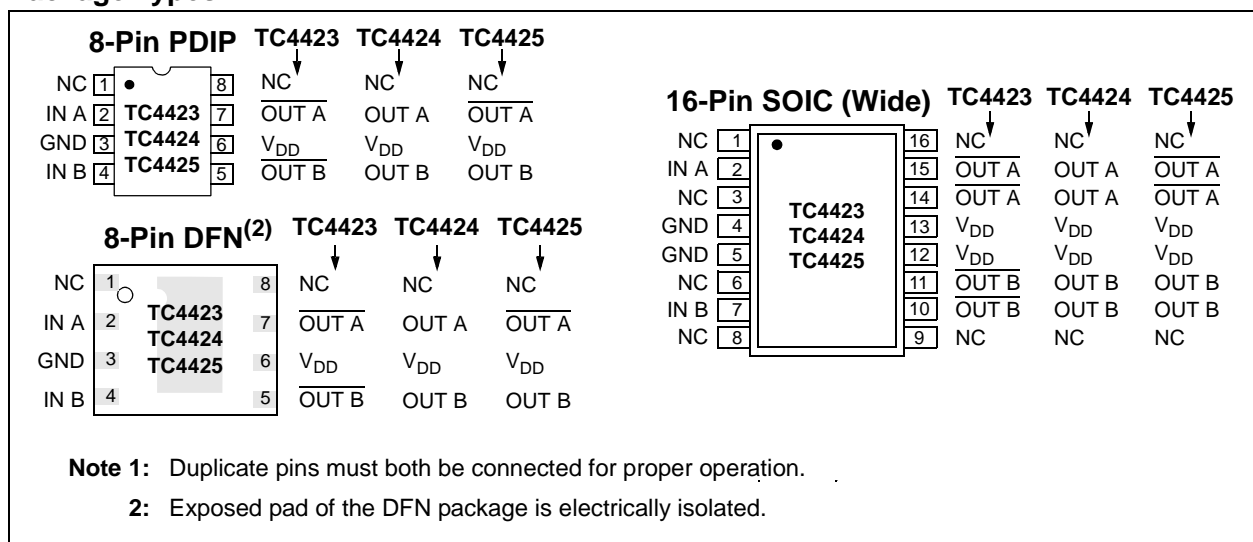
As MOSFET drivers, the TC4423/TC4424/TC4425 can easily charge 1800 pF gate capacitance in under 35 nsec, providing low enough impedances in both the on and off states to ensure the MOSFET's intended state will not be affected, even by large transients.

The TC4423/TC4424/TC4425 inputs may be driven directly from either TTL or CMOS (2.4V to 18V). In addition, the 300 mV of built-in hysteresis provides noise immunity and allows the device to be driven from slowly rising or falling waveforms.

Applications

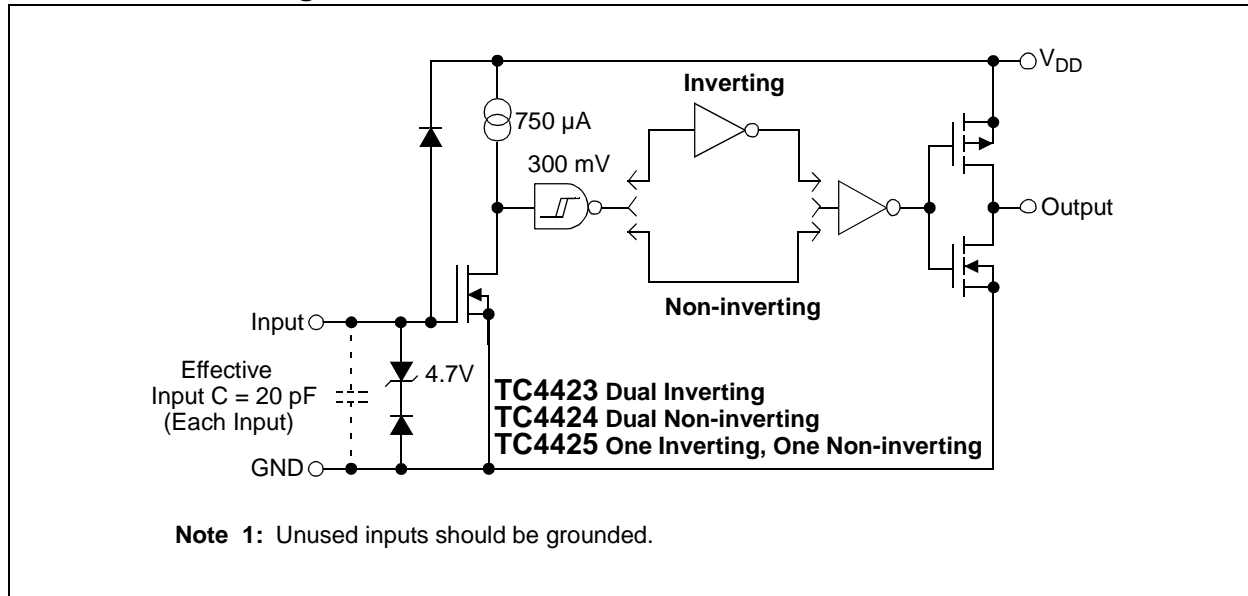
- Switch Mode Power Supplies
- Pulse Transformer Drive
- Line Drivers

Package Types⁽¹⁾



TC4423/TC4424/TC4425

Functional Block Diagram⁽¹⁾



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

| | |
|-----------------------------------------------------------|-----------------------------------|
| Supply Voltage | +22V |
| Input Voltage, IN A or IN B | ($V_{DD} + 0.3V$) to (GND – 5V) |
| Package Power Dissipation ($T_A \leq 70^\circ\text{C}$) | |
| DFN | Note 2 |
| PDIP | 730 mW |
| SOIC | 470 mW |

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

| Electrical Specifications: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, with $4.5V \leq V_{DD} \leq 18V$. | | | | | | |
|-----------------------------------------------------------------------------------------------------------------------|-----------|------------------|------|-------|---------------|------------------------------------------------------|
| Parameters | Sym | Min | Typ | Max | Units | Conditions |
| Input | | | | | | |
| Logic '1', High Input Voltage | V_{IH} | 2.4 | — | — | V | |
| Logic '0', Low Input Voltage | V_{IL} | — | — | 0.8 | V | |
| Input Current | I_{IN} | -1 | — | 1 | μA | $0V \leq V_{IN} \leq V_{DD}$ |
| Output | | | | | | |
| High Output Voltage | V_{OH} | $V_{DD} - 0.025$ | — | — | V | |
| Low Output Voltage | V_{OL} | — | — | 0.025 | V | |
| Output Resistance, High | R_{OH} | — | 2.8 | 5 | Ω | $I_{OUT} = 10 \text{ mA}$, $V_{DD} = 18V$ |
| Output Resistance, Low | R_{OL} | — | 3.5 | 5 | Ω | $I_{OUT} = 10 \text{ mA}$, $V_{DD} = 18V$ |
| Peak Output Current | I_{PK} | — | 3 | — | A | |
| Latch-Up Protection Withstand Reverse Current | I_{REV} | — | >1.5 | — | A | Duty cycle $\leq 2\%$, $t \leq 300 \mu\text{sec}$. |
| Switching Time (Note 1) | | | | | | |
| Rise Time | t_R | — | 23 | 35 | ns | Figure 4-1, Figure 4-2, $C_L = 1800 \text{ pF}$ |
| Fall Time | t_F | — | 25 | 35 | ns | Figure 4-1, Figure 4-2, $C_L = 1800 \text{ pF}$ |
| Delay Time | t_{D1} | — | 33 | 75 | ns | Figure 4-1, Figure 4-2, $C_L = 1800 \text{ pF}$ |
| Delay Time | t_{D2} | — | 38 | 75 | ns | Figure 4-1, Figure 4-2, $C_L = 1800 \text{ pF}$ |
| Power Supply | | | | | | |
| Power Supply Current | I_S | — | 1.5 | 2.5 | mA | $V_{IN} = 3V$ (Both inputs) |
| | | — | 0.15 | 0.25 | | $V_{IN} = 0V$ (Both inputs) |

Note 1: Switching times ensured by design.

2: Package power dissipation is dependent on the copper pad area on the PCB.

TC4423/TC4424/TC4425

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

| Electrical Specifications: Unless otherwise indicated, operating temperature range with $4.5V \leq V_{DD} \leq 18V$. | | | | | | |
|------------------------------------------------------------------------------------------------------------------------------|-----------|------------------|------|-------|----------|------------------------------------------------------------|
| Parameters | Sym | Min | Typ | Max | Units | Conditions |
| Input | | | | | | |
| Logic '1', High Input Voltage | V_{IH} | 2.4 | — | — | V | |
| Logic '0', Low Input Voltage | V_{IL} | — | — | 0.8 | V | |
| Input Current | I_{IN} | -10 | — | +10 | μA | $0V \leq V_{IN} \leq V_{DD}$ |
| Output | | | | | | |
| High Output Voltage | V_{OH} | $V_{DD} - 0.025$ | — | — | V | |
| Low Output Voltage | V_{OL} | — | — | 0.025 | V | |
| Output Resistance, High | R_{OH} | — | 3.7 | 8 | Ω | $I_{OUT} = 10 \text{ mA}, V_{DD} = 18V$ |
| Output Resistance, Low | R_{OL} | — | 4.3 | 8 | Ω | $I_{OUT} = 10 \text{ mA}, V_{DD} = 18V$ |
| Peak Output Current | I_{PK} | — | 3.0 | — | A | |
| Latch-Up Protection Withstand Reverse Current | I_{REV} | — | >1.5 | — | A | Duty cycle $\leq 2\%$, $t \leq 300 \mu\text{sec}$ |
| Switching Time (Note 1) | | | | | | |
| Rise Time | t_R | — | 28 | 60 | ns | Figure 4-1, Figure 4-2, $C_L = 1800 \text{ pF}$ |
| Fall Time | t_F | — | 32 | 60 | ns | Figure 4-1, Figure 4-2, $C_L = 1800 \text{ pF}$ |
| Delay Time | t_{D1} | — | 32 | 100 | ns | Figure 4-1, Figure 4-2, $C_L = 1800 \text{ pF}$ |
| Delay Time | t_{D2} | — | 38 | 100 | ns | Figure 4-1, Figure 4-2, $C_L = 1800 \text{ pF}$ |
| Power Supply | | | | | | |
| Power Supply Current | I_S | — | 2.0 | 3.5 | mA | $V_{IN} = 3V$ (Both inputs) $V_{IN} = 0V$ (Both inputs) |

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

| Electrical Specifications: Unless otherwise noted, all parameters apply with $4.5V \leq V_{DD} \leq 18V$. | | | | | | |
|-------------------------------------------------------------------------------------------------------------------|---------------|-----|------|------|---------------|----------------------------------------------------|
| Parameters | Sym | Min | Typ | Max | Units | Conditions |
| Temperature Ranges | | | | | | |
| Specified Temperature Range (C) | T_A | 0 | — | +70 | $^{\circ}C$ | |
| Specified Temperature Range (E) | T_A | -40 | — | +85 | $^{\circ}C$ | |
| Specified Temperature Range (V) | T_A | -40 | — | +125 | $^{\circ}C$ | |
| Maximum Junction Temperature | T_J | — | — | +150 | $^{\circ}C$ | |
| Storage Temperature Range | T_A | -65 | — | +150 | $^{\circ}C$ | |
| Package Thermal Resistances | | | | | | |
| Thermal Resistance, 8L-6x5 DFN | θ_{JA} | — | 33.2 | — | $^{\circ}C/W$ | Typical four-layer board with vias to ground plane |
| Thermal Resistance, 8L-PDIP | θ_{JA} | — | 125 | — | $^{\circ}C/W$ | |
| Thermal Resistance, 16L-SOIC | θ_{JA} | — | 155 | — | $^{\circ}C/W$ | |

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

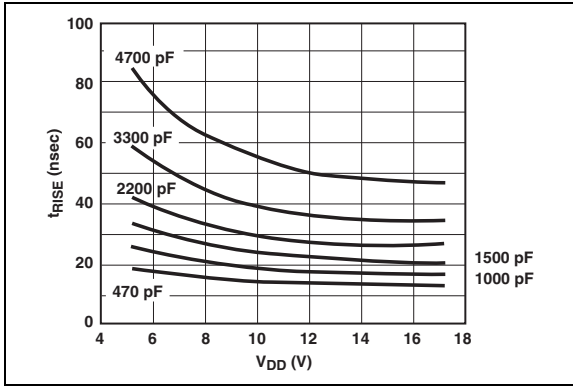


FIGURE 2-1: Rise Time vs. Supply Voltage.

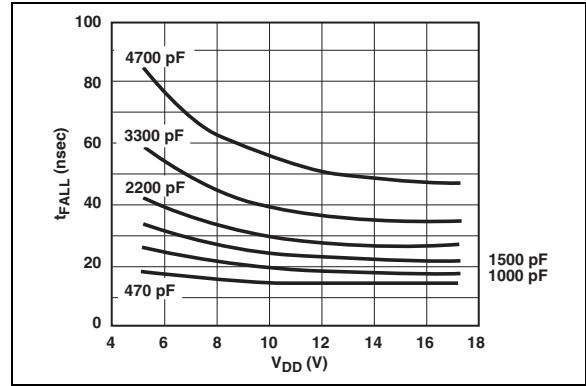


FIGURE 2-4: Fall Time vs. Supply Voltage.

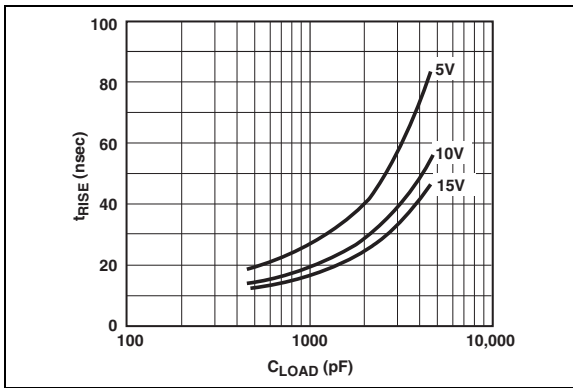


FIGURE 2-2: Rise Time vs. Capacitive Load.

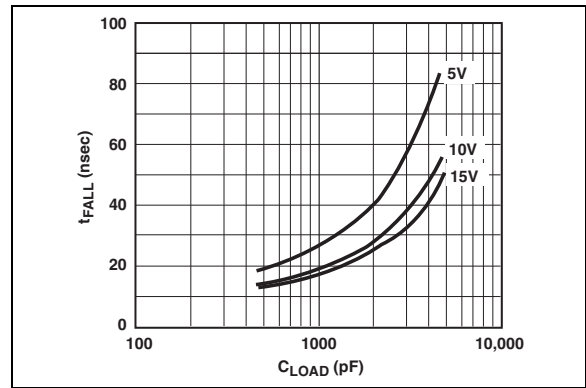


FIGURE 2-5: Fall Time vs. Capacitive Load.

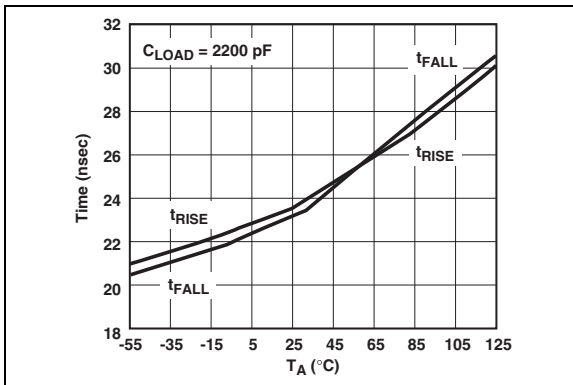


FIGURE 2-3: Rise and Fall Times vs. Temperature.

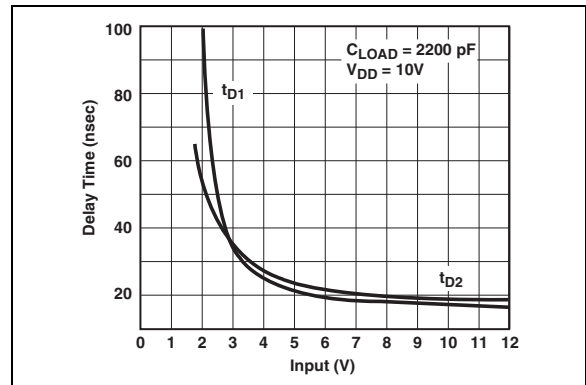


FIGURE 2-6: Propagation Delay vs. Input Amplitude.

TC4423/TC4424/TC4425

Typical Performance Curves (Continued)

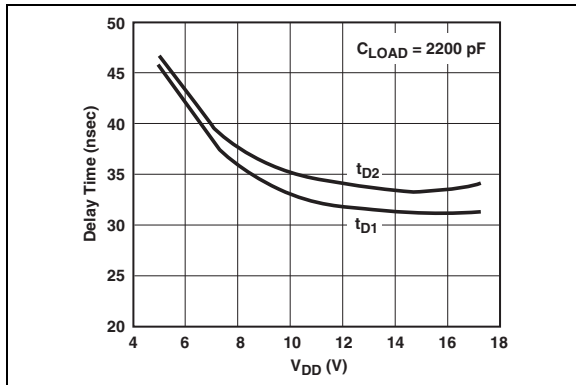


FIGURE 2-7: Propagation Delay Time vs. Supply Voltage.

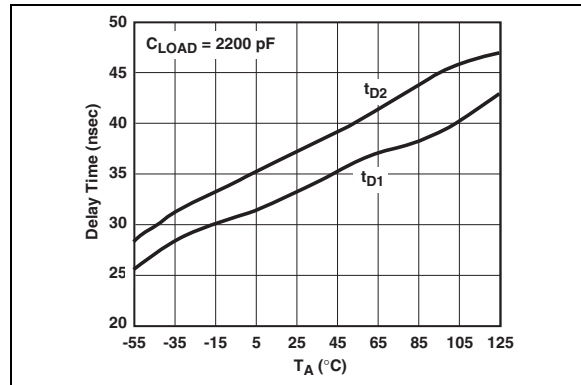


FIGURE 2-10: Propagation Delay Time vs. Temperature.

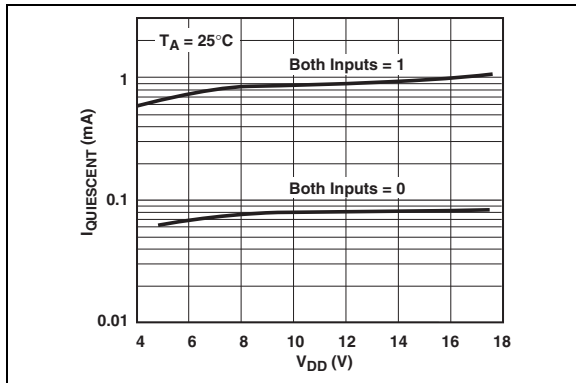


FIGURE 2-8: Quiescent Current vs. Supply Voltage.

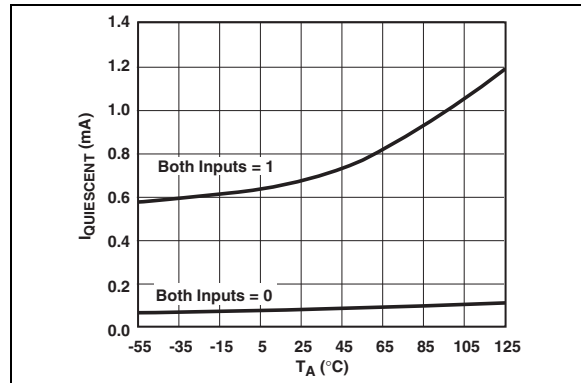


FIGURE 2-11: Quiescent Current vs. Temperature.

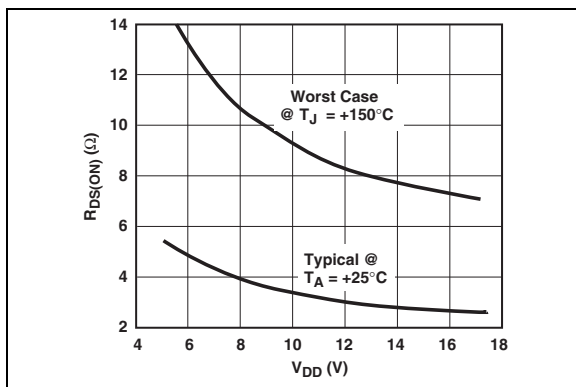


FIGURE 2-9: Output Resistance (Output High) vs. Supply Voltage.

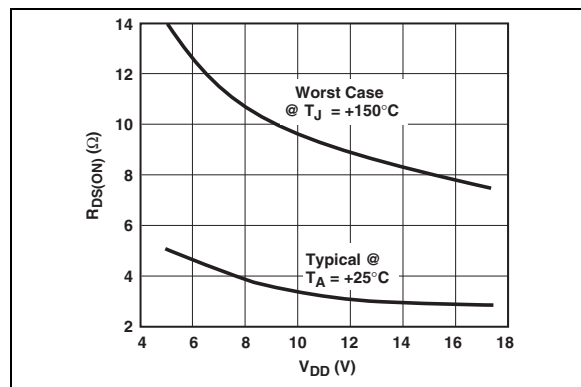


FIGURE 2-12: Output Resistance (Output Low) vs. Supply Voltage.

Typical Performance Curves (Continued)

Note: Load on single output only

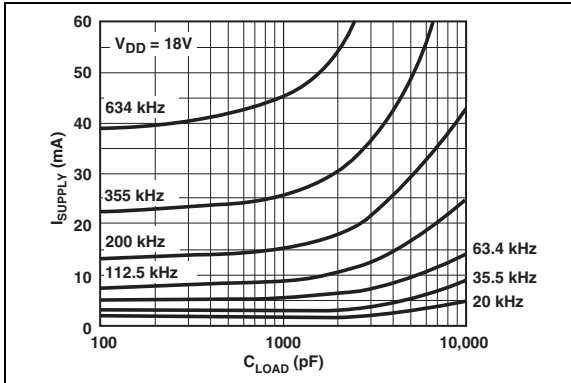


FIGURE 2-13: Supply Current vs. Capacitive Load.

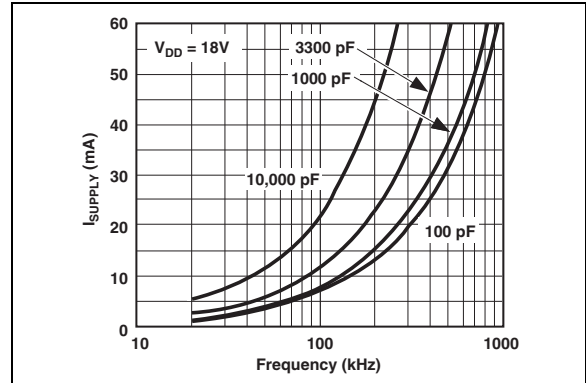


FIGURE 2-16: Supply Current vs. Frequency.

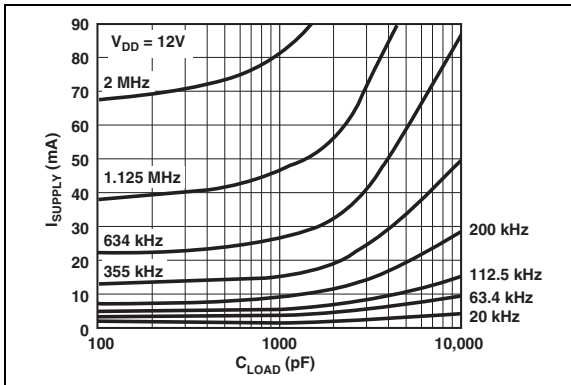


FIGURE 2-14: Supply Current vs. Capacitive Load.

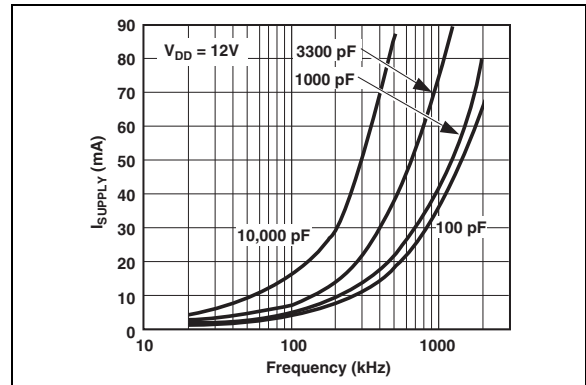


FIGURE 2-17: Supply Current vs. Frequency.

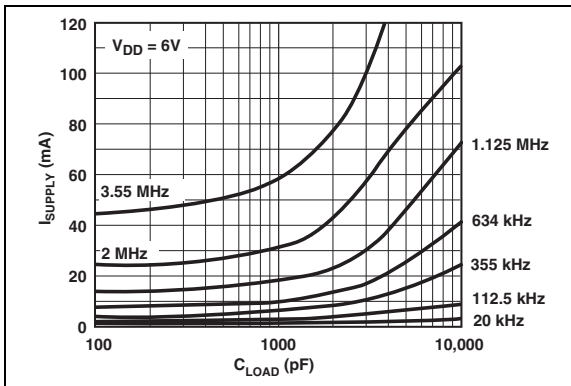


FIGURE 2-15: Supply Current vs. Capacitive Load.

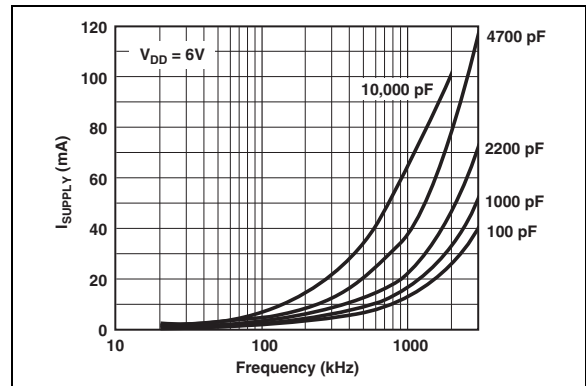


FIGURE 2-18: Supply Current vs. Frequency.

TC4423/TC4424/TC4425

Typical Performance Curves (Continued)

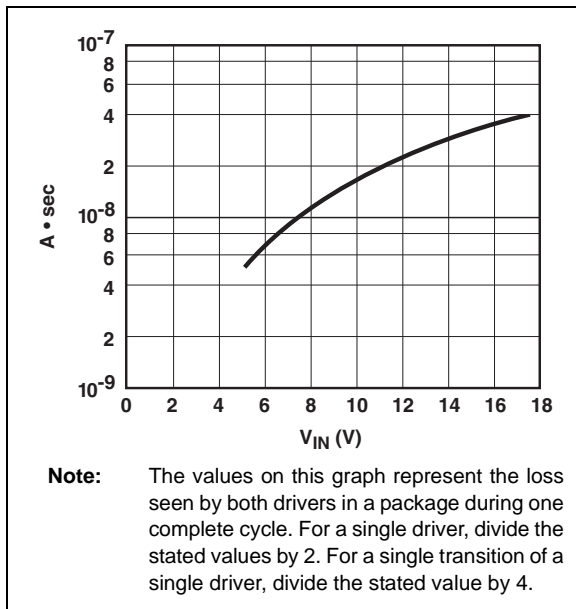


FIGURE 2-19: *TC4423 Crossover Energy.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE (1)

| 8-Pin PDIP | 8-Pin DFN | 16-Pin SOIC (Wide) | Symbol | Description |
|------------|-----------|--------------------|-----------------|-------------------|
| 1 | 1 | 1 | NC | No connection |
| 2 | 2 | 2 | IN A | Input A |
| — | — | 3 | NC | No connection |
| 3 | 3 | 4 | GND | Ground |
| — | — | 5 | GND | Ground |
| — | — | 6 | NC | No connection |
| 4 | 4 | 7 | IN B | Input B |
| — | — | 8 | NC | No connection |
| — | — | 9 | NC | No connection |
| 5 | 5 | 10 | OUT B | Output B |
| — | — | 11 | OUT B | Output B |
| 6 | 6 | 12 | V _{DD} | Supply input |
| — | — | 13 | V _{DD} | Supply input |
| 7 | 7 | 14 | OUT A | Output A |
| — | — | 15 | OUT A | Output A |
| 8 | 8 | 16 | NC | No connection |
| — | PAD | — | NC | Exposed Metal Pad |

Note 1: Duplicate pins must be connected for proper operation.

3.1 Inputs A and B

Inputs A and B are TTL/CMOS compatible inputs that control outputs A and B, respectively. These inputs have 300 mV of hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals, and to provide noise immunity.

3.2 Outputs A and B

Outputs A and B are CMOS push-pull outputs that are capable of sourcing and sinking 3A peaks of current (V_{DD} = 18V). The low output impedance ensures the gate of the external MOSFET will stay in the intended state even during large transients. These outputs also have a reverse current latch-up rating of 1.5A.

3.3 Supply Input (V_{DD})

V_{DD} is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local ceramic capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are to be provided to the load.

3.4 Ground (GND)

Ground is the device return pin. The ground pin(s) should have a low-impedance connection to the bias supply source return. High peak currents will flow out the ground pin(s) when the capacitive load is being discharged.

3.5 Exposed Metal Pad

The exposed metal pad of the 6x5 DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a printed circuit board to aid in heat removal from the package.

TC4423/TC4424/TC4425

4.0 APPLICATIONS INFORMATION

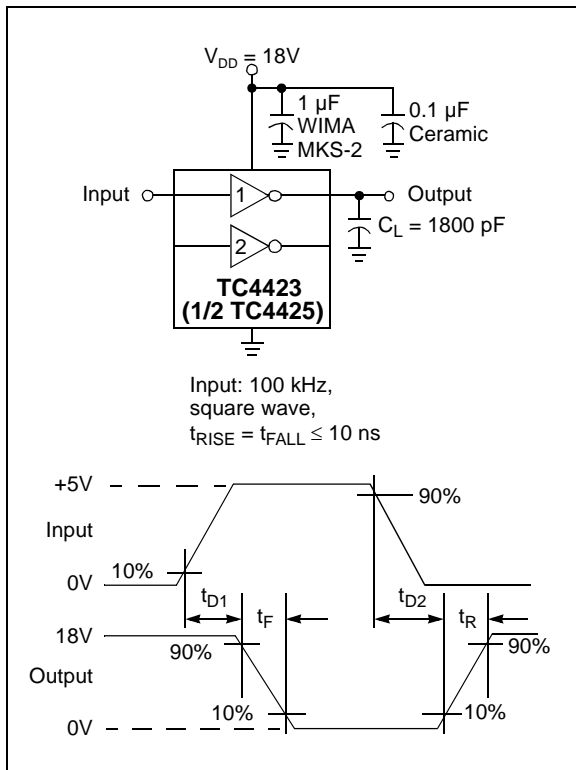


FIGURE 4-1: Inverting Driver Switching Time.

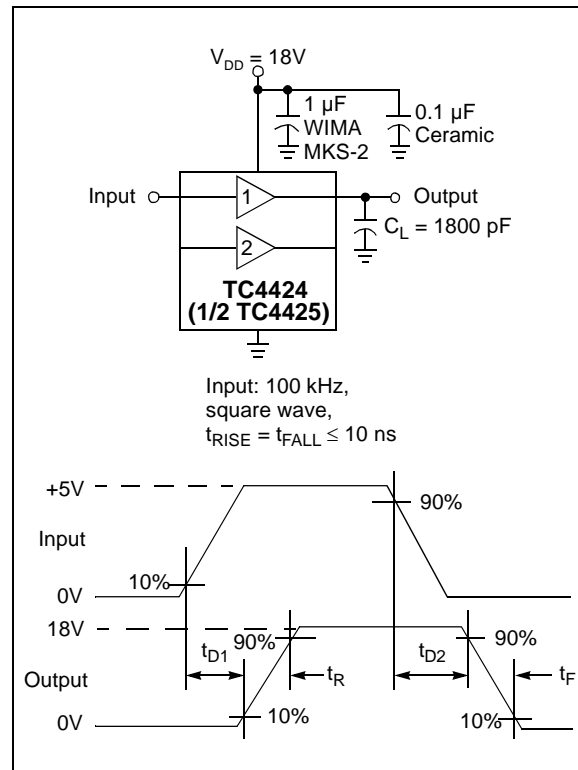
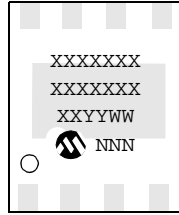


FIGURE 4-2: Non-inverting Driver Switching Time.

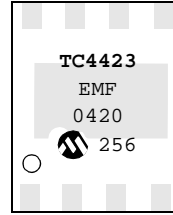
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

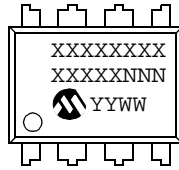
8-Lead DFN



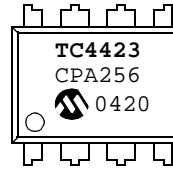
Example:



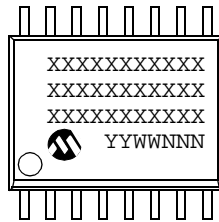
8-Lead PDIP (300 mil)



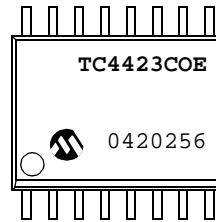
Example:



16-Lead SOIC (300 mil)



Example:



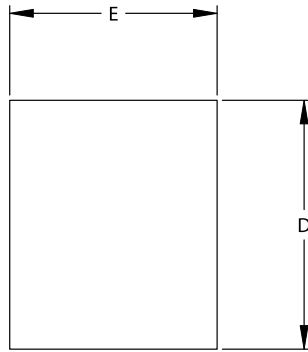
| | | |
|----------------|--------|------------------------------------------------------------------------------------------------------------------|
| Legend: | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

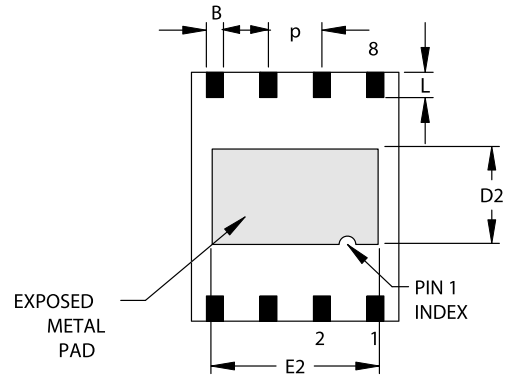
TC4423/TC4424/TC4425

8-Lead Plastic Dual Flat No Lead Package (MF) 6x5 mm Body (DFN-S) – Saw Singulated

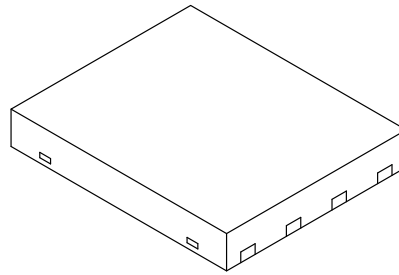
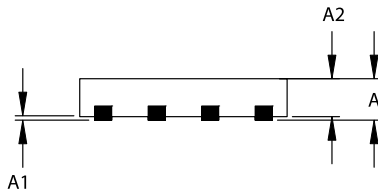
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



TOP VIEW



BOTTOM VIEW



| Dimension Limits | Units | INCHES | | | MILLIMETERS* | | |
|--------------------|-------|----------|-------|------|--------------|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 8 | | | 8 | |
| Pitch | p | .050 BSC | | | 1.27 BSC | | |
| Overall Height | A | .033 | .035 | .037 | 0.85 | 0.90 | 0.95 |
| Package Thickness | A2 | .031 | .035 | .037 | 0.80 | 0.89 | 0.95 |
| Standoff | A1 | .000 | .0004 | .002 | 0.00 | 0.01 | 0.05 |
| Base Thickness | A3 | .007 | .008 | .009 | 0.17 | 0.20 | 0.23 |
| Overall Length | E | .195 | .197 | .199 | 4.95 | 5.00 | 5.05 |
| Exposed Pad Length | E2 | .152 | .157 | .163 | 3.85 | 4.00 | 4.15 |
| Overall Width | D | .234 | .236 | .238 | 5.95 | 6.00 | 6.05 |
| Exposed Pad Width | D2 | .089 | .091 | .093 | 2.25 | 2.30 | 2.35 |
| Lead Width | B | .014 | .016 | .019 | 0.35 | 0.40 | 0.47 |
| Lead Length | L | .024 | | .026 | 0.60 | | 0.65 |

Notes:

JEDEC equivalent: MO-220

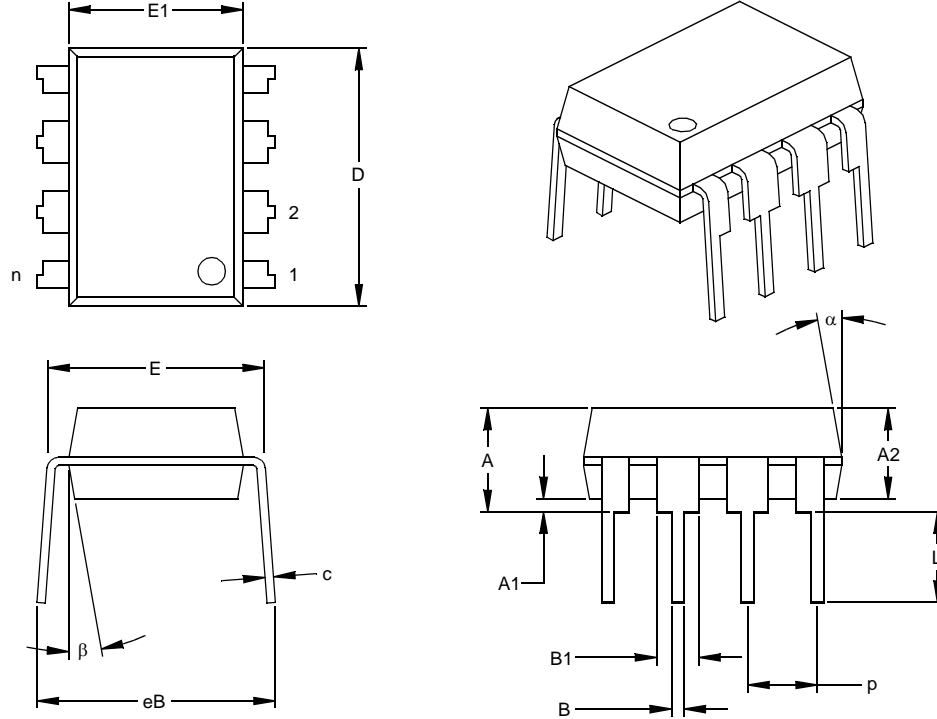
Drawing No. C04-122

Revised 11/3/03

TC4423/TC4424/TC4425

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | INCHES* | | | MILLIMETERS | | |
|----------------------------|-------|---------|------|------|-------------|------|-------|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 8 | | | 8 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .140 | .155 | .170 | 3.56 | 3.94 | 4.32 |
| Molded Package Thickness | A2 | .115 | .130 | .145 | 2.92 | 3.30 | 3.68 |
| Base to Seating Plane | A1 | .015 | | | 0.38 | | |
| Shoulder to Shoulder Width | E | .300 | .313 | .325 | 7.62 | 7.94 | 8.26 |
| Molded Package Width | E1 | .240 | .250 | .260 | 6.10 | 6.35 | 6.60 |
| Overall Length | D | .360 | .373 | .385 | 9.14 | 9.46 | 9.78 |
| Tip to Seating Plane | L | .125 | .130 | .135 | 3.18 | 3.30 | 3.43 |
| Lead Thickness | c | .008 | .012 | .015 | 0.20 | 0.29 | 0.38 |
| Upper Lead Width | B1 | .045 | .058 | .070 | 1.14 | 1.46 | 1.78 |
| Lower Lead Width | B | .014 | .018 | .022 | 0.36 | 0.46 | 0.56 |
| Overall Row Spacing | § eB | .310 | .370 | .430 | 7.87 | 9.40 | 10.92 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

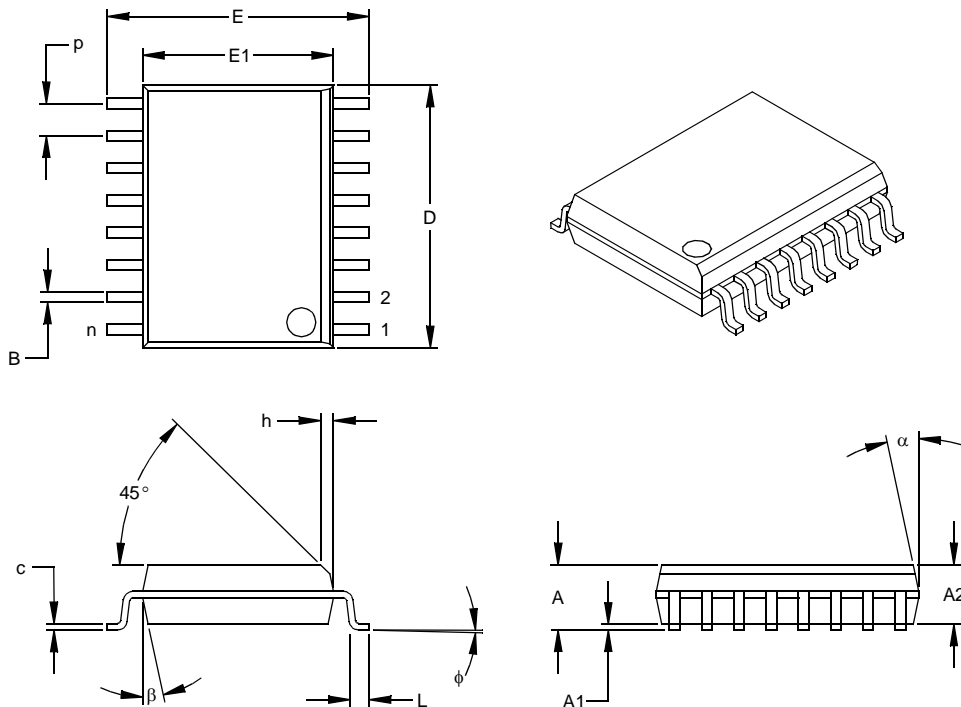
* Controlling Parameter
 § Significant Characteristic

Notes:
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
 JEDEC Equivalent: MS-001
 Drawing No. C04-018

TC4423/TC4424/TC4425

16-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | INCHES* | | | MILLIMETERS | | |
|--------------------------|-------|---------|------|------|-------------|-------|-------|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 16 | | | 16 | |
| Pitch | p | | .050 | | | 1.27 | |
| Overall Height | A | .093 | .099 | .104 | 2.36 | 2.50 | 2.64 |
| Molded Package Thickness | A2 | .088 | .091 | .094 | 2.24 | 2.31 | 2.39 |
| Standoff § | A1 | .004 | .008 | .012 | 0.10 | 0.20 | 0.30 |
| Overall Width | E | .394 | .407 | .420 | 10.01 | 10.34 | 10.67 |
| Molded Package Width | E1 | .291 | .295 | .299 | 7.39 | 7.49 | 7.59 |
| Overall Length | D | .398 | .406 | .413 | 10.10 | 10.30 | 10.49 |
| Chamfer Distance | h | .010 | .020 | .029 | 0.25 | 0.50 | 0.74 |
| Foot Length | L | .016 | .033 | .050 | 0.41 | 0.84 | 1.27 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .009 | .011 | .013 | 0.23 | 0.28 | 0.33 |
| Lead Width | B | .014 | .017 | .020 | 0.36 | 0.42 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter
 § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-013

Drawing No. C04-102

6.0 REVISION HISTORY

Revision E (December 2012)

Added a note to each package outline drawing.

TC4423/TC4424/TC4425

TC4423/TC4424/TC4425

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u> | <u>X</u> | <u>XX</u> | <u>XXX</u> | <u>X</u> | |
|---------------------------------------------------------------------------------------------|-------------------|---------------------------------------------------------------------------------------|-------------|----------|--|
| Device | Temperature Range | Package | Tape & Reel | PB Free | |
| Device: | TC4423: | 3A Dual MOSFET Driver, Inverting | | | |
| | TC4424: | 3A Dual MOSFET Driver, Non-Inverting | | | |
| | TC4425: | 3A Dual MOSFET Driver, Complementary | | | |
| Temperature Range: | C = | 0°C to +70°C (PDIP & SOIC Only) | | | |
| | E = | -40°C to +85°C | | | |
| | V = | -40°C to +125°C | | | |
| Package: | MF = | Dual, Flat, No-Lead (6x5 mm Body), 8-lead | | | |
| | MF713 = | Dual, Flat, No-Lead (6x5 mm Body), 8-lead (Tape and Reel) | | | |
| | OE = | SOIC (Wide), 16-pin | | | |
| | OE713 = | SOIC (Wide), 16-pin (Tape and Reel) | | | |
| | PA = | Plastic DIP, (300 mil body), 8-lead | | | |
| PB Free: | G = | Lead-Free device * | | | |
| | | = Blank | | | |
| * Available on selected packages. Contact your local sales representative for availability. | | | | | |
| Examples: | | | | | |
| a) | TC4423COE: | 3A Dual Inverting MOSFET Driver, 0°C to +70°C, 16LD SOIC package. | | | |
| b) | TC4423CPA: | 3A Dual Inverting MOSFET Driver, 0°C to +70°C, 8LD PDIP package. | | | |
| c) | TC4423VMF: | 3A Dual Inverting MOSFET Driver, -40°C to +125°C, 8LD DFN package. | | | |
| a) | TC4424COE713: | 3A Dual Non-Inverting, MOSFET Driver, 0°C to +70°C, 16LD SOIC package, Tape and Reel. | | | |
| b) | TC4424EPA: | 3A Dual Non-Inverting, MOSFET Driver, -40°C to +85°C, 8LD PDIP package. | | | |
| a) | TC4425EOE: | 3A Dual Complementary, MOSFET Driver, -40°C to +85°C, 16LD SOIC package. | | | |
| b) | TC4425CPA: | 3A Dual Complementary, MOSFET Driver, 0°C to +70°C, PDIP package. | | | |

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1. Your local Microchip sales office
2. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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TC4423/TC4424/TC4425

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