



# THE DATASHEET OF STGD7NB60KT4





# STGD7NB60K STGP7NB60K

N-channel 600V - 7A - TO-220 / DPAK  
Short circuit rated PowerMESH™ IGBT

## General features

Type	V <sub>CES</sub>	V <sub>CE(sat)</sub> Max @25°C	I <sub>C</sub> @100°C
STGD7NB60K	600V	< 2.8V	7A
STGP7NB60K	600V	< 2.8V	7A

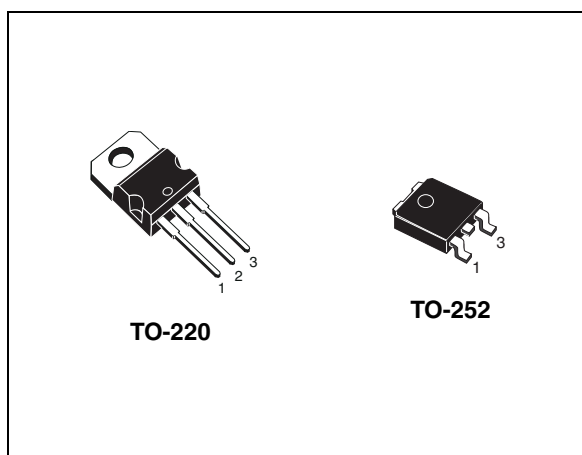
- High input impedance (voltage driven)
- Low on-voltage drop (V<sub>cesat</sub>)
- Low gate charge
- High current capability
- High frequency operation
- Short circuit rated

## Description

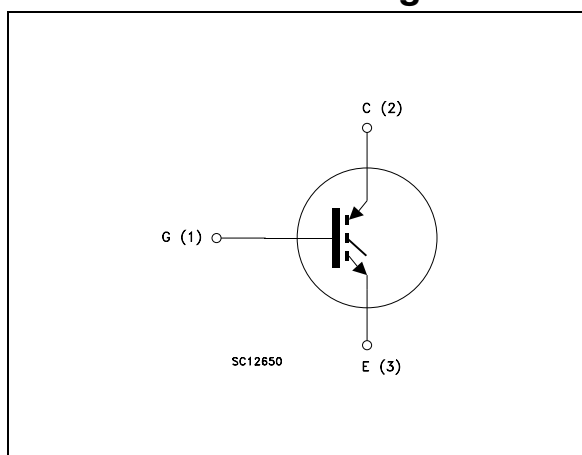
Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix "K" identifies a family optimized for high frequency motor control applications with short circuit withstand capability.

## Applications

- High frequency motor controls
- SMPS and PFC in both hard switching and resonant topologies



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STGD7NB60KT4	GD7NB60K	DPAK	Tape & reel
STGP7NB60K	GP7NB60K	TO-220	Tube

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220	DPAK	
V <sub>CES</sub>	Collector-emitter voltage (V <sub>GS</sub> = 0)	600		V
I <sub>C</sub> <sup>(1)</sup>	Collector current (continuous) at T <sub>C</sub> = 25°C	14		A
I <sub>C</sub> <sup>(1)</sup>	Collector current (continuous) at T <sub>C</sub> = 100°C	7		A
I <sub>CM</sub> <sup>(2)</sup>	Collector current (pulsed)	56		A
V <sub>GE</sub>	Gate-emitter voltage	±20		V
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25°C	80	70	W
T <sub>SC</sub>	Short circuit withstand	0.64	0.56	µs
T <sub>stg</sub>	Storage temperature	– 65 to 150		°C
T <sub>j</sub>	Operating junction temperature	150		

1. Calculated according to the iterative formula::

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. Pulse width limited by max junction temperature

**Table 2. Thermal resistance**

Symbol	Parameter	TO-220	DPAK	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case Max	1.56	1.4	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient Max	62.5	100	°C/W

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 1mA, V_{GE} = 0$	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15V, I_C = 7A$		2.3	2.8	V
		$V_{GE} = 15V, I_C = 7A, T_C = 125^{\circ}C$		1.9		V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}, I_C = 250 \mu A$	5		7	V
$I_{CES}$	Collector cut-off current ( $V_{GE} = 0$ )	$V_{CE} = \text{Max rating}, T_C = 25^{\circ}C$			50	$\mu A$
		$V_{CE} = \text{Max rating}, T_C = 125^{\circ}C$			500	$\mu A$
$I_{GES}$	Gate-emitter leakage current ( $V_{CE} = 0$ )	$V_{GE} = \pm 20V, V_{CE} = 0$			$\pm 100$	nA
$g_{fs}$	Forward transconductance	$V_{CE} = 15V, I_C = 7A$		3.7		S

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{ies}$ $C_{oes}$ $C_{res}$	Input capacitance	$V_{CE} = 25V, f = 1MHz,$ $V_{GE} = 0$		495		pF
	Output capacitance			77		pF
	Reverse transfer capacitance			13		pF
$Q_g$ $Q_{ge}$ $Q_{gc}$	Total gate charge	$V_{CE} = 480V, I_C = 7A,$ $V_{GE} = 15V,$ <i>(see Figure 17)</i>		32.7	45	nC
	Gate-emitter charge			5.9		nC
	Gate-collector charge			18.3		nC
tscw	Short circuit withstand time	$V_{CE} = 0.5V V_{BR(CES)}, R_G = 10\Omega$ $V_{GE} = 15V, T_j = 125^{\circ}C$	10			$\mu s$

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Current rise time	$V_{CC} = 480V, I_C = 7A$ $R_G = 10\Omega, V_{GE} = 15V,$ $T_J = 25^\circ C$ (see Figure 18)		15 6		ns ns
$(di/dt)_{on}$ $E_{on}^{(1)}$	Turn-on delay time Turn-on switching losses	$V_{CC} = 480V, I_C = 7A$ $R_G = 10\Omega, V_{GE} = 15V,$ $T_J = 125^\circ C$ (see Figure 18)		980 95		A/ $\mu s$ $\mu J$
$t_c$ $t_r(V_{off})$ $t_{d(off)}$ $t_f$ $E_{off}^{(2)}$ $E_{ts}$	Cross-over time Off voltage rise time Turn-off delay time Current fall time Turn-off switching losses Total switching losses	$V_{CC} = 480V, I_C = 7A,$ $R_{GE} = 10\Omega, V_{GE} = 15V,$ $T_J = 25^\circ C$ (see Figure 18)		105 30 50 100 140 200		ns ns ns ns $\mu J$ $\mu J$
$t_c$ $t_r(V_{off})$ $t_{d(off)}$ $t_f$ $E_{off}^{(1)}$ $E_{ts}$	Cross-over time Off voltage rise time Turn-off delay time Current fall time Turn-off switching losses Total switching losses	$V_{CC} = 480V, I_C = 7A,$ $R_{GE} = 10\Omega, V_{GE} = 15V,$ $T_J = 125^\circ C$ (see Figure 18)		227 68 52 150 300 395		ns ns ns ns $\mu J$ $\mu J$

1.  $E_{on}$  is the turn-on losses when a typical diode is used in the test circuit in figure 2. If the IGBT is offered in a package with a co-pack diode, the co-pack diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C)

2. Turn-off losses include also the tail of the collector current

## 2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

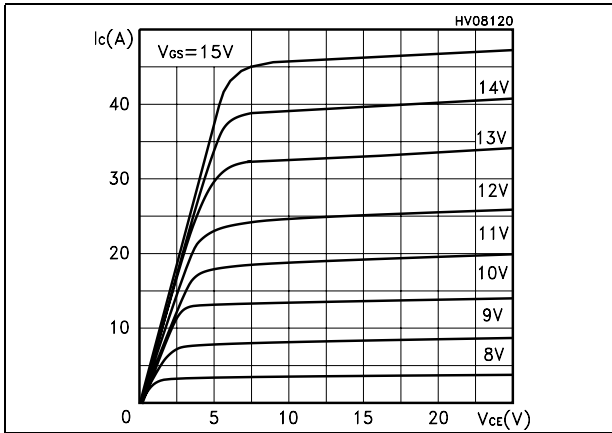


Figure 2. Transfer characteristics

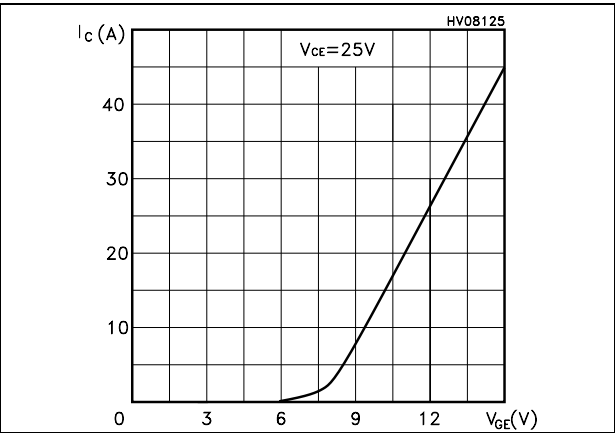


Figure 3. Transconductance

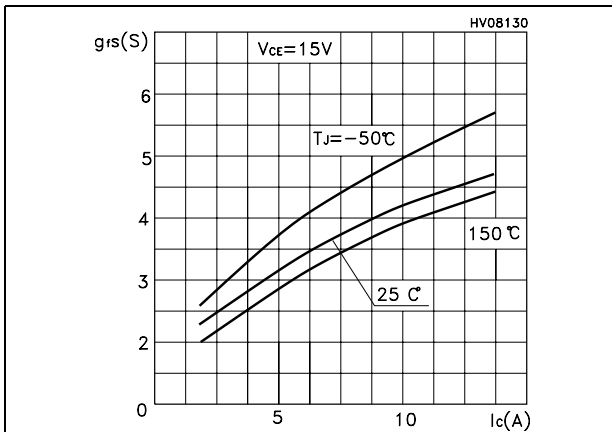


Figure 4. Normalized collector-emitter on voltage

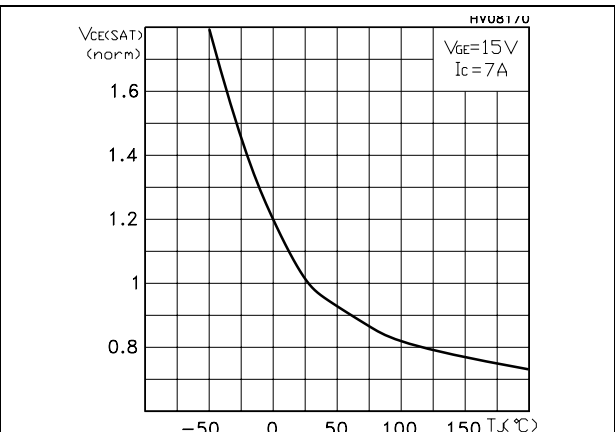


Figure 5. Gate charge vs gate-source voltage

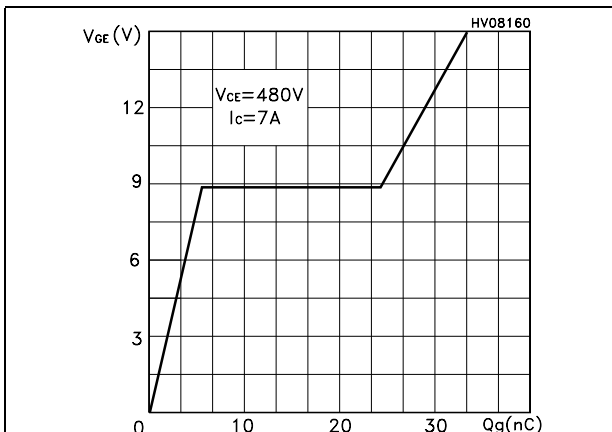


Figure 6. Capacitance variations

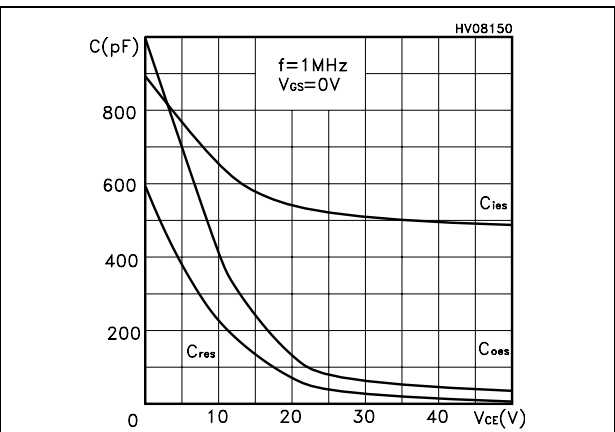


Figure 7. Normalized gate threshold voltage vs temperature

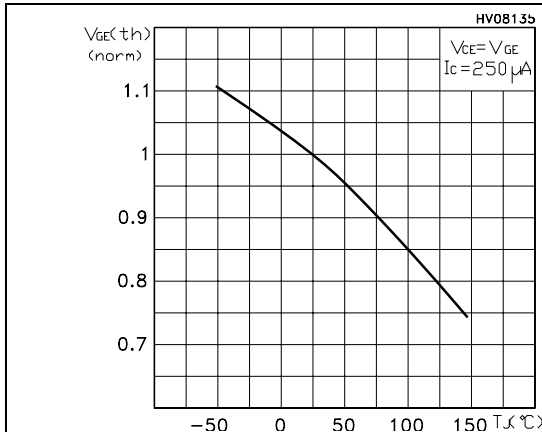


Figure 8. Collector-emitter on voltage vs collector current

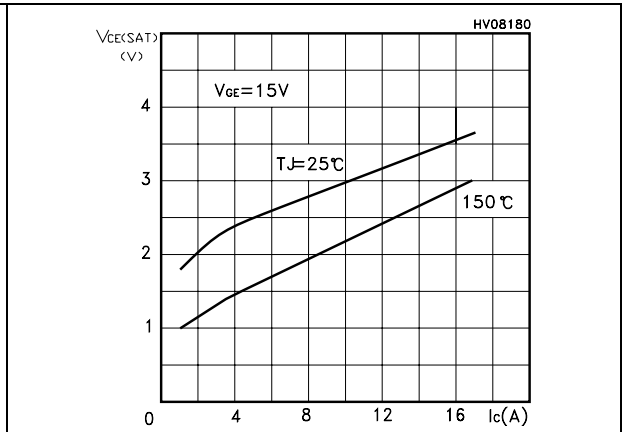


Figure 9. Normalized breakdown voltage vs temperature

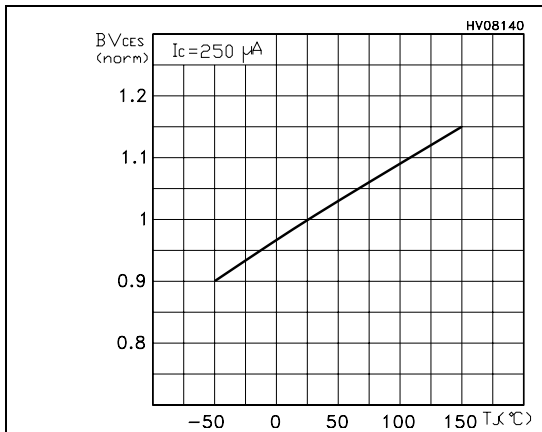


Figure 10. Switching losses vs temperature

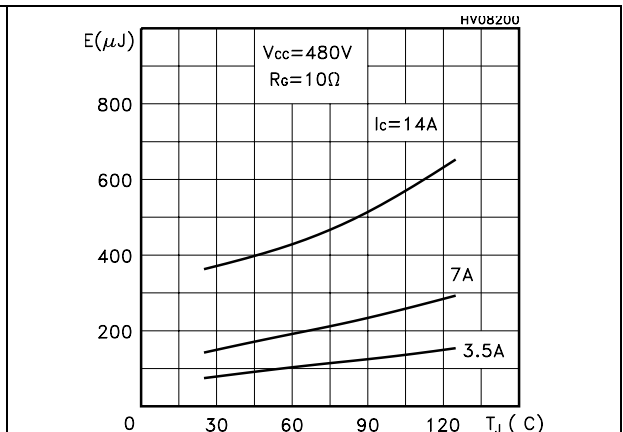


Figure 11. Switching losses vs gate resistance

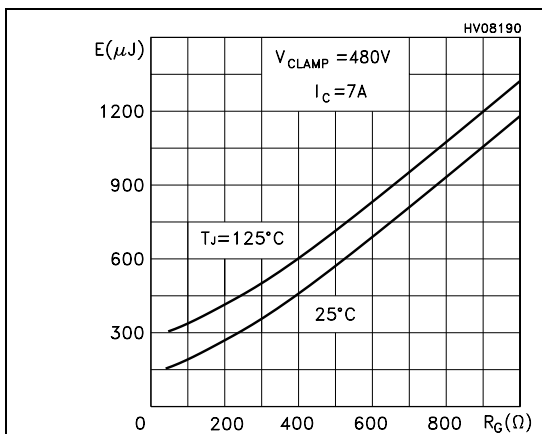


Figure 12. Switching losses vs collector current

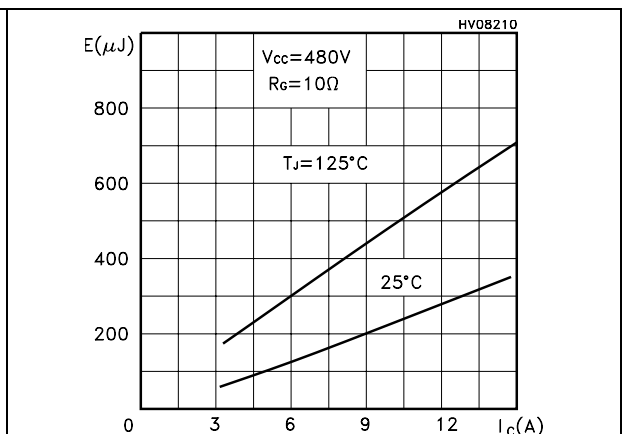


Figure 13. Thermal Impedance for DPAK

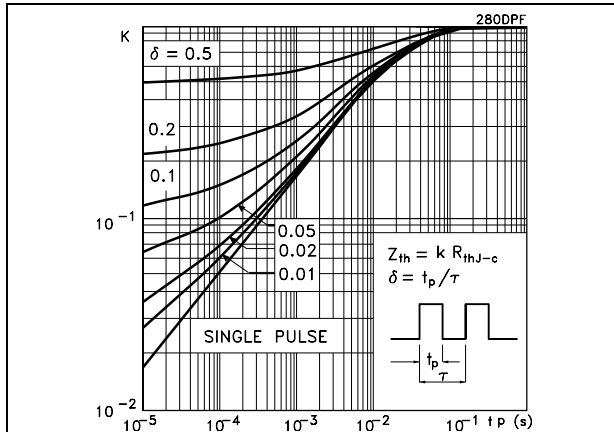


Figure 14. Thermal Impedance

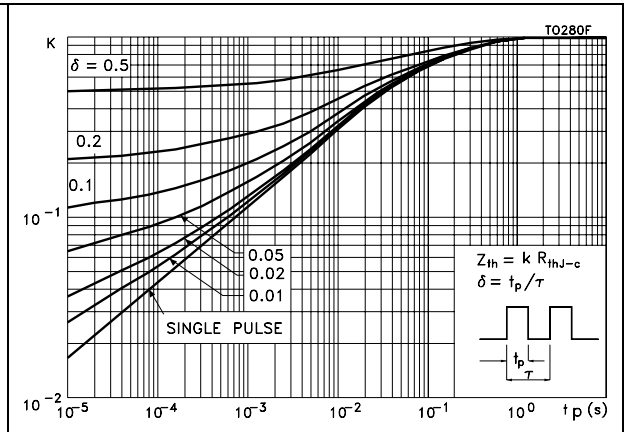
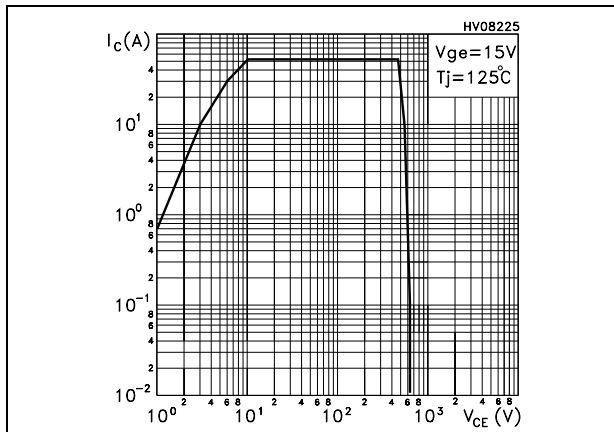


Figure 15. Turn-off SOA



### 3 Test circuit

Figure 16. Test circuit for inductive load switching

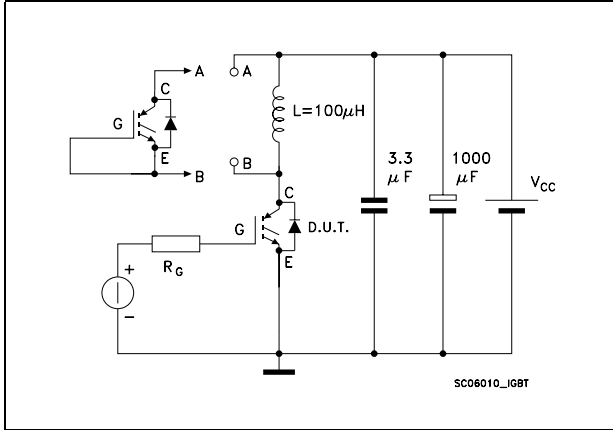


Figure 18. Switching waveform

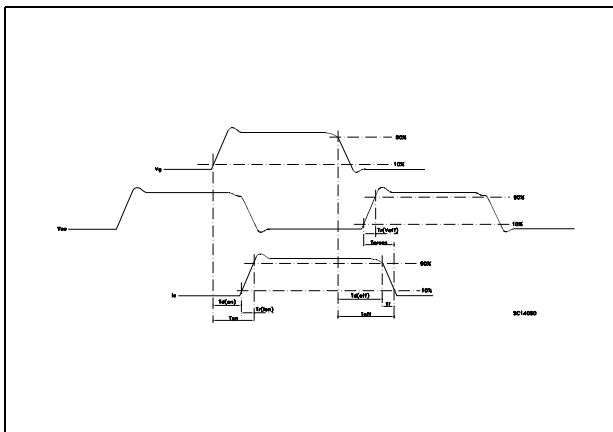


Figure 17. Gate charge test circuit

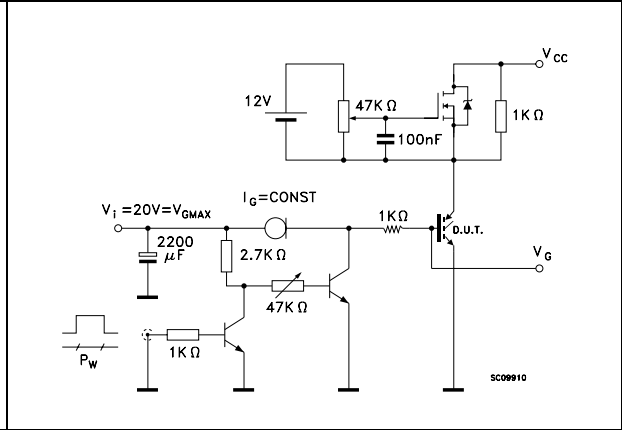
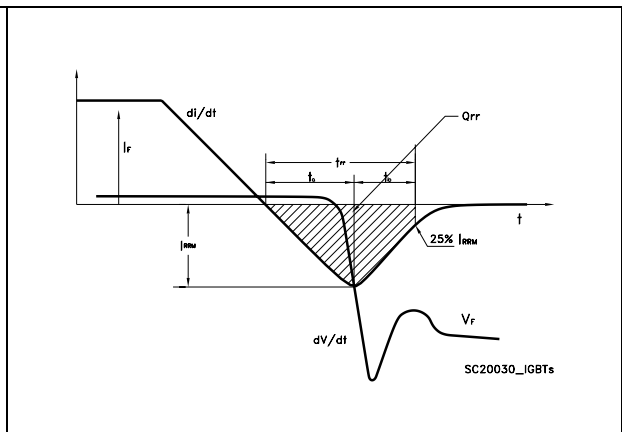


Figure 19. Diode recovery time waveform



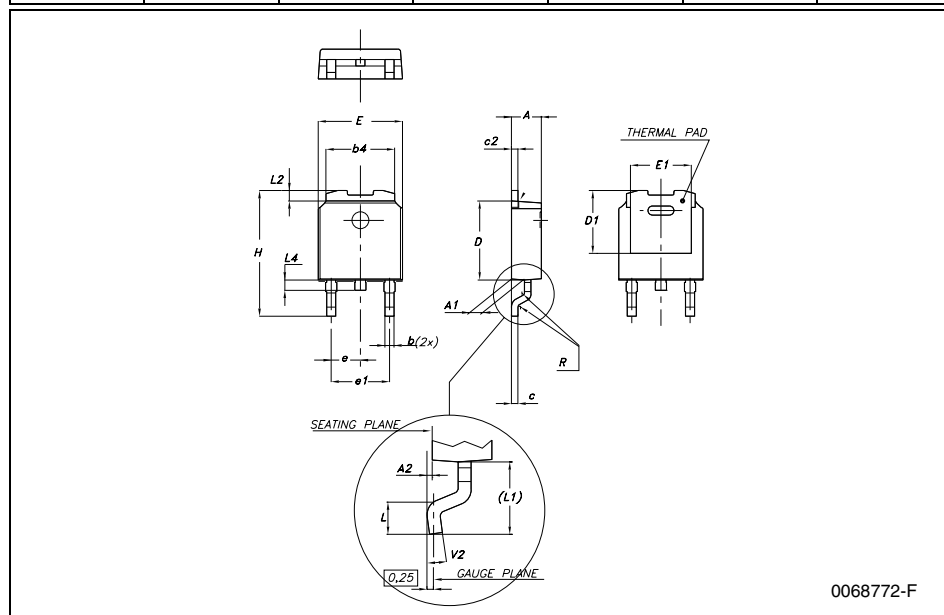
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)



**DPAK MECHANICAL DATA**

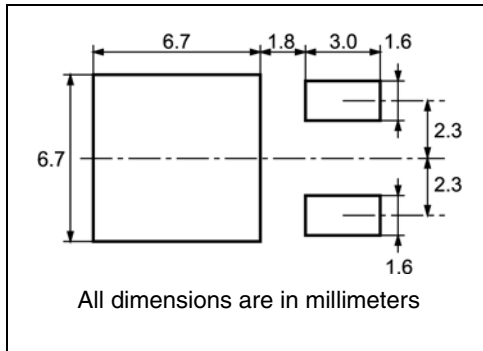
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



0068772-F

## 5 Packaging mechanical data

### DPAK FOOTPRINT



### TAPE AND REEL SHIPMENT

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY		BULK QTY	
2500		2500	

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

## 6 Revision history

**Table 6. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
21-Mar-2005	1	First release
23-Jun-2006	2	The document has been reformatted
26-Jan-2007	3	Typing error

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